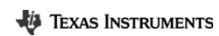
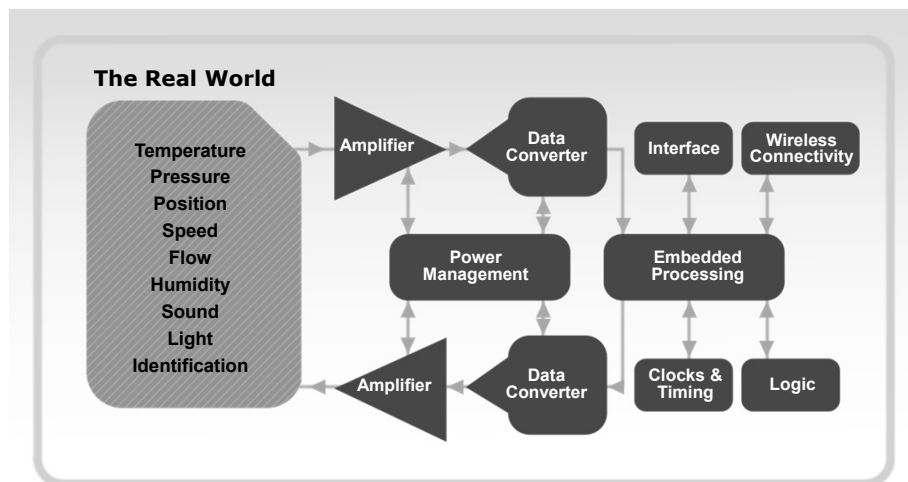


# TI Overview



Unlock the possibilities

with TI's complete solutions across the board



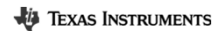
Unlock the possibilities

## by doing more with TI's analog and embedded processing technologies

- **Broad and deep product portfolio**
  - Embedded processors + full signal chain + power
  - Analog integrated circuits
  - DLP®; revolutionary digital display chip
  - OMAP processors and wireless connectivity solutions product lines focusing on embedded markets
  - More than 100,000 products; 900 new products per year
  - New acquisitions, more capacity
- **Systems expertise and technical support**
  - Engineer-to-engineer community engagement
  - > 130 sales offices
  - Extensive global network of sales and applications engineers
  - > 60 design centers worldwide



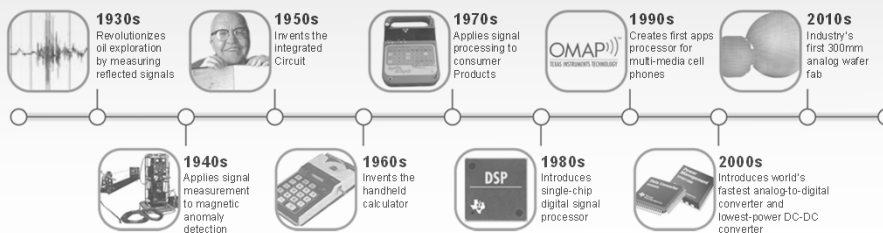
Integrated solutions, custom products, catalog products



Unlock the possibilities

## through TI's history of innovation

Innovation in signal processing has been the technology thread for nearly 90 years.





## Unlock the possibilities through increasing focus on analog & embedded processing



**\$ 12.2 – Total Revenue**  
(in billions of dollars)

### \$7.2 Analog

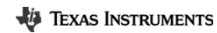
- High-Volume Analog & Logic
- Power Management
- High-Performance Analog
- Silicon Valley Analog

### \$2.4 Embedded Processing

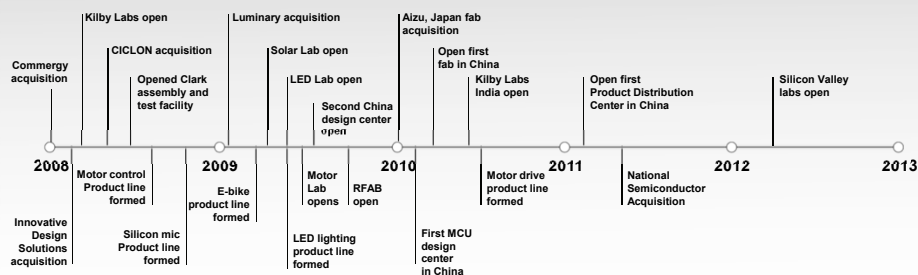
- Processors
- Microcontrollers
- Connectivity

### \$2.6 Other

- DLP® Products
- Custom ASIC
- Calculators
- Royalties
- Legacy Wireless Products



## Unlock the possibilities by capitalizing on its continued growth



Unlock the possibilities

## through TI's commitment to innovation

Nearly \$9B invested over the last five years\*

### Product development



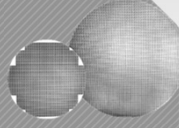
- More than 100,000 products
- Highly integrated custom products
- Software tools

### R&D Labs



- Innovation centers, focused on high risk breakthroughs
- Technology-specific labs

### Manufacturing technology



- Differentiated process and packaging technologies
- Flexible CMOS development model

### University and industry



- R&D partnerships with leading universities worldwide
- Engagement with industry consortia

\*Cumulative 2009, 2010, 2011, 2012, 2013



Unlock the possibilities

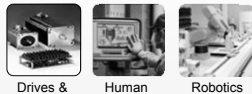
## with analog & embedded processors in every electronic product in the world

### INDUSTRIAL



White goods & HVAC

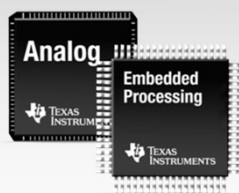
Automation



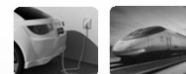
Drives & motion control

Human machine interface

Robotics



### TRANSPORTATION & AUTOMOTIVE



Hybrid electric vehicles

Railway systems



Aviation

Infotainment

### COMPUTING & COMMUNICATIONS



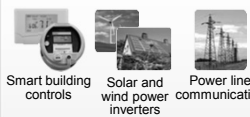
Thin client

Mobile devices

Base station

Portable mobile computing

### RENEWABLE ENERGY & SMART GRID

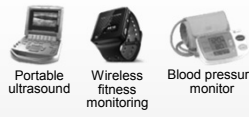


Smart building controls

Solar and wind power inverters

Power line communication

### HEALTH & FITNESS



Portable ultrasound

Wireless fitness monitoring

Blood pressure monitor



Unlock the possibilities

## through analog & embedded processors at work in the real world

### Gather analog information from the real world

- Temperature
- Pressure
- Position
- Speed
- Flow
- Humidity
- Sound
- Light
- Etc.

### Convert



Analog-to-digital converter gathers information while also managing power and battery levels.

### Process



Embedded processor compresses, processes and refines the signals to produce the crisp, clear sharpness we expect in today's top-of-the-line technology products.

### Convert



Digital-to-analog converter processes and "decodes" again for the real world.

### Relay processed information back to the real world

- Such as...
- Real-time braking systems
  - Vibrant digital images
  - Precise efficient motors
  - Etc.



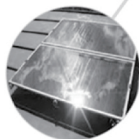
Unlock the possibilities

## with analog & embedded processors that enable better electronics

**SMARTER**  
E-books for the blind thanks to screens with tactile feedback



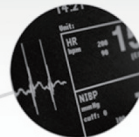
**GREENER**  
Solar panel optimizers squeeze more power from sunlight



**SAFER**  
Cars that brake automatically when a car gets too close to the one in front



**HEALTHIER**  
Portable devices that monitor vital signs and send details to doctor via smartphone

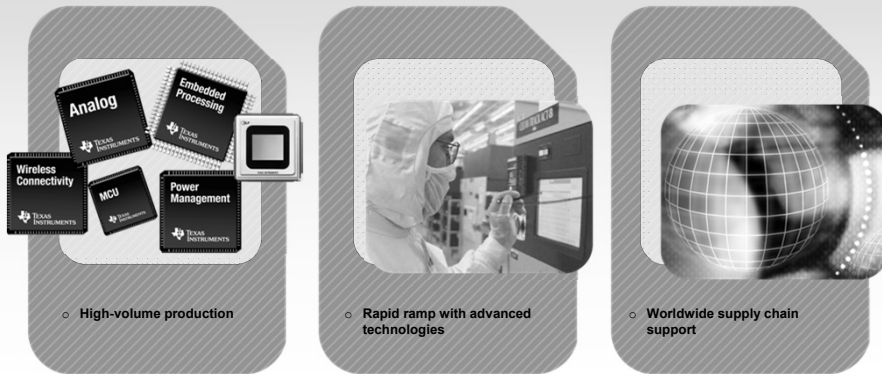


**MORE FUN**  
TI technology changes the way we live, work and play.



Unlock the possibilities

**with its quality process, manufacturing  
and supply chain**



 TEXAS INSTRUMENTS

Unlock the possibilities

**with a local partner worldwide**



TI has manufacturing, design or sales in more than 35 countries,  
serving more than 100K customers worldwide

 TEXAS INSTRUMENTS

Unlock the possibilities

**by collaborating with some of the  
industry's top minds**

Open  
opportunity



Insightful  
innovation



Smart  
collaboration



Highest  
standards



Winning  
determination



 TEXAS INSTRUMENTS

Unlock the possibilities

**by depending on a trustworthy name – TI**



Financial stability for  
nearly 90 years



Ongoing investments in  
R&D and manufacturing



Trusted partner for  
the long run

 TEXAS INSTRUMENTS

Unlock the possibilities

## with a financially stable company

### Grow:

- Gaining market share in Analog and Embedded Processing
  - \$2.5B in organic revenue growth in Analog and Embedded Processing, 2009-2013, with 9% CAGR

### Generate cash:


- Strategic focus on Analog and Embedded Processing
  - 79% of our revenue in 2013
- Using manufacturing to our strategic advantage
  - Long-lived assets support long-lived product
  - Manufacturing assets purchased opportunistically and ahead of demand keep capital spending stable and low
- Strong free cash flow\*

### Return cash:

- Committing to return 100% of free cash flow (less debt repayment) to shareholders through dividends and stock repurchases
  - Increased dividends for 10 consecutive years – dividend rate up 43% in 2013
  - Share count reduced by >35% since the beginning of 2005

\*Free cash flow = cash flow from operations minus capital expenditures.



 TEXAS INSTRUMENTS

Unlock the possibilities

## TIDesigns 参考设计库，助力系统设计

- 目前拥有超过 220 款参考设计方案，不断更新
- 支持工业、汽车、消费、医疗等广泛应用领域
- 提供完整原理图/方框图、测试报告、设计文件、物料清单(BOM)
- 国内外资深专业团队集智打造

### TIDesigns

#### 参考设计库

迅速投身于系统设计并加快产品上市步伐

- » 全面的设计包括原理图或者方框图、物料清单、设计文件以及测试报告
- » 设计由具备深厚的系统及产品知识的专家创建
- » 涵盖 TI 的模拟、嵌入式处理器以及连接产品系列
- » 支持广泛的应用，包括工业、汽车、消费、医疗等等

🔗 查看 TI 设计重要通告，包括使用授权、知识产权事宜及免责声明。

#### 搜索 TI Designs

按关键字搜索

搜索

搜索

按应用范围搜索

所有应用

按产品搜索

所有产品

#### 更多 TI 参考设计库

##### TIDesigns

TI 高精度设计是完整的板级和系统级电路库，旨在帮助工程师快速评估和定制其系统，同时扩展其模拟知识。提供三种级别的设计（参考、已验证和已认证），其中组合了我们的最高精度模拟专家提供的原理、方法、仿真、测试结果和设计文件。

[查看所有高精度设计 »](#)

##### TIDesigns

TI 的 PowerLab 参考设计库包含超过 1,000 种经过全面测试的电源管理参考设计，几乎涵盖每一种应用，可让您快速识别满足自己独特设计需求的有效电源解决方案。

[搜索全部 1,000 多种设计 »](#)

[www.ti.com.cn/tidesigns](http://www.ti.com.cn/tidesigns)

 TEXAS INSTRUMENTS

Unlock the possibilities

## 注册my.TI，简单四步

 购物车 |  简体中文 |  English |  日本語 | [my.TI 登录](#)

- 登录my.ti.com.cn，建立您的简易档案
- 勾选您感兴趣的应用/产品领域
- 订阅电子新闻简报
- 勾选您的电子邮件偏好

## 加入my.TI会员，精彩连连

- 申请免费样片
- 参与TI 在线技术支持社区
- 使用WEBENCH 工具轻松设计及仿真
- 订阅产品更新，获取最新资讯
- 更多精彩，等您发现

## 马上加入，惊喜无限

规则：即日起 ~ 2014 年 12 月 26 日止  
凡成功加入 my.TI 会员并留有完整信息者，我们每季将随机抽取250 名幸运儿，寄送精美礼品。每月另有不同抽奖活动等您参与！



 TEXAS INSTRUMENTS

# Catalog Processor

TI Confidential – NDA Restrictions

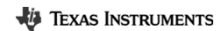
 TEXAS INSTRUMENTS



## Strong Embedded portfolio

	Processors	Connectivity
<ul style="list-style-type: none"> <li>• &gt;1300 products, from \$0.25 to \$25</li> <li>• Industry's lowest power consumption</li> <li>• Optimized solutions for control and safety</li> <li>• Unmatched analog and connectivity integration</li> <li>• Broad applications base with a strong core in industrial and automotive</li> </ul>	<ul style="list-style-type: none"> <li>• &gt;700 products, single core and multicore – DSP and ARM</li> <li>• Unmatched performance, power, and integration</li> <li>• Optimized solutions for: Wireless infrastructure, automotive infotainment &amp; driver assistance</li> <li>• Expanding to new markets: factory &amp; building automation, medical imaging, machine vision, etc.</li> </ul>	<ul style="list-style-type: none"> <li>• More than 130 products today shipping</li> <li>• Supporting 14 wireless technologies – focus on ease of use and low power</li> <li>• Enabling the "Internet of things" where everything gets connected... Bluetooth, WiFi and Zigbee</li> <li>• Broad application base - In-building, portable, automotive</li> </ul>

TI Confidential – NDA Restrictions



## Building a Stronger Processor Portfolio

ARM Industrial, Multimedia, Security	DSP Industrial, Analytics, Media
<b>Single Core ARM</b> <ul style="list-style-type: none"> <li>• AM335x</li> <li>• AM437x</li> </ul>	<b>Single Core DSP</b> <ul style="list-style-type: none"> <li>• C6654/55, C6671, C674x</li> </ul>
<b>Multicore ARM</b> <ul style="list-style-type: none"> <li>• AM5K2E02/04</li> </ul>	<b>Multicore DSP</b> <ul style="list-style-type: none"> <li>• C6657</li> <li>• C6672/4/8</li> </ul>
<b>ARM + DSP + Multimedia</b> <ul style="list-style-type: none"> <li>• AM5728</li> <li>• AM5718</li> </ul>	<b>ARM + DSP</b> <ul style="list-style-type: none"> <li>• 66AK2H14/12/06, 66AK2G02</li> <li>• 66AK2E02/05, OMAPL138</li> </ul>

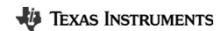
TI Confidential – NDA Restrictions



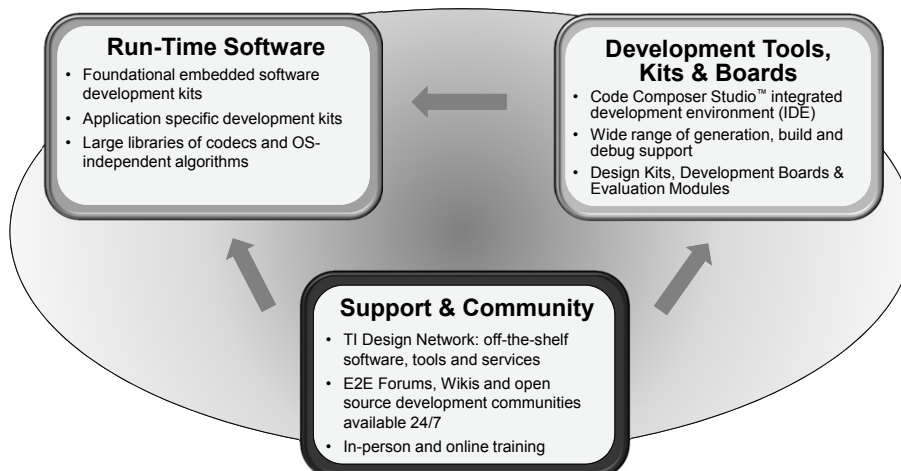


## New Devices in 2014

RTM DATE	PART NUMBER (Code Name)	KEY DIFFERENTIATORS	WHERE DO WE WIN?
2Q14	<b>AM437x</b> "Aegis"	1x Cortex A9 up to 1GHz 32 bit DDR3, QSPI 1GigE Switch, SGX 2x PRU Tamper, Security	<i>Industrial Automation Building Automation PPC replacement Broad Market</i>
2Q14	<b>C5517</b> "Broad Mkt launch"	16-bit fixed point C55x up to 200Mhz Ultra-low power	<i>Biometric analytics, Audio, Voice, Portable medical, Portable radio</i>
3Q14	<b>AM5K2Exx/ 66AK2Exx</b> "Edison"	4x 1.4 GHz A15 4MB of L2 Network Accelerator PCIe, USB, 10GigE	<i>2-, 4-, or 8-core PPC replacement Defense &amp; Aerospace Industrial Automation Broad Market</i>
3Q14	<b>AM572x</b> "J6/Vayu"	2x Cortex A15 up to 1.5GHz 2x C66x DSP, 2x M4 Video, 2x SGX, 2D 2x PRU, 1GigE, USB3	<i>HMI Industrial Automation Building Automation Broad Market</i>
4Q14	<b>AM571x</b> "J6Eco"	1x Cortex A15 up to 1.5GHz 1x C66x DSP, 2x M4 Video, SGX, 2D 2x PRU, 1GigE, USB3	<i>HMI Industrial Automation Building Automation Broad Market</i>



## TI's Embedded Processing Ecosystem



TI continues to invest heavily in its software and tools ecosystem



## Catalog Processors Run-Time Software: Foundational SDKs

**Linux®:** Complete Linux software development kits (SDKs) speed application development

- Mainline kernel and U-Boot support with Linaro™ GNU compiler collection (GCC) tool chain and a Yocto Project™ OE Core compatible file system
- Icon-based graphical user interface for easy navigation
- Complete documentation, libraries, benchmarks, utilities and examples

[www.ti.com/mainline](http://www.ti.com/mainline)

**TI-RTOS:** TI's real-time kernel (formerly known as SysBIOS)

- Provided at no charge and directly supported by TI
- Real-time kernel (SYS/BIOS) is optimized for TI devices and includes scheduling, memory management and utilities
- Support today via MCSDK including libraries and examples
- Industrial specific support available in BIOS-based Industrial Software Development Kit

<http://www.ti.com/tool/bioslinuxmcsdk>

<http://www.ti.com/tool/sysbiossdk-ind-sitara>



TEXAS INSTRUMENTS

## Sitara™ Run-Time Software: Android™ SDK for Sitara processors

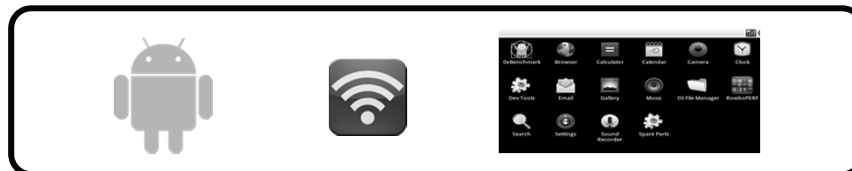
**Android:** Optimized Android releases jumpstart solution creation

- Complete Open Source software solution with a full featured application framework, multimedia and 3D graphics
- Allows for easy integration of applications via Java
- [www.arowboat.org](http://www.arowboat.org) community portal hosts newest developmental releases
- Android development tools (ADT) plug-in available for Code Composer Studio™ IDE v5

**Android SDK for Sitara processors can be downloaded on TI.com for free**  
ARM® Cortex™-A8

- Derived from rowboat releases with additional system testing
- Requires no run-time royalties and includes:
  - Complete documentation, libraries, benchmarks, utilities, performance benchmarks and examples
  - And more...
- **Third party partners to provide future releases and support**






[www.ti.com/sitaraandroid](http://www.ti.com/sitaraandroid)



TEXAS INSTRUMENTS

## Commercial O/S partners

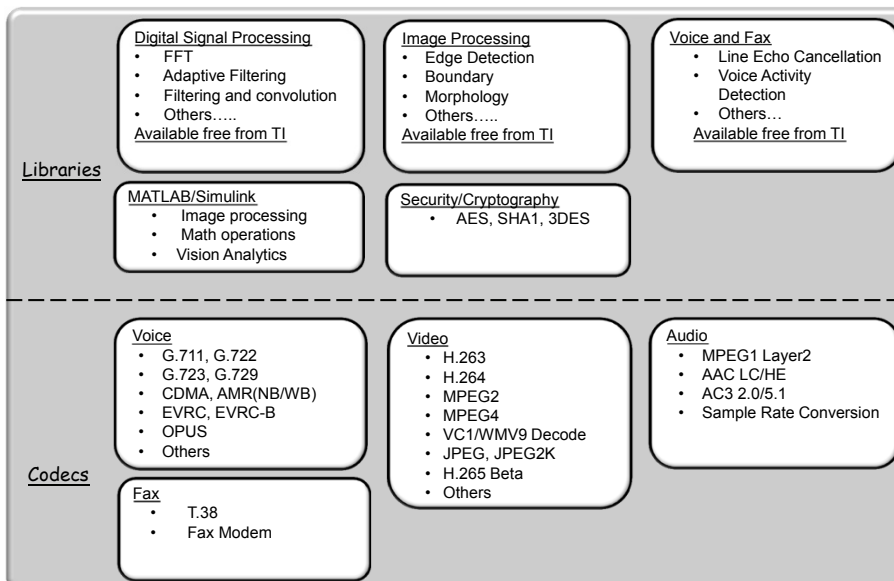
Operating System (O/S) partners offer proprietary operating systems, tools and services for a range of requirements including real-time and safety critical support

Vendor	Capabilities	Supported platforms	Contact
	<b>INTEGRITY</b> is a real-time operating system (RTOS) from Green Hills Software. It is royalty-free, POSIX certified, and intended for use in embedded systems needing reliability, availability and fault tolerance. It is used with 32-bit embedded processors with MMU support.	T1 ARM9™, A8™, A9™, and A15™ based products	<a href="http://www.ghs.com">www.ghs.com</a> Sales GHS <a href="mailto:info@ghs.com">info@ghs.com</a>
	QNX Neutrino is a microkernel-based architecture and is based on the idea of running most of the OS in the form of a number of small tasks. Neutrino is widely used as the basis for automotive, industrial control systems, medical instruments and other mission-critical applications.	Sitara ARM9, A8, and A15 based products	<a href="http://www.qnx.com">www.qnx.com</a> Peter McCarthy <a href="mailto:pmccarthy@qnx.com">pmccarthy@qnx.com</a>
	Wind River's VxWorks Operating System is based on a multitasking kernel with preemptive and round-robin scheduling for fast interrupt response times. It is POSIX certified and used in transportation, networking and communication systems and a wide variety of embedded systems.	T1 ARM9, A8, A9, and A15 based products	<a href="http://www.windriver.com/products/vxworks/">www.windriver.com/products/vxworks/</a> Lepine, Emery A (Joe) <a href="mailto:Joe.Lepine@windriver.com">Joe.Lepine@windriver.com</a>
	Mentor Graphics Nucleus Operating System is a real-time kernel designed to run on embedded processors. It targets low power and limited memory systems with a scalable memory footprint claimed to be as low as 2k for memory constrained environments.	Sitara ARM9 and A8 based products	<a href="http://www.mentor.com/embedded_info@mentor.com">http://www.mentor.com/embedded_info@mentor.com</a>
	Microsoft's Windows Embedded CE and Compact Operating System is a component-based, embedded, real-time operating system. It has a deterministic interrupt latency supporting up to 256 priority levels and thread based execution.	T1 ARM9, A8, A9, and A15 based products	Support from MS Windows Embedded Gold Partner Adeneo-Embedded <a href="http://www.adeneo-embedded.com">http://www.adeneo-embedded.com</a> <a href="mailto:sales@adeneo-embedded.com">sales@adeneo-embedded.com</a>

Operating System (OS/RTOS) Overview for Texas Instruments



## DSP Software – Libraries & Codecs Summary

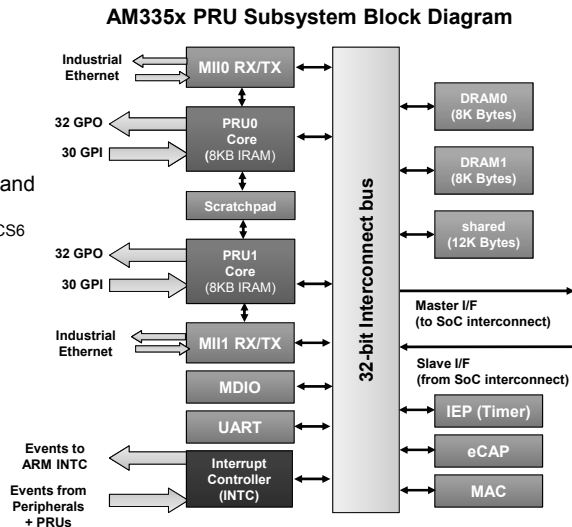


[http://processors.wiki.ti.com/index.php?title=Software\\_libraries](http://processors.wiki.ti.com/index.php?title=Software_libraries)



## Programmable Real-Time Unit (PRU) Subsystem

- PRU is a **highly differentiated**, low-latency microcontroller subsystem
- Dual PRU cores per subsystem
  - 200MHz – 5ns per instruction
  - Single cycle execution
  - Available on AM335x, AM4, AM5x
- Broad market support collateral and promotion coming in **July 2014**
  - New C-compiler – available now in CCS6
  - Linux Driver
  - C & ASM code examples
  - Technical collateral: AM335x TRM & Datasheet, FAQ, GSG
  - PRU Cape for BeagleBone
  - Training
- Example Use Cases
  - Anything requiring low latency
  - Motor Control (PWM)
  - Bit banded serial interfaces
  - 10/100 Ethernet
  - Parallel Camera input

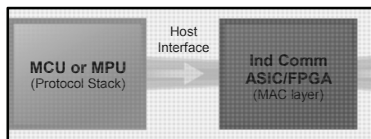


TEXAS INSTRUMENTS

## Industrial Communication Integration

**TI's ARM + PRU solution = Best in class**

- Meets critical latency requirements: 100us
- FPGA and FSL do not meet the latency requirements: 10ms



**Communication Protocols but not limited to**



**TI Designs**

**AM335x** (Multi-protocol)  
**AM437x** (Multi-protocol)  
**AM57xx** (Multi-protocol, host/slave)

**ARM CPU**  
 (Stack and application)

**Shared Memory**

**UART/MII**

**Timer**

**PRU**

**PRU-ICSS**

✓ PRU-ICSS (PRU based Industrial Communications Subsystem)

**TI's ARM + PRU solution = many benefits**

- System BOM **savings** (>40%) by eliminating the external ASIC
- Supports **multiple protocols** using the same hardware (PRU is completely programmable)
- Easily adapt to changing standards or **create own** (requires PRU expertise or 3P help)
- Scalable solution for HMI, PLC and I/O devices

TEXAS INSTRUMENTS

## JTAG Debug Probes

### MSP430



- USB interface
- 3 models based on JTAG headers (14pin TI, 20pin TI, 20/10pin ARM)
- \$79

### XDS100v2 – Entry Level



- ARM & DSP
- 3 models based on JTAG headers (14pin TI, 20pin TI, 20/10pin ARM)
- \$79

### XDS200 – Mid Range



- ARM & DSP
- 20pin TI, 14pin TI, 20pin ARM and 10pin ARM connectors
- \$295

### XDS560v2 – High Performance

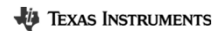


- USB or USB + Ethernet interfaces
- Includes multiple JTAG adapters (14pin TI, 20pin TI, 20pin ARM, 60pin MIPI, some include 60pin TI)
- System Trace
- \$995 - \$1495

### XDS560v2 Pro Trace Receiver



- Trace Receiver for ARM & DSP
- USB + Ethernet interfaces
- MIPI60 and 60pin TI adapters
- DSP, ARM & System Trace to pins
- \$3495



## Development Tools, Kits & Boards: Development kits for catalog processors

### Development Kits

Provide a range of hardware and software combinations to simplify development

- Evaluation and starter kits
- Complete development kits
- Reference designs for a variety of applications including portable communications, electronic point of service, industrial and more
- Kits include run-time software and development tools along with example hardware

### Featured Kits



TMDXEVM437x - \$599  
AM437x Evaluation Module (EVM)



TMDSSK3358 - \$199  
AM335x Starter Kit (SK)



TMDSEVM6678 - \$399  
C6678 Evaluation Module (EVM)



TMDSICE3359 - \$179  
AM3359 Industrial Communications Engine (ICE)



EVMK2H - \$997  
66AK2H Evaluation Module (EVM)



## Processor developer kits

Kit	Part Number	Price*	Availability
AM335x EVM	<a href="#">TMDXEVM3358</a>	\$995	TI
C6678 EVM	<a href="#">TMDSEVM6678</a>	\$399 baseboard \$599 w/ XDS560V2	TI
AM437x EVM	<a href="#">TMDXEVM437X</a>	\$599	TI
66AK2H EVM	<a href="#">EVMK2H</a>	\$997	TI
66AK2E EVM	XEVM2KE	\$1495 pre-production end June	TI

\* Pricing subject to change

Get Started  
Today



AM335x EVM



AM437x EVM



AM335x EVM



C6678 EVM



66AK2H EVM



66AK2E EVM

- Eval board & documentation
- SDK (Linux and SysBIOS)
- Support by TI ([e2e.ti.com](http://e2e.ti.com))

TEXAS INSTRUMENTS

## Sitara™ low-cost kits

Kit	Part Number	Price*	Availability
BeagleBone Black (AM335x 1GHz)	<a href="#">BEAGLEBK</a>	\$45	Community
BeagleBone (AM335x 720 MHz)	<a href="#">BEAGLEBK</a>	\$89	Community
BeagleBoard-xM (DM37x/AM37x)	<a href="#">BEAGLEXM</a>	\$149	Community
Starter Kit (AM335x)	<a href="#">TMDSSK3358</a>	\$199	TI

\* Pricing subject to change

Get Started  
Today



AM335x Starter Kit



BeagleBone



BeagleBone Black

- Low-cost development boards
- Allows HW expansions and community software content

TEXAS INSTRUMENTS

## Support & Community: For catalog processors

### TI's Design Network

Offers customers a global community of respected, well-established companies providing products and services that complement TI's solutions

- Broad range of reference designs
- Turnkey products and services
- System modules
- Embedded software
- Development tools
- Engineering services

<http://www.ti.com/designnetwork>  
or see Sitara and DSP Support pages

### Training and Community

<http://www.ti.com/sitarasupport>  
<http://www.ti.com/dspsupport>

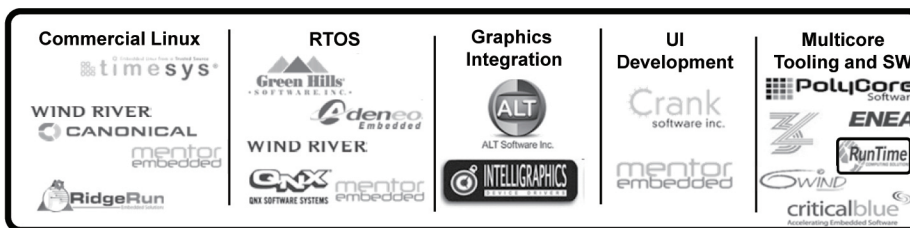
#### • Online resources

- [e2e Community Forums](#)
- [Embedded Processing Mediawiki](#)
- For issues with tracking numbers [SDOWP](#)



#### • Software related forums

- [Development Kits](#)
  - [Code Composer Studio](#), [TI compilers](#)
- [Embedded Software](#)
  - [Linux](#), [Android](#), [BIOS](#), [Codecs](#)



Logos are links to partners' external web sites







## **TI AM437x Microprocessors Featuring ARM® Cortex™-A9**

Technical Overview

### **Agenda**

- AM437x Silicon Overview
- AM437x EVMs
- AM437x Docs and Tools

# AM437x Cortex™-A9 based processors

## Benefits

- High performance Cortex-A9 up to 1GHz
- Single-cycle Vector Floating Point (VFP)
- Dual camera and display signal processing
- Security features: crypto and secure boot
- PRU-ICSS enables simultaneous industrial Ethernet protocols and motor feedback protocols
- PRU-ICSS enables Sigma-Delta modulation
- Simplified power sequence for flexible or system cost efficient power designs

## Software and development tools

- Free Linux SDK directly from TI
- RTOS (QNX, Nucleus, Green Hills, etc) from partners
- Full featured and low cost development board options (EVM, SK, IDK)

## Power Targets

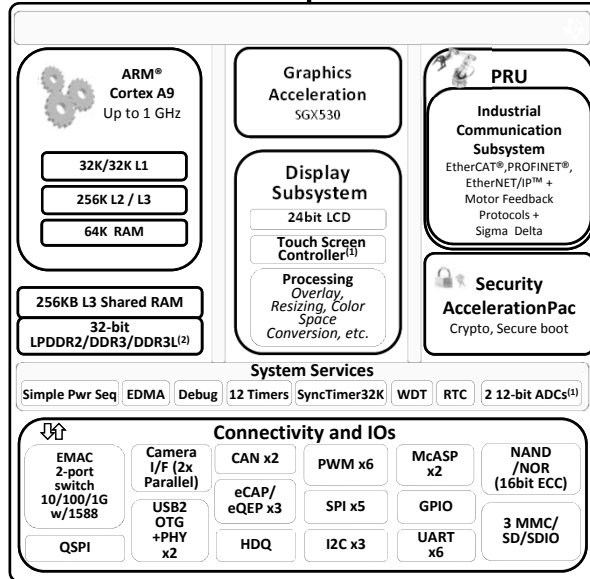
- Total Power: <1000mW
- Deep sleep: ~4mW
- RTC-only mode: <0.03mW

## Schedule and packaging

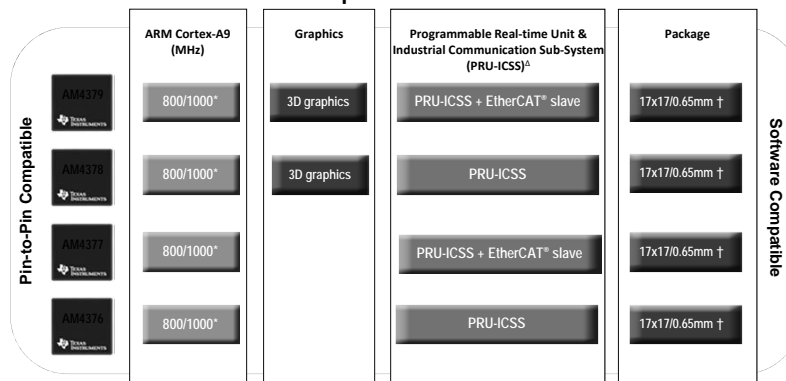
- Samples and Dev. Tools: 2Q 2014
- Production: 4Q 2014
- Package: 17x17mm, 0.65 VCA, 0.8mm-pitch effective routing

### NOTES:

- (1) Use of TSC will limit availability of channels on one ADC.
- (2) Max clock: LPDDR2=266MHz; DDR3=400MHz.



## AM437x: A scalable platform with 4 pin-to-pin compatible devices



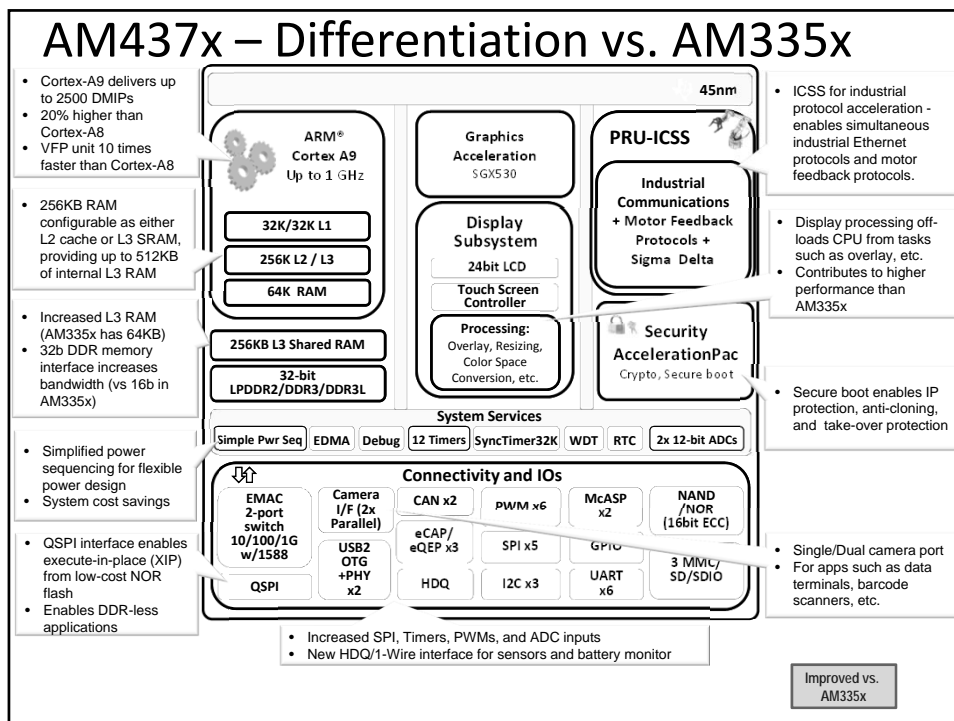
<sup>Δ</sup> PRU-ICSS is commonly used for slave industrial communication protocols such as PROFIBUS, PROFINET™, Powerlink, Ethernet/IP™ and EnDat

<sup>†</sup> Via Channel Array technology provides 0.8mm-pitch effective layout routing rules.

\*pending silicon characterization

## AM437x Sample Applications

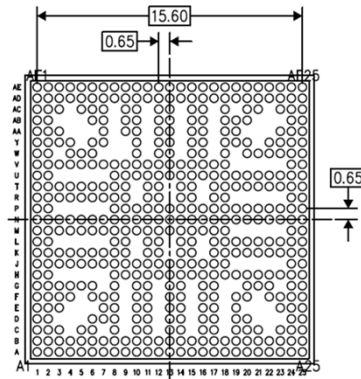
- Industrial / Home Automation
- Portable Navigation Devices
- Robotics
- Consumer electronics
- Smart Appliances
- Low power instrumentation
- Wireless Accessories
- Networking



# Package

### ZDN Package:

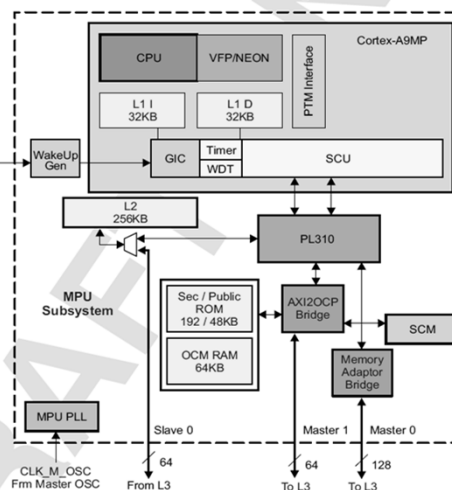
- 17x17 mm 0.65 pitch via channel array [0.8 routable] package
- Separate VDD\_MPU and VDD\_CORE



## Cortex-A9 (AM437x) vs Cortex-A8 (AM335x)

- VFP Fully Pipelined ~10x floating point speed up
- Out of order processing and other performance improvements giving 2.5 DMIPS/MHz (~16% in actual tests)
- External PL310 cache controller
- L2 Cache can be used as generic Sy Inter 224 Interr SRAM (SRAM or Cache - no mixing)
- Interrupts (more interrupts, 224)
  - Generic Interrupt Controller
  - Wakeup Gen
- local counter, watchdog timer
- Up to 1GHz MPU clock

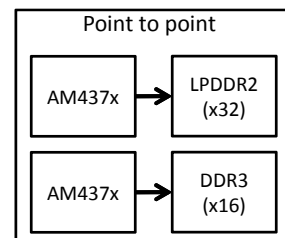
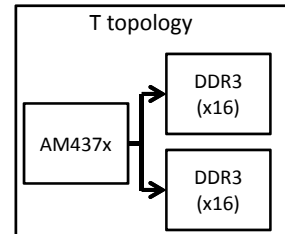
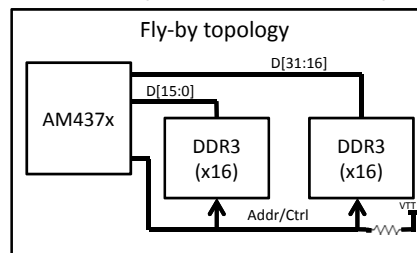
Figure 1. MPU Subsystem Block Diagram



## AM437x Memory interface (LPDDR2/DDR3)

### Features of the EMIF4D include:

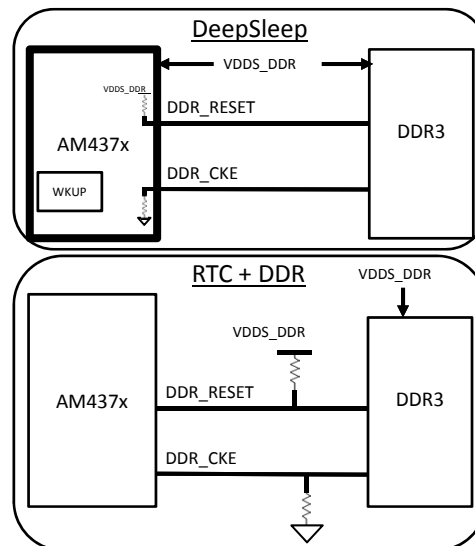
- Frequency Targets
  - LPDDR2: 266 MHz Clock (532 MHz Data Rate)
  - DDR3 (1.5V) /DDR3L (1.35V): 400 MHz Clock (800 MHz Data Rate)
  - No support for mDDR or DDR2
- 16 or 32 bit data bus
- 2GB total addressable space
- Supported Memory configurations
  - 1 load (x32 device)
  - 2 loads (x16 devices)
  - 4 loads (x8 devices)
- Supports a maximum of 4 address loads DDR3, 2 data loads for LPDDR2 and 1 data load for DDR3
- Plan to support HW leveling, characterization still in progress



## AM437x DDR3 Low Power

### •Low power enhancements for DDR3

- Fail Safe I/O for DDR\_RESET: Facilitates external pull-up to keep DDR in self-refresh during RTC+DDR.
- PMIC: Load Switch facilitates separation of DDR voltage to AM437x and DDR memory
- Added extra signaling in hardware to facilitate suspend/resume sequencing



# External memory interfaces

## Features of the GPMC include:

- 8-bit and 16-bit wide data bus
- Programmable cycle timings for each chip select
- Up to 16-bit ECC support for NAND Flash using BCH code (t=4, 8 or 16) or Hamming code for 8-bit or 16-bit NAND-flash
- Integrated ELM (Error Locator Module) to provide ECC calculation (up to 16b) for NAND support. Supports 4-bit, 8-bit and 16-bit per 512byte block error location based on BCH algorithms
- used to connect NAND, NOR (async and sync), FPGAs, etc

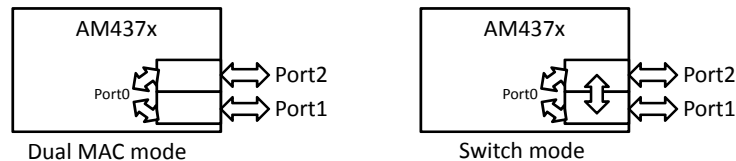
## Features of the MMC/SD include support for:

- 3 MMC/SD ports
- Multimedia card (MMC v4.3/ SD 2.0 ), supports >2GB capacity on eMMC boot on MMC0
- Card detect and write protect on each MMCSD port
- 48 MHz maximum I/O clock rate (up to SDR25 speeds)

## Features of the QSPI:

- Supports up to 4bit read, 1bit write
- Up to 48MHz clock, Master only
- Supports eXecute-In-Place (XIP) from serial NOR flash
- Primarily intended for fast boot from quad-SPI flash devices

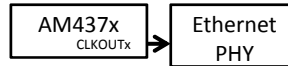
# EMAC – Ethernet Media Access Controller switch



- Ethernet Subsystem is an upgrade from AM335x
- 10/100/1000Mb 3 port Ethernet switch
- Supports standard Media Independent Interface (MII) and Reduced Media Independent Interface (RMII) & Gig Reduced Media Independent Interface (RGMII) to physical layer device (PHY)
- Includes MDIO interface to control/communicate with PHY
- Reset Isolation
- EXTDEV PLL to provide clock to external PHY

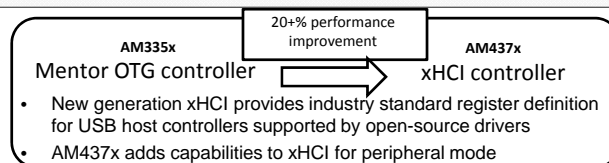
## Ethernet: changes from AM335x

- Added capability to derive REFCLK for Ethernet PHY from AM437x
  - Added Low Jitter EXTDEV PLL
  - Saves cost of external crystal or oscillator for PHY
    - 25MHz REFCLK for other PHYs
    - 50MHz REFCLK for RMII PHY clock (default for ROM for boot)
- Separated voltage domains of MDIO clk/data and Ethernet I/F in all I/O sets
  - Compliant to IEEE Ethernet Vmin=2.0V spec
- Expanded pinmux options
  - NAND + Dual Ethernet supported
- IEEE1588 TimeStamp
  - Provides accurate time based control over Ethernet
  - Ability to provide separate PLL (reusing Display PLL) with Fractional M multiplier for time stamping
  - IPV6 time stamping. Now supporting Annex D, E, F
- Added support for Ethernet operation in CORE OPP50
- Internal TX Delay mode supported by default to enable RGMII boot



## USB 2.0 – Universal Serial Bus

Benefit: 2x xHCI DRD (dual role device) USB controllers with embedded DMA and integrated PHYs provide a mechanism that complies with the USB2.0 standard for data transfer between USB devices up to 480 Mbps. Its dual-role feature allows the capability to operate as a host or peripheral.



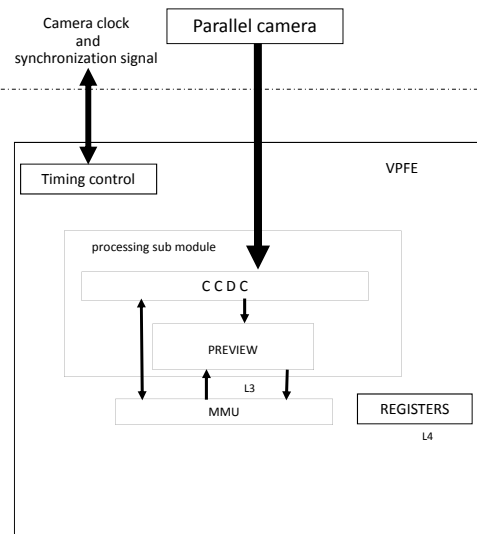
- 2 ports (USB0 and USB1)
- Both ports bootable
  - USB0 as peripheral,
  - USB1 as host. Can boot off of a MSD (ie, flash drive)
  - Swappable DP/DM to facilitate routing
- Operating as a host, it complies with USB2.0 standard for high-speed, full-speed and low-speed operation with a peripheral
- Operating as a peripheral, it complies with USB2.0 standard for high-speed and full-speed operation with a host
- SuperSpeed is not supported! (Did not integrate SuperSpeed PHY)
- Supports all modes of transfers (control, bulk, interrupt, and isochronous)
- Supports 15 simultaneous Transmit (TX) and 15 Receive (RX) endpoints, in addition to endpoint 0
- All new devices (Keystone, Vayu, etc.) going forward will be using xHCI controller (driver compatibility)

# Display Subsystem (DSS)

- Display Subsystem
- Reuse of AM37x (OMAP3630) DSS with the following omissions:
  - No support for VENC (Composite Video, S-Video), and Serial Interface (DSI or SDI)
  - H/W rotation engine and mirroring not implemented
- Up to 100MHz pixel clock
- Up to 2048x2048 resolution, highly dependent on frame rate, bpp, etc.
- Display Controller :
- Display modes :
  - Programmable pixel display modes (1, 2, 4, 8, 12, 16, 18 and 24 bit-per-pixel modes)
  - Programmable display size (2048x2048 pixel max)
  - 256 x 24-bit entry palette in RGB
- Display support :
  - Passive & Active Matrix panel.
  - Remote Frame Buffer support through the RFBI module.
- Signal processing :
  - Overlay support for Graphics, Video1 and Video2
  - Video resizer : upsampling (up to x8) downsampling (down to 1/4)
  - Transparency color key (source and destination)
  - Programmable video color space conversion YcbCr 4:2:2 into RGB
  - Gamma curve support
  - Programmable Color Phase Rotation (CPR)

# Camera Subsystem

- Same as AM35x VPFE
- Dual Port 8/10bit BT656 interface
- Single port 12-bit interface
- YUV422/RGB422, BT656, RAW input formats
- Up to 75MHz input pixel clock
- Bar code scanner





## AM437x has numerous serial peripherals...

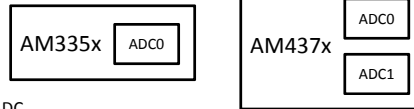
- 12 GP Timers & 1 watchdog timer
  - Free-running 32-bit upward counter. Runs off 32KHz or 19.2, 24, 25, 26 MHz system clock.
  - WDT: MPU Watchdog (runs off of 32KHz system clock)
- 1 Sync Timer (32KHz)
  - Special always on 32K timer for OS
- I2C (3)
  - 3 I2C ports compliant with Philips I2C specification version 2.1
  - Support for standard (up to 100K bits/s) and fast (up to 400K bits/s) modes
- General-Purpose I/O (GPIO) Interface (6 banks)
  - Synchronous interrupt requests in active mode from each channel are processed by GIC (General Interrupt Controller) in MPUSS.
  - Asynchronous wake-up request
  - 192 total GPIOs muxed with other signals
- Multichannel Audio Serial Port Interface (2)
  - Data Clock 50 MHz ,
  - Two Clock Zones and up to 4 Serial Data Pins per McASP port
  - Supports TDM, I2S and Similar Formats
  - Supports DIT mode
- Universal Asynchronous Receiver Transmitters (UART) (6)
  - UART1 will support full Modem Control (CTS,RTS,DTR, DSR, DCD, RIN)
  - All UARTs support IrDA, CIR and RTS, CTS flow control.
  - Supports baud rate up-to 3.6M bits/s.

## AM437x has numerous serial peripherals (cont.)...

- PWM Subsystem
  - eCAP (3)
    - Up to Three 32-bit enhanced Capture Modules – configurable as 3 capture inputs or 3 auxiliary PWM outputs
  - eHRPWM (6)
    - Up to Six Enhanced High Resolution PWM modules (eHRPWM) – with dedicated 16-bit time base counter with time and frequency controls.
  - eQEP (3)
    - Up to Three 32-bit enhanced Quadrature Pulse Encoder modules
- HDQ/1-wire
  - For connection to battery gauges
- DCAN (2)
  - Same as AM335x
- McSPI (5)
  - Master/Slave operation, 48MHz clock
  - Up to 4 channels for each McSPI0,1, two channels on McSPI2,3

## AM437x: Two ADCs

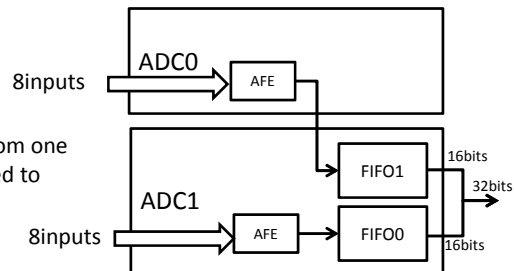
New feature vs. AM335x



- ADC0 (Touchscreen)
  - 12-bit Successive Approximation Register (SAR) ADC
  - 867KSPS
  - 8 analog inputs
  - Can be configured as a Touchscreen Controller. When configured as TSC, it takes away pins/channels for general purpose ADC use.
- ADC1
  - 12-bit Successive Approximation Register (SAR) ADC with preamp
  - 867KSPS
  - 8 analog inputs
  - .

### Simultaneous mode

- ADC1 controls ADC0 AFE
- 2 16bit results can be read from one 32bit register inputs converted to 32bit value



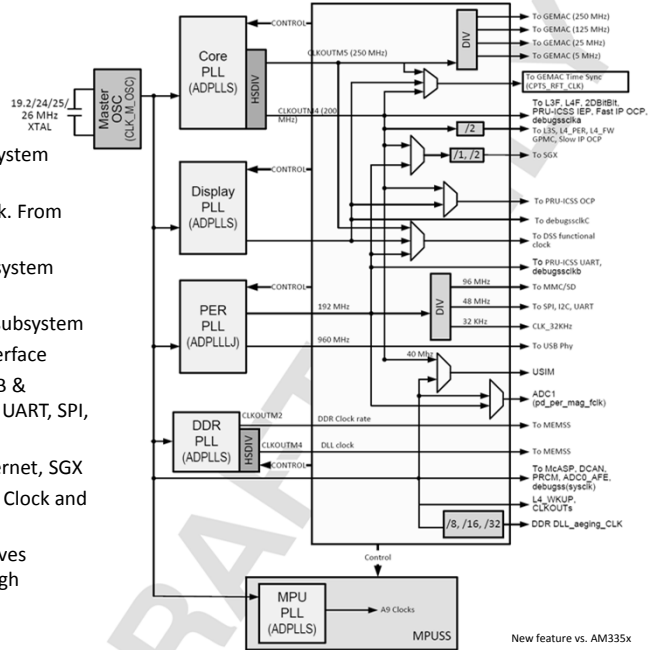
## Internal Memory

New feature vs. AM335x

- ARM internal RAM 64KBytes
- OCMC RAM
  - 256KBytes
- L2 cache as L3 RAM
  - 256KBytes, for a total of 512KBytes possible

# Clocks

- Input Clocks to device
  - 19.2, 24, 25, 26 MHz system clock
  - RTC Clock - 32kHz clock. From Crystal or PER PLL
- 6 PLLs to generate various system clocks:
  - MPU PLL - ARM MPU subsystem
  - DDR PLL – for DDR interface
  - PER low jitter PLL - USB & Peripherals (MMC/SD, UART, SPI, I2C, etc.)
  - CORE PLL - L3, L4, Ethernet, SGX
  - Display PLL – DSS Pixel Clock and IEEE1588
  - EXT low jitter PLL – drives external devices through CLKOUTx






## AM437x ROM

New feature vs. AM335x

- Boot from a number of sources, selectable with SYSBOOT pins
  - Memory boot
    - SD cards
    - eMMC – support for >2GB on either MMC0 or MMC1
    - NOR flash – support for muxed and non-muxed XIP boot
    - NAND flash - 8 or 16 bit
    - SPI EEPROMs
    - QSPI - XIP boot from serial flash
    - USB Host (USB1) – USB mass storage devices, USB thumb drives, great for product upgrades
  - Peripheral boot
    - Ethernet – support for MII, RMII, and RGMII boot.
    - USB client (USB0)
    - UART
- Other SYSBOOT selectable features
  - USB data polarity
  - Some pinmux options on certain interfaces (QSPI, NAND)
  - Input frequency (19.2, 24, 25, 26MHz)
  - Enable CLKOUT1
- Boot occurs in MPU and CORE OPP50 in all modes

## EVMs and Tools

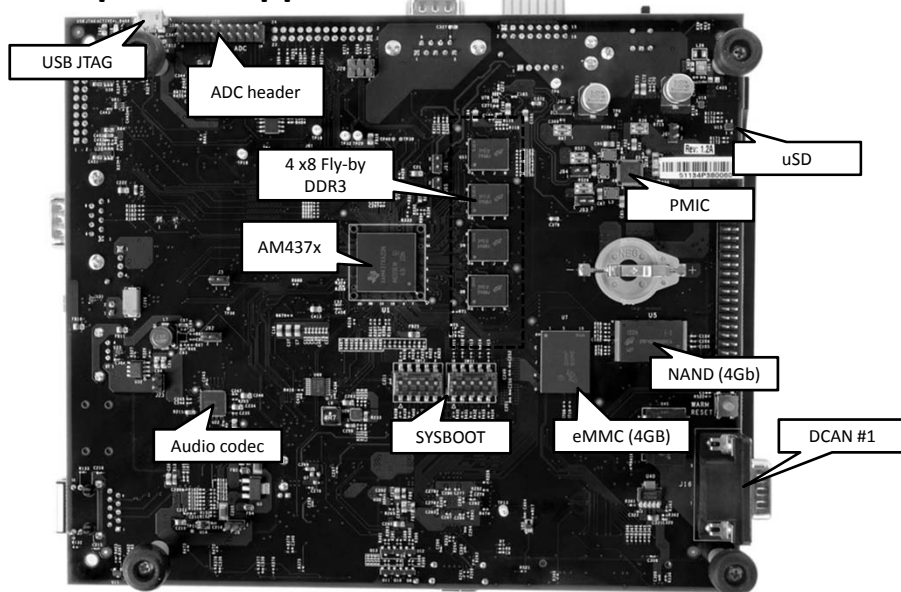
### Get to market fast with AM437x dev. tools

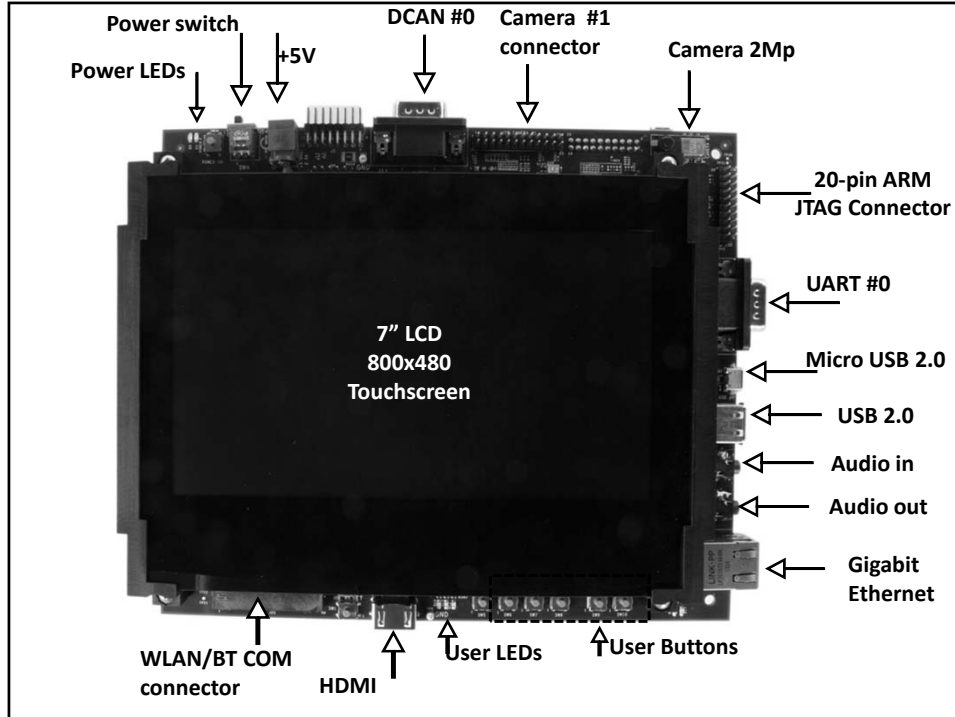
	TMDXEVM437X	TMDXSK437X	TMDXIDK437X
			
CPU-Freq	AM4378 – Up to 1GHz	AM4378 – Up to 1GHz	AM4379 – Up to 1GHz
Memory	2GB DDR3	1GB DDR3L	1GB DDR3
Display	7" Cap Touch / LCD	4.3" Cap Touch / LCD	None
PMIC	TPS65218	TPS65218	Discrete solution
WLAN/BT	Connector for WiLink8	Connector for WiLink8	N/A
Key Features	2x Camera modules 1x Gb Ethernet port NAND/eMMC 2x DCAN HDMI/LCD In/Out audio	1x Camera module 2x Gb Ethernet ports QSPI-NOR Flash No DCAN LCD only In/Out audio	1x Camera module QSPI-NOR Flash 1x Gb Ethernet PWM & ADC No display 2x Industrial Ethernet
Software	Linux	Linux	SYS/BIOS
Available	2Q 2014	4Q 2014	3Q 2014
	Target: \$599	Target: \$299	Target: \$329

# EVM design approaches

- Limited muxing options on each board
  - Facilitated modularization of interfaces (easier for customers to reference)
  - All I/F not available on one board.
- Several different DDR layout references
  - GP EVM: 4 devices (x8) DDR3 fly-by topology with VTT termination
  - SK: 2 devices (x16) T- topology, no VTT termination
  - IDK: 2 devices (x16) fly by topology, with VTT termination
- PMIC
  - GP EVM: TPS65218, DDR3=1.5V
    - includes external 1.8V LDO to demo RTC only mode (workaround for PMIC errata pre V2.0)
  - StarterKit: TPS65218, DDR3L=1.35V
    - no 1.8V LDO (plan to use PMIC v2.0)
  - IDK: Discrete solution, not optimal cost.
    - Power efficiency was key goal (single stepdown converters from 24V).
    - Demos power sequencing optimizations (uses 1.8V internal LDO)

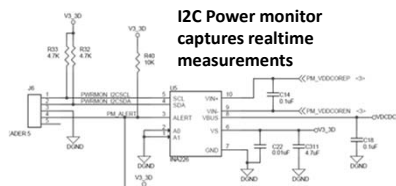
## Peripheral support on AM437x GP EVM



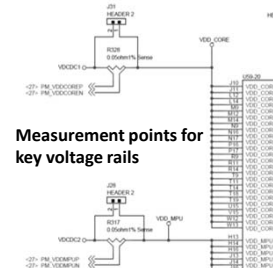
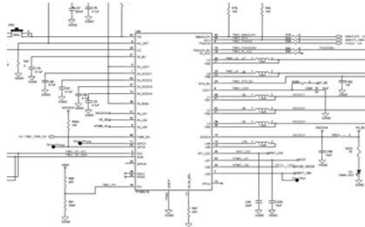


## GP EVM: design features

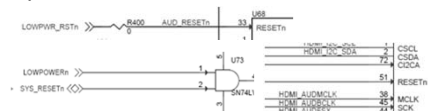
### GP EVM: Power Management features



TPS65218 PMIC: reference for all voltage rails and power control

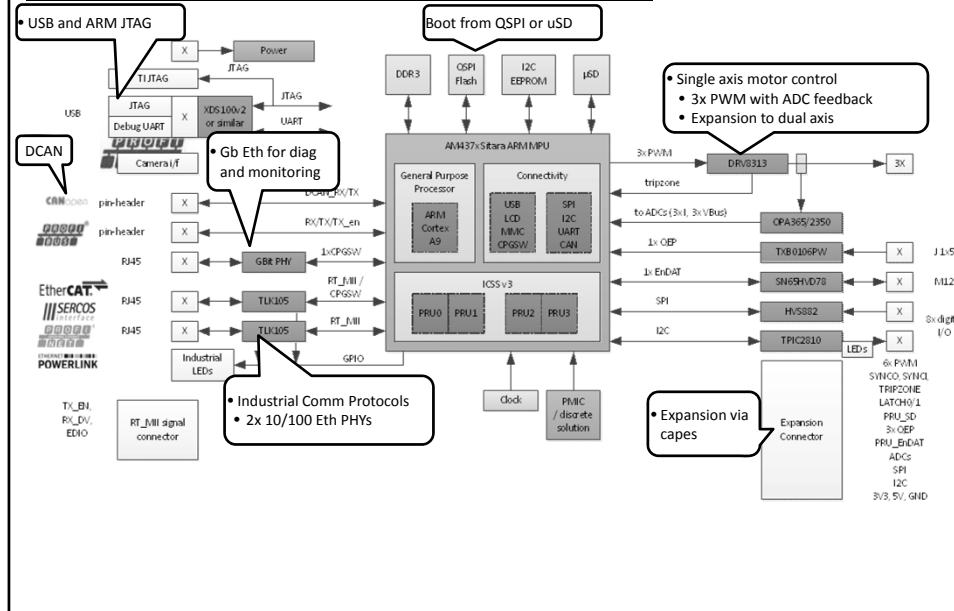


GPIO control of external peripherals for system low power



## AM437x Industrial Development Kit (IDK)

### Motor control with communications



## AM437x documentation

- [http://ap-fpdsp-swapps.dal.design.ti.com/index.php/AM437x\\_Collaterals](http://ap-fpdsp-swapps.dal.design.ti.com/index.php/AM437x_Collaterals)
  - EVM
    - Schematics, Board files (layout), PCB design specs, H/W users guide
  - AM437x
    - TRM and datasheet
- By RTM
  - Errata: PG1.2 production, errata will mention PG1.1
  - EVMs: Diagnostic Code, Symbols and Footprints
  - Schematic review checklist, Migration Guides
  - Tools: Clock Tree Tool (CTT), Pinmux tool, Power Estimation Tool (PET)
  - Layout Guidelines for DDR and USB
  - Throughput app notes
  - Power Consumption summaries
  - BSDL and IBIS models

# Pinmux tool for AM437x

Choose I/F to be used, tool will automatically select pinmux

Choose I/F voltage

I/O set automatically chosen

Choose any available pin or fix a pin

Package view of pins used

The screenshot shows the Pinmux tool interface for the AM437x device. The interface includes a menu bar (File, Devices, Load, Save, Save As, Generate, About), a toolbar, and a main workspace. The workspace is divided into several sections:

- Available Peripherals:** A list of peripherals with checkboxes for selection. Selected items include ADC (0/2), ARM (0/1), CAM (0/2), DCAN (0/2), DEBUSS (0/1), DSS (1/1), eCAP (0/3), eDMA4 (0/1), eHRPWM (0/6), EMIF (1/1), GPIO (0/6), GPAC (1/1), HDQ\_1V (0/1), I2C (0/3), MCASP (1/2), MDO (0/1), MDIO\_PRUSS1 (0/1), MI (0/2), MI\_PRUSS1 (0/2), MMC (0/3), OSC (0/2), PRU\_PRUSS0 (0/2), QSPI (0/1), RGMII (0/2), RMI (0/2), RTC (0/1), SPI (0/5), TIMER (0/6), UART (0/6), UART\_PRUSS0 (0/1), UART\_PRUSS1 (0/1), and USB (0/2).
- My DSS:** A section for configuring the DSS (Display Subsystem). It includes fields for Name (My DSS 1), New Case (24-bit Raster mode), Preferred Voltage (3.3V), and IO Set (DSS\_IOSH1 (View IO Set)).
- DSS Signals:** A table of signals with checkboxes for selection. Signals include VSYNC(dss\_vsync), HSYNC(dss\_hsync), PCLK(dss\_pclk), AC\_BIAS\_EF(dss\_ac\_bias\_en), DATA0(dss\_data0), DATA1(dss\_data1), DATA2(dss\_data2), DATA3(dss\_data3), DATA4(dss\_data4), DATA5(dss\_data5), DATA6(dss\_data6), DATA7(dss\_data7), DATA8(dss\_data8), DATA9(dss\_data9), DATA10(dss\_data10), and DATA11(dss\_data11).
- DSS Pins:** A table of pins with checkboxes for selection. Pins include Any(B23), Any(A23), Any(A22), Any(A24), Any(B22), Any(A21), Any(B21), Any(C21), Any(A20), Any(B20), Any(C20), Any(E19), Any(A19), Any(B19), Any(A18), and Any(B18).
- Package view of pins used:** A diagram of the AM437x package showing the locations of pins used by the selected peripherals. Pins are color-coded: black for 'Pin Not Assigned' and grey for 'Pin Assigned'.

Below the screenshot, a list of features is provided:

- Automatically optimizes pin selection as user adds interfaces
- Conflicts are identified
- Outputs Starterware header files (device tree files coming!)
- Standard tool for other devices (AM335x, Vayu AM57x, Galileo, etc.)





# KeyStone SoC Architecture Overview

KeyStone Training



## Agenda

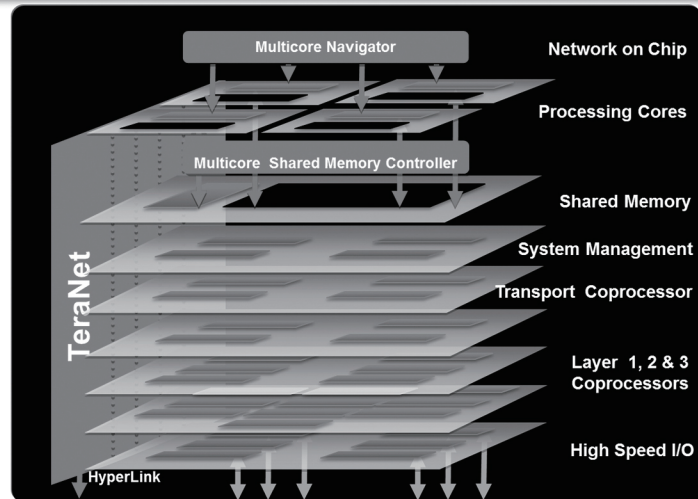
- Keystone SoC Innovation and Application
- KeyStone I Architecture
  - CorePac & Memory Subsystem
  - Internal Communications and Transport
  - External Interfaces
  - Coprocessors and Accelerators
  - Miscellaneous
- KeyStone II Architecture
  - ARM Cortex-A15 CorePac
  - Performance/Throughput Improvements
- KeyStone Platform
  - Debug
  - Device-Specific Offerings



YA2

## KeyStone Multicore SOC Architecture

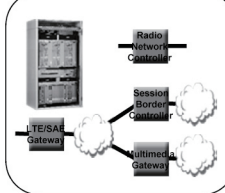
*The first network on chip infrastructure to unleash full multicore entitlement*



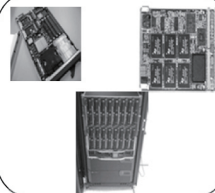
TEXAS INSTRUMENTS

## TI Keystone SoC Applications

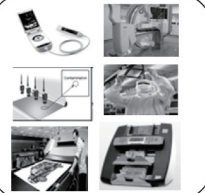
### Media Gateways & Networking



### High Performance & Cloud Computing



### Imaging Applications



### Video Surveillance



### Video & Audio Infrastructure



### Mission Critical



### SDR/BTS



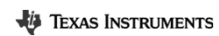
### Test and Automation



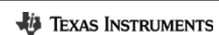
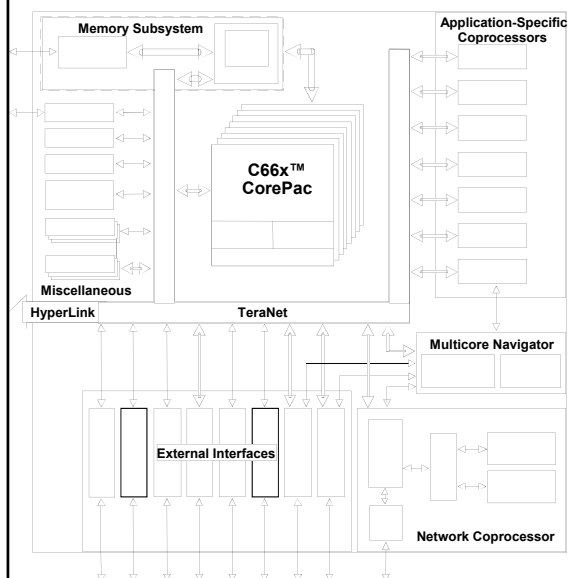
TEXAS INSTRUMENTS

# KeyStone I Architecture

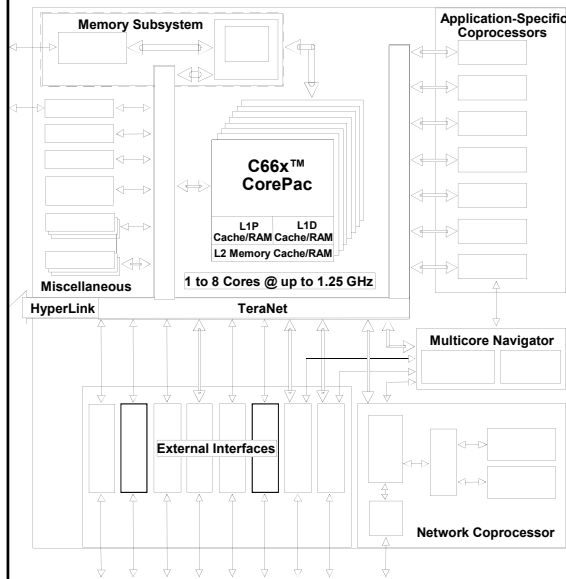
- CorePac & Memory Subsystem
- Internal Communications and Transport
- External Interfaces
- Coprocessors and Accelerators
- Miscellaneous



## KeyStone I Device Architecture



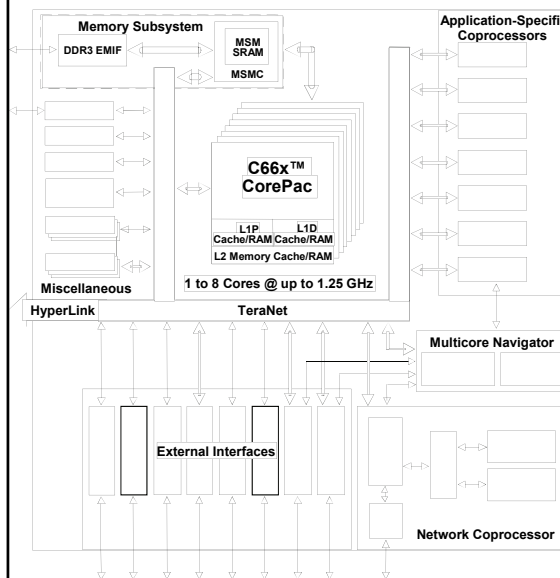
# KeyStone I CorePac



- 1 to 8 C66x CorePac DSP Cores operating at up to 1.25 GHz
  - Fixed- and floating-point operations
  - Code compatible with other C64x+ and C67x+ devices
- L1 Memory
  - Can be partitioned as cache and/or RAM
  - 32KB L1P per core
  - 32KB L1D per core
  - Error detection for L1P
  - Memory protection
- Dedicated L2 Memory
  - Can be partitioned as cache and/or RAM
  - 512 KB to 1 MB Local L2 per core
  - Error detection and correction for all L2 memory
- Direct connection to memory subsystem



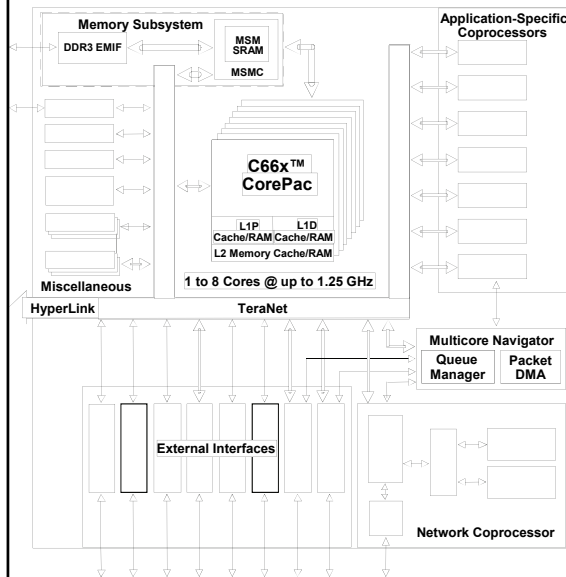
# KeyStone I Memory Subsystem



- Multicore Shared Memory (MSM SRAM)
  - 1 to 4 MB
  - Available to all cores
  - Can contain program and data
  - All devices except C6654
- Multicore Shared Memory Controller (MSMC)
  - Arbitrates access of CorePac and SoC masters to shared memory
  - Provides a connection to the DDR3 EMIF
  - Provides CorePac access to coprocessors and IO peripherals
  - Provides error detection and correction for all shared memory
  - Memory protection and address extension to 64 GB (36 bits)
  - Provides multi-stream pre-fetching capability
- DDR3 External Memory Interface (EMIF)
  - Support for 16-bit, 32-bit, and (for C667x devices) 64-bit modes
  - Specified at up to 1600 MT/s
  - Supports power down of unused pins when using 16-bit or 32-bit width
  - Support for 8 GB memory address
  - Error detection and correction



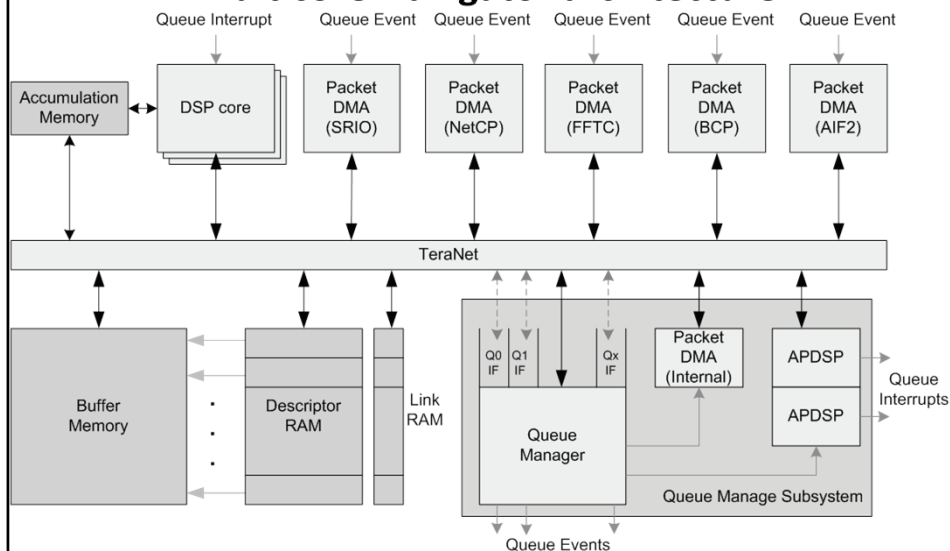
## KeyStone I Multicore Navigator



- Provides seamless inter-core communications (messages and data exchanges) between cores, IP, and peripherals. “Fire and forget”
- Low-overhead processing and routing of packet traffic to and from peripherals and cores
- Supports dynamic load optimization
- Data transfer architecture designed to minimize host interaction while maximizing memory and bus efficiency
- Consists of a Queue Manager Subsystem (QMSS) and multiple, dedicated Packet DMA (PKTDMA) engines

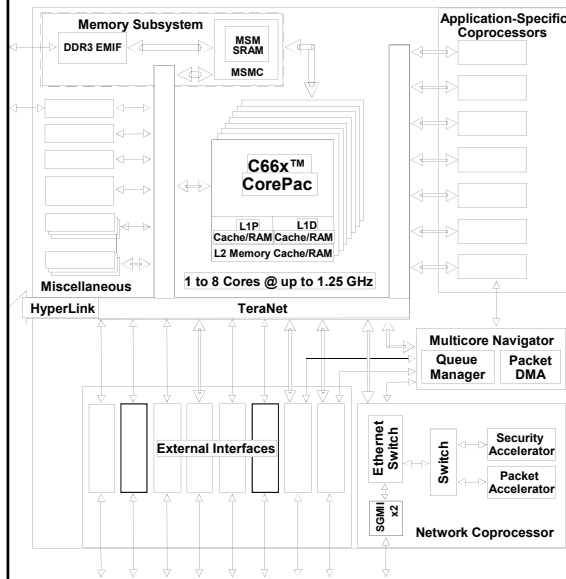
TEXAS INSTRUMENTS

## Keystone I Multicore Navigator architecture



TEXAS INSTRUMENTS

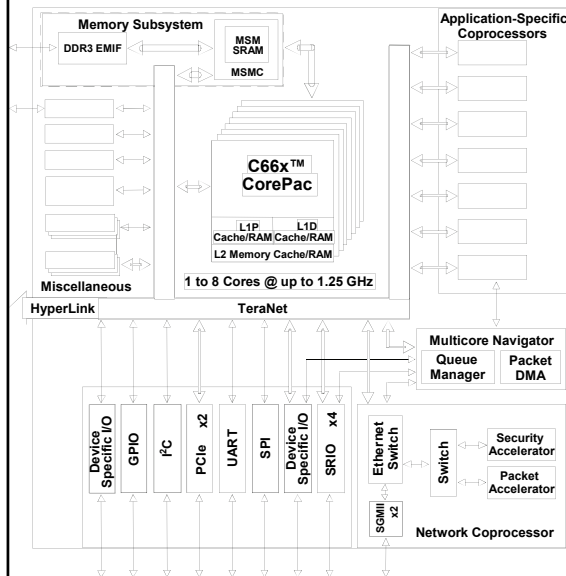
# KeyStone I Network Coprocessor



- Provides hardware accelerators to perform L2, L3, and L4 processing and encryption that was previously done in software
- Packet Accelerator (PA)
  - Single or multiple IP address option
  - UDP (and TCP) checksum and selected CRCs
  - L2/L3/L4 support
  - Quality of Service (QoS)
  - Multicast to multiple destinations inside the device
  - Timestamps
- Security Accelerator (SA)
  - Hardware encryption, decryption, and authentication
  - Supports IPsec ESP, IPsec AH, SRTP, and 3GPP protocols

TEXAS INSTRUMENTS

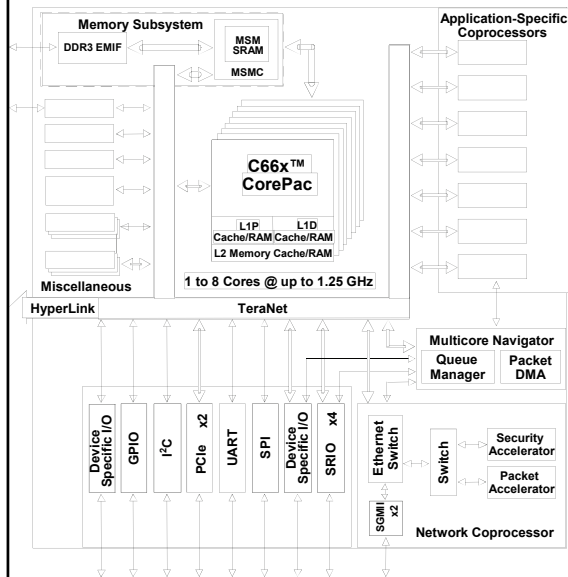
# KeyStone I External Interfaces



- 2x SGMII ports support 10/100/1000 Ethernet
- 4x high-bandwidth Serial RapidIO (SRIO) lanes
- 2x PCIe at 5 Gbps
- SPI for boot operations
- UART for development/testing
- I2C for EPROM at 400 Kbps
- GPIO
- Device-specific Interfaces
  - Wireless Applications
  - General Purpose Applications

TEXAS INSTRUMENTS

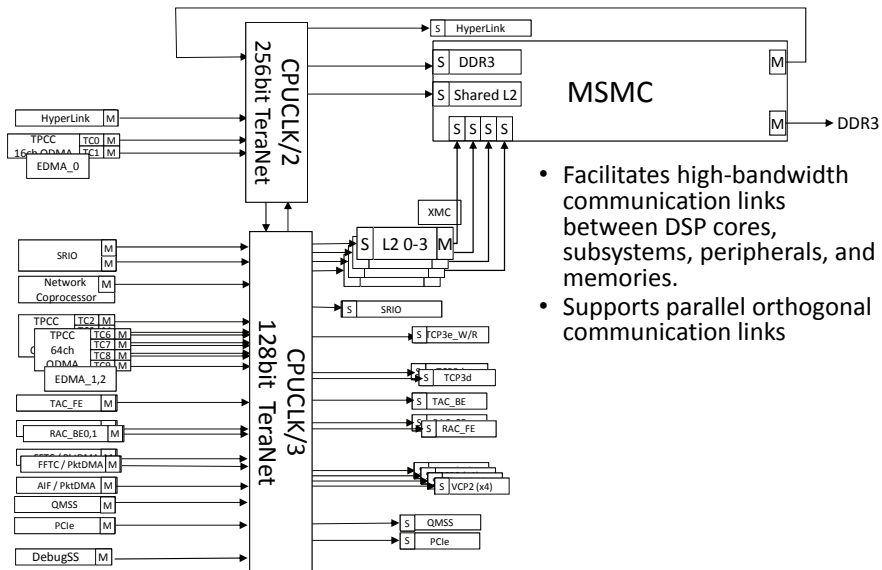
## TeraNet Switch Fabric



- A non-blocking switch fabric that enables fast and contention-free internal data movement
- Provides a configured way – within hardware – to manage traffic queues and ensure priority jobs are getting accomplished while minimizing the involvement of the CorePac cores
- Facilitates high-bandwidth communications between CorePac cores, subsystems, peripherals, and memory

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## KeyStone I TeraNet Data Connections

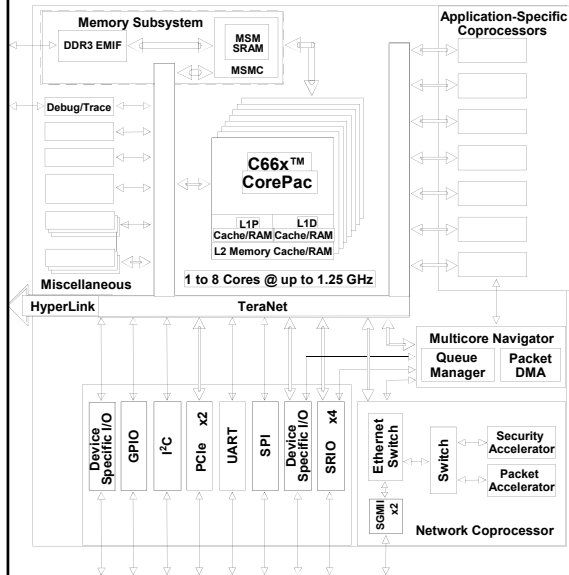


- Facilitates high-bandwidth communication links between DSP cores, subsystems, peripherals, and memories.
- Supports parallel orthogonal communication links

TEXAS INSTRUMENTS



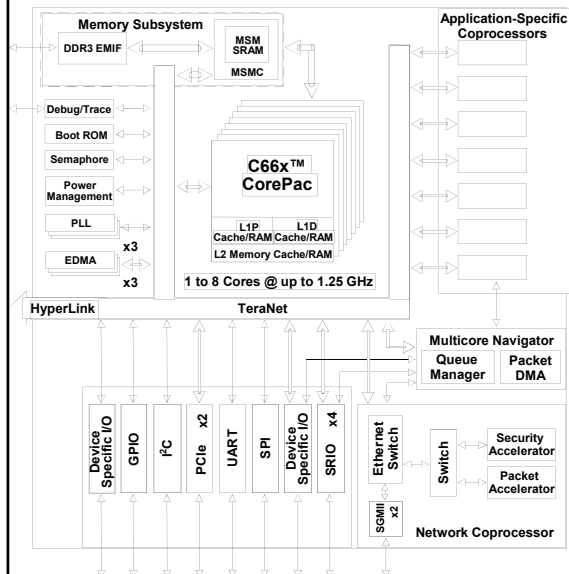
## KeyStone I HyperLink Bus



- Provides the capability to expand the device to include hardware acceleration or other auxiliary processors
- Supports four lanes with up to 12.5 Gbaud per lane

TEXAS INSTRUMENTS

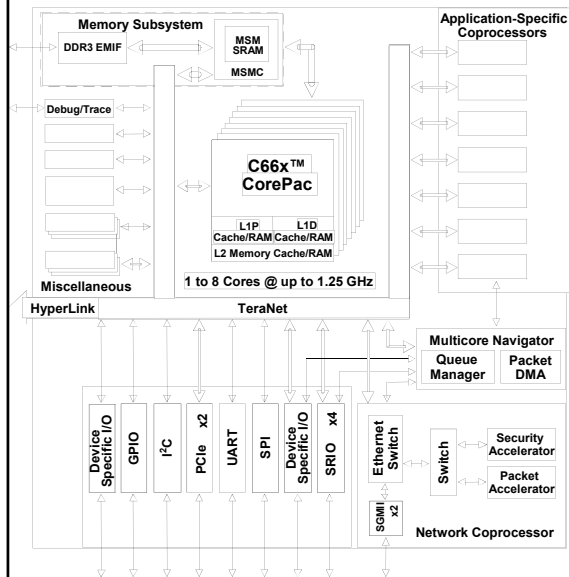
## KeyStone I Miscellaneous Elements



- Boot ROM
- Semaphore module provides atomic access to shared chip-level resources.
- Power Management
- Three on-chip PLLs:
  - PLL1 for CorePacs, except
  - PLL2 for DDR3
  - PLL3 for Packet Acceleration
- Three EDMA controllers
- Eight 64-bit timers
- Inter-Processor Communication (IPC) Registers

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## Diagnostic Enhancements



- Embedded Trace Buffers (ETB) enhance the diagnostic capabilities of the CorePac.
- CP Monitor enables diagnostic capabilities on data traffic through the TeraNet switch fabric.
- Automatic statistics collection and exporting (non-intrusive)
- Monitor individual events for better debugging
- Monitor transactions to both memory end point and Memory-Mapped Registers (MMR)
- Configurable monitor filtering capability based on address and transaction type

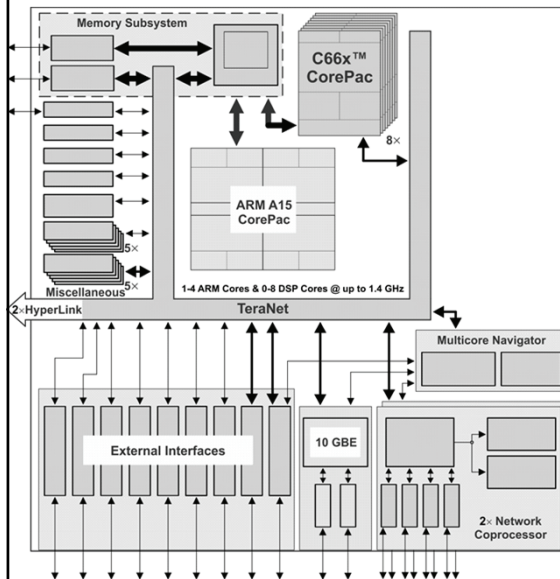
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## KeyStone II Architecture

- ARM Cortex-A15 CorePac
- Performance/Throughput Improvements

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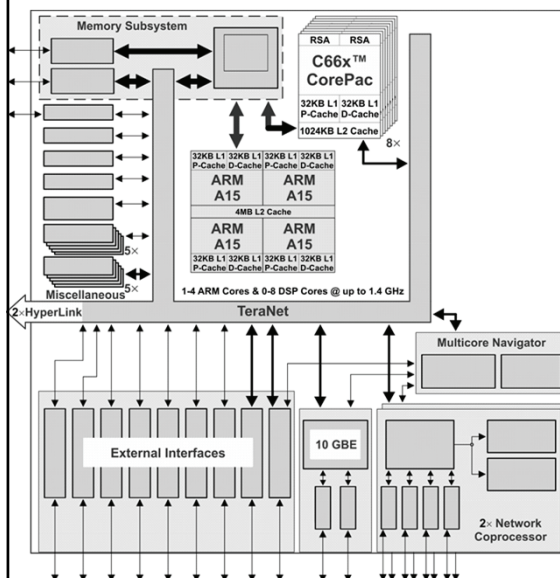
# KeyStone II Device Architecture



C66x CorePac
ARM A15 CorePac
Memory Subsystem
Multicore Navigator
Network Coprocessor
TeraNet Switch Fabric
10 Gigabit Ethernet (10 GBE)
External Interfaces
HyperLink Bus
Miscellaneous

TEXAS INSTRUMENTS

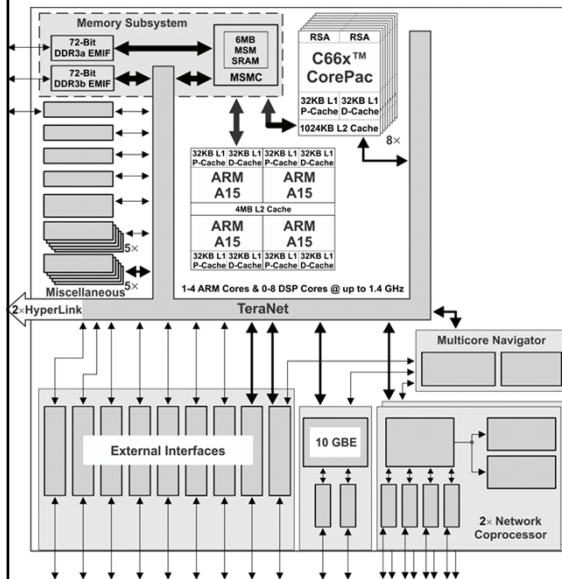
## ARM Cortex-A15 CorePac



- Single, Dual, or Quad-ARM A15 CorePac operating at up to 1.4 GHz.
  - Full implementation of ARMv7-A architecture instruction set
  - Integrated Neon and Vector Floating-Point Unit
- L1 Memory: 32KB L1 per ARM A15 for caching program and data
- L2 Memory:
  - Shared L2 Cache Memory with full cache coherency using Snoo Control Unit (SCU)
  - 4 MB L2 Cache is shared between the 1 to 4 ARM A15 core(s).
- The AMBA 4.0 AXI Coherency Extension (ACE) master port is connected directly to the MSMC2 for short-path access to shared MSMC SRAM.
- The ACE also provides IO-coherent access to the shared memory and external memory connected through the EMIF.
- Cluster-level and core-level power management and low-power standby modes (also known as WFI/WFE modes)

TEXAS INSTRUMENTS

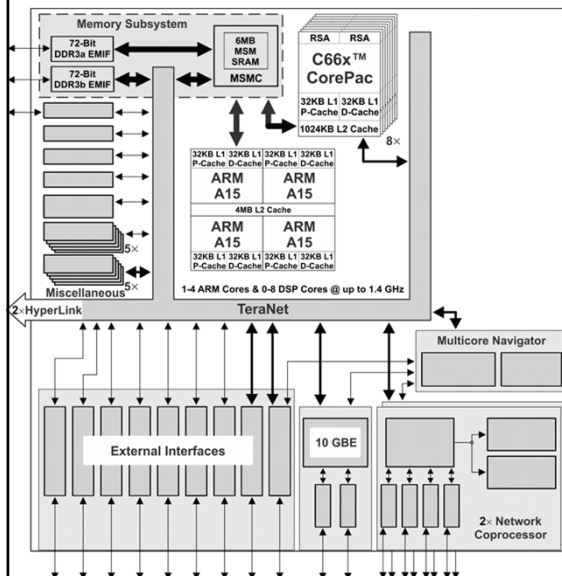
## KeyStone II Memory Subsystem: MSM/MSMC



- Multicore Shared Memory (MSM SRAM)
  - 2-6 MB shared among the C66x and ARM A15 CorePacs.
  - May contain program and data
- Multicore Shared Memory Controller (MSMC version 2.0)
  - Arbitrates access of C66x and ARM A15 CorePac and SoC masters to shared and external memory through DDR3 EMIF
  - Provides error detection and correction for all shared memory
  - Memory protection and address extension to 64 GB (36 bits)
  - Provides multi-stream pre-fetching capability
  - Support for ARM coherency with EDMA/peripheral masters in DDR3A and MSMC SRAM space
  - 8 SRAM banks
  - Runs at the DSP frequency, thereby increasing memory access by fourfold compared to previous MSMC v1.0

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## KeyStone II Memory Subsystem: DDR3

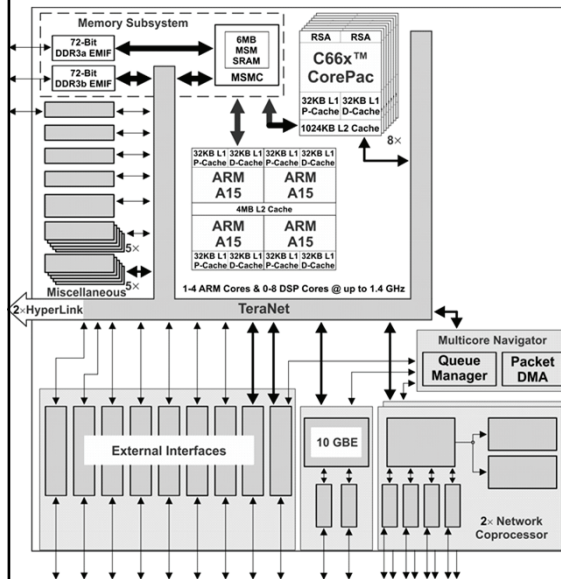


Up to two DDR3 subsystem(s) per device:

- The first DDR3 subsystem (DDR3A) supports up to 8 GB memory addresses and is connected to the CorePac(s) through the MSMC.
- When present, the second DDR3 subsystem (DDR3B) supports up to 2GB memory address and is connected directly to the TeraNet.
- Each DDR consists of a 64b/72b EMIF controller:
  - Supports 16-bit, 32-bit, and 64-bit modes .
  - **Operates at up to 1600 MT/s**
  - Supports power down of unused pins when using 16-bit or 32-bit width

TEXAS INSTRUMENTS

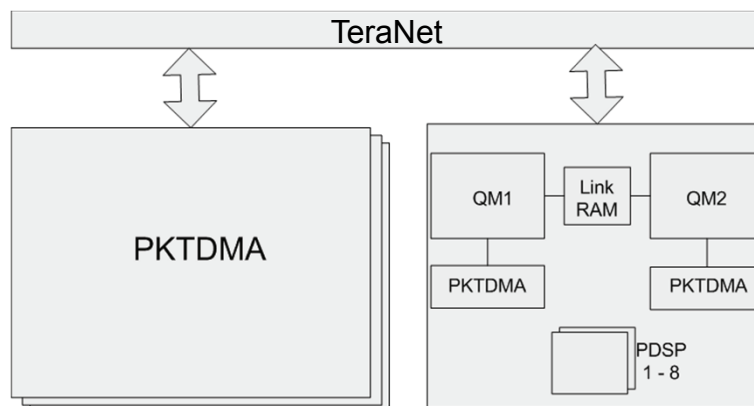
## KeyStone II Multicore Navigator



- Consists of the following:
  - 2x Queue Manager
  - Multiple, dedicated Packet DMA engines
  - 2x infrastructure DMAs
- Provides seamless inter-core communications (messages and data exchanges) between cores, IP, and peripherals. “Fire and forget.”
- Low-overhead processing and routing of packet traffic to and from peripherals and cores
- Supports dynamic load optimization
- Data transfer architecture designed to minimize host interaction while maximizing memory and bus efficiency
- Supports up to 16K hardware queues and 1M descriptors (32K internal).

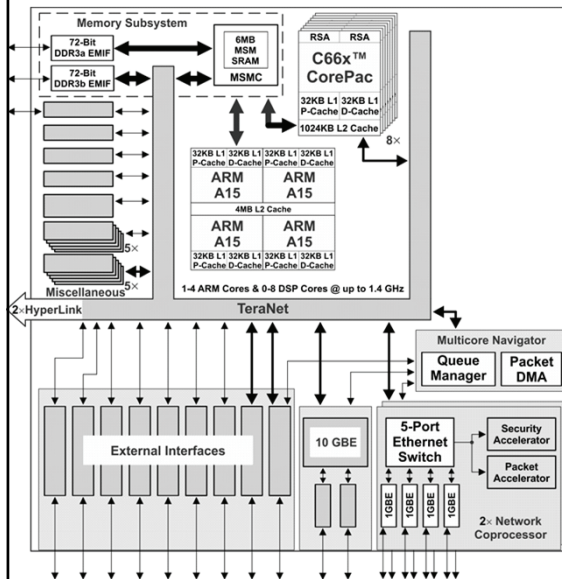
TEXAS INSTRUMENTS

## KeyStone II Multicore Navigator Architecture



TEXAS INSTRUMENTS

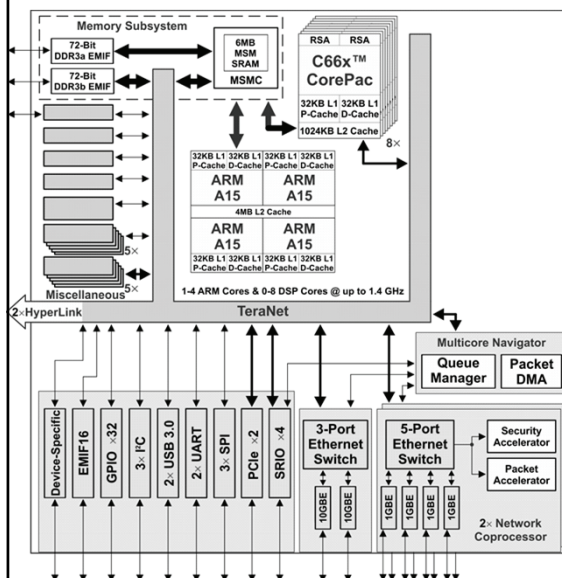
# KeyStone II Network Coprocessor (NETCP)



- Consists of one or two Network Coprocessor(s)
- Provides hardware accelerators to perform L2, L3, and L4 processing and encryption that was previously done in software
- Packet Accelerator (PA)
  - Single IP address option
  - UDP (and TCP) checksum and selected CRCs
  - L2/L3/L4 support
  - Quality of Service (QoS)
  - Multicast to multiple queues
  - Timestamps
- Security Accelerator (SA)
  - Hardware encryption, decryption, and authentication
  - Supports IPsec ESP, IPsec AH, SRTP, and 3GPP protocols
- 2x 5-port Ethernet switches (depending on number of instances of NETCP) with 4-8 ports connecting to 4-8 SGMII ports and one port connecting to the Packet and Security Accelerators.

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# KeyStone II External Interfaces

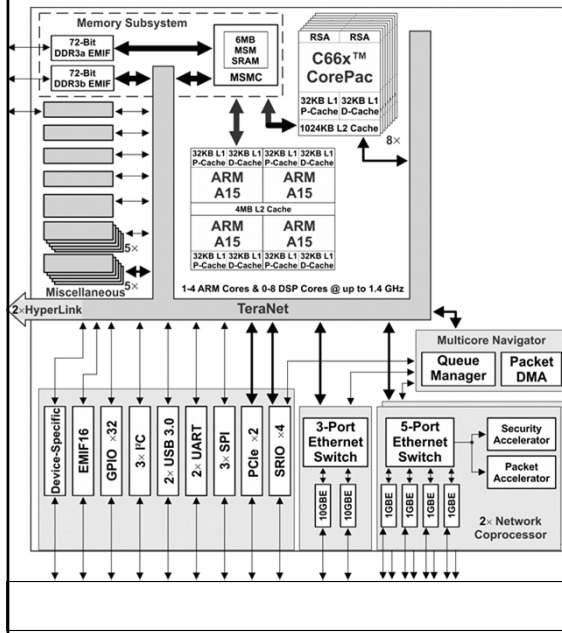


- 8x SGMII ports support 10/100/1000M Ethernet through 1-2x 5-port Ethernet switch(es).
- 2x XGMII ports support up to 10G Ethernet through a 3-port Ethernet switch.
- 4x high-bandwidth Serial RapidIO (SRIO v2.1) lanes for inter-DSP applications
- 2x PCIe at 5 Gbps
- 3x SPI modules with up to four chip selects per module.
- 2x UART for development/testing
- 2x USB 3.0
- 3x I2C at 400 Kbps
- 32 GPIO pins
- EMIF 16
- Device-specific interfaces

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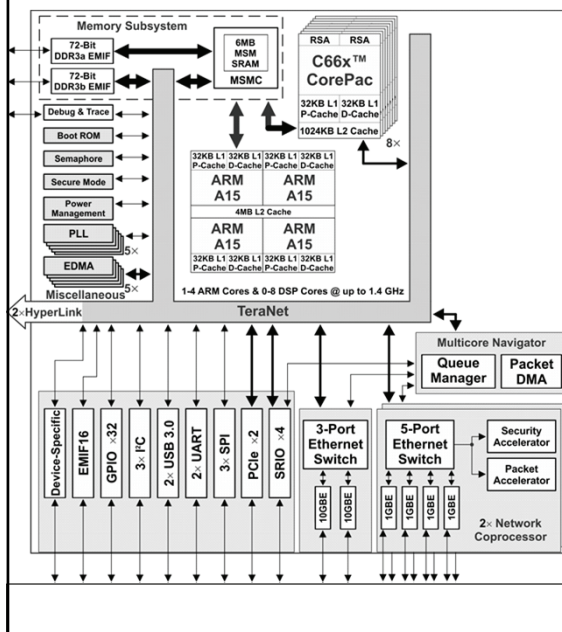
## KeyStone II HyperLink Bus



- Provides TI-proprietary, high-speed interconnects termed HyperLink.
- Up to 2x HyperLink modules with 4 lanes each.
- Provides the capability to expand the device to include hardware acceleration or other auxiliary processors
- Supports up to 12.5 Gbaud per lane

TEXAS INSTRUMENTS

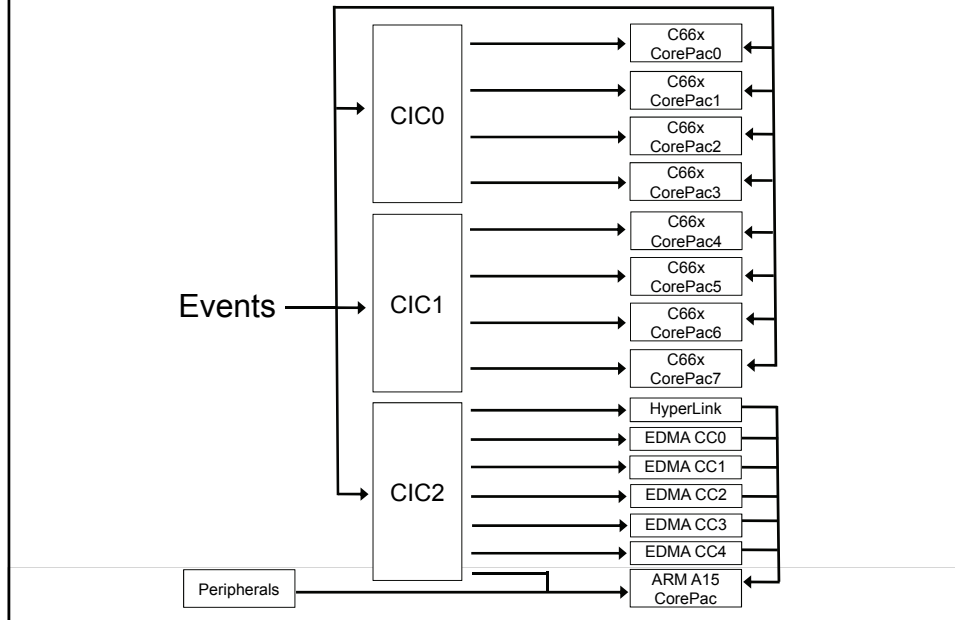
## KeyStone II Miscellaneous Elements



- ARM- and DSP-driven Boot ROM:
  - C66x CorePacs support booting from SRIO, PCIe, I2C Master, I2C Slave, SPI, Ethernet, XIP, and HyperLink.
  - ARM CorePacs support booting from UART, NAND, XIP, SPI, Ethernet, PCIe, I2C, SRIO and HyperLink.
  - Support varies by peripheral availability
- Semaphore module provides atomic access to shared chip-level resources.
- Secure Mode (1-time burn security key)
- Power Management:
  - Manages power- and clock-switching of individual IPs and CorePac(s).
  - Supports Dynamic Power Switching (DPS):
    - Power-state hibernation modes 1 and 2
    - Manages each C66x CorePac, each ARM core, and/or the entire ARM CorePac
  - Reset isolation capability on select peripherals
  - SmartReflex Class 0 and Class 3
- Up to 5 on-chip PLLs:
  - One Main PLL
  - One PLL for DDR3A
  - One PLL for DDR3B
  - One PLL for ARM CorePac
  - One PLL for Packet Accelerator
- 5x EDMA controllers
- 20x 64-bit timers
- Inter-Processor Communication (IPC) Registers

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## KeyStone II Central Interrupt Controller

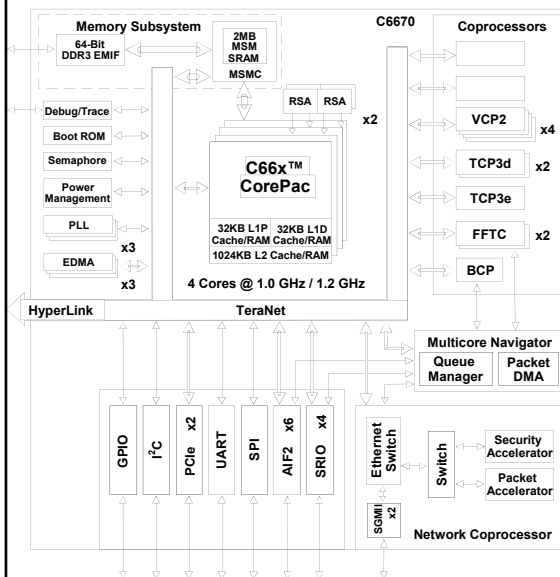


## KeyStone Platform

Device-Specific Offerings



## Device-Specific: C6670 for Wireless Apps



### Device-specific Coprocessors:

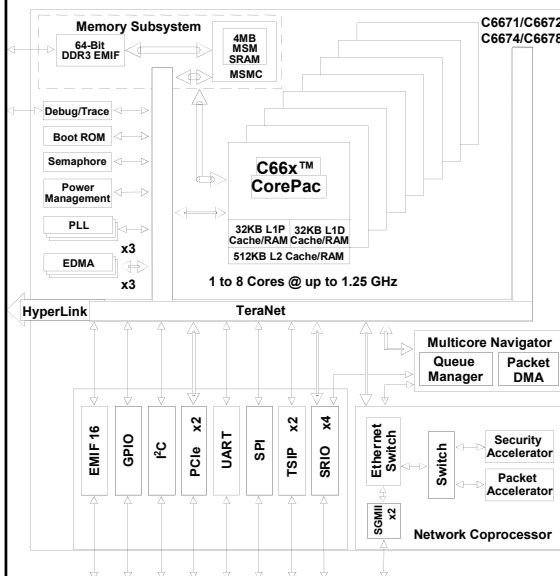
- 2x FFT Coprocessor (FFTC)
- Turbo Decoder/Encoder Coprocessor (TCP3d/3e)
- 4x Viterbi Coprocessor (VCP2)
- Bit-rate Coprocessor (BCP)
- 2x Rake Search Accelerator (RSA)

### Device-specific Interfaces:

- 6x Antenna Interface 2 (AIF2)

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## Device-Specific: C667x General Purpose

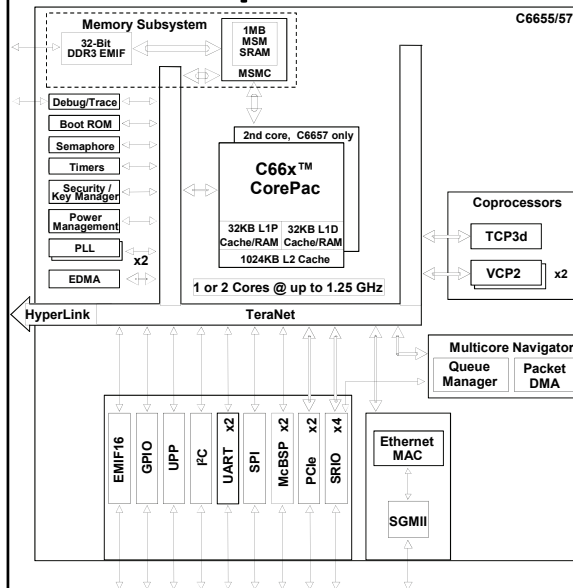


### Device-specific Interfaces:

- 2x Telecommunications Serial Port (TSIP)
- Asynchronous Memory Interface (EMIF16):
  - Connects memory up to 256 MB
  - Three modes:
    - Synchronized SRAM
    - NAND flash
    - NOR flash

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## Device-Specific: C665x General Purpose



### Device-specific Coprocessors:

- Turbo Decoder Coprocessor (TCP3d)
- 2x Viterbi Coprocessor (VCP2)

### Device-specific Interfaces:

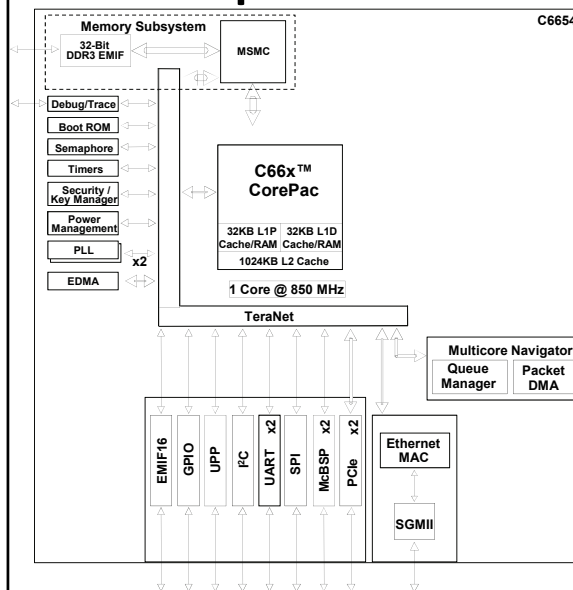
- Asynchronous Memory Interface (EMIF16)
- Universal Parallel Port (UPP)
- 2x Multichannel Buffered Serial Ports (McBSP)

### Device-specific Memory:

- 1 MB Multicore Shared Memory (MSM SRAM)
- 32-bit DDR3 Interface



## Device-Specific: C665x Power Optimized



### Device-specific Interfaces:

- Asynchronous Memory Interface (EMIF16)
- Universal Parallel Port (UPP)
- 2x Multichannel Buffered Serial Ports (McBSP)

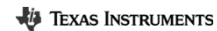
### Device-specific Memory:

- 32-bit DDR3 Interface

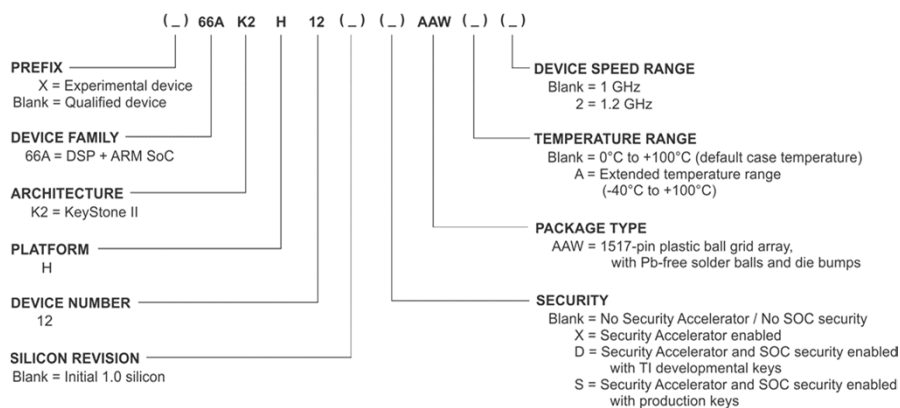


## KeyStone C665x: Key HW Variations

HW Feature	C6654	C6655	C6657
CorePac Frequency (GHz)	0.85	1 @ 1.0, 1.25	2 @ 0.85, 1.0, 1.25
Multicore Shared Memory (MSM)	No	1024KB SRAM	
DDR3 Maximum Data Rate	1066	1333	
Serial Rapid I/O Lanes	No	4x	
HyperLink	No	Yes	
Viterbi Coprocessor (VCP)	No	2x	
Turbo Coprocessor Decoder (TCP3d)	No	Yes	
Network Coprocessor (NETCP)	No	No	



## KeyStone II Part Numbering

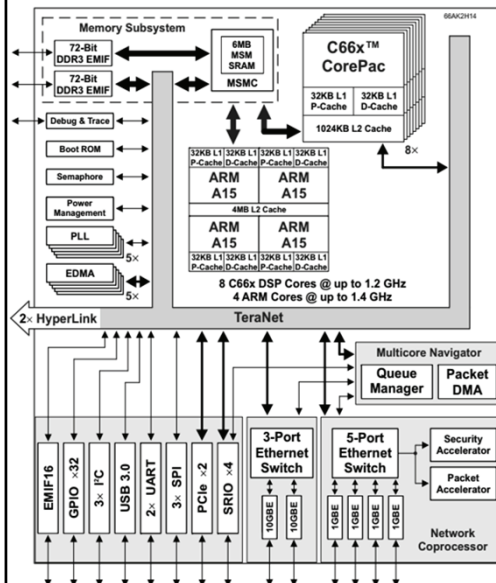


## K2H Compared to K2E

Platform	C66x DSP	ARM A15	Max Clock Ghz	MSMC Shared Memory – MB	Navigator Queues	DDR3 EMIF 72-bit 1600 MT/s	5-Port 1GB Switch	3-Port 10GB Switch	USB 3.0	HyperLink	SRIO x4	PCIe x2	TSIP
K2E	0x to 1x	1x to 4x	ARM = 1.4 DSP = 1.4	2	8K	1x	1x to 2x	1x	2x	1x	--	2x	1x
K2H	4x to 8x	2x to 4x	ARM = 1.4 DSP = 1.2	6	16K	2x	1x	1x	1x	2x	1x	1x	--

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## K2H Platform Device Variations

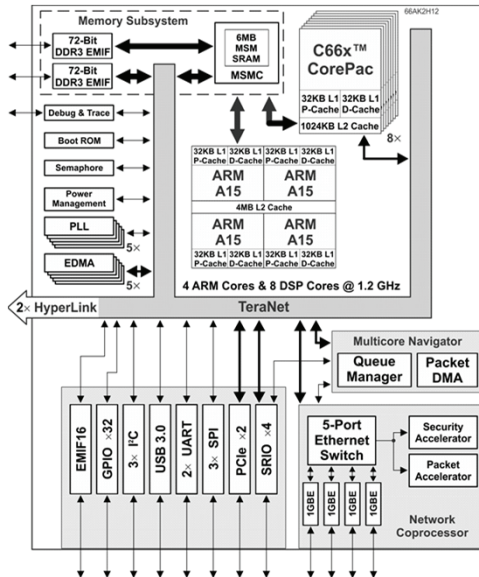


The K2H platform has two variations:

- 66AK2H14
  - 8x C66x CorePacs
  - Quad-ARM A15 CorePac
  - 2x Queue Managers support up to 16K queues
  - 1x 5-port Network Coprocessor (NETCP)
  - 1x USB3.0 to support solid state drive
  - 1x 3 port 10GBE Switch Subsystem

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## K2H Platform Device Variations

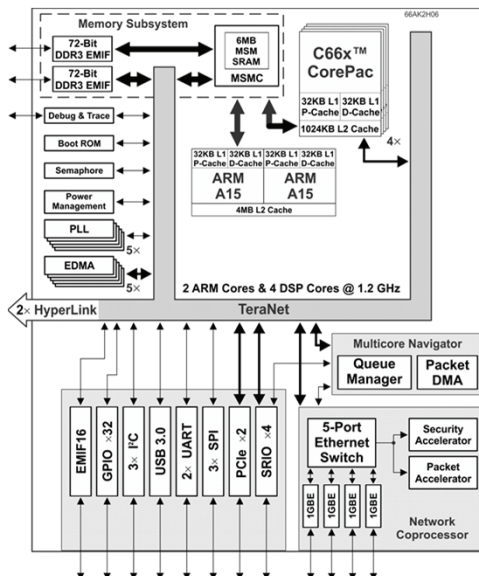


The K2H platform has two variations:

- 66AK2H14
  - 8x C66x CorePacs
  - Quad-ARM A15 CorePac
  - 2x Queue Managers support up to 16K queues
  - 1x 5-port Network Coprocessor (NETCP)
  - 1x USB3.0 to support solid state drive
  - 1x 3 port 10GBE Switch Subsystem
- 66AK2H12
  - Scaled-down version of 66AK2H14
  - 10GBE interface is NOT available.

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## K2H Platform Device Variations

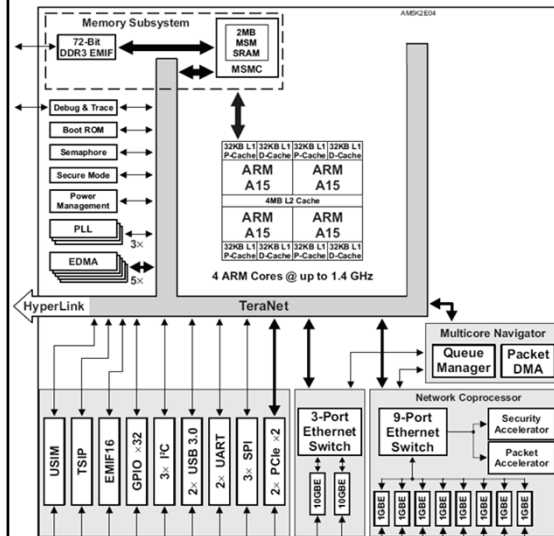


The K2H platform has two variations:

- 66AK2H14
  - 8x C66x CorePacs
  - Quad-ARM A15 CorePac
  - 2x Queue Managers support up to 16K queues
  - 1x 5-port Network Coprocessor (NETCP)
  - 1x USB3.0 to support solid state drive
  - 1x 3 port 10GBE Switch Subsystem
- 66AK2H12
  - Scaled-down version of 66AK2H14
  - 10GBE interface is NOT available.
- 66AK2H06
  - Scaled-down version of 66AK2H12
  - 4x C66x CorePacs
  - Dual-ARM A15 CorePac

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## K2E Platform Device Variations

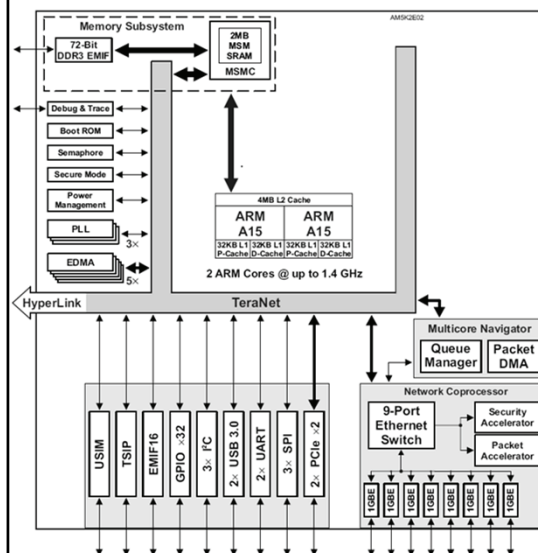


The K2E platform has four variations:

- AM5K2E04
  - First ARM-only TI multicore device
  - Quad-ARM A15 CorePac
  - 1x Queue Manager supports up to 8K queues
  - 1x 9-port Network Coprocessors (NETCP)
  - 1x 3 port 10GBE Switch Subsystem
  - 2-port PCIe2
  - Telecommunications Serial Port (TSIP)
  - 2x USB 3.0 to support solid state drive
  - No SRIO



## K2E Platform Device Variations

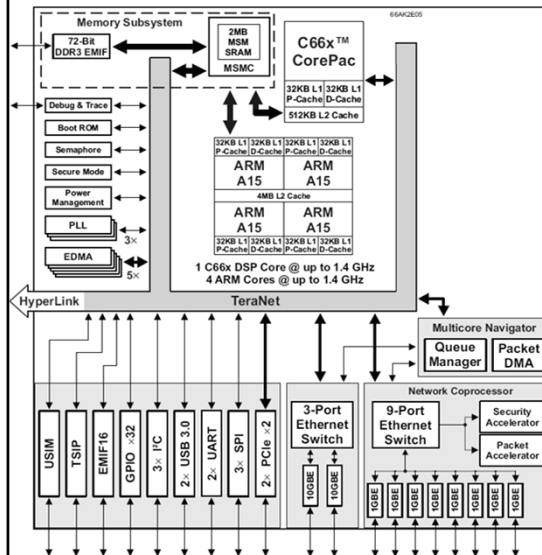


The K2E platform has four variations:

- AM5K2E04
  - First ARM-only TI multicore device
  - Quad-ARM A15 CorePac
  - 1x Queue Manager supports up to 8K queues
  - 1x 9-port Network Coprocessors (NETCP)
  - 1x 3 port 10GBE Switch Subsystem
  - 2-port PCIe2
  - Telecommunications Serial Port (TSIP)
  - 2x USB 3.0 to support solid state drive
  - No SRIO
- AM5K2E02
  - Scaled-down version of AM5K2E04
  - Dual-ARM A15 CorePac
  - 10GBE not included



## K2E Platform Device Variations

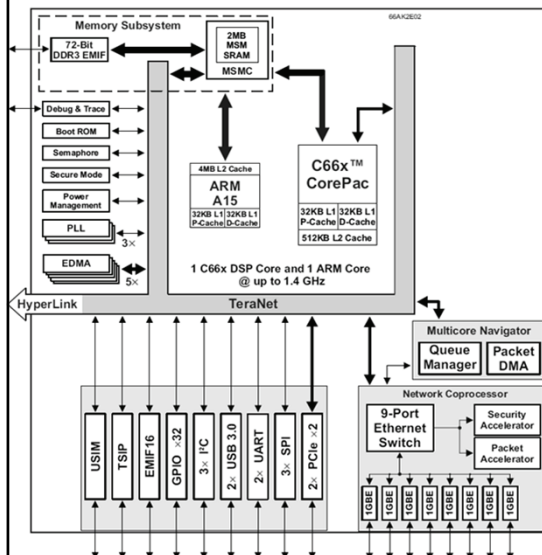


The K2E platform has four variations:

- AM5K2E04
  - First ARM-only TI multicore device
  - Quad-ARM A15 CorePac
  - 1x Queue Manager supports up to 8K queues
  - 1x 9-port Network Coprocessors (NETCP)
  - 1x 3 port 10GBE Switch Subsystem
  - 2-port PCIe2
  - Telecommunications Serial Port (TSIP)
  - 2x USB 3.0 to support solid state drive
  - No SRIO
- AM5K2E02
  - Scaled-down version of AM5K2E04
  - Dual-ARM A15 CorePac
  - 10GBE not included
- 66AK2E05
  - Same as AM5K2E04 with a single C66x CorePac added



## K2E Platform Device Variations



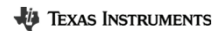
The K2E platform has four variations:

- AM5K2E04
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  - Dual-ARM A15 CorePac
  - 10GBE not included
- 66AK2E05
  - Same as AM5K2E04 with a single C66x CorePac added
- 66AK2E02
  - Same as AM5K2E02 with a single-ARM A15 CorePac and a single C66x CorePac added



# KeyStone I Compared to KeyStone II

IP block	KeyStone I	KeyStone II
ARM Cortex-A15 core	No	4x
MSMC	Ver1.0	Ver2.0
DDR3 EMIF (64-bit)	1x	2x
MSMC SRAM	2 Mbytes	6 Mbytes
DDR3A memory (max)	8 Gbytes	8 Gbytes
DDR3B memory (max)	No	2 Gbytes (for ARM and DSP cores) 512 Mbytes (system masters)
ARM Boot ROM	No	256 Kbytes
OTP memory	No	4 Kbits
Queue Manager Subsystem + PKTDMA	1x	2x
EDMA3CC	3x	5x
EDMA3TC	10x	14x
HyperLink	1 x 4	2 x 4
10 Gigabit Ethernet (10GBE)	No	1 x 2
UART	1x	2x
SPI	1x	3x
I2C	1x	3x
GPIO	1x 16	1x 32
Timer64	8x	20x
USB3	No	1x to 3x
PLL controller + On-chip PLLs	3x	5x
ARM Subsystem ETB (16 KB)	No	1x
DSP TETB (4 KB)	4x	8x
Tracer	16x	32x
MPU	6x	15x
Security Manager	No	1x



## For More Information

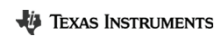
- Device-specific Data Manuals for the KeyStone SoCs can be found at [TI.com/multicore](http://TI.com/multicore).
- Multicore articles, tools, and software are available at [Embedded Processors Wiki for the KeyStone Device Architecture](#).
- View the complete [C66x Multicore SOC Online Training for KeyStone Devices](#), including details on the individual modules.
- For questions regarding topics covered in this training, visit the support forums at the [TI E2E Community](#) and [Deyisupport](#) website.



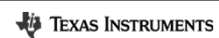




# TI Catalog Processor IDH & Solution Introduction



**Vane**



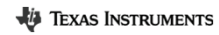
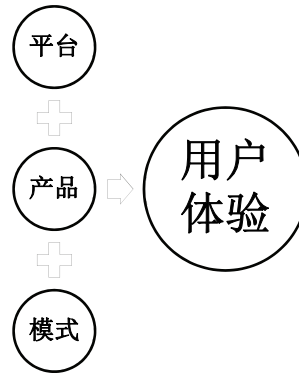


## 😊 风向标核心理念：

✓ 第三方开放云平台

✓ 合作伙伴智能硬件

✓ 多方共赢模式



- ◆ 监测报警
- ◆ 自动录制
- ◆ 实时流媒体监控



安全

- ◆ 提升空气质量
- ◆ 调节湿度
- ◆ 控制温度



健康

- ◆ 设备监控
- ◆ 电量监测
- ◆ 能源管理



能源

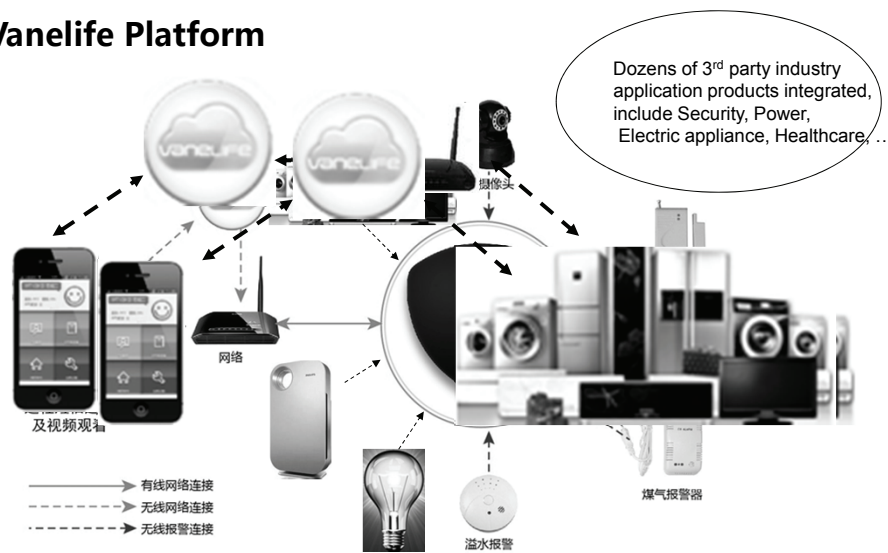
- ◆ 远程控制、监测
- ◆ 一键模式、情景模式
- ◆ 客制化联动模式



模式



## Vanelife Platform



TEXAS INSTRUMENTS

## Vanelife 风向标开放平台



### Features :

- 支持 iOS , Android
- 远程控制 , 监测
- 客制化 一键模式 , 情景模式
- 客制化 联动模式
- 大数据收集 , 分析 , 提案



TEXAS INSTRUMENTS

## Vanelife 风向标开放平台优势



- ✓ 近四年第三方开放 云+硬件 平台持续投入
- ✓ 与智能硬件厂家完全互补合作
- ✓ 云-平台-终端-PCBA-BOM 灵活的接入方式
- ✓ 更快速产品化，导入量产
- ✓ 更具性价比
- ✓ 更好的用户体验



风向标科技官网



风向标科技官方微博



风向标科技微信公众平台



风向标科技天猫旗舰店

### 浙江风向标科技有限公司

地址：上海市徐汇区龙华中路596号绿地中心东楼1701-03室  
电话：+86 (021) 6433-3233  
传真：+86 (021) 5186-2723  
邮编：ZIP200032



# Embest



## About Embest

Embest is a leading global solution provider for easy-to-use development tools, industrial control boards and design services based on the ARM Technology. The products and design services will make electronics development faster and more reliable, so that customers can save development time and process and improved product quality with an obvious cost down.

Embest was established in China since year 2000, with 150 staffs now, among them there are 80 experienced engineers in software, hardware design and testing. The company was acquired by Premier Farnell in June, 2012, a listed company in UK with a history of more than 70 years in electronics distribution business. Embest is the strategic partner of ARM and TI.



## Embest products based on TI Technology



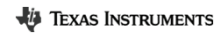
element14 BeagleBone Black(Rev C)  
Based on TI AM3358 ARM Cortex-A8 processor,  
1GHz, 512MByte DDR3, 4GB eMMC with OS  
Debian7.4



SBC8600B  
Core board based on TI AM3359 ARM Cortex-A8  
MPU @720 MHz, 512MByte DDR3 SDRAM,  
512MByte NAND Flash



Devkit 8600  
Evaluation board Based on TI AM3359  
ARM Cortex-A8 MPU @720MHz,  
512MByte DDR3 SDRAM, 512MByte NAND Flash



## Design Service

Embest provides comprehensive services to specify, develop and produce products and help customer to implement innovative technology and product features. Progressing from prototyping to the final product within a short timeframe and thus shorten the time to market, and to achieve the lowest production costs possible.

Embest provides customized design service based on TI technology for global customers. Embest can help customer on:

- Design files
- Image files
- Software source codes
- Relevant documents
- PCB/PCBA

### Contacts of Custom Services:

[globalsales@embest-tech.com](mailto:globalsales@embest-tech.com)



# Serial Design



## TI Cortex-A8

### SD-AM3358-EVM/SD-AM3358-SOM

Ethernet接口: 2个, 千兆  
LCD接口: 1个, 16/24bit  
RS232接口: 2个  
RS485接口: 1个  
CAN接口: 1个  
USB Host接口: 1个  
USB OTG接口: 1个

Linux  
Linux v3.12.10  
AM335xSDK 07\_00\_00

MMC接口: 2个  
ADC接口: 4个, 12bit  
RTC: 1个  
JTAG接口: 1个, 14-Pin  
GPMC总线接口: 1个, 8bit  
外设接口: UART、SPI、  
McASP、I2C、PWM

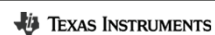
Android  
Android Jelly Bean v4.2.2  
Linux Kernel v3.2  
SDK: v4.1.1



Starterware  
V2.00.01.01

#### 开发调试仿真器

开发系统自带隔离, 可靠性更高, 可以满足  
工业调试  
支持TI全系列DSP、ARM处理器  
支持Code Composer Studio v4和以上版本





## TI AM335x参考设计

**HMI**：电梯招呼板，热电厂控制系统，双彩LED控制等

**EPOS机**：手持终端（无线/有线），台式终端（无线/有线）

**医疗终端**：生化分析仪，黄疸分析仪，血液分析仪等

**智能家居**：智能遥控器，智能家居中央控制，门禁控制等

**家用电器**：冰箱，洗衣机，空调，热水器等

**消费类产品**：GPS，PDA，PAD等

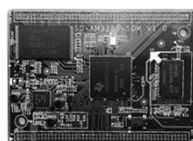
**工业控制**：PLC，机器人，工控机，工业以太网，数据采集，运动伺服等



物流扫码枪：



最小系统定制板  
(SOM)



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## Forlink

TEXAS INSTRUMENTS

## A8的性能 ◆ ARM9的价格 飞凌嵌入式携手 TI 引领 A8 进入普及时代

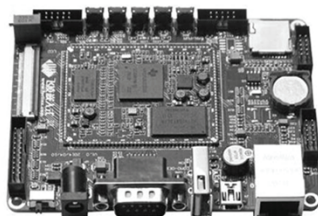
强大的真工业级开发板——OK335xS-II

800MHz  
主频

1600  
Dmips

硬件3D  
图形加速

-40°C~+85°C  
运行温度



| Cortex-A8 TI AM3354处理器  
| 多总线，双网口支持，6路串口  
| 真工业级开发板，运行温度-40°C~+85°C

海量测试程序和应用例程



Linux  
用户使用手册



Wince  
用户使用手册

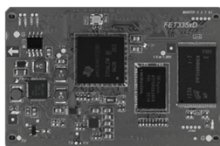
惊爆价 **298** 元

TEXAS INSTRUMENTS

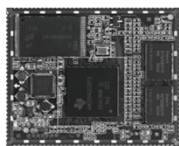


## Forlinx专注嵌入式领域20年

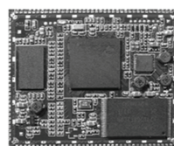
ARM核心控制板卡制造专家 嵌入式解决方案专业提供商



FET335xD



FET335xS



FET335xS-II

### 应用案例



矿井信息采集系统



医疗标签打印机设备



汽车仪表盘



智能家居中央控制系统

TEXAS INSTRUMENTS

# Witstech

TEXAS INSTRUMENTS

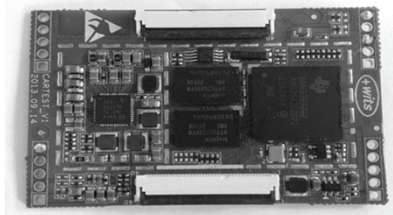
## 南京九能科技有限公司

南京九能科技有限公司成立于2004年,长期从事智能数码产品开发和生产。其核心团队由海外留学高级学术人才,国家重点实验室研发人员,以及在国际大型科技企业长期工作的高级专家组成。团队不仅具备强大的产品研发能力,也具备丰富的企业管理经验。

九能科技和美国德州仪器公司(TI)在内嵌式平台进行长达5年深入的战略合作,成功的推出了基于DM3730和AM335 的整体解决方案平台。该平台已被各行业众多客户成功应用于工业级智能物流终端,智能家居,智能旅游等领域。

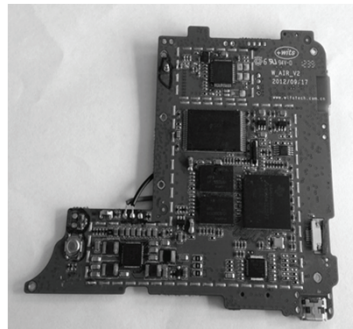
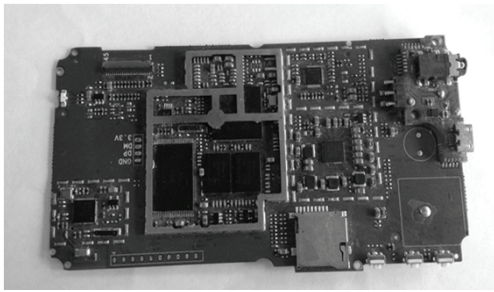
放眼未来,智能型生活已经朝我们大步走来。九能科技将以科技为基础,人才为框架,充分借助金融,互联网的翅膀,凭借优质产品和经营诚信,在智能设备领域做出重要贡献。

产品简介:



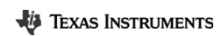
基于AM335X核心板

TEXAS INSTRUMENTS

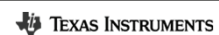


基于AM335X智能终端主板  
基于AM335X人机界面主板

- 地址：南京市秦淮区公园路42号体育大厦1803室
- 电话：025-83115162
- Email:support@jiunengtech.com



**EMA**



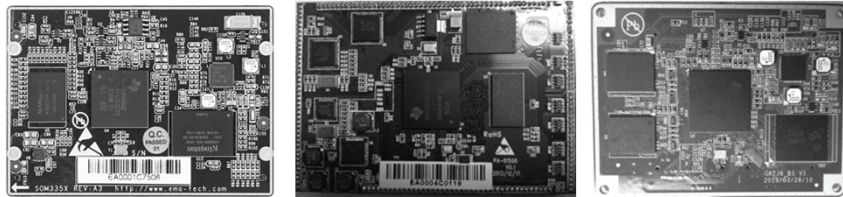
## EMA SOM335x 核心板

**SOM335x**是基于TI **AM335x**系列处理器的低功耗嵌入式核心板。相比 beagle bone等模块，更具产品化，更稳定，资源更丰富；

工业级设计，工作温度-40℃~85℃，通过盐雾试验，适用于工业应用；

提供产品级的Linux 3.2 + QT4.5+SQLite、工业级Android 4.0系统支持；

**EMA** 提供多种规格核心板，适合不同场合的应用；



TEXAS INSTRUMENTS

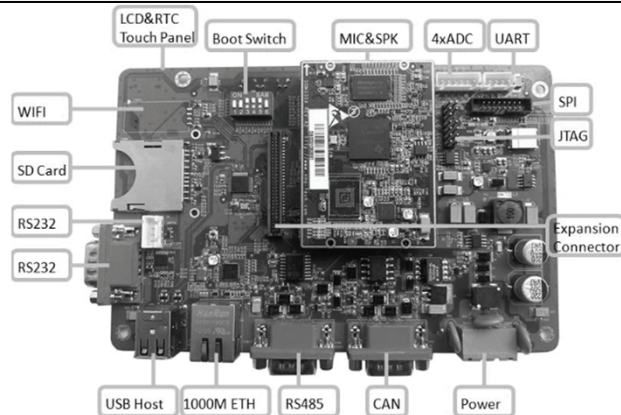
## 基于AM335x的工业级主板HMI335x

基于SOM335x核心板，通过EMC/EMI测试，低成本、低功耗、功能齐全

9~24V宽压输入，提供HMI应用常用接口：CAN、RS485、RS232

支持Linux3.2 + QT4.5 + SQLite软件方案，或Android4.0 + EMA-I/O方案

典型案例：家庭中央空调控制器、工业HMI、银行等行业自助终端

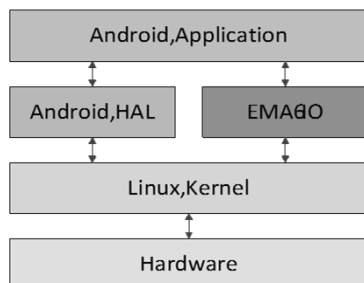


TEXAS INSTRUMENTS



## SOM335x Android软件 - EMA-IO

- EMA-IO Android系统中间件软件，突破了标准Android系统的资源接口限制, 使得应用程序访问底层设备成为现实。从而填补了Android系统在专用领域发展中的空白局面。
- 标准 Android 系统在加载 EMA-IO 后, 应用程序只需通过简单的编程实现, 即可安全地访问所需底层设备, 为用户节省大量开发成本。
- EMA-IO 涵盖CAN、GPIO、I2C 以及各类基于UART的设备。



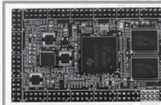
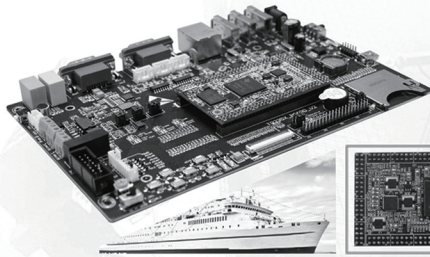
**Embedsky**

## 公司及产品简介

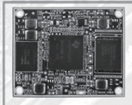
广州天嵌计算机科技有限公司是一家专业提供嵌入式开发和解决方案的高科技企业，在行业内有很高的知名度。雄厚的研发实力和优质的售后服务，让您的产品研发更简单！更快捷！更有保障！

TQ\_335x是基于TI-AM335x（Cortex-A8核心架构）系列芯片设计的一款性能稳定的开发平台。产品适用于：工业控制系统、HMI人机界面、医疗电子、智能仪表、智能家居控制……。

## TQ 3358工控系列



TQ 3358 Core A



TQ 3358 Core B



TQ 3358 Core C

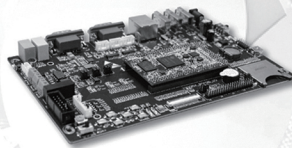
## TQ 3358 成功案例



工业控制—HMI



商业消费—智能检测仪



智能家居—智能网关



医疗电子—6通道荧光仪

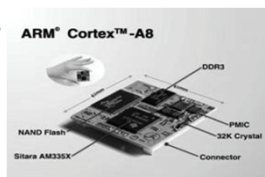
# StrongKiwi

TEXAS INSTRUMENTS

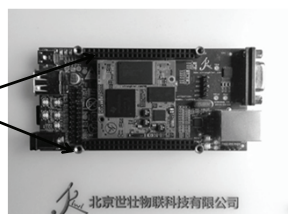
## StrongKIWI Product

### - Cortex – A8 Core Board

To be the authorized 3<sup>rd</sup> design party of TI, StrongKIWI released the core board with the Cortex-A8 minimum system.



配套底板：  
扩展槽和  
**Beaglebone Black**  
完全兼容。



特 点	
处理器	AM3352AZCZ100 ARM Cortex-A8 32位 RISC 微控制器
图像引擎	SGX530 3D (与处理器型号相关)
SDRAM	1Gbits DDR3
FLASH	1Gbits NAND
PCB	6层
电源管理	TPS65217C
外接接口	间距为0.8mm的82B标准接口, 80pinsX2
尺寸大小	42 (W) x 42(L) x 7.7(H) mm
整体重量	12g

软件支持  
None OS / Linux /Android / Windows Embedded

游戏外设  
物联网自动售货机  
衡器  
家庭工业自动化  
高端玩具  
教育控制台  
智能收费系统  
消费类医疗器械  
打印机  
解决方案

TEXAS INSTRUMENTS



## StrongKIWI's Service

圆产品梦  
就这么简单!

BeagleBone to **Bingo!**

超值核心板  
42x42mm

HOW?  
I don't know, How to do!!

Cortex™-A8 (AM335X)  
NAND Flash >Gbits  
DDR3 SDRAM >Gbits  
工业级插插件 80pinsX2  
PMIC(TPS65217C)

免费软件升级移植  
安装1个免费软件  
升级包即可

高性价比硬件服务  
可提供配套底板:  
原理图设计、PCB  
布板和样机制作服务

TI 第三方合作研发机构 -  
北京世壮物联科技有限公司 ( StrongKIWI )  
电话 : 010-67857759  
邮箱 : Marketing@strongkiwi.com

 TEXAS INSTRUMENTS

Assem

 TEXAS INSTRUMENTS

## Beijing Assem Technology LTD.,Co.

### 1. 在行业专用设备领域，有着领先技术和自主知识产权的系统软件设计

- 对嵌入式Linux内核进行了深度优化
- 针对长期使用的特点，对外围设备的驱动程序进行了大量的优化

### 2. 在行业专用设备领域，有着领先技术的硬件设计

- 能够灵活运用特有的技术手段发挥产品的性能，同时又能减少成本
- 十分熟悉可与ARM产品匹配使用的外围器件，保证产品的稳定性

### 3. 从研发到量产成品的全过程经验与技术

- 针对ARM系列处理器有丰富的工业产品设计经验
- 有多年整机成品批量生产的经验，充分了解产品的整个生产过程
- 十分了解产品在生产过程中的问题，在产品设计时即以满足大批量生产和苛刻使用为目标




## Beijing Assem Technology LTD.,Co.

- 海尔集团物联网家电核心合作伙伴，量产智能家电信息化模块唯一供应商
- 卡萨帝冰箱/洗衣机物联网模块产品，海尔空调物联网模块产品
- 海尔医疗设备智能控制产品
- 海尔云平台技术服务方
- 海尔智能家居对讲系统设计和制造方
  - 基于TI Sitara AM335X 处理器
  - CORTEX-A8处理器完美替代ARM9，HMI操作友好速度快
  - 回声消除、安防、按键、音频播放/录音、MMC系统更新、网络等模块
  - 通过各类电气特性测试的工业级平台
- 世界最大金融机具公司VeriFone针对国内市场研发的第一个产品的嵌入式操作系统技术提供商
- 国家信息中心政务虚拟化系统桌面终端



# ENE A

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## Enea (瑞典宜能) 公司简介

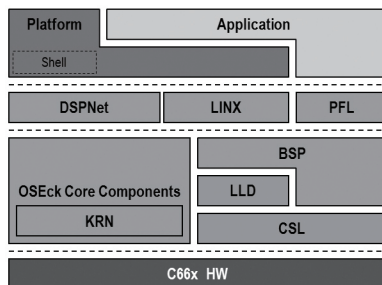
- Enea (宜能)是全球领先的嵌入式软件提供商，1968年在瑞典成立，1989年上市。  
解决方案包括：多核芯片RTOS软件平台、分布式通讯中间件(IPC)、CGL实时Linux等。  
。客户产品如：基站、雷达、声纳、电子对抗、航空航天、网络设备等。
- Enea 是 TI 的全球白金(Platinum)合作伙伴，提供针对 TI 多核 DSP/SoC(如 C6678/K2/66AK) 整套的高性能基础软件开发平台，包括：  
☐ RTOS软件平台   ☐ 分布式中间件   ☐ 开发调试工具
- Enea 部分客户列表：



[info\\_china@enea.com](mailto:info_china@enea.com)

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- RTOS, 中间件, 工具



- OSEck专门针对TI C66优化模块
- TI 软件模块



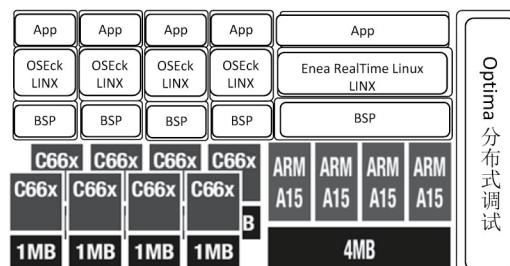
1. 针对TI KeyStone Multicore Navigator优化的OSEck 实时操作系统。
2. 针对核间通讯优化的进程间通讯模块—LINUX IPC
  - ✓ DSP内核间 LINUX CDMA通讯
  - ✓ DSP间/板卡间LINUX Rapid/IO通讯(Message和DIO)
  - ✓ DSP间/板卡间的LINUX Ethernet通讯
3. 针对各种外设优化的BSP驱动, 包括CDMA, Ethernet, Rapid/IO等。
4. DIO 高性能SRIO通讯机制
5. 高性能的DSPNet TCP/IP协议
6. Shell 用户界面
7. 针对 UDP包优化的网络加速软件模块 – PFL。
8. 系统死后分析工具—Core Dump
9. Eclipse系统级调试工具—内存、CPU Profile等。
10. Log Analyzer- 离线日志分析工具

info\_china@enea.com



平台- (RTOS, 实时Linux, 中间件, 工具)

1. **OSEck – 多核DSP软件平台**
    - ✓ OSEck实时稳定的内核,
    - ✓ OSEck LINUX – 支持多DSP核无缝通讯的进程间通讯模块
  2. **Enea Linux – 实时商业Linux**
    - ✓ 基于Yocto的图形Linux开发调试环境
    - ✓ Enea 实时Linux优化
  3. **LINUX IPC – ARM核(Linux) 到DSP核(OSEck)的无缝 进程间通讯 模块**
    - ✓ 支持多芯片, 多板卡的无缝通讯
    - ✓ RapidIO, Ethernet, 共享内存等。
  4. **Optima/CDA – 优化调试工具**
    - ✓ 开发、调试
    - ✓ 死后分析
    - ✓ 性能调优工具。
  5. **DSP BootLoading**
    - ✓ Enea Linux下载DSP映像并启动DSP.
- 
- |             |             |             |
|-------------|-------------|-------------|
| App         | App         | App         |
| OSEck LINUX | OSEck LINUX | OSEck LINUX |
| BSP         | BSP         | BSP         |
- C66x C66x C66x



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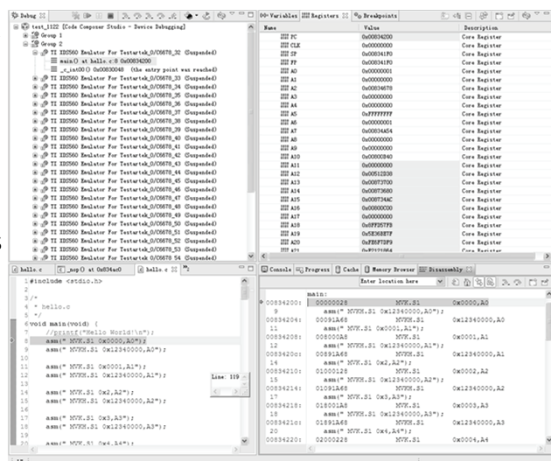


# Testartek(泰星达)



## 泰星达C6678 综合调试平台

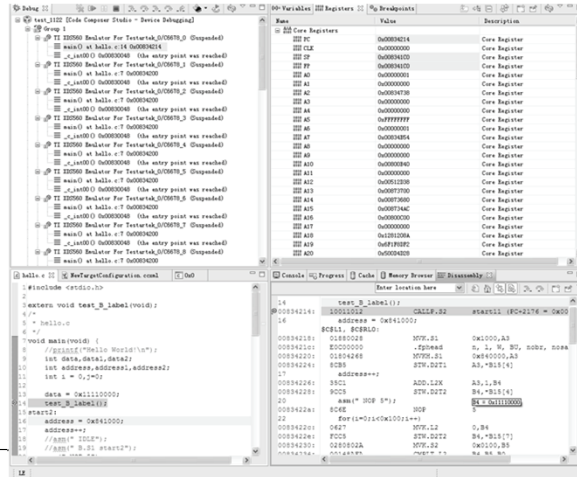
- Testartek TI C667X 系列综合调试平台，可以在不用硬件仿真器情况下对C 6678芯片进行各种调试。降低了开发、测试、整合及维护应用程序的难度，满足于单核及多核心、海量处理器的超级应用。尤其是大量DSP的调试十分方便。
- 满足跨板卡，不同处理器之间的调试。
- 与CCS无缝兼容，用户界面仍是CCS，CCS版本升级对其无影响。
- 能够实现大量处理器的同时调试和监测。
- 便于海量运算的处理器管理，通信调度。
- 可以通过不同的接口来进行调试，比如：PCI-E，以太网等。
- 无需硬件仿真器实现下载，运行，断点，单步，观察内存等调试功能



# 泰星达C6678 综合调试平台

- 针对DDR3, EDMA, IDMA, SRIO, GE等, 开发了更高效的通信模块, 非常适用于视频算法、大数据处理等每秒钟上万次通信的算法

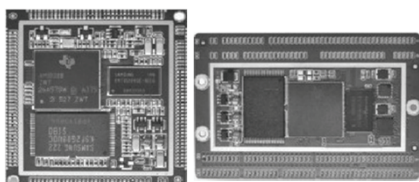
- 泰星达(北京)科技有限公司
- 王寿龙 13301197747



Lierda

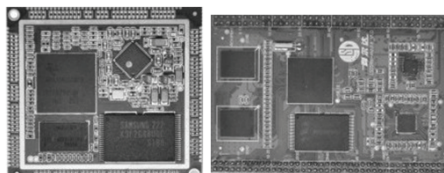


### ➤ AM1808标准核心板



ARM926EJ-S内核，最高主频达到456MHZ。本核心板带有128MB的DDR2、256MB的Nand Flash。

### ➤ AM335x标准核心板



Cortex-A8内核，最高主频达到720MHZ。本核心板带有256MB的DDR2、256MB的Nand Flash。

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EA

### ➤ 智能HMI显示终端

#### HMI-显示板



#### 产品简介

本方案的目的在于满足物联网时代智能家电追求高用户体验，高可扩展性的人机交互界面的要求。使用AM335X A8处理器，搭载Android4.2.2操作系统，配置10点超灵敏电容触摸屏，通过谷歌免费提供的SDK可以方便地设计出功能强大且体验上佳的人机界面，同时预留wifi、以太网等接口，可轻松实现联网等扩展应用。

#### 性能特点

- Android4.2.2操作系统
- 1GHz cortex-A8 cpu
- 预留1路USB host模式和1个OTG接口
- 100M/10M以太网、WIFI802.11 b/g/n
- 支持6个uart，支持SPI、CAN、i2c总线扩展
- 支持音频输出及录音功能

#### 技术参数

- 输入电压：5V-42V
- 操作系统：Android4.2.2
- 处理器：AM3358(1GHz Cortex-A8)
- 运行内存:512MB DDR3
- 显示屏：7inch 800\*480 1670万色 电容屏

#### TI main device

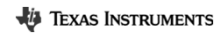
AM335X  
TPS65910  
TLV320AIC3106

#### Business Model

- system solutions

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# Advantech



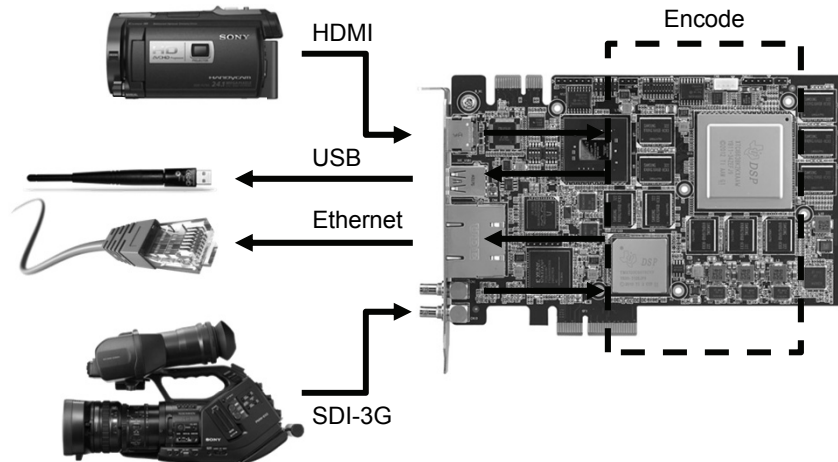
## Advantech Products for HEVC Encode & Decode (w/ SMPTE 2022 & SDI-3G Input)

Product	DSP-8681	DSP-8682	DSP-8683	DSP-8684	DSP-8685	DSP-8901	HVS-9600
Picture							
DSP Core	C66x x32	C66x x64	C66x x16	C66x x32	C66x x32	C66x x160	C66x x160
ARM Core	-	-	A15 x4	A15 x4	A15 x4	-	A15 x80
HEVC Encode	1080p60	4Kp30	1080p30	1080p60	1080p60	4Kp60	4Kp120
HEVC Decode	4Kp60	4Kp60 x2	4Kp30	4Kp60	4Kp60	4Kp60 x5	4Kp60 x5
SDI-3G	-	-	In/Out	In/Out	-	-	-
HDMI	-	-	In	In	-	-	-
SMPTE 2022	-	-	-	-	10GbE In	-	10GbE In
IP	1GbE	1GbE x2	1GbE x2	1GbE x2	1GbE x1	10GbE x2	10GbE x20
PCIe	Gen2 x8	Gen3 x8	Gen2 x2	Gen3 x8	Gen3 x8	-	-
Power	54W	110W	40W	70W	70W	300W	(TBD)



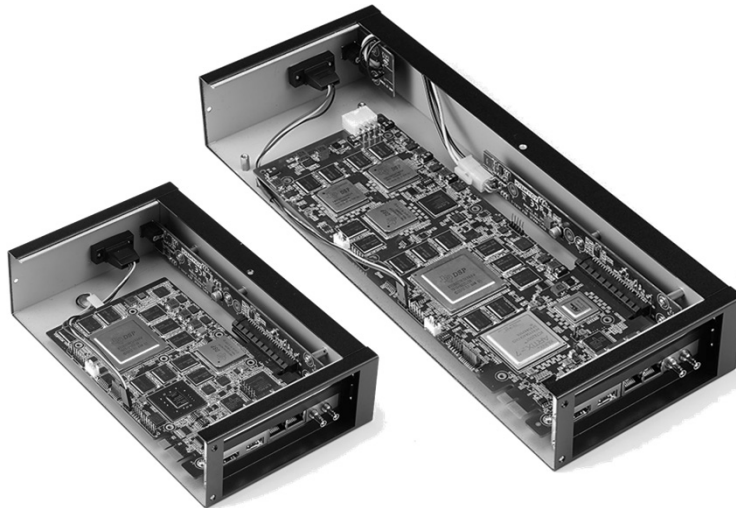


### DSPC-8683/8684 KeyStone-2 PCIe Card Use Case (HEVC Video Acquisition, Encoding & Streaming)



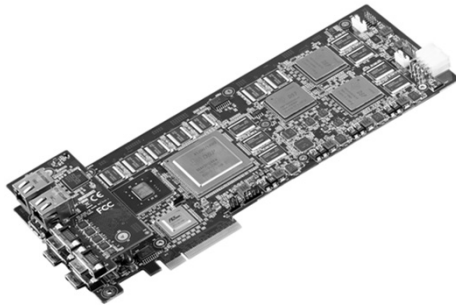
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### DSPC-8683/8684 KeyStone-2 Standalone Use Case (HEVC Video Acquisition, Encoding & Streaming)



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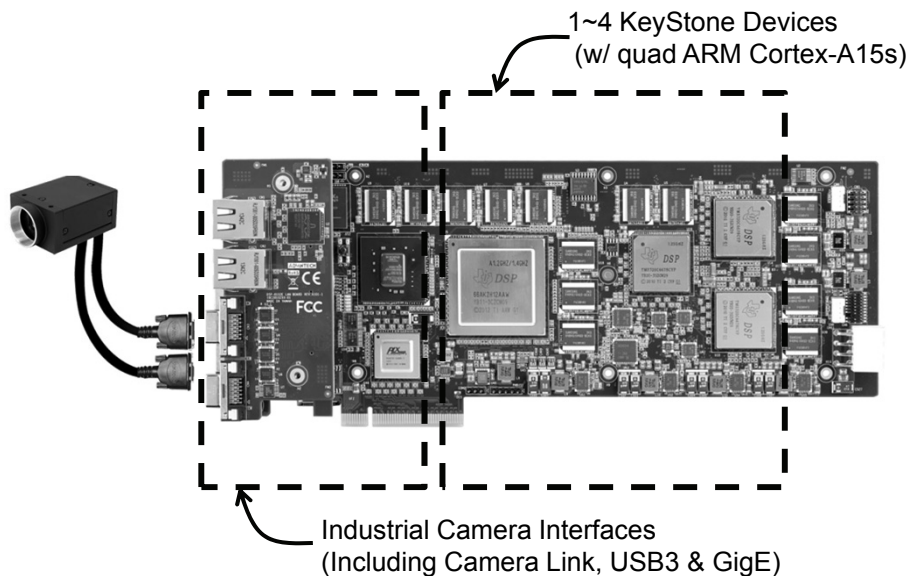
## DSP-8102 PCIe Card for Machine Vision (Intelligent Frame Grabber w/ KeyStone-2)



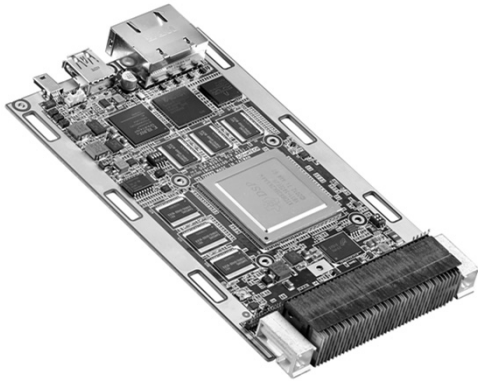
- **TI KeyStone-2 (12-core) x 1**
  - 4x ARM Cortex-A15 cores
  - 8x C66x DSP cores
- **TI KeyStone-1 (8-core) x 3**
  - 8x C66x DSP cores
- Xilinx Kintex-7 reprogrammable FPGA
- Dual-Full Camera Link input
- GbE & USB3 connectors
- Full-Length PCIe card (8-lane)
- Include video analytic SDK
- Target applications including
  - frame grabber
  - machine vision & analytic
  - computing acceleration



## DSP-8102 PCIe Card for Machine Vision (Intelligent Frame Grabber w/ KeyStone-2)



## DSP-8201 OpenVPX 3U KeyStone-2 Blade (High-Speed Signal Processing)



- **TI KeyStone-2 (12-core) x 1**
  - 4x ARM Cortex-A15 cores
  - 8x C66x DSP cores
- 1/10 Gigabit Ethernet, Serial RapidIO, PCI Express and HyperLink backplane interconnection
- IPMC support
- Target applications including
  - mission critical
  - defense



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Lauterbach

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# Lauterbach = 34 Years of Confidence

- Worldwide market leader for hardware assisted debug tools
- Founded in 1979 by Lothar Lauterbach
- Headquarters near Munich in Germany
- ~ 120 employees, ~ 150 M\$ revenue in 2013
- ~ 100,000 installed debuggers

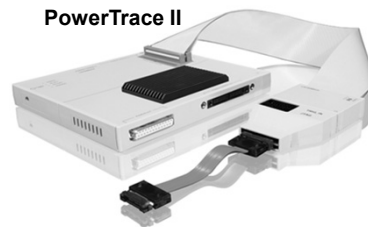


## Powerful Hardware Options

PowerDebug II



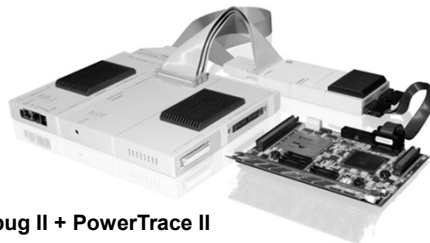
PowerTrace II



μTrace



PowerDebug II + PowerTrace II



**Thank You !**





# TI Keystone II ARM Subsystem Intro

KeyStone Training

TI Information – Selective Disclosure

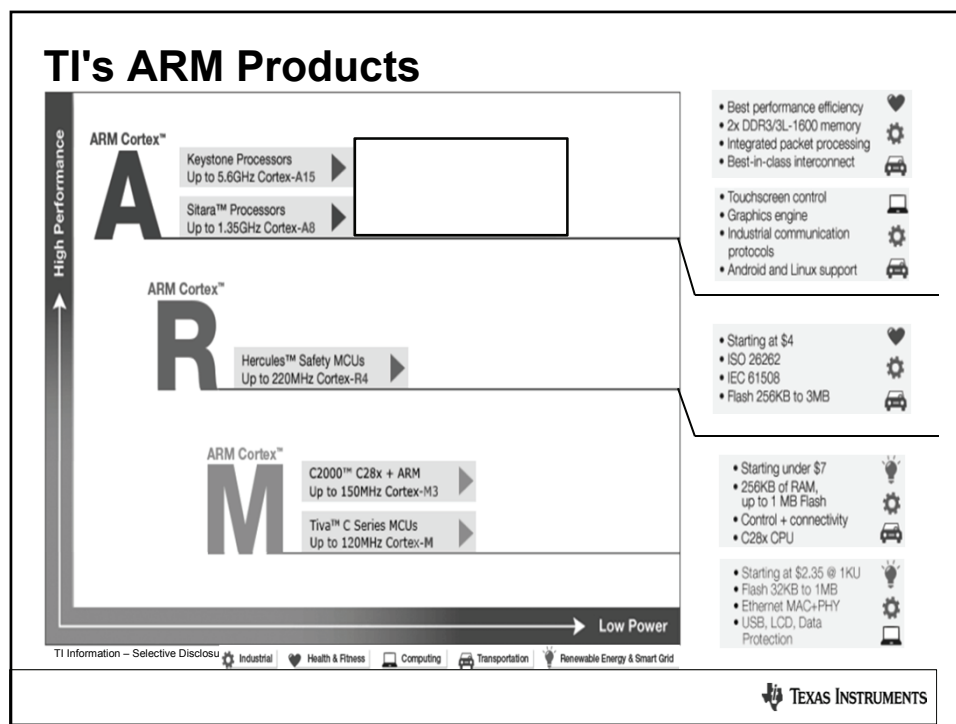


## TI Keystone II ARM Subsystem Introduction

- **ARM Overview and Basics**
  - ARM Architecture and Categories
- **ARM Cortex-A15 in TI Keystone II Devices**
- **Software Provided of TI Keystone II ARM Parts**

TI Information – Selective Disclosure





## TI Keystone II ARM Subsystem Introduction

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  - Cortex-A15 Features in TI Keystone II Devices
  - Basic Benchmark Comparison
  - Interconnections and Buses
  - Memory Architectures
  - ARM Interrupt Sub-modules
  - SoC Boot with ARM Master
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## Why Cortex-A15?

### Wild Application Fields

- High performance computing
- Low power server
- Wireless infrastructure
- High-end digital home
- Mobile computing

### Open Software Ecosystem

- Linux and Ubuntu
- Java SE, Java FX
- Android
- Microsoft Windows Embedded

### Why Cortex-A15

### Advanced Architecture

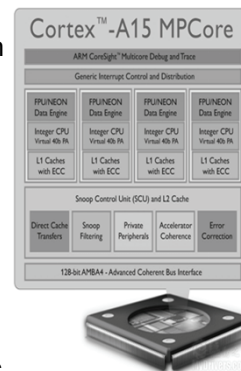
- Full ARMv7-A Architecture Instruction Set
- Up to 4MB low-latency L2 cache
- Up to 1.4-GHz Processor Core Speed
- AMBA 4.0 AXI ACE Master Port
- Support NEON, VFP V4, and Thumb V2

### Popular Features Support

- Up to 4 Core SMP
- Support LPAE for more than 4GB DDR3
- Virtualization support for virtual machine
- Trust Zone support with Monitor mode
- Java and Jazelle environment support

## Cortex-A15 Features in TI Keystone II Devices

- Cortex A15 MPCore processor
  - Cortex A15 MPCore version **R2P4**, 1, 2, 4 cores in one cluster
  - **Standard** ARM v7-A architecture
  - Full support of **Trust Zone** and **Virtualization** features
  - **Multi-issue, out-of-order, superscalar pipeline**
  - **Dynamic branch prediction** with BTB and GHB, a return stack, and an indirect predictor
  - Per core **NEON** (SIMDv2) and **VFP** (VFPv4)
  - L1 instruction and data cache of **32 KB, 2-way, 16 word line** with **128 bit interface**
  - Integrated L2 cache **up to 4MB, 16-way, 16 word line, 128-bit interface** to L1 along with **ECC/parity**
  - **128-bit AMBA4 AXI** with ACE protocol, 32-bit APB

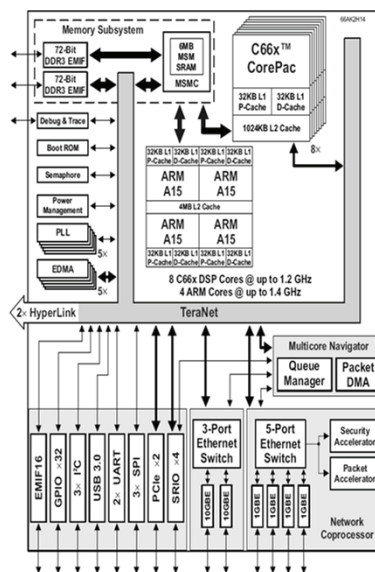


TI Information – Selective Disclosure

## Flexible Configurations in TI Keystone II Devices

Keystone II Multicore DSPs				
	1 Cortex - A15	2 Cortex - A15	4 Cortex - A15	
0 TMS320C66x DSP		AM5K2E02	AM5K2E04	
1 TMS320C66x DSP	66AK2E02		66AK2E05	
4 TMS320C66x DSP		66AK2H06		
8 TMS320C66x DSP			66AK2H12 66AK2H14	

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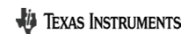
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## Benchmarks – Core, Memory Latency

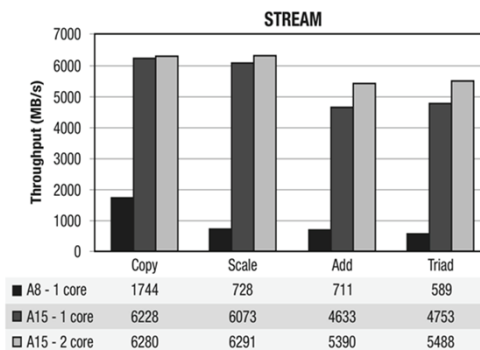
- Dhrystone, DMIPS/MHz, CPU core and L1 only
  - **3.5DMIPS/MHz** (highly dependant on compiler)
  - **19600DMIPS** with KeyStone II Quad-ARM Cortex-A15 CorePac at 1.4GHz
- Floating point
  - Quad single-precision IEEE-754 FMAC per cycle
- Memory Latency, load-to-use latency
  - 4cc L1D hit, typically hidden by A15 micro architecture
  - 20cc L2 hit (4MB)
  - MSMC2 SRAM: ~50cc
  - External Memory: ~100ns (~140 cycles) L2 miss to DDR page that is open

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## Benchmark Comparison – Bandwidth

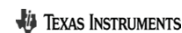
- STREAM benchmark is the industry-standard benchmark for the measurement of sustainable memory bandwidth.
- It including:
  - COPY: floating-point loads and stores
  - SCALE: floating-point multiply
  - SUM: floating-point add
  - TRIAD: floating-point multiply and add



Cortex-A8: 1 GHz, 64-bit DDR2-1333 memory, Codesourcery GCC v4.6.3 compiler;  
Cortex-A15: 1.4 GHz, 64-bit DDR3-1600 memory, Linaro GCC v4.6.3 compiler

- These results represent substantial improvements resulting from the Cortex-A15 processor's VFPv4 floating-point processing and from Keystone II's MSMC-based path to memory.
- <http://www.ti.com/lit/wp/spry223/spry223.pdf>

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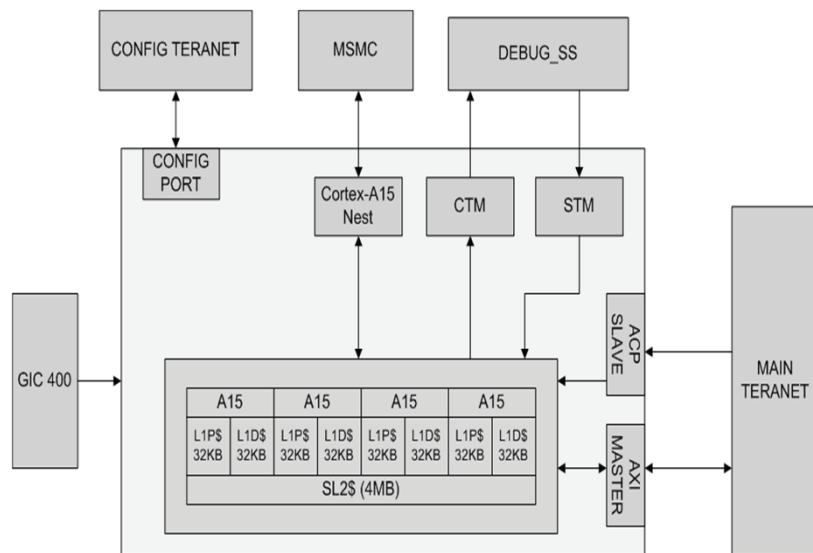
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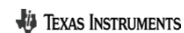
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## Functional Diagram on 66AK2H12



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## **Cortex-A15 Memory Management Unit (MMU)**

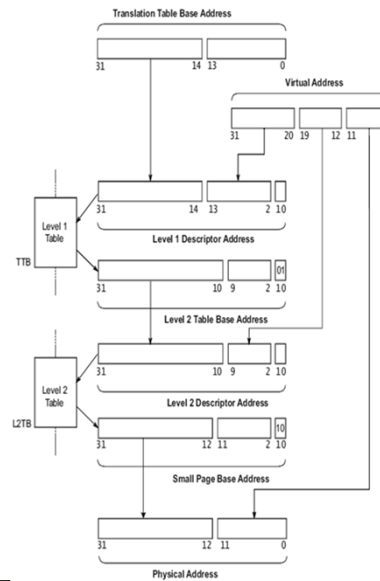
- Logical-to-Physical memory translation:
  - User protected
  - Hardware manages the actual memory
- Large physical addressing up to 40-bit (1TB)
- Up to 3-level data structure for virtual 4kB page:
  - Two levels for virtual 2MB pages (Linux huge pages)
  - Translation Look-aside Buffers (TLB) cache one page of address translations per entry to speed up the translation process:
    - L1 instruction access
    - L1 data access
    - L2 TLB

TI Information – Selective Disclosure

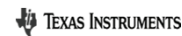


## Cortex-A15 Memory Management Unit (MMU)

- The core performs MMU to translate virtual addresses generally as follow steps:
  - Core issues a 32-bit virtual address
  - MMU uses several bit-fields of virtual address to index TLBs, or perform translation table walk if missed in TLBs
  - MMU combines the physical address MSBs from the page table entry with previous LSBs to the actual physical address with the page table defined memory attributes

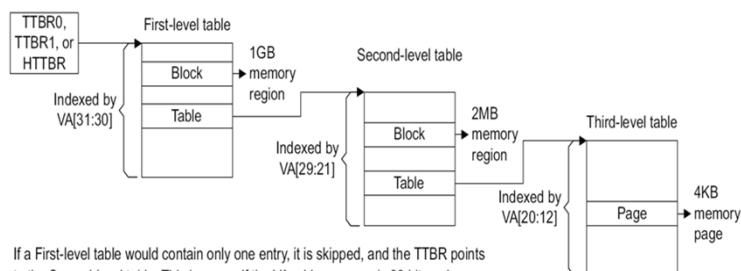


TI Information – Selective Disclosure



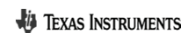
## Cortex-A15 MMU - LPAE

- Cortex-A15 support Large Physical Address Extensions (LPAE) for connecting physical memory larger than 4GB
- LPAE provides:
  - New translation table format – long descriptor format
  - 32-bit virtual addresses, with 40-bit physical addresses
  - New memory attributes added



If a First-level table would contain only one entry, it is skipped, and the TTBR points to the Second-level table. This happens if the VA address range is 30 bits or less.

TI Information – Selective Disclosure



## Cortex-A15 Cache

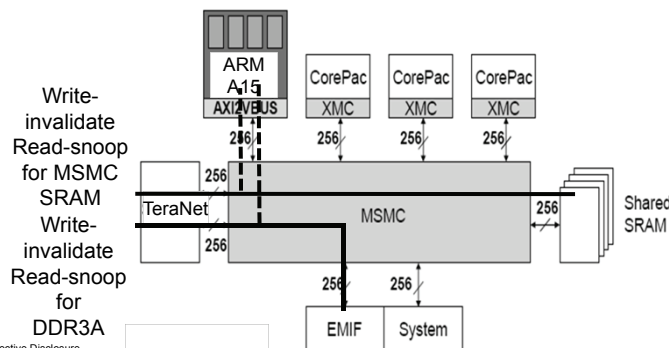
- Cortex-A15 implements with **fixed 32KByte L1** instruction and data cache per core
- Cortex-A15 implements with **up to 4MByte L2** shared cache per cluster
- Cortex-A15 can **automatically maintain data coherency across other L1/L2 caches** if:
  - Configure with correct memory type(normal, shared, etc)
  - CPUs are in the same domain
- MMU uses translation tables to control which memory area are cached
- Caches handle data in lines (64 bytes per line)

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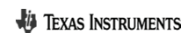


## I/O Coherency

- Keystone II devices support memory coherency accesses between A15 core(s) and other non-core master peripherals (Ex: EDMA) in the DDR3A and MSMC SRAM space.(not for DDR3B, each DSP cores or between A15 cores and DSP cores)
- Non-core master can recognize and access the A15 core L1D and L2 cache to maintain the coherency through AMBA-4 ACE



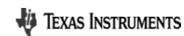
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## TI Keystone II ARM Subsystem Introduction

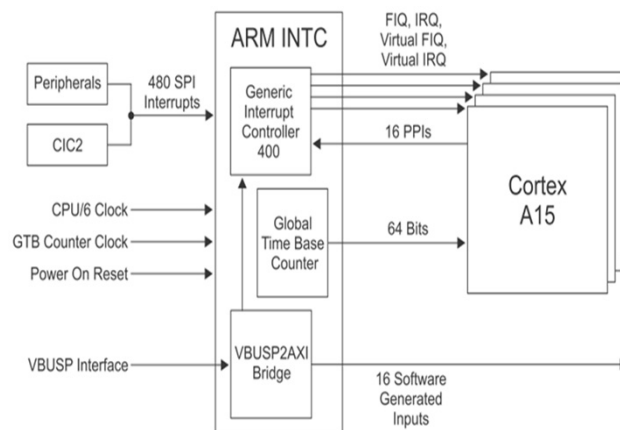
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  - Basic Benchmark Comparison
  - Interconnections and Buses
  - Memory Architectures
  - ARM Interrupt Sub-modules
  - SoC Boot with ARM Master
  - ARM Communication with DSP
- **Software Provided of TI Keystone II ARM Parts**

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## ARM INTC on Keystone II Devices

- ARM INTC (AINTC) subsystem includes the GIC-400 with a Global time base counter and a VBUSP2AXI interface for registers' configuration



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## GIC-400 on Keystone II Devices

- Keystone II devices integrate GIC-400 (**r0p0rel1**) for ARM INTC
- GIC-400 provides a scalable solution for up to **480 peripheral interrupts** with 1-to-n broadcast capability
- Each interrupt can be steered to **nFIQ or nIRQ with individual priority**
- GIC-400 allows software to configure each interrupt line to be **level-sensitive or edge-sensitive** by configuring GICD\_ICFGR
- GIC-400 on Keystone II devices support:
  - **16 SGIs** (Software Generated Interrupts) (per each A15 core)
  - **6 external PPIs** (Private Peripheral Interrupts ) (per each A15 core)
  - **1 internal PPI** (per each A15 core)
  - **480 SPIs** (Shared Peripheral Interrupts ) (for A15 4 cores cluster)

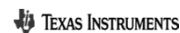
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## Cortex-A15 Exceptions – Handling

- When the exception asserts, the following steps should be processed for this exception:
  - **1. Save processor status**
    - Copy CPSR to SPSR\_<mode>
    - Store the return address in R14 LR\_<mode>
  - **2. Change the processor status for exceptions**
    - Mode field bits, ARM or Thumb status
    - Interrupt disable bits, set PC to vector address
  - **3. Execute the exception handler**
  - **4. Return to main application**
    - Restore CSPR from SPSR\_<mode>, clear interrupt disable bit
    - Restore PC from R14 LR\_<mode> with adjustment offset
- Step 1&2 are performed by processor automatically, step 3&4 are responsible by software

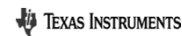
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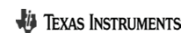


## Boot mode when ARM as boot master

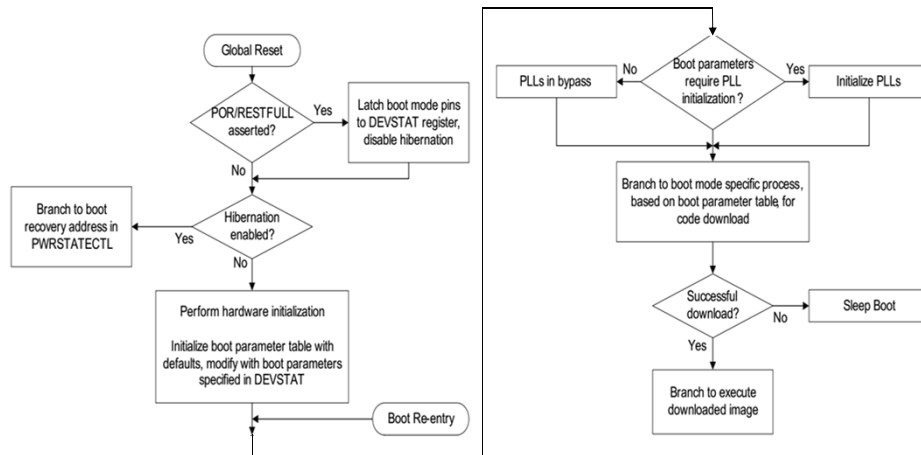
- Keystone II devices support several boot modes for boot master is ARM Core0
- Boot mode is selected by 16 Pins mapped to relative 16 bits in DEVSTAT register
- Supported boot mode and Pins configuration on 66AK2H12 is as follow

DEVSTAT Boot Mode Pins ROM Mapping																									
16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Mode									
X	X	0	ARMEN	SYSN	ARM PLL CONFIG				SYS PLL CONFIG				Min	0	0	0	SLEEP								
SlaveAddr	1	Port												0	0	1	I <sup>2</sup> C SLAVE								
X	X	X	Bus Addr		Param Idx				X				Port	0	0	1	I <sup>2</sup> C MASTER								
Width	Csel	Mode							Npin					0	1	0	SPI								
0	Base Addr	Wait	Width		ARM PLL CONFIG				Boot Master				Min	0	1	0	EMIF (ARM Master)								
1	First Block	Clear	X Chip Sel														EMIF (DSP Master)								
			ARM PLL CONFIG														NAND (ARM Master)								
X Chip Sel								NAND (DSP Master)																	
Lane	Ref Clock	Data Rate			ARM PLL CONFIG												SYS PLL CONFIG				Min	1	0	0	SRIO (ARM Master)
X					Lane Setup																				SRIO (DSP Master)
PA clk	Ref clk	Ext Con			ARM PLL CONFIG									1	0	1	Ethernet (ARM Master)								
Ref clk	Bar Config			Rsvd Lane Setup													Ethernet (DSP Master)								
				ARM PLL CONFIG													PCle (ARM Master)								
				SerDes Cfg													PCle (DSP Master)								
Port	Ref clk	Data Rate			ARM PLL CONFIG								1	1	1	0	HyperLink (ARM Master)								
X	X	X	X	SerDes Cfg													HyperLink (DSP Master)								
X	X	X	X	Port	X	X	X										Min	1	1	1	UART (ARM Master)				
																									UART (DSP Master)

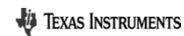
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## ARM Boot High Level Flow

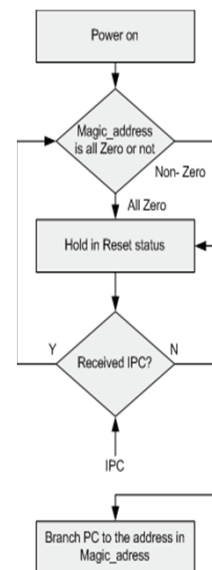


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## ARM Boot Related Info

- ARM initial status on Keystone II Devices
  - Only ARM core 0 is powered on when the device is up, the rest ARM cores are powered off by default
  - ARM core is in supervisor mode by default after power on
  - All the interrupts except IPC are disabled, MMU and Cache are disabled
- Boot secondary ARM cores
  - Please refer the flow chart on the right side



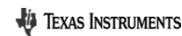
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## ARM Communication with DSP

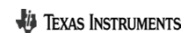
- **Hardware Queue**
  - Use hardware queue (general propose) as the media
  - Use descriptor to transfer the message between Cores
  - Can pending the queue or use interrupts.
- **Hardware IPC**
  - Use hardware IPC to generate interrupt to dedicate Core(s)
  - Support up to 28 different Source IDs per Core

0x02620240	0x02620243	48	IPCGR0	IPC Generation Register for C66x CorePac0
0x02620244	0x02620247	48	IPCGR1	IPC Generation Register for C66x CorePac1
0x02620248	0x0262024B	48	IPCGR2	IPC Generation Register for C66x CorePac2
0x0262024C	0x0262024F	48	IPCGR3	IPC Generation Register for C66x CorePac3
0x02620250	0x02620253	48	IPCGR4	IPC Generation Register for C66x CorePac4
0x02620254	0x02620257	48	IPCGR5	IPC Generation Register for C66x CorePac5
0x02620258	0x0262025B	48	IPCGR6	IPC Generation Register for C66x CorePac6
0x0262025C	0x0262025F	48	IPCGR7	IPC Generation Register for C66x CorePac7
0x02620260	0x02620263	48	IPCGR8	IPC Generation Register for ARM CorePac0
0x02620264	0x02620267	48	IPCGR9	IPC Generation Register for ARM CorePac1
0x02620268	0x0262026B	48	IPCGR10	IPC Generation Register for ARM CorePac2
0x0262026C	0x0262026F	48	IPCGR11	IPC Generation Register for ARM CorePac3
0x02620270	0x0262027B	128	Reserved	Reserved
0x0262027C	0x0262027F	48	IPCGRH	IPC Generation Register for Host
0x02620280	0x02620283	48	IPCAR0	IPC Acknowledgement Register for C66x CorePac0
0x02620284	0x02620287	48	IPCAR1	IPC Acknowledgement Register for C66x CorePac1
0x02620288	0x0262028B	48	IPCAR2	IPC Acknowledgement Register for C66x CorePac2
0x0262028C	0x0262028F	48	IPCAR3	IPC Acknowledgement Register for C66x CorePac3
0x02620290	0x02620293	48	IPCAR4	IPC Acknowledgement Register for C66x CorePac4
0x02620294	0x02620297	48	IPCAR5	IPC Acknowledgement Register for C66x CorePac5
0x02620298	0x0262029B	48	IPCAR6	IPC Acknowledgement Register for C66x CorePac6
0x0262029C	0x0262029F	48	IPCAR7	IPC Acknowledgement Register for C66x CorePac7
0x026202A0	0x026202A3	48	IPCAR8	IPC Acknowledgement Register for ARM CorePac0
0x026202A4	0x026202A7	48	IPCAR9	IPC Acknowledgement Register for ARM CorePac1
0x026202A8	0x026202AB	48	IPCAR10	IPC Acknowledgement Register for ARM CorePac2
0x026202AC	0x026202AF	48	IPCAR11	IPC Acknowledgement Register for ARM CorePac3

Figure 8-23 IPC Generation Registers (IPCGRx)

31	30	29	28	27	8	7	6	5	4	3	1	0
SRC57	SRC56	SRC55	SRC54	SRC53	SRC52	SRC51	SRC50	Reserved	Reserved	Reserved	Reserved	IPC

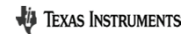
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  - Compiler and CCS Support
  - MCSDK ARM and Linux Support
  - TI Keystone II U-Boot & Linux Kernel Versions and Features

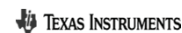
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## Compiler and CCS support

- Linaro GCC cross compiler
  - Released by the Linaro organization, **open source** under the GPL license
  - Bases on GNU GCC baseline and has both versions to **support both bare-metal** (Launchpad) **and Linux ABI** (Linaro) compilations
  - **Better support Cortex-A15** pipeline and optimizations since GCC 4.7
  - TI and ARM are major members, recommend to use Linaro compiler
- Linaro GCC bare-metal cross compiler are integrated in CCS since V5.4.0.00091
  - Started with GCC v4.7.3
- Linaro GCC Linux ABI cross compiler are available in the following link
  - <https://launchpad.net/gcc-linaro/4.7/4.7-2013.03/+download/gcc-linaro-4.7-2013.03.tar.bz2>

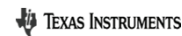
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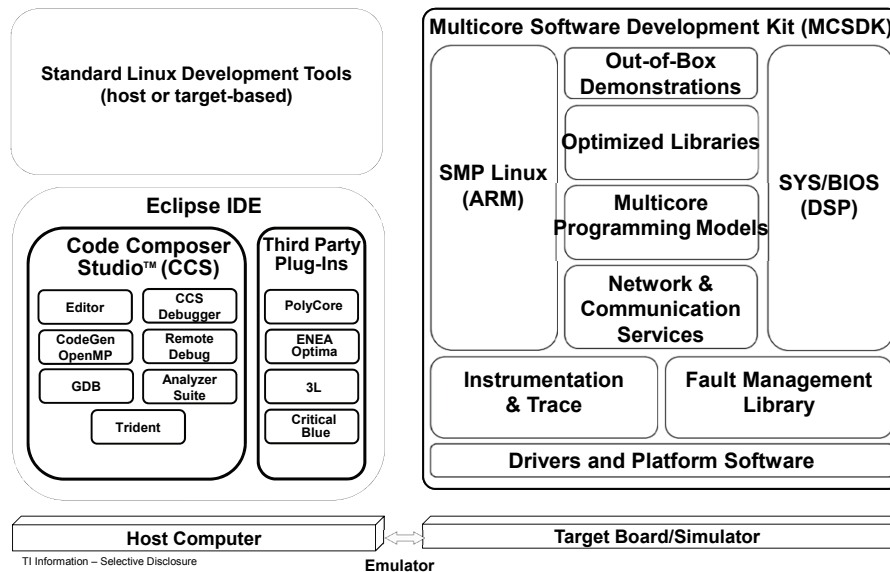
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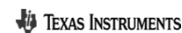
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## Development Ecosystem



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## Linux Development Support

- Linux-based software platform for development, deployment, and execution of ARM A15 on KeyStone II.
- Actively upstreaming Keystone II support to the open-source community
- Source code and prebuilt images of u-boot and kernel
- Open-source Linaro tool-chain for compilation (GCC) and debug (GDB)
- Load-and-run Linux kernel using Code Composer Studio
- Telnet into device to view console print as device boots and to mount root filesystem

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## TI Open Source Presence

- Active member of Linux Foundation
- Founding member of Linaro
- Sponsor of BeagleBoard and PandaBoard
- Top open hardware and open embedded software projects
- Top 10 contributor to kernel, leads embedded-processing industry contributions

Most active 34 employers

By changesets			By lines changed		
(None)	1156	10.8%	(None)	108509	15.5%
Intel	1138	10.6%	Intel	67464	9.7%
Red Hat	960	9.0%	Red Hat	65966	9.4%
(Unknown)	688	6.4%	(Unknown)	50900	7.3%
Texas Instruments	428	4.0%	IBM	36800	5.3%
IBM	381	3.6%	Oracle	26617	3.8%
Novell	372	3.5%	Texas Instruments	25687	3.7%
(Consultant)	298	2.8%	Samsung	24966	3.6%
Wolfson Microelectronics	286	2.7%	NVIDIA	20604	2.9%
Samsung	234	2.2%	Linux Foundation	16917	2.4%
Google	222	2.1%	ST Ericsson	15792	2.3%
Oracle	188	1.8%	Novell	15185	2.2%
Freescale	175	1.6%	Wolfson Microelectronics	14039	2.0%
Qualcomm	161	1.5%	(Consultant)	13495	1.9%
Linaro	143	1.3%	AMD	10151	1.5%
Broadcom	140	1.3%	Freescale	10102	1.4%
NetApp	133	1.2%	Linaro	9360	1.3%
MITAC	133	1.2%	Google	9070	1.3%
AMD	132	1.2%	Qualcomm	8972	1.3%

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## Baseline Versions and Features

- TI Keystone II Linux kernel Baseline
  - Based on **Linux Kernel v3.8.4** in community (latest has **v3.10.10**)
  - Have **both regular and PREEMPT\_RT** branches
  - Fully support **FDT** (Flat Device Tree) for hardware description
  - Fully support **LPAE** for **up to 36-Bit physical address**
  - Integrated frequently used **BSP&Drivers for Keystone II EVM**
  - Support most **popular file system** such as ramfs, ubifs
- TI Keystone II U-Boot Baseline
  - Based on **2013.01** version U-Boot
  - Support **both Tags and FDT** for passing kernel parameters
  - Integrated **daily used function command** such as EVM POST, DSP core Power OFF, image generation tools with SPL, image burning tools, etc
- Cross Compiler Baseline
  - Based on Linaro GCC v4.7.3 (20130313), better support Cortex-A15 features

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## To Get the Source Code and MCSDK Prebuilt Image

- Prebuilt Images in MCSDK 3.x
  - Including prebuilt U-Boot images (bin & gph format), boot monitor, DTB, ulmage, file systems of ramfs (cpio) and ubifs (ubi image and ubifs format) for both regular and RT versions
  - MCSDK GA and updated versions are available
  - Integrated daily used PDK test images in the prebuilt root filesystem
  - Latest version download links:
  - [http://software-dl.ti.com/sdoemb/sdoemb\\_public\\_sw/mcsdk/latest/index\\_FDS.html](http://software-dl.ti.com/sdoemb/sdoemb_public_sw/mcsdk/latest/index_FDS.html)
- Source Code on Git.TI site
  - U-Boot:
  - <http://git.ti.com/cgi/cgit.cgi/keystone-linux/u-boot.git/>
  - Linux Kernel:
  - <http://git.ti.com/cgi/cgit.cgi/keystone-linux/linux.git/>
  - Boot Monitor:
  - <http://git.ti.com/cgi/cgit.cgi/keystone-linux/boot-monitor.git/>

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**Thank  
You!**

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# TI Keystone Networking Coprorocessor Introduction

KeyStone Training



## Why Network Co Processor (NetCP):

### Motivation behind NETCP:

- Use firmware based PDSP (Packet Descriptor Processors) to do processing and encryption.

### Goals for both Packet Accelerator and Security Accelerator:

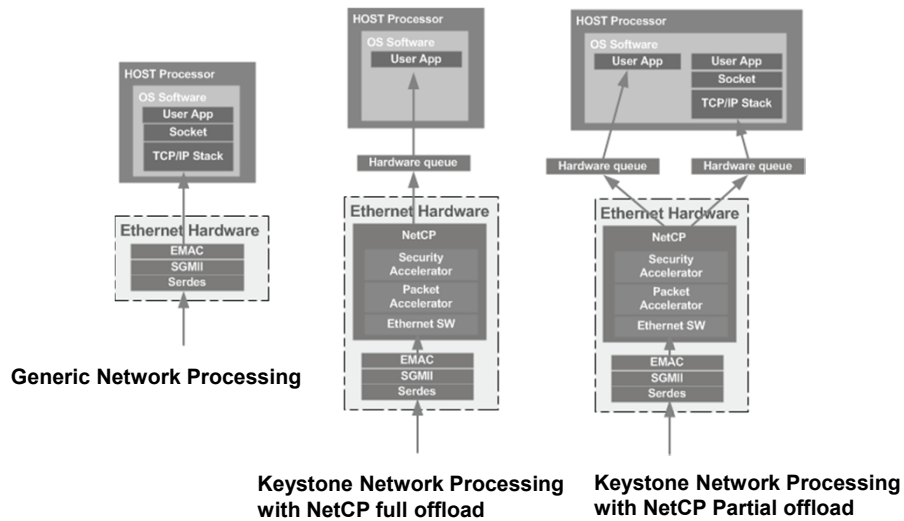
- Offload processing from the cores
- Improve system integration
- Allow cost savings at the system level

### Security Key applications:

- IPSec tunnel endpoint (e.g. LTE eNB, ...)
- Secure RTP (SRTP)
- Air interface (2G/3G/4G) security processing



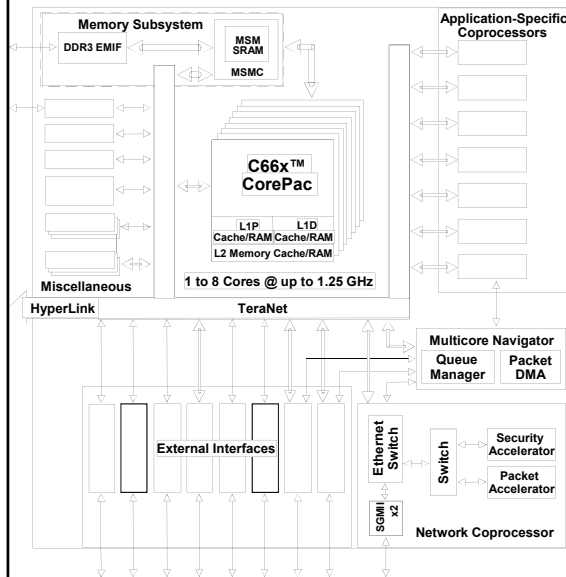
## Why Network Co Processor (NetCP)



## Agenda

- KeyStone I/NetCP1.0
  - Overview
  - Typical Application
  - PA 1.0
- KeyStone II/ NetCP1.5
  - Overview
  - Typical Application
  - PA 1.5
  - NetCP QMSS/PDSP Firmware/RA
- NetCP 1.0 Vs NetCP1.5
- Security Accelerator
  - Overview
  - Channel Configuration
  - Data Process

# KeyStone I Network Coprocessor

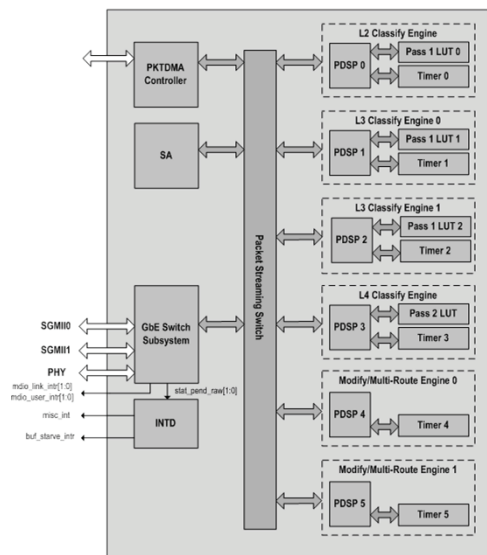


- Provides hardware accelerators to perform L2, L3, and L4 processing and encryption that was previously done in software
- Packet Accelerator (PA)
  - Single or multiple IP address option
  - UDP (and TCP) checksum and selected CRCs
  - L2/L3/L4 support
  - Quality of Service (QoS)
  - Multicast to multiple destinations inside the device
  - Timestamps
- Security Accelerator (SA)
  - Hardware encryption, decryption, and authentication
  - Supports IPsec ESP, IPsec AH, SRTP, and 3GPP protocols

TEXAS INSTRUMENTS

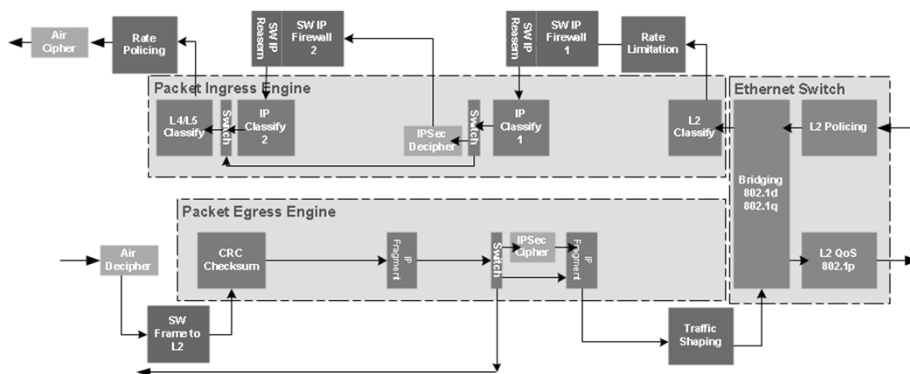
# Packet Accelerator 1.0 Block Diagram

- Provides hardware accelerators to perform the packet classification for Ethernet L2, L3, and L4
  - Hardware Lookup table (LUT1 64 entry/table, LUT2 8K entry/table)
- Based on use case firmware can be redefined/developed
- Engines for modification (IP header/UDP header checksum, IP fragmentation, update PPPoE header)
- Multi routing (same packet can be copied and routed to 8 different queue)



TEXAS INSTRUMENTS

## NetCP1.0 Typical Application



- Software for IP reassembly
- Software IP Firewall
- Software for Packet Framing on to-network direction

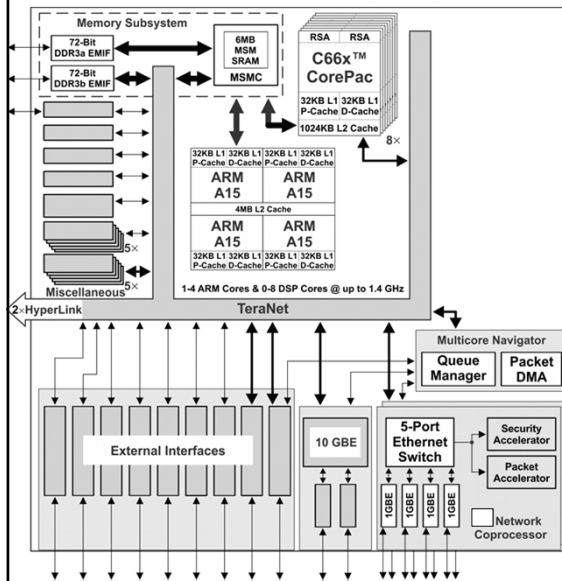
TEXAS INSTRUMENTS

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TEXAS INSTRUMENTS

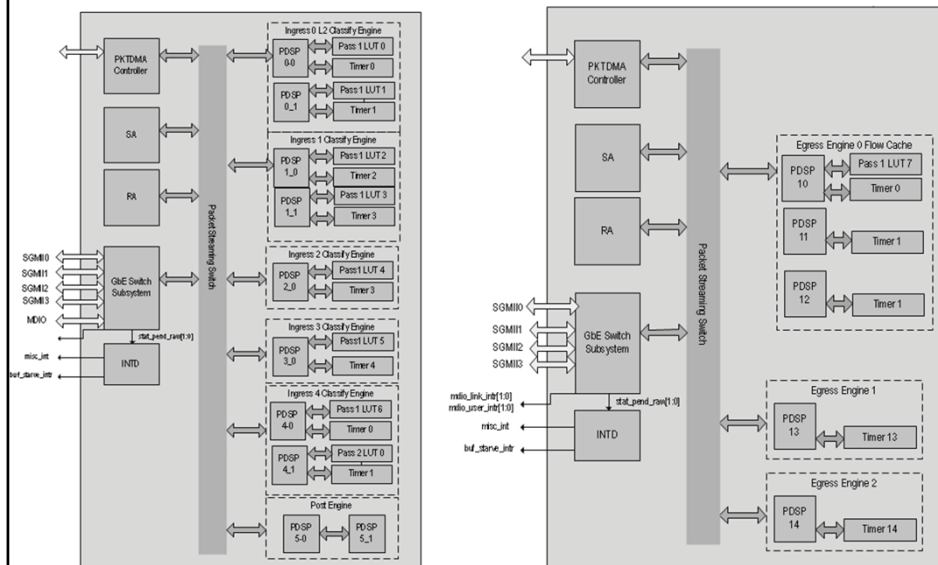
# KeyStone II Network Coprocessor (NETCP)



- Consists of one or two Network Coprocessor(s)
- Provides hardware accelerators to perform L2, L3, and L4 processing and encryption that was previously done in software
- Packet Accelerator (PA)
  - Single IP address option
  - UDP (and TCP) checksum and selected CRCs
  - L2/L3/L4 support
  - Quality of Service (QoS)
  - Multicast to multiple queues
  - Timestamps
- Security Accelerator (SA)
  - Hardware encryption, decryption, and authentication
  - Supports IPsec ESP, IPsec AH, SRTP, and 3GPP protocols
- 2x 5-port Ethernet switches (depending on number of instances of NETCP) with 4-8 ports connecting to 4-8 SGMII ports and one port connecting to the Packet and Security Accelerators.

TEXAS INSTRUMENTS

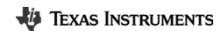
## Packet Accelerator 1.5 Block Diagram



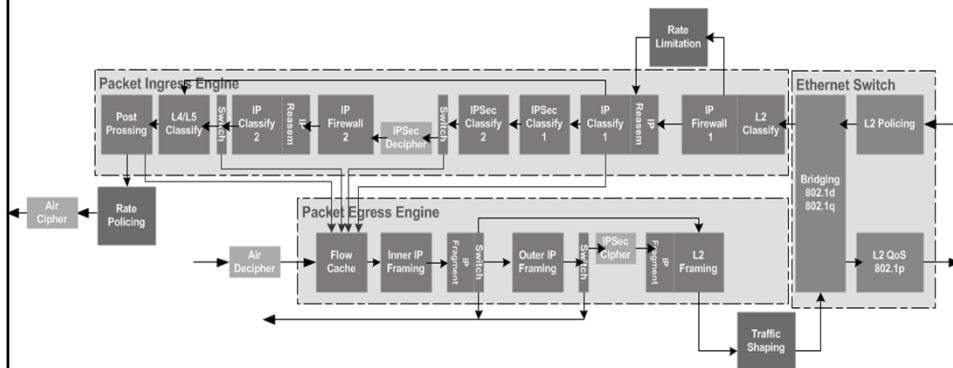
TEXAS INSTRUMENTS

## Packet Accelerator 1.5

- PA LLD interface and features are compatible with NetCP1.0
- Provides hardware accelerators to perform the packet classification for Ethernet L2, L3, and L4
  - Hardware Lookup table (LUT1 256 entry/table, LUT2 3K entry/table) with mask/range configuration
- Each PDSP can do more complex processing (MAX to 3K instructions)
- Egress direction has capability to modify a packet as configuration and route it to Ethernet directly



## NetCP1.5 Typical Application



- Hardware accelerators to do L2, L3, and L4 processing, packet classify
- Hardware accelerators for IPSec/air cipher encryption
- Hardware QoS for PQ/WRR
- Hardware accelerators for IP reassembly
- Hardware accelerators for Flow Cache
- Hardware accelerators for IP Firewall





# NetCP QMSS

- The primary use case is for handling CDMA based packet flows between PA and the Security Accelerator (SA) and Reassembly (RA) engines.
- Using the PA1.5 queue management subsystem offloads DMA and queue operations from the global PA CDMA and chip-level QMSS.
- Provides support for 128 total queues (2 Queue Managers supporting 64 queues each)
  - Supports up to 16K descriptors
  - Supports 16 memory regions for storage of descriptors with each region storing up to 16K descriptors
- Provides support for monitoring 21 queues (queues 0 through 20 of Queue Manager 0) by exporting hardware signals indicating queue status to a local CPPI DMA engine.
- Provides a 128KB memory region for fast local storage of packet descriptors and/or buffers



# PDSP firmware

```

44
45 /* This file contains the PDSP instructions in a C array which are to
46 /* be downloaded from the host CPU to the PDSP instruction memory.
47 /* This file is generated by the PDSP assembler.
48
49 const uint32_t dsp_insts[] = {
50     0x1001000,
51     0x00000000,
52     0x00000007,
53     0x20000000,
54     0x00000000,
55     0x00000000,
56     0x20000000,
57     0x20000000,
58     0x20000000,
59     0x20000000,
60     0x20000000,
61     0x20000000,
62     0x20000000,
63     0x20000000,
64     0x20000000,
65     0x20000000,
66     0x20000000,
67     0x20000000,
68     0x20000000,
69     0x20000000,
70     0x20000000,
71     0x20000000,
72     0x20000000,
73     0x20000000,
74     0x20000000,
75     0x20000000,
76     0x20000000,
77     0x20000000,
78     0x20000000,
79     0x20000000,
80     0x20000000,

```

Name	Size	Type	Date Modified
insts.dsp	4 KB	File	2013-09-28 04:40
insts.dsp	7 KB	File	2013-09-28 04:40
insts.dsp	6 KB	File	2013-09-28 04:40
insts.dsp	4 KB	File	2013-09-28 04:40
insts.dsp	5 KB	File	2013-09-28 04:40
insts.dsp	6 KB	File	2013-09-28 04:40
insts.dsp	6 KB	File	2013-09-28 04:40
insts.dsp	5 KB	File	2013-09-28 04:40
insts.dsp	6 KB	File	2013-09-28 04:40
insts.dsp	6 KB	File	2013-09-28 04:40
insts.dsp	4 KB	File	2013-09-28 04:40
Module.vi	11 KB	File	2013-09-28 04:40
insts.dsp	17 KB	File	2013-09-28 04:40
insts.dsp	31 KB	File	2013-09-28 04:40
insts.dsp	28 KB	File	2013-09-28 04:40
insts.dsp	21 KB	File	2013-09-28 04:40
insts.dsp	25 KB	File	2013-09-28 04:40
insts.dsp	26 KB	File	2013-09-28 04:40
insts.dsp	25 KB	File	2013-09-28 04:40
insts.dsp	29 KB	File	2013-09-28 04:40
insts.dsp	22 KB	File	2013-09-28 04:40
insts.dsp	21 KB	File	2013-09-28 04:40
insts.dsp	26 KB	File	2013-09-28 04:40
insts.dsp	29 KB	File	2013-09-28 04:40
insts.dsp	20 KB	File	2013-09-28 04:40
insts.dsp	21 KB	File	2013-09-28 04:40
insts.dsp	15 KB	File	2013-09-28 04:40
insts.dsp	5 KB	File	2013-09-28 04:40
insts.dsp	5 KB	File	2013-09-28 04:40
insts.dsp	3 KB	File	2013-09-28 04:40

- Each PDSP has dedicated firmware file with array and binary format



# Reassembly Engine

- The Reassembly engine is a hardware accelerator block for reassembling fragmented IPv4 and IPv6 Packets
- Supports reassembly at 10Gbps rate for up to 1K concurrent contexts
- There will be 2 in the system
  - Pre-SA decrypt
  - Post-SA decrypt
- The timeouts will be from 100 to  $2^{32} * 2^{10}$  clock cycles@400MHz



# Agenda

- KeyStone I/NetCP1.0
  - Overview
  - Typical Application
  - PA 1.0
- KeyStone II/ NetCP1.5
  - Overview
  - Typical Application
  - PA 1.5
  - NetCP QMSS/PDSP Firmware/RA
- NetCP 1.0 Vs NetCP1.5
- Security Accelerator
  - Overview
  - Channel Configuration
  - Data Process



# NetCP 1.0 Vs 1.5

Applications	1.0	1.5
Maximum IP packet size	9KB	64KB
PDSP	PA 6 PDSPs 8KB IRAM/PDSP	PA 15 PDSPs 12KB IRAM/PDSP
LUT	3 LUT1 with 64 entries 1 LUT2 with 8K entries(32 bit each)	8 LUT1 (256 entries), mask/range supported 1 LUT2 with 3K entries (64 bit each), range supported
Hardware Firewall	No	256 entries/ACL for outer IP & 256 entries/ACL for Inner IP
Hardware IP Reassembly	No	Outer IP and inner IP reassembly by hardware
Flow cache	No	Yes
IPSec	Replay widows 128	Replay widows 1024 Performance 2x 1.0
Air Cipher	Separate Air Ciphering and Authentication No ZUC F8/F9 and Snow3G F9	Simultaneous Air Ciphering and Authentication Support ZUC F8/F9 and Snow3G F9
Internal memory ECC	No	Yes
Internal QMSS	No	Yes
PKT DMA	9 Tx channels 24 Rx channels	21 Tx channels 91 Rx channels
QoS	PQ+WRR	PQ+WRR Performance 4x 1.0

## Agenda

- KeyStone I/NetCP1.0
  - Overview
  - Typical Application
  - PA 1.0
- KeyStone II/ NetCP1.5
  - Overview
  - Typical Application
  - PA 1.5
  - NetCP QMSS/PDSP Firmware/RA
- NetCP 1.0 Vs NetCP1.5
- Security Accelerator
  - Overview
  - Channel Configuration
  - Data Process

# Security Accelerator Overview

## Motivation

- Hardware Encryption, Decryption, and Authentication
- Faster than software

## Supported Protocols

- IPsec ESP
- IPsec AH
- SRTP
- 3GPP

## Each security accelerator supports:

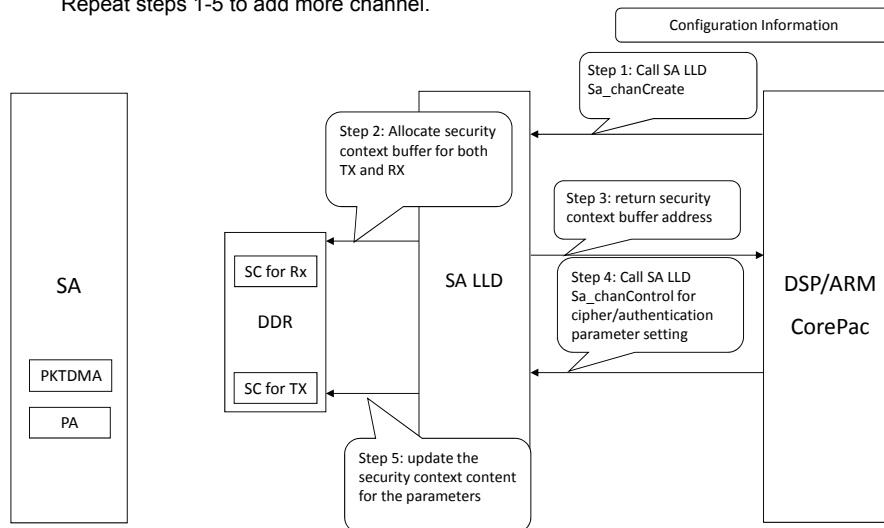
- Loosely coupled accelerator at 1.5M packets per second
- Authentication and replay protection at Gigabit Ethernet wire rate
- Pre- and post- algorithm packet header processing and security association maintenance
- Context caching for security associations (SW or HW managed)
- Can be used by NetCP without host intervention and by SW in parallel

Module Name	Block size (Bits)	Throughput (Mbits/sec)	Remark
AES modes	128	3x 2,800.0	AES 256-bit key numbers, worst case for modes other than CCM
3DES modes	64	2x 1,493.3	3DES 3 key numbers, worst case
Galois Multiplier	128	2x 8,960.0	Galois multiplier core used for GCM mode
AES modes 128 bit key	128	3x 3,200.0	AES 128-bit key numbers, worst case for modes other than CCM
AES-CCM - 256 bits AES Key	128	3x 1,400.0	In CCM mode, AES is run twice for same block.
Kasumi	64	1244.4	Kasumi in F8 mode
Snow3G	320	1154.6	SNOW 3G in F8 mode. 40 bytes in one block, for 1500 byte blocks the throughput is above 5Gbit/s
HMAC-SHA1	512	2x 2,185.4	SHA 1 core
HMAC-MD5	512	2x 2,715.2	MD5 core
HMAC-SHA2	512	2x 2,715.2	SHA 2 core(max 256 bit hash)



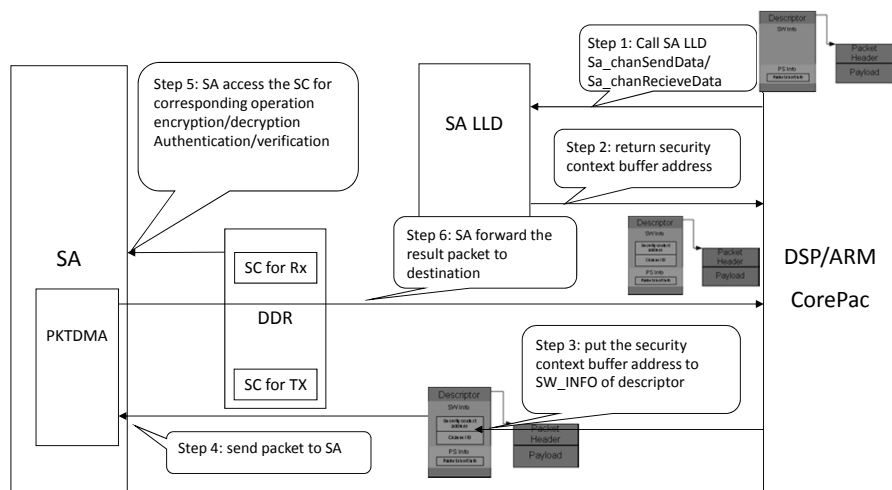
# SA LLD: Channel Configuration

Repeat steps 1-5 to add more channel.



## SA LLD: Packet Process (Air Cipher)

Repeat steps 1-6 send more packet.



TEXAS INSTRUMENTS

## For More Information

- Device-specific Data Manuals for the KeyStone SoCs can be found at [TI.com/multicore](http://TI.com/multicore).
- Multicore articles, tools, and software are available at [Embedded Processors Wiki for the KeyStone Device Architecture](http://Embedded Processors Wiki for the KeyStone Device Architecture).
- View the complete [C66x Multicore SOC Online Training for KeyStone Devices](http://C66x Multicore SOC Online Training for KeyStone Devices), including details on the individual modules.
- For questions regarding topics covered in this training, visit the support forums at the [TI E2E Community](http://TI E2E Community) and [Deyisupport](http://Deyisupport) website.

TEXAS INSTRUMENTS



# Keystone Design Consideration

KeyStone Training



## Agenda

- **Marketplace Challenges and KeyStone Solutions**
- KeyStone SoC Hardware Design
- Software Development



## Common Usage Cases

- Network gateway, speech/voice processing
  - Typically hundreds or thousands of channels
  - Each channel consumes about 30 MIPS
- Cloud computing
- Server and Storage
- Large, complex, floating point FFT
- Video processing
- Medical imaging
- LTE, WiMAX, other wireless physical layers
- Scientific processing (Oil explorations)
  - Large complex matrix manipulations
- Your applications?



## Marketplace Challenges

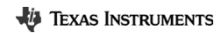
- Increase of data rate
  - Think about Ethernet, from 10Mbps to 10Gbps
- Increase in algorithm complexity
  - Think about typical face recognition, finger prints, cloud computing
- Increase in development cost
  - Hardware and software development
- **KeyStone SOC devices are a solution**
  - Fast peripherals part of the device
  - High performances, fixed point and floating point processing power. Parallel data movement.
  - Off-the-shelf devices
  - Elaborate set of software tools





## To Fulfill Large Data Transmission

- Fast peripherals are needed to:
  - Receive high bit-rate data into the device
  - Transmit the processed HBR data out of the device
- KeyStone devices have a variety of high bit-rate peripherals, including the following:
  - 10/100/1000 Mbps Ethernet
  - 10G Ethernet
  - SRIO
  - PCIe
  - AIF2
  - TSIP



## Enable Complex Algorithms

- 8 functional units of the C66x CorePac provide:
  - Fixed- and Floating-point native instructions
  - Many SIMD instructions
  - Many Special Purpose Powerful instructions
  - Fast (0 wait state) L1 memory
  - Fast L2 memory
- ARM Core provides
  - Fixed- and Floating-point native instructions
  - Many SIMD instructions
  - Fast (0 wait state) private L1 cache memory for each A15
  - Fast shared coherent L2 cache memory



## Inter-Processor Communication

- Shared memory
  - Very fast and large external DDR interface(s).
  - DSP Core provides 32- to 36-bit address translation enables access of up to 10GB of DDR. ARM core uses MMU to translate 32 bits logical address into 40 bits physical address
  - Fast, shared L2 memory is part of the sophisticated and fast MSMC.
- Hardware provides ability to move data and signals between cores with minimal CPU resources.
  - Powerful transport through Multicore Navigator
  - Multiple instances of EDMA
- Other hardware mechanisms that help facilitate messages and communications between cores.
  - IPC registers, semaphore block



## Minimizing Resource Contention

- Each DSP CorePac has a dedicated port into the MSMC.
- MSMC supports pre-fetching to speed up loading of data.
- Shared L2 has multiple banks of memory that support concurrent multiple access.
- ARM core uses AMBA bus to connect directly to the MSMC, provide coherency and efficiency
- Wide and fast parallel Teranet switch fabric provides priority-based parallel access.
- Packet-based HyperLink bus enables the seamless connection of two KeyStone devices to increase performance while minimizing power and cost.



## Multicore SOC Design Challenges

- Hardware design
  - Specific design requirements
  - high-speed interface design
  - Reference design solution
- Software development
  - Multicore work allocation and load balance
  - Multicore communication
  - Low level hardware driver
  - Application library



## Agenda

- Marketplace Challenges and KeyStone Solutions
- **KeyStone SoC Hardware Design**
  - *Minimum System Design*
  - *Peripherals Design*
  - *Reference Design - EVM*
- Software Development

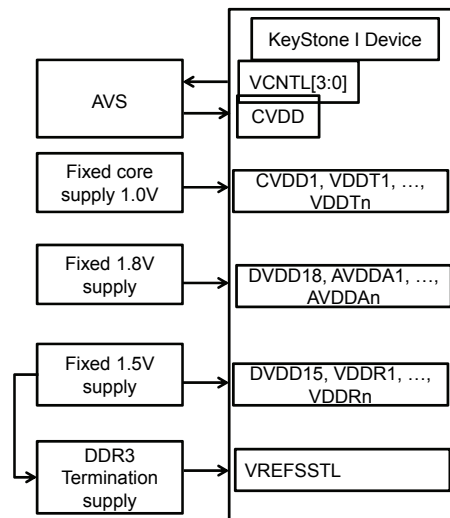


## Minimum System Design

- Power Supplies
- Clocking
- DDR3 Design
- Boot Design
- JTAG

## Power Supplies - KI

- Power Types
    - AVS for CVDD
      - Interface VCNTL[3:0]: 4-pin 6-bit dual-phase
      - with initial voltage 1.1V;
      - Two classes solutions
        - » LM10011: [P7256](#), [P7303](#)
        - » UCD92xx: Refer to EVM Schematic
    - Fixed power: 1.0/1.5/1.8V
- Design Details see section 2 of "Hardware design guide SPRABI2C".
- Available tools to calculate the DSP power consumption and current value.
- The data is application-dependent and the model is used to get the accurate results.
- Power Consumption Model** download link:  
<http://www.ti.com/product/tms320c66xx> (Software & Tools -> Models)
- Power Supply Sequence
    - Core voltage start before IO voltage
      - CVDD -> CVDD1 -> DVDD18 -> DVDD15
    - IO voltage start before core voltage
      - DVDD18 -> CVDD -> CVDD1 -> DVDD15
- Details requirement refer to the device data manual.



## Power Supplies - KII

### • Power Types

- AVS for CVDD
  - Interface VCNTL[5:0]: 4-pin 6-bit dual-phase or 6-pin 6-bit single phase
  - with initial voltage 1.0v;
  - Two classes solutions
    - » LM10011: P7256, P7303, EVMK2E Schematic
    - » UCD92xx: EVMK2H Schematic
- Fixed power: 0.95/0.85/1.5/1.8V/3.3

Design Details see section 2 of "Hardware design guide SPRABV0".

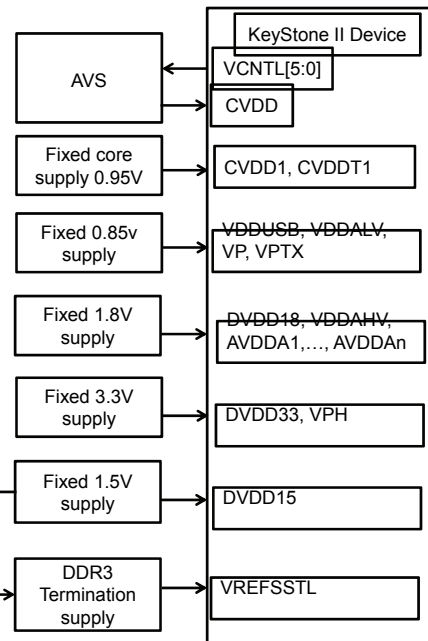
### • Available tools to calculate the DSP power consumption and current value.

The data is application-dependent and the model is used to get the accurate results.

### • Power Supply Sequence

- Core voltage start before IO voltage
  - CVDD -> CVDD1, DVDD18, VDDAHV, AVDDAx-> DVDD15->VDDALV, VDDUSB, VP, VPTX->DVDD33
- IO voltage start before core voltage
  - DVDD18, VDDAHV, AVDDAx->CVDD->CVDD1-> DVDD15->VDDALV, VDDUSB, VP, VPTX->DVDD33

Details requirement refer to the device data manual.



TEXAS INSTRUMENTS

## Clocking - KI

### • Clock Types

- Necessary: Clock for Main PLL (CORECLK or ALT CORECLK).
- Selective: Clock for peripherals(depend on design)

### • Design Requirements

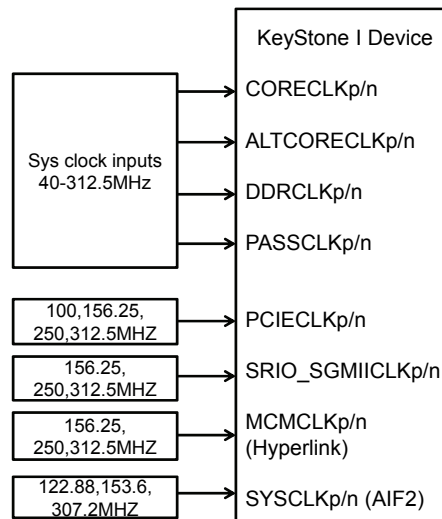
- Should satisfy with the jitter requirements;
- Should select the valid input frequencies;
- Unused clock inputs should be connected as figure 13 in SPRABI2C.

### • Reference Design Guide

- See the "Clock Design guide (SPRABI4)" and section 3 of "Hardware design guide (SPRABI2C)" for clock design details.
- See the EVM schematic and PCB layout for reference.

### • Recommend Clock Parts

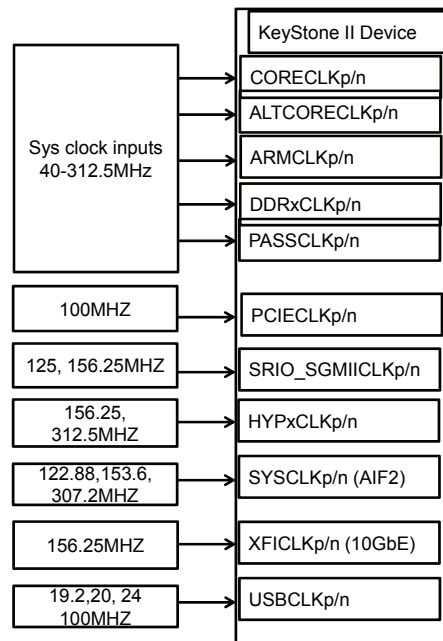
- CDCM6208
- CDCE62005
- CDCE62002



TEXAS INSTRUMENTS

## Clocking - KII

- Clock Types
  - Necessary: Clock for Main PLL (CORECLK or ALT CORECLK).
  - Selective: Clock for peripherals(depend on design)
- Design Requirements
  - Should satisfy with the jitter requirements;
  - Should select the valid input frequencies;
  - Unused clock inputs should be connected as figure 15 in SPRABV0.
- Reference Design Guide
  - See the "Clock Design guide (SPRABI4)" and section 3 of "Hardware design guide(SPRABV0)" for clock design details.
  - See the EVM schematic and PCB layout for reference.
- Recommend Clock Parts
  - CDCM6208
  - CDCE62005
  - CDCE62002



## DDR3 Design

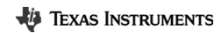
- Design Guide
  - See the "DDR3 Design Requirement for Keystone Devices(SPRABI1A)" for information regarding supported topologies and layout guidelines.
  - See the section "Input clock requirements" of the "Hardware design guide for KI devices (SPRABI2C)" and SPRABV0 for KII devices for the input reference clock and unused pin requirements.
- Available tools to generate DDR3 configuration values
 

The DDR3 configuration registers' value depend on board layout and the selected SDRAM. Refer to the "Keystone I DDR3 Initialization SPRABL2B" for the DDR3 initialization sequence and use the [DDR3 spreadsheet](#) to generate your value, then update the DDR3 initial value of the demo code [STK](#).

## Boot Design

- Boot Modes
  - Memory boot: EMIF, SPI, and I2C master boot.
  - Host Boot: UART, SRIO, PCIe, EMAC, Hyperlink and I2C slave boot.

For boot details, see the SPRUGY5B for KI, SPRUGY9C for KII DSP bootloader, and SPRUHJ3 for KII ARM bootloader.
- Boot Configuration Pins
  - Boot mode and configurations are chosen using bootstrap pins on the device, and Pins are latched and stored in the DEVSTAT register during POR. To determine the boot configuration, BOOTMODE[13:0] are used for KI, BOOTMODE[15:0] are used for KII.
  - See the device data manual for details of the pins configuration.
- See the [RBL](#) source code for detailed boot sequence.



## JTAG

- Design Guide
  - All JTAG pins are 1.8v IO, a voltage converter is needed if the selected emulator doesn't support 1.8v IO levels.
  - For JTAG connection design guide refer to:  
[http://processors.wiki.ti.com/index.php/XDS\\_Target\\_Connection\\_Guide](http://processors.wiki.ti.com/index.php/XDS_Target_Connection_Guide)
  - Details about trace emulator design, see the "Emulator and Trace Headers Technical Reference Manual (SRPU655H)"
- JTAG Emulator Selection  
<http://www.ti.com/lscds/ti/tools-software/emulators.page>

### JTAG Probes and Trace Receivers



XDS100v2/v3



XDS200



XDS510



XDS560v2 STM



XDS560v2 Pro Trace

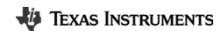
- Emulation header selection
  - 14-pin and 20-pin can satisfy with the general debug
  - 20-pin can support export of system trace data
  - 60-pin can support export of core trace, and it can also support export of system trace data.

notes: For DSP device has on chip trace buffer, the XDS560 14pin/20pin generation emulator support core trace too.
- For JTAG problems, refer to:  
[http://processors.wiki.ti.com/index.php/Debugging\\_JTAG\\_Connectivity\\_Problems](http://processors.wiki.ti.com/index.php/Debugging_JTAG_Connectivity_Problems)



## Peripherals Design

- General Peripherals
  - I2C/SPI/EMIF16/UART/uPP/TSIP/GPIO
- High Speed Peripherals
  - USB
  - EMAC
  - 10GbE
  - PCIe
  - SRIO
  - Hyperlink
  - AIF2



## General Peripherals

- Design Requirements
  - All the interfaces operate at 1.8v, voltage level translator is needed to tolerant other voltage such as 2.5v or 3.3v.
  - Requirement of external resistor is interface-dependent, suggest select the recommended resistor values in the hardware design guide, or maybe need to use the IBIS module to determine the best resistor.
  - Unused pins requirements are interface-dependent, it can be left unconnected if with internal pull-up or pull-down resistors.
- Reference Design Guide
  - For detail design requirements of each interface, see the related section of file "Hardware design guide for KI devices(SPRABI2C)" and SPRABV0 for KII devices.
- Throughput Performance
  - For theory and measurement throughput performance refer to the "Throughput performance guide(SPRABK5A)".





## High Speed Peripherals – USB/EMAC/10GbE/PCIe/SRIO/Hyperlink/AIF2

- Reference Design Guide
  - For the input reference clock requirements see the section “Input clock requirements” of the “Hardware design guide for KI devices (SPRABI2C)” and “SPRABV0 for KII devices”.
  - See the “SerDes Implementation Guide for Keystone I Devices (SPRABC1)” and “SPRUHO3 for KII devices” for serdes layout rules constraints and the serdes registers configuration.
  - See the respective section of “Hardware design guide for KI devices (SPRABI2C)” and “SPRABV0 for KII devices” for the unused pins requirement.
  - See the EVM schematic and PCB layout for reference design.
- Throughput Performance
  - For theory and measurement throughput performance see the “Throughput performance guide (SPRABK5A)”.



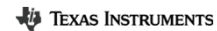
## Reference Design - EVM

- EVM Types
  - [EVM6678L/LE](#)
  - [EVM6657L/LE](#)
  - [EVM6670L/LE](#)
  - [EVMK2H/K2HX](#)
- Click the above EVM link, you can find the below EVM information
  - EVM Quick Setup Guide.
  - Technical Reference Guide.
  - Schematic.
  - PCB Layout.
  - EVM Firmware such as the UCD file for power and FPGA file.
  - .....
- In all, the EVM is a good reference design guide for startup.

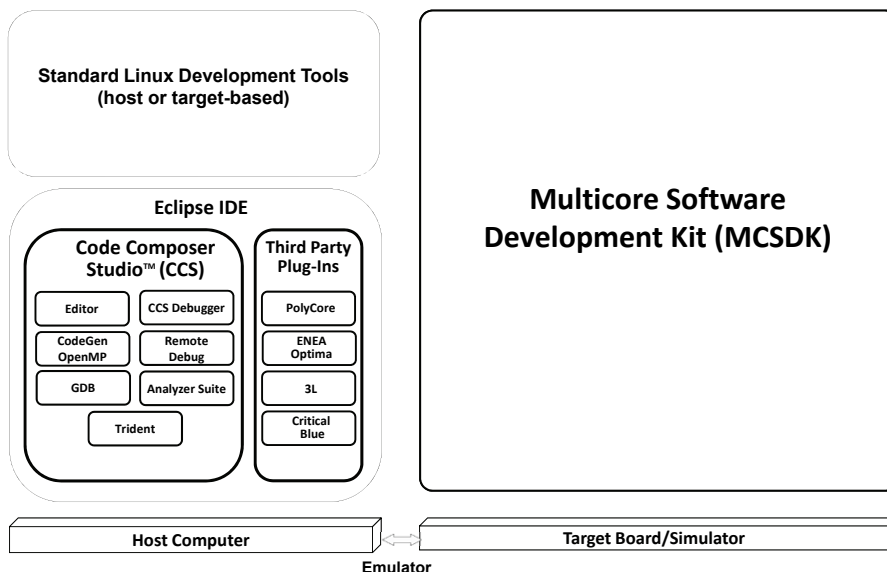


## Agenda

- Marketplace Challenges and KeyStone Solutions
- KeyStone SoC Hardware Design
- **Software Development**
  - *Software Development Ecosystem*
  - *CCS Eclipse IDE v5*
  - *Multicore Software Development Kit (MCSDK)*
  - *Multicore Program*
  - *Application Software*

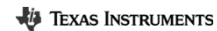


## Multicore SW Development Ecosystem



## CCS Eclipse IDE v5

- Code Composer Studio (CCS) is an Eclipse-based IDE that supports application development on multiple cores/devices:
  - Support simulator, debug/emulation, remote Debug, instrumentation and visualization.
  - Integrated compiler tools with support for OpenMP.
  - Allows developers to integrate third-party software tools assisting for multicore programming, profiling and analysis capabilities.CCSv5 details see: [http://processors.wiki.ti.com/index.php/Category:Code\\_Composer\\_Studio\\_v5](http://processors.wiki.ti.com/index.php/Category:Code_Composer_Studio_v5)
- Download [CCS](#) and the [compiler](#).
- CCS License:
  - Free for 90days for CCSv5,
  - free license file for C66x EVMs [here](#) (under "Keystone EVM Info" section of the download page)
  - more about [CCS-License](#).

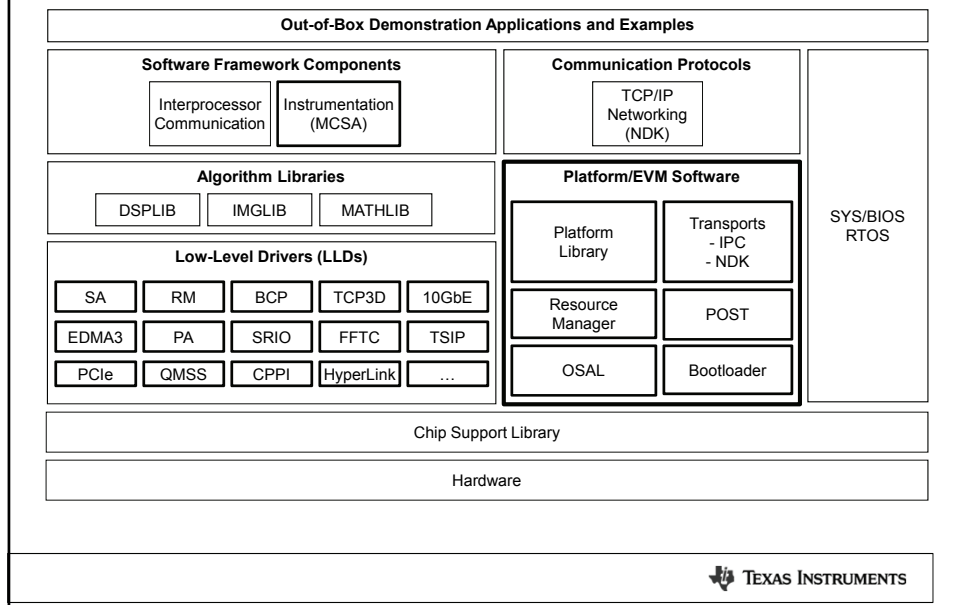


## MCSDK: Overview

- Set of software building blocks to facilitate development of applications
- DSP and ARM platform software, low-level drivers, high-level APIs and other utilities
- Source and prebuilt libraries are included
- Embedded OS: SYS/BIOS RTOS on C66; Linux on ARM
- Development OS: Windows and Linux PC support
- Free to download with all components in one installer



# C66x MCSDK Overview



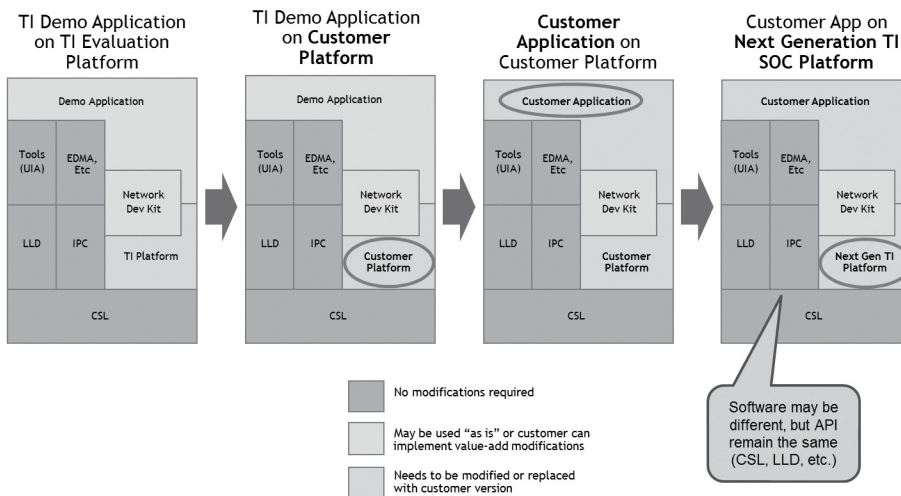
## ARM Linux Perspective: Overview

- Linux-based software platform for development, deployment, and execution of ARM A15 on KeyStone II.
- Actively upstreaming Keystone II support to the open-source community
- Source code and prebuilt images of u-boot and kernel
- Open-source Linaro toolchain for compilation (gcc) and debug (gdb)
- Load-and-run Linux kernel using Code Composer Studio
- Telnet into device to view console print as device boots and to mount root filesystem

## Drivers & Platform Software: Summary

Module	DSP (CSL)	DSP (LLD)	ARM (CSL)	ARM (User Mode LLD)	ARM (Linux kernel)
Timer64	x		x		
ARM Arch Timer					x
ARM Intc (GIC)			x		x
CPINTC	x		x		
CPSW (5-port 10G)	x		x		x
USB 3.0	x		x		x
GPIO	x		x		x
EMIF16 - NAND	x		x		x
I2C	x		x		x
USIM	x		x		x
UART	x		x		x
SPI	x		x		x
AIIF2	x	x			
SRIO	x	x	x		x
PCle	x	x	x		x
PA	x	x	x	x	x
SA	x	x	x	x	x
CPSW (5-port 1G)	x		x		x
QMSS + PktDMA	x	x	x	x	x
RAC	x				
TAC2	x				
VCP2	x				
TCP3D	x	x			
BCP	x	x			
FFTC	x	x			
EDMA	x	x			
HyperLink	x	x	x	x	
HW Semaphore	x				x
PSC					x

## Getting Started: Development Flow



## Getting Started: Algorithm Libraries

Algorithm libraries contain C66x C-callable, hand-coded, assembly-optimized functions for specific usage:

- **Fundamental Math & Signal Processing Libraries**

- **DSPLIB**: Signal-processing math and vector functions
- **MathLIB**: Floating-point math functions

- **Image & Video Processing Libraries**

- **IMGLIB**: Image/video processing functions
- **VLIB**: Video analytics and vision functions

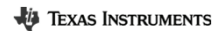
- **Telecommunication Libraries**

- **VoLIB**: Voice over IP application related functions
- **FaxLIB**: FAX application related functions

- **Medical Libraries**

- **STK-MED**: Ultrasound and optical coherence tomography algorithms

More info: [http://processors.wiki.ti.com/index.php/Software\\_libraries](http://processors.wiki.ti.com/index.php/Software_libraries)



## Getting Started: Out-of-Box Demos

### Keystone I & II demos:

- **Utility Application Demo**

- Provides system information (OS version, CPU info, network interfaces), System statistics (mem/cpu usage, TX/RX pkts), Flash NAND/EEPROM, etc.

- **Image Processing Demo**

- Image edge detection demo

### Keystone II demos:

- **IPC Demo**

- Load DSP out file from ARM and perform ARM-DSP communication

- **Transport Net Demo**

- NetCP capabilities including PA, SA and Ethernet Switch Subsystem



## Multicore Program

- For basic multicore program knowledge, see "Multicore Program Guide (SPRAB27B)".
- Program Model
  - See the Hua and Image processing demos in the MCSDK.
  - See the [multicore video infrastructure](#) demo for multicore software demo.
  - See [OpenMP](#) for its usage in multicore program.
- Below table lists the basic IPC engines comparison between traditional and keystone devices.

	Traditional Solution	Keystone Solution
<b>Inter-Processor Communication</b>	EDMA ISR	EDMA ISR, IPC, Hardware Semaphore, Navigator, SRIO
<b>Data Transfer Engines</b>	EDMA, Ethernet, SRIO, AIF	EDMA, Ethernet, SRIO, AIF; Navigator, Hyperlink, 10GbE
<b>Shared Resource Management</b>	Global Flag	Global Flag, Hardware Semaphore, IPC

## Application Software

- [MCSDK Video Demos](#): Provides multiple video demos to demonstrate capability of C66x multi-core DSPs on computation intensive video processing.
- [Industrial Image Demo](#): Focuses on the natural ability to parallelize image processing algorithms with employing open-source packages such as OpenMP and OpenCV.
- [Medical Imaging Demo](#): Illustrates the system-level integration of key medical imaging algorithm modules on multicore DSPs, currently focuses on the Ultrasound and Optical Coherence Tomography(OCT) application domains.
- For more other application software see the Target End Equipments [here](#).

## Keystone I Development Tool Availability

- Keystone I Evaluation Modules: Available
  - <http://www.ti.com/tool/tmdxevm6678>
  - <http://www.ti.com/tool/tmdxevm6670>
  - <http://www.ti.com/tool/tmdxevm6657>
- MCSDK 2.x: Available
  - <http://www.ti.com/tool/bioslinuxmcsdk>
- EVM Materials and Support:
  - <http://www.advantech.com/Support/TI-EVM/>
  - <http://www.einfochips.com/index.php/partnerships/texas-instruments/tms320c6657-evm#5-resources>



## Keystone II Development Tool Availability

- Keystone II Evaluation Modules: Available
  - <http://www.ti.com/tool/evmk2h>
- EVM Materials and Support:
  - <http://www.advantech.com/Support/TI-EVM/>
- MCSDK 3.0: Available
  - <http://www.ti.com/tool/bioslinuxmcsdk>
- Toolchain: Now
  - Linaro GCC bare-metal cross compiler are integrated in CCS since V5.4.0.00091
    - Started with GCC v4.7.3
  - Linaro GCC Linux ABI cross compiler are available in the following link
    - [https://launchpad.net/linaro-toolchain-binaries/trunk/2013.03/+download/gcc-linaro-arm-linux-gnueabihf-4.7-2013.03-20130313\\_linux.tar.bz2](https://launchpad.net/linaro-toolchain-binaries/trunk/2013.03/+download/gcc-linaro-arm-linux-gnueabihf-4.7-2013.03-20130313_linux.tar.bz2)
- Linux:
  - Uboot: <http://arago-project.org/git/projects/?p=u-boot-keystone.git;a=summary>
  - Kernel: <http://arago-project.org/git/projects/?p=linux-keystone.git;a=summary>
  - Boot Monitor: <http://arago-project.org/git/projects/?p=boot-monitor.git;a=summary>





## For More Information

- [Multicore Program Guide](#)
- Multicore articles, tools, and software are available at [Embedded Processors Wiki for the KeyStone Device Architecture](#).
- View the complete [C66x Multicore SOC Online Training for KeyStone Devices](#), including details on the individual modules.
- For questions regarding topics covered in this training, visit the support forums at the [TI E2E Community](#) and [德州仪器中文社区](#).



# Sitara™ PRU-ICSS Training



## Agenda

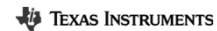
- **Introduction to the PRU Subsystem (PRU-ICSS on AM335x)**
- Getting Started Programming
  - PRU Assembler (PASM)
  - PRU Development Support Integrated in CCS&C Compiler
  - Linux PRU Application Loader
- PRU Application
- Other Resources



## Introduction to the PRU SubSystem

- What is PRU SubSystem?
  - Programmable Real-time Unit SubSystem
  - Dual 32bit RISC processors
  - Local instruction and data RAM; access to SoC resources.
  
- What devices include PRU SubSystem?
  - Legacy PRUSS: OMAPL137/ AM17x, OMAPL138/ AM18x, C674x
  - PRU-ICSS\* (PRUSSv2): AM335x
  
- Why PRU SubSystem?
  - Full programmability allows adding customer differentiation
  - Efficient in performing embedded tasks that require manipulation of packed memory mapped data structures
  - Efficient in handling of system events that have tight real-time constraints.

\* PRU-ICSS = Programmable Real-time Unit and Industrial Communication SubSystem.



## PRU Subsystem Is / Is-Not

IS	IS-Not
Dual 32-bit RISC processor specifically designed for manipulation of packed memory mapped data structures and implementing system features that have tight real time constraints	In not a H/W accelerator to speed up <b>algorithm computations</b> .
Simple RISC ISA - Approximately 40 instructions  - Logical, arithmetic, and flow control ops all complete in a single cycle	Is <b>not a general purpose RISC processor</b> - No multiply hardware/instructions - No cache - No pipeline
Could be used to enhance the existing peripheral feature set or implement new peripheral capability with software bit bang	Is not a stand alone configurable peripheral and will need some hardware assist for configurable peripheral implementation
Includes example code to demonstrate various features. Examples can be used as building blocks.	No Operating System or high level application software stack



## PRU Value

- Extend connectivity and peripheral capability
  - Implement Industrial Communications protocols (like EtherCAT®, PROFINET, EtherNet/IP™, PROFIBUS, POWERLINK, SERCOS III)
  - Implement special peripherals and bus interfaces (like soft UARTs interfaces)
  - Digital IOs with latency in ns
  - Implement smart data movement schemes (especially useful for audio algorithms like reverb, room correction, etc.)
- Reduce system power consumption
  - Allows switching off both ARM and DSP clocks
  - Implement smart power controller by evaluating events before waking up DSP and/or ARM. Maximized power down time.
- Accelerate system performance
  - Full programmability allows custom interface implementation
  - Specialized custom data handling to offload CPU



## PRU-ICSS Subsystem on AM335x

	ARM Cortex-A8 (MHz)	Graphics	PRU-ICSS for Slave Industrial Communications	Package	Availability
AM3359	800	3D graphics	PRU-ICSS + EtherCAT slave	15x15 / 0.8mm	In Production
AM3358	600/800/1000	3D graphics	PRU-ICSS	15x15 / 0.8mm	In Production
AM3357	300/600/800		PRU-ICSS + EtherCAT slave	15x15 / 0.8mm	In Production
AM3356	300/600/800		PRU-ICSS	15x15 / 0.8mm	In Production
AM3354	600/800/1000	3D graphics		15x15 / 0.8mm 13x13 / 0.65mm*	In Production
AM3352	300/600/800/1000			15x15 / 0.8mm 13x13 / 0.65mm*	In Production

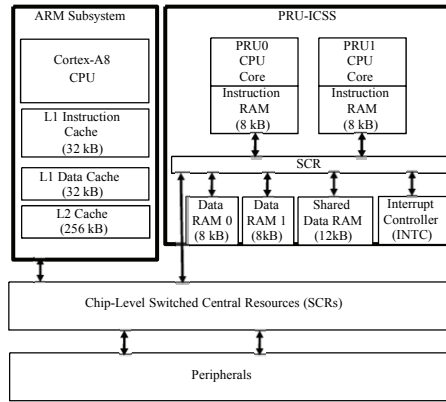
✓ PRU-ICSS is used for slave industrial communication protocols such as Profibus, Profinet, Powerlink & Ethernet/IP

Package	15x15mm (ZCZ)	*13x13mm (ZCE)
ARM speed	Up to 1000 MHz	Up to 600 MHz
USB 2.0 OTG + PHY	x2	x1
EMAC	2-port switch	Single port



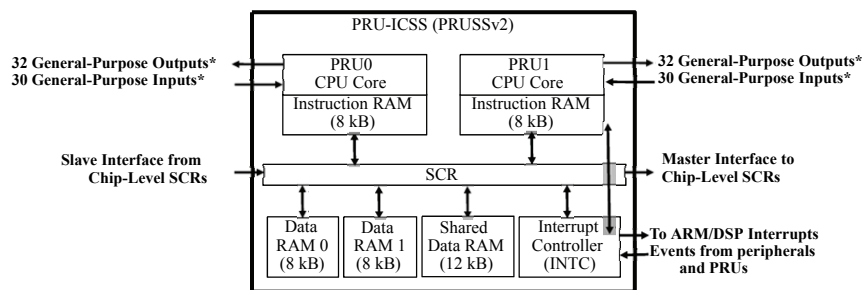
## Chip-level Integration of the PRU-ICSS (PRUSSv2)

- ARM has access to PRU-ICSS memory
- PRU-ICSS has access to its own local memories and other chip-level memory resources and peripherals



TEXAS INSTRUMENTS

## PRU-ICSS (PRUSSv2) Block Diagram



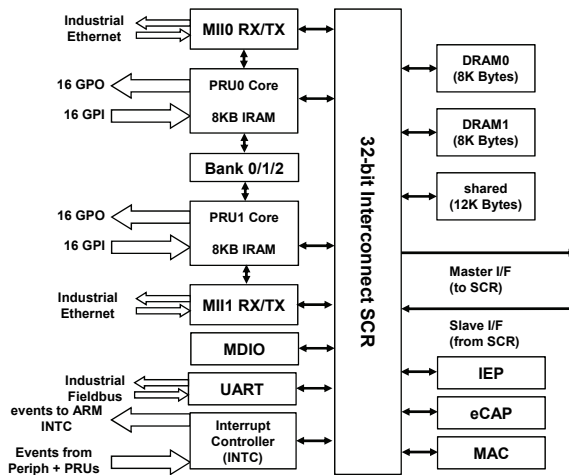
\* On AM335x, only 15 General-Purpose Outputs and 16 General-Purpose Inputs are pinned out.

TEXAS INSTRUMENTS

## PRU-ICSS Subsystem

- Provides two independent programmable real-time (PRU) cores
  - 32-Bit Load/Store RISC architecture
  - no pipeline
  - 200MHz / 5ns
  - 8K Byte instruction RAM (2K instructions) per core
  - 8K Bytes data RAM per core
  - 12K Bytes shared RAM
- Includes Interrupt Controller for system event handling
- Fast I/O interface
  - 16 inputs and 16 outputs on external pins on AM335x via R30/R1
  - EDIO via IEP SYNC unit
- Power management via single PSC

PRUv2 Subsystem Functional Block Diagram



TEXAS INSTRUMENTS

## Enhancements in PRU-ICSS compared to Legacy PRUSS

- Memory
  - Additional data memory (8K Bytes vs 512 Bytes)
  - Additional instruction memory (8K Bytes vs 4K Bytes)
  - 12 KB Shared RAM
  - All memories within PRU-ICSS support parity
- PRU Resources
  - Enhanced GPIO (EGPIO), adding serial, parallel, and MII capture capabilities
  - Multiplier with optional accumulation (MAC)
  - Scratch pad (SPAD) with broadside interface
- Internal peripheral modules
  - UART
  - eCAP
  - MII\_RT
  - MDIO
  - IEP
- Operating frequency
  - Legacy PRUSS:  $\frac{1}{2}$  CPU frequency
  - PRU-ICSS: 200 MHz

TEXAS INSTRUMENTS

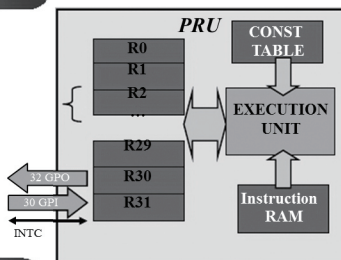
## PRU Functional Block Diagram

### General Purpose Registers

- ❖ All instructions are performed on registers and complete in a single cycle
- ❖ Register file appears as linear block for all register to memory operations

### Constant Table

- ❖ Ease SW development by providing freq used constants
- ❖ Peripheral base addresses
- ❖ Few entries programmable



### Special Registers (R30 and R31)

- ❖ R30
  - ❖ Write: 32 GPO (AM335x: 16 GPO pinned out)
- ❖ R31
  - ❖ Read: 30 GPI + 2 Host Int status (AM335x: 17 GPI pinned out)
  - ❖ Write: Generate INTC Event

### Execution Unit

- ❖ Logical, arithmetic, and flow control instructions
- ❖ Scalar, no Pipeline, Little Endian
- ❖ Register-to-register data flow
- ❖ Addressing modes: Ld Immediate & Ld/St to Mem

### Instruction RAM

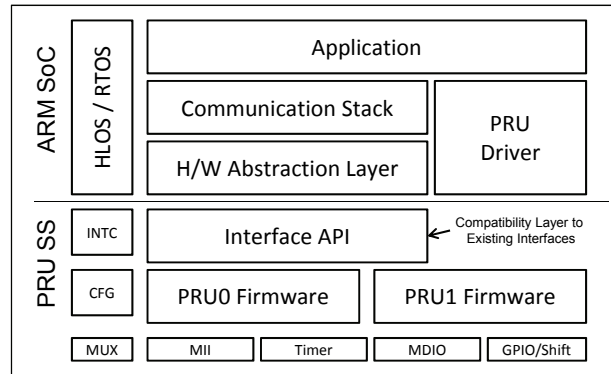
- ❖ 8KB in size; 2K Instructions
- ❖ Can be updated with PRU reset

## Agenda

- Introduction to the PRU Subsystem (PRU-ICSS on AM335x)
- Getting Started Programming
  - **PRU Assembler (PASM)**
  - PRU Development Support Integrated in CCS&C Compiler
  - Linux PRU Application Loader
- PRU Application
- Other Resources



## Generic PRU Programming Model



## PASM Overview

- PASM is a command-line assembler for the PRU cores
  - Converts PRU assembly source files to loadable binary data
  - Output format can be raw binary, C array (default), or hex
    - The C array can be loaded by host processor (ARM or DSP) to kick off PRU
  - Other debug formats also can be output
- Command line syntax:
 

```
pasm_2 -V3 [-bcmldxz] SourceFile [-Dname=value] [-CArrayname]
```
- The PASM tool generates a single monolithic binary
  - No linking, no sections, no memory maps, etc.
  - Code image begins at start of IRAM (offset 0x0000)

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## PRU Development Support Integrated in CCS

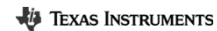
		CCS 5.x
pasm (PRU assembler)		No
AM335x PRU Debug Tools	Disassembly window	Yes
	Memory windows	Yes
	Register windows	Yes
	Execution controls	Yes
	Soft reset control	Yes
	Sleep control	Yes

Download the CCS 5.x here:

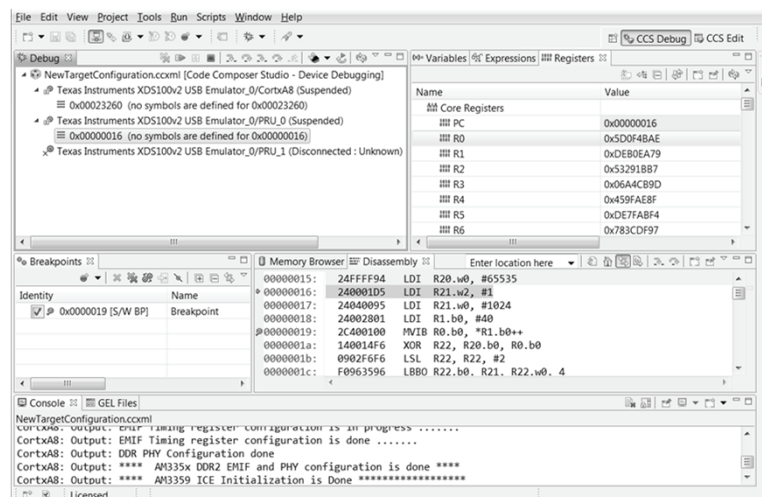
[http://processors.wiki.ti.com/index.php/Download\\_CCS](http://processors.wiki.ti.com/index.php/Download_CCS)

## Summary of PRU Debug Capabilities

- Disassembly window to show PRU assembly code
- Memory windows to show PRU program and data memory contents
  - Ability to load/fill memory contents
  - Ability to save memory contents
  - Ability to load PRU code binaries
- Register windows to show PRU subsystem control, data and status registers
  - View and modify PRU subsystem registers
- Execution controls
  - Run/Halt
  - Single-stepping through assembly instructions
  - Breakpoint control
- PRU soft reset control



## Execution Control Screenshot



## C Compiler

- Developed and maintained by TI CGT team
  - Remains very similar to other TI compilers
- Full support of C/C++
- Adds PRU-specific functionality
  - Can take advantage of PRU architectural features automatically
  - Contains several intrinsics
    - List can be found in Compiler documentation
- Full instruction-set Assembler for hand-tuned routines



## TI PRU CGT Assembler vs PASM

- **Advantages of using TI PRU Assembler over PASM**
  - The biggest advantage is that the TI PRU linker produces ELF files that enable source-level debugging within CCS. No more debugging in disassembly window!!
  - The TI PRU assembler uses the same shell as other TI compilers. Customers only need to learn one set of conventions, directives, etc.
  - TI PRU assembler will be maintained in the future, while PASM will not be updated anymore.
  - The TI PRU assembler uses the powerful TI linker which allows more flexibility than PASM and facilitates linking PRU programs with host CPU image for runtime loading and symbol sharing.
- **Disadvantages of using TI PRU Assembler over PASM**
  - Have to learn new directives if already used to PASM
  - TI PRU assembler requires more command line options and a linker command file.
  - Some porting effort required for reusing legacy PASM projects.

There are some differences in the instructions and directives supported by TI PRU Assembler versus PASM. These are listed in the TI PRU Compiler package release notes which is located at the root of the install folder.



## TI PRU CGT Assembly vs C

- Advantages of coding in Assembly over C
  - Code can be tweaked to save every last cycle and byte of RAM
  - No need to rely on the compiler to make code deterministic
  - Easily make use of scratchpad
- Advantages of coding in C over Assembly
  - More code reusability
  - Can directly leverage kernel headers for interaction with kernel drivers
  - Optimizer is extremely intelligent at optimizing routines
    - “Accelerating” math via MAC unit, implementing LOOP instruction, etc.
  - Not mutually exclusive - inline Assembly can be easily added to a C project



## Agenda

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  - **Linux PRU Application Loader**
- PRU Application
- Other Resources

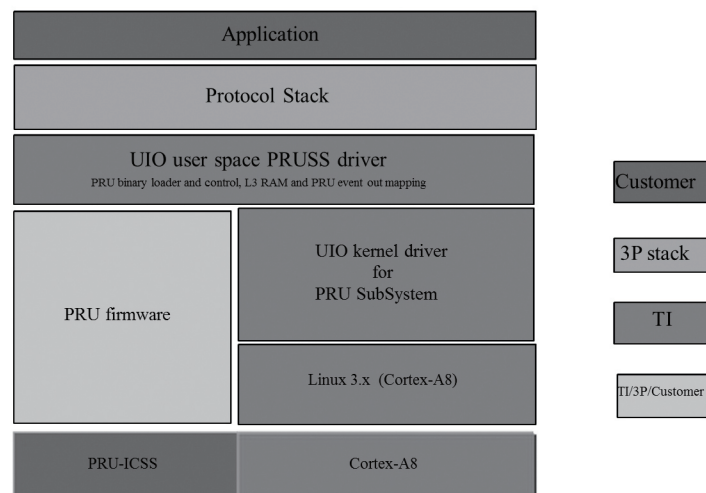


## PRU Linux Loader

- Host processor of SoC must load code to a PRU and initiate its execution
- ARM processor can load code to PRU instruction memory and interact with PRU from user space using the application loader
- Application loader is available in open-source
- Application PRU Loader
  - API's allow ARM to interact with PRU in user space
  - Supports BSD licensing
  - Can be used for protocol emulation and user space applications



## Application Loader S/W Architecture



## Application Loader Examples



AM1808 SDK

- AM335x PRU package includes several basic PRU application example code. These examples use the Linux application loader.
  - Additional PRU examples can be found in the AM1808 SDK.
  - The AM18x PRUSS to AM335x PRU-ICSS Software Migration Guide provides reference of how these examples can be ported to AM335x.
- PRU example code demonstrates:
  - Memory transfers
  - Accessing constant tables \*
  - Interrupts
  - Toggling GPIOs \*
  - eDMA configuration \*
- AM1808 SDK can be downloaded at:  
[http://software-dl.ti.com/dsp/dsp\\_public\\_sw/sdo\\_sb/targetcontent/sdk/AM1x/latest/index\\_FDS.html](http://software-dl.ti.com/dsp/dsp_public_sw/sdo_sb/targetcontent/sdk/AM1x/latest/index_FDS.html)

\* Only included in AM1808 examples.



## Steps to use develop code

- To Use,
  - Build UIO kernel driver as module
  - Build User space API's, link to application code
  - Compile application code using API
  - Compile PRU binaries using PASM
- On file system, install UIO kernel driver, application executables, PRU binaries



## Agenda

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  - Linux PRU Application Loader
- **PRU Application**
- Other Resources



## PRU (Programmable Real-time Unit) For Configurable Logic *Enabling real-time Ethernet Slave communications*

### Architecture

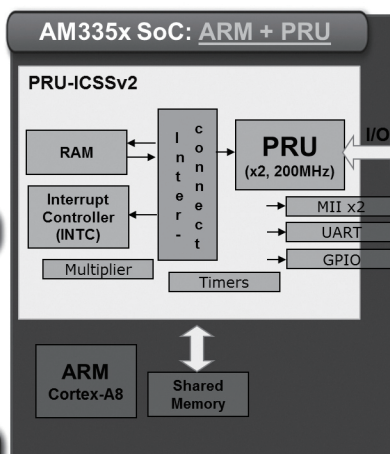
- Real-time oriented – 100% Deterministic
- Two 32-bit RISC cores for real-time functions each running at 200MHz
- 8KB IRAM, 8KB DRAM, 12KB Shared RAM
- Single-cycle execution & Direct I/O interface sampling at ~5ns
- Very easy to program
- Logic, Control and arithmetic instructions
- 32-bit MULT and Interrupt controller

### Capabilities

- Implement Real-time communication interfaces : PROFIBUS, EtherCAT, PROFINET & Ethernet/IP
- Implement custom IP (such as EnDAT 2.2, SINC3 decimation, PWMs, DP Memory, Manchester Coding, 9 bit UART or a Backplane bus)

### Advantages

- Easy to program & completely Flexible
- Reduce system cost & complexity





***Preliminary – Future dates are Subject to change***

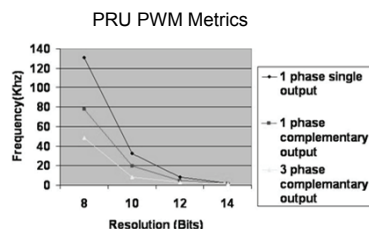
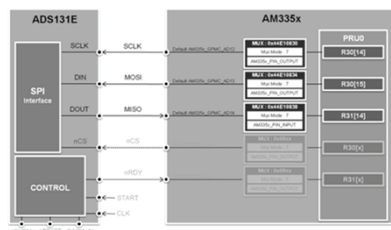
Protocol	Configuration	SW Availability	3 <sup>rd</sup> party Stack Partners
Profibus	Slave (AM1810 & AM335x)	SDK Release (AM1810): Now Certification (AM1810): Now GA SDK release (AM335x) – Now	TMG
EtherCAT	Slave only (AM335x)	Beta SDK release – Now GA SDK Release – Now Certification: Now	ETG Koenig, Acontis, Port
Ethernet/IP (w/ Gb switch)	Slave only (AM335x)	EA SDK Release: Now Certification: 2Q14 GA SDK Release: 3Q14	Molex
Ethernet/IP (w/ PRU)	Slave only (AM335x)	EA SDK Release: Now Certification: 2Q14 GA SDK Release: 3Q14	Molex
PROFINET-RT/IRT	Slave only (AM335x)	EA SDK Release: NOW Certification: NOW; 2Q14 (IRT) GA SDK release: 3Q14	Molex
OpenMAC for Powerlink	Slave only (AM335x)	Available from 3P (Port)	Port
Sercos-3	Slave Only (AM335x)	Available from 3P (Automata)	Automata
IEC61850	Client/Server (AM335x)	Available from 3P (TriangleMicroWorks)	TMW

SDK: Software Development Kit



## PRU – Simple Coding Examples

Project	Scale	Comment
<u>SPI Interface with ADS131E0</u>	Scale up to 8 SPIs	eliminates 4 x STM32
<u>3 Phase PWM</u>	8 kHz compl 3 phase	overcome pin-mux
<u>SINC3 Filter for Sigma Delta Modulator</u>	2 channel 10MHz	
<u>Soft-UART</u>	up to 115200 baud	Two full duplex Soft-UARTS per PRU



## Agenda

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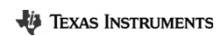


## PRU-ICSS Documentation and Resources

- CCS External Download at  
[http://processors.wiki.ti.com/index.php/Download\\_CCS](http://processors.wiki.ti.com/index.php/Download_CCS)
- AM335x PRU-ICSS Documentation is available in the  
AM335x PRU-ICSS package



# Backup



## IA-SDK Links

- Download:
  - <http://www.ti.com/tool/sysbiossdk-ind-sitara>
- **Getting Started Guide** (generic):
  - [http://processors.wiki.ti.com/index.php/AM335x\\_SYSBIOS\\_Industrial\\_SDK\\_Getting\\_Started\\_Guide](http://processors.wiki.ti.com/index.php/AM335x_SYSBIOS_Industrial_SDK_Getting_Started_Guide)
- **Release Notes** (release dependent):
  - [http://processors.wiki.ti.com/index.php/AM335x\\_SYSBIOS\\_Industrial\\_SDK\\_01.00.00.08\\_Release\\_Notes](http://processors.wiki.ti.com/index.php/AM335x_SYSBIOS_Industrial_SDK_01.00.00.08_Release_Notes)
- **User Guide** (release dependent):
  - [http://processors.wiki.ti.com/index.php/AM335x\\_SYSBIOS\\_Industrial\\_SDK\\_01.00.00.08\\_User\\_Guide](http://processors.wiki.ti.com/index.php/AM335x_SYSBIOS_Industrial_SDK_01.00.00.08_User_Guide)
- Default install path:
  - <drive>:/ti/am335x\_sysbios\_ind\_sdk\_x.x.x.x
  - Should be aligned with CCS and Sys/Bios paths



# Communication Slave Architecture

## TI Software

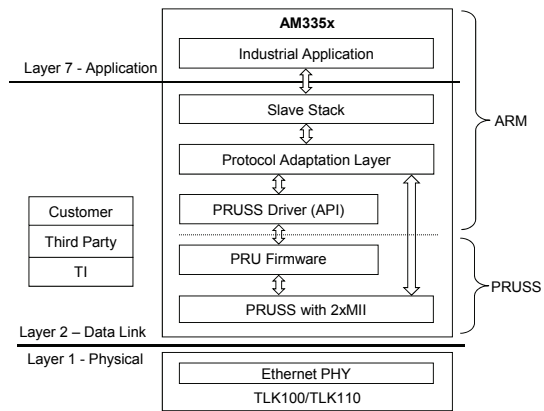
- SYS/BIOS based IA-SDK
- Starterware device drivers
- Protocol adaptation layer
- PRU-ICSS firmware implementing communication protocol HW layer

## Third Party Software

- Slave stack source code

## Customer Software

- Industrial Application
- Sample application provided by TI



TEXAS INSTRUMENTS

# Example: EtherCAT Slave

## TI Software

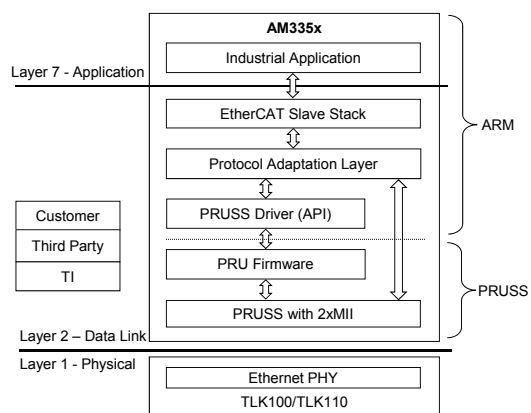
- SYS/BIOS based SDK
- Starterware device drivers
- Protocol adaptation layer for EtherCAT
- PRUSS EtherCAT firmware

## Third Party Software

- Fully validated evaluation version of Beckhoff Slave stack included in Software Development Kit
- Free production license for ETG members (ETG membership is free)
- Compatible with other third party EtherCAT stacks

## Customer Software

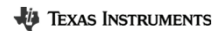
- Industrial Application
- Sample application provided by TI



TEXAS INSTRUMENTS

## IA-SDK contents

[docs]	- main documentation
[drivers]	- PRUSS, LED, MMU and UART drivers for ICS/IDK
[examples]	
...[ethercat_slave]	- EtherCAT example (to be used with SSC)
...[powerlink_slave]	
...[profibus_slave]	
...[uartecho]	
[platform]	- generic AM335x drivers (based on Starterware)
[protocols]	- PRU firmware and API libs
...[EtherCAT_slave]	
...[Powerlink_slave]	
[starterware]	- base SoC code, drivers and tools
[tools]	- GEL, post build and FLASH tools



## EtherCAT Protocol

[docs]	- EtherCAT Firmware/API docs
[firmware]	- PRUSS binary as header files for PRUSS driver usage
[ecat_appl]	- EtherCAT example to be patched on SSC 5.0.1 sources
[include]	- header files for EtherCAT slave controller (ESC) API and Slave Sample Code
[stack]	- pre-compiled library of Beckhoff SSC (proprietary sw)

- SSC source code is available for free from Beckhoff for all ETG members.
- SSC source required to modify stack options and/or change EtherCAT application
- Future IA-SDK to be based on latest SSC release at the time

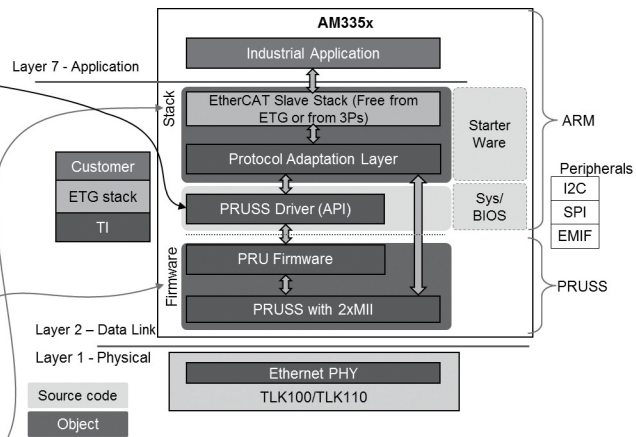


## IA-SDK File Structure

```

|--- sdk
|   |--- docs
|   |   |--- AM335x Industrial SDK User Guide
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|   |   |   |--- evm-am335x
|   |   |   |   |--- include
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|   |--- protocols
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|   |   |   |--- firmware
|   |   |   |--- include
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```



ETG: EtherCAT Technology Group

