KeyStone SoC Architecture Overview

KeyStone Training

Texas Instruments

Agenda

- Keystone SoC Innovation and Application
- KeyStone I Architecture
  - CorePac & Memory Subsystem
  - Internal Communications and Transport
  - External Interfaces
  - Coprocessors and Accelerators
  - Miscellaneous
- KeyStone II Architecture
  - ARM Cortex-A15 CorePac
  - Performance/Throughput Improvements
- KeyStone Platform
  - Debug
  - Device-Specific Offerings

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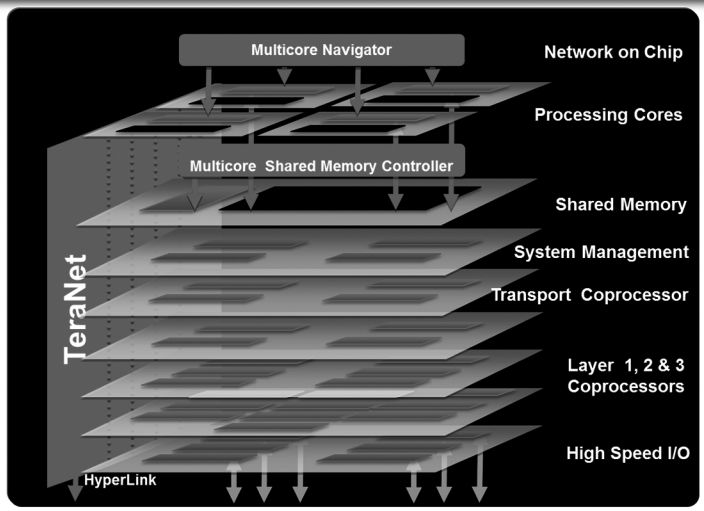
YA2

KeyStone Multicore SOC Architecture

The first network on chip infrastructure to unleash full multicore entitlement



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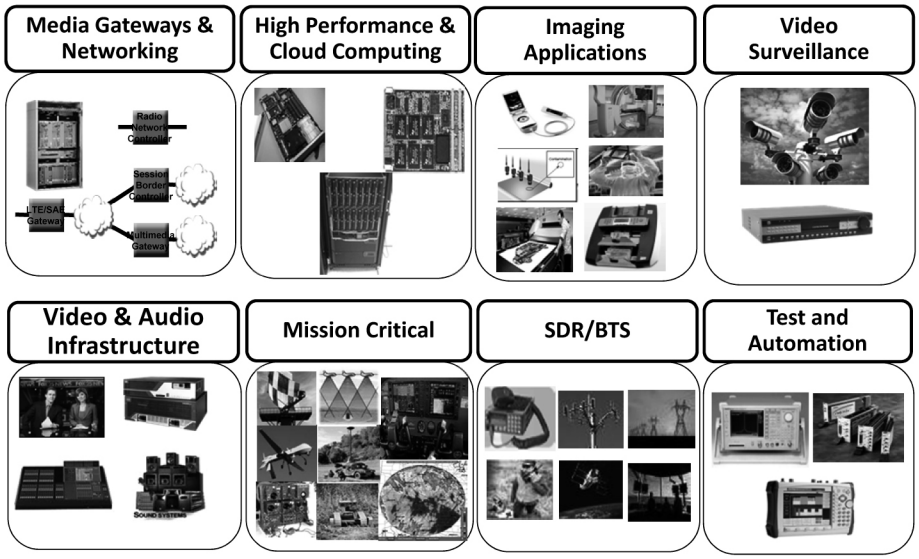
TI Keystone SoC Applications



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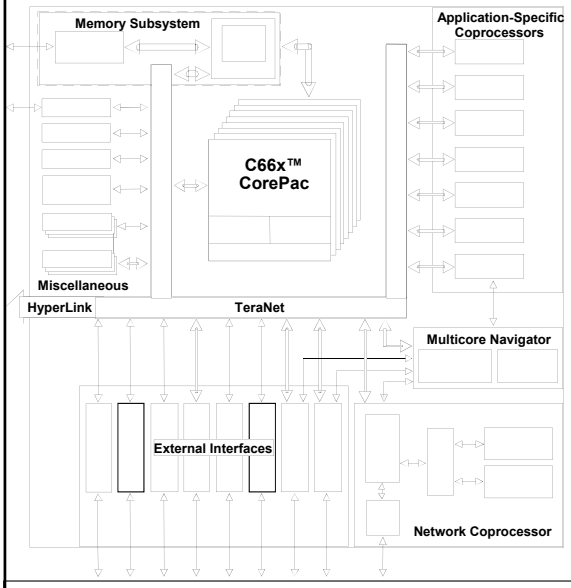
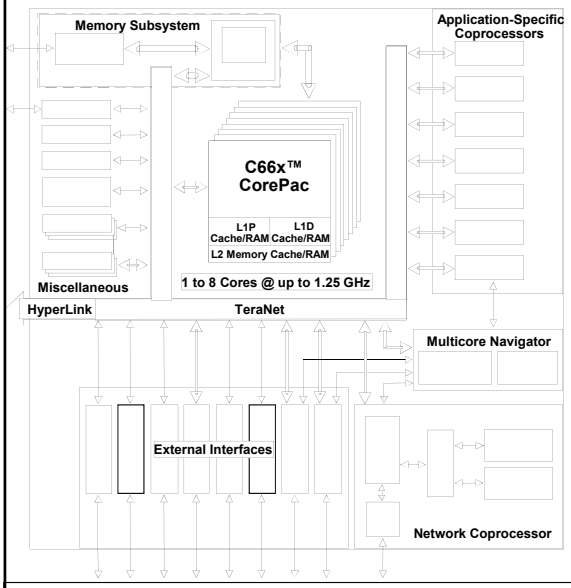
KeyStone I Architecture

- CorePac & Memory Subsystem
- Internal Communications and Transport
- External Interfaces
- Coprocessors and Accelerators
- Miscellaneous

KeyStone I Device Architecture



KeyStone I CorePac



- 1 to 8 C66x CorePac DSP Cores operating at up to 1.25 GHz
  - Fixed- and floating-point operations
  - Code compatible with other C64x+ and C67x+ devices
- L1 Memory
  - Can be partitioned as cache and/or RAM
  - 32KB L1P per core
  - 32KB L1D per core
  - Error detection for L1P
  - Memory protection
- Dedicated L2 Memory
  - Can be partitioned as cache and/or RAM
  - 512 KB to 1 MB Local L2 per core
  - Error detection and correction for all L2 memory
- Direct connection to memory subsystem

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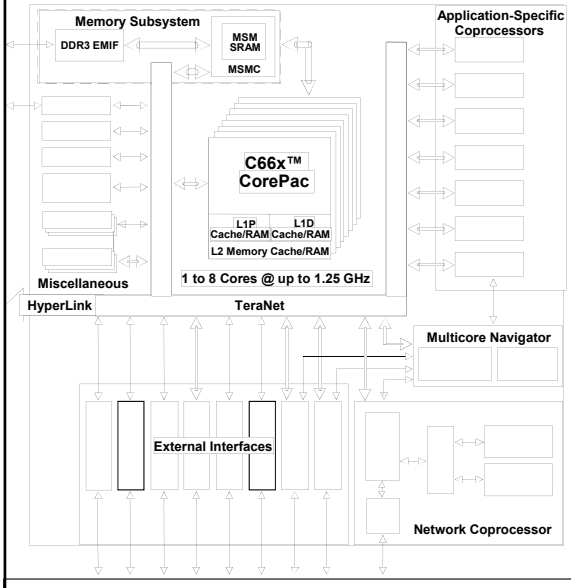
KeyStone I Memory Subsystem



- Multicore Shared Memory (MSM SRAM)
  - 1 to 4 MB
  - Available to all cores
  - Can contain program and data
  - All devices except C6654
- Multicore Shared Memory Controller (MSMC)
  - Arbitrates access of CorePac and SoC masters to shared memory
  - Provides a connection to the DDR3 EMIF
  - Provides CorePac access to coprocessors and IO peripherals
  - Provides error detection and correction for all shared memory
  - Memory protection and address extension to 64 GB (36 bits)
  - Provides multi-stream pre-fetching capability
- DDR3 External Memory Interface (EMIF)
  - Support for 16-bit, 32-bit, and (for C667x devices) 64-bit modes
  - Specified at up to 1600 MT/s
  - Supports power down of unused pins when using 16-bit or 32-bit width
  - Support for 8 GB memory address
  - Error detection and correction

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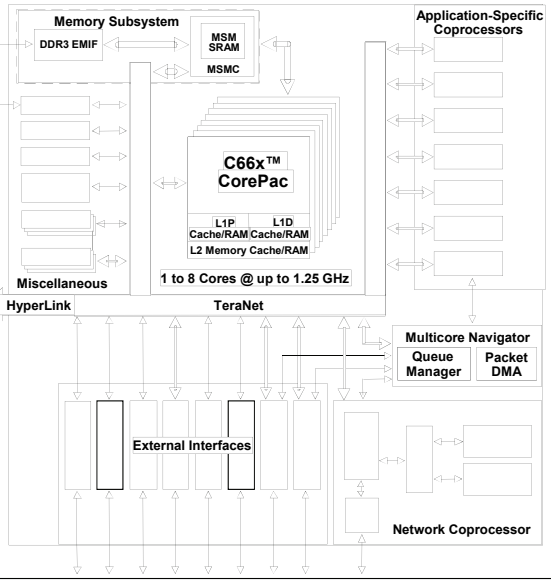
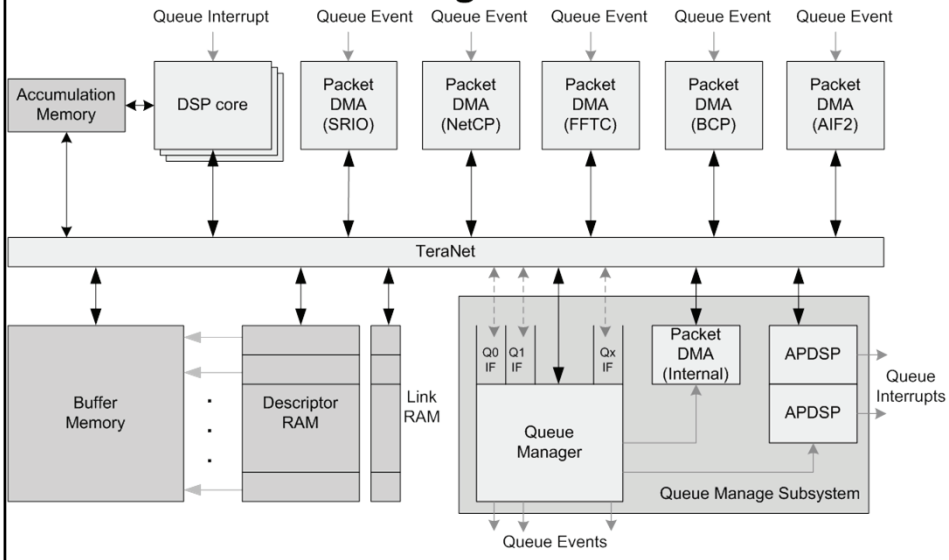
KeyStone I Multicore Navigator

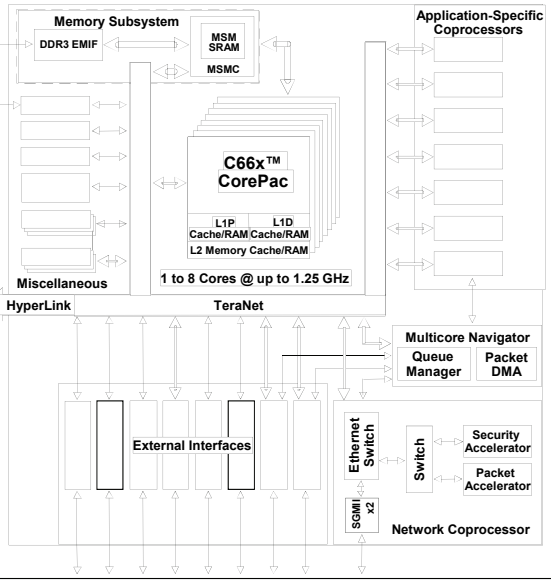


- Provides seamless inter-core communications (messages and data exchanges) between cores, IP, and peripherals. "Fire and forget"
- Low-overhead processing and routing of packet traffic to and from peripherals and cores
- Supports dynamic load optimization
- Data transfer architecture designed to minimize host interaction while maximizing memory and bus efficiency
- Consists of a Queue Manager Subsystem (QMSS) and multiple, dedicated Packet DMA (PKTDMA) engines

Keystone I
Multicore Navigator architecture

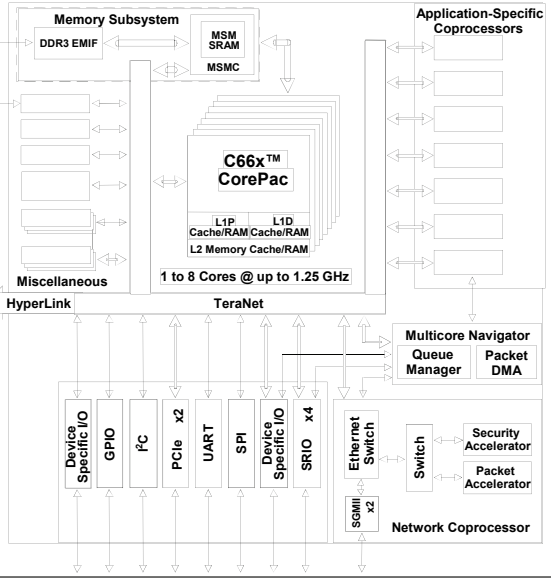


KeyStone I Network Coprocessor



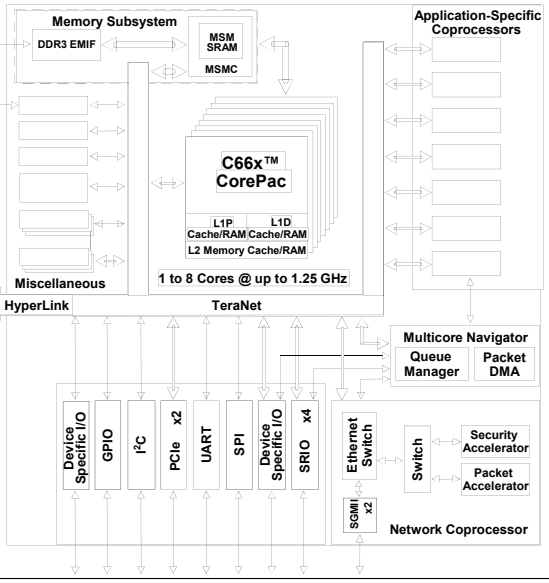
- Provides hardware accelerators to perform L2, L3, and L4 processing and encryption that was previously done in software
- Packet Accelerator (PA)
  - Single or multiple IP address option
  - UDP (and TCP) checksum and selected CRCs
  - L2/L3/L4 support
  - Quality of Service (QoS)
  - Multicast to multiple destinations inside the device
  - Timestamps
- Security Accelerator (SA)
  - Hardware encryption, decryption, and authentication
  - Supports IPsec ESP, IPsec AH, SRTP, and 3GPP protocols

KeyStone I External Interfaces



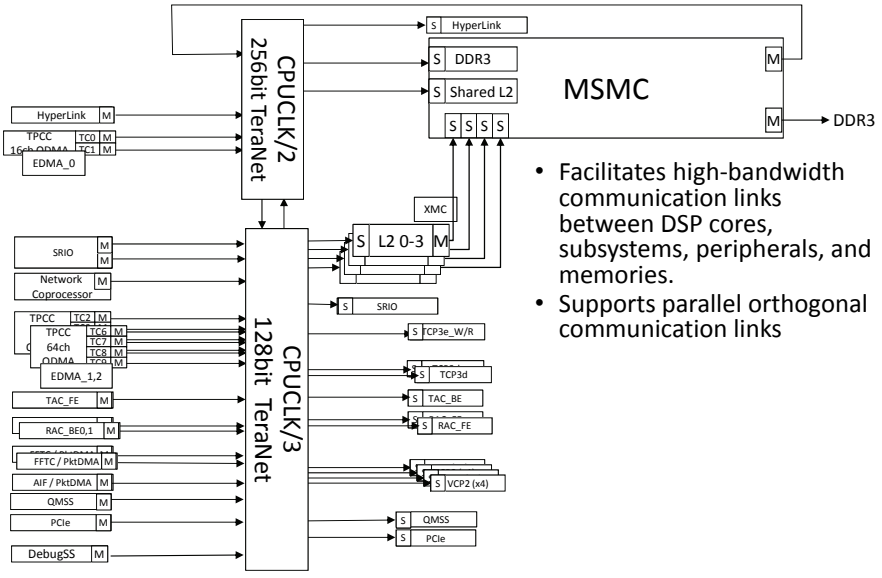
- 2x SGMII ports support 10/100/1000 Ethernet
- 4x high-bandwidth Serial RapidIO (SRIO) lanes
- 2x PCIe at 5 Gbps
- SPI for boot operations
- UART for development/testing
- I2C for EPROM at 400 Kbps
- GPIO
- Device-specific Interfaces
  - Wireless Applications
  - General Purpose Applications

TeraNet Switch Fabric



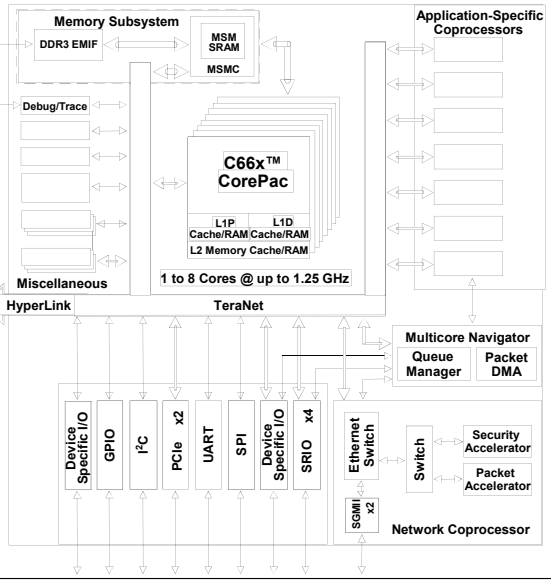
- A non-blocking switch fabric that enables fast and contention-free internal data movement
- Provides a configured way – within hardware – to manage traffic queues and ensure priority jobs are getting accomplished while minimizing the involvement of the CorePac cores
- Facilitates high-bandwidth communications between CorePac cores, subsystems, peripherals, and memory

KeyStone I TeraNet Data Connections



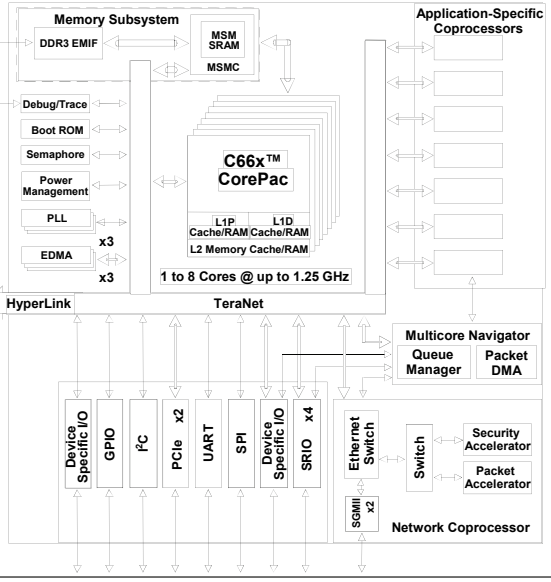
- Facilitates high-bandwidth communication links between DSP cores, subsystems, peripherals, and memories.
- Supports parallel orthogonal communication links

KeyStone I HyperLink Bus



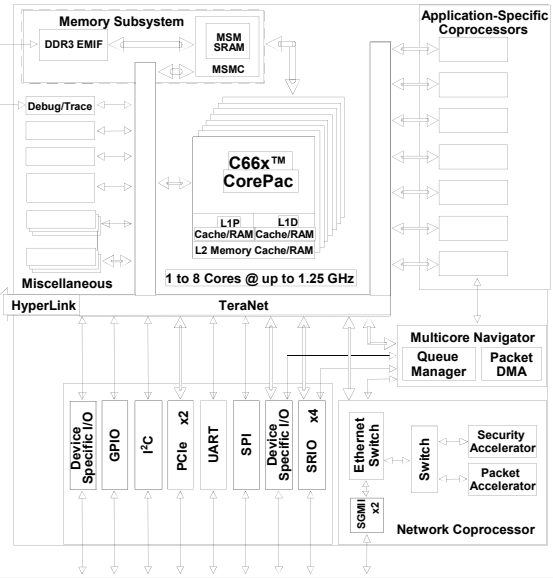
- Provides the capability to expand the device to include hardware acceleration or other auxiliary processors
- Supports four lanes with up to 12.5 Gbaud per lane

KeyStone I Miscellaneous Elements



- Boot ROM
- Semaphore module provides atomic access to shared chip-level resources.
- Power Management
- Three on-chip PLLs:
  - PLL1 for CorePacs, except
  - PLL2 for DDR3
  - PLL3 for Packet Acceleration
- Three EDMA controllers
- Eight 64-bit timers
- Inter-Processor Communication (IPC) Registers

Diagnostic Enhancements

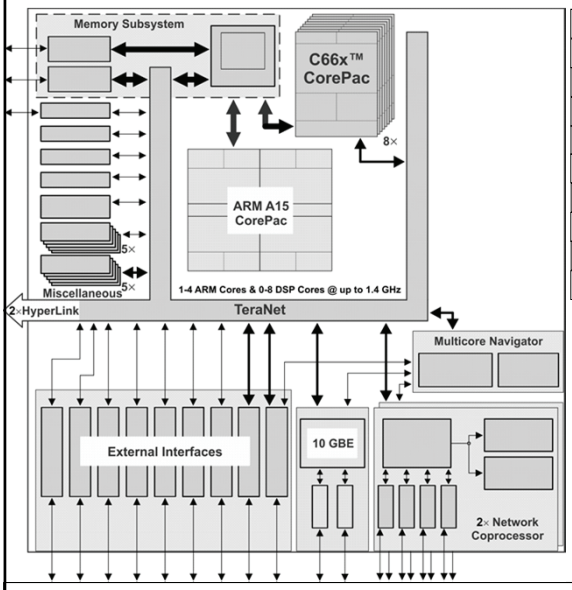


- Embedded Trace Buffers (ETB) enhance the diagnostic capabilities of the CorePac.
- CP Monitor enables diagnostic capabilities on data traffic through the TeraNet switch fabric.
- Automatic statistics collection and exporting (non-intrusive)
- Monitor individual events for better debugging
- Monitor transactions to both memory end point and Memory-Mapped Registers (MMR)
- Configurable monitor filtering capability based on address and transaction type

KeyStone II Architecture

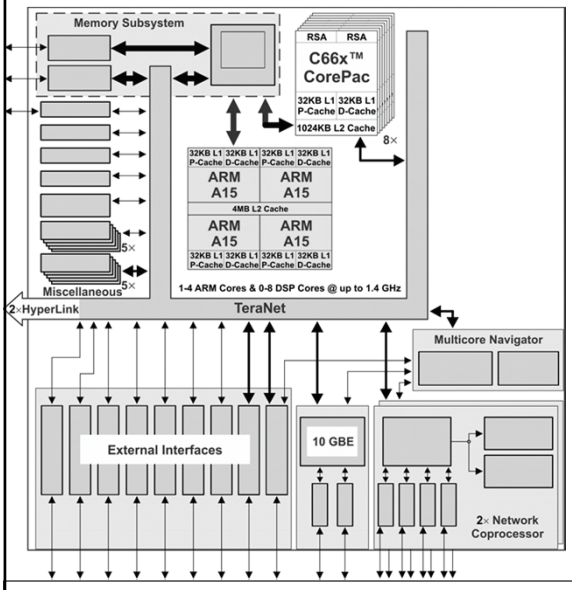
- **ARM Cortex-A15 CorePac**
- **Performance/Throughput Improvements**

KeyStone II Device Architecture



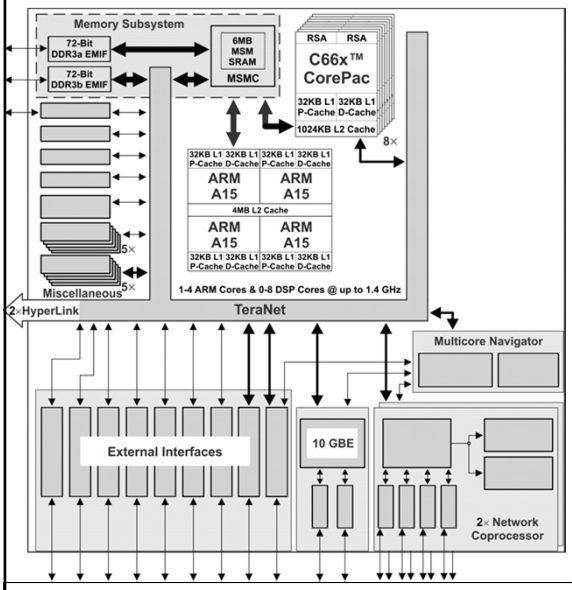
C66x CorePac
ARM A15 CorePac
Memory Subsytem
Multicore Navigator
Network Coprocessor
TeraNet Switch Fabric
10 Gigabit Ethernet (10 GBE)
External Interfaces
HyperLink Bus
Miscellaneous

ARM Cortex-A15 CorePac



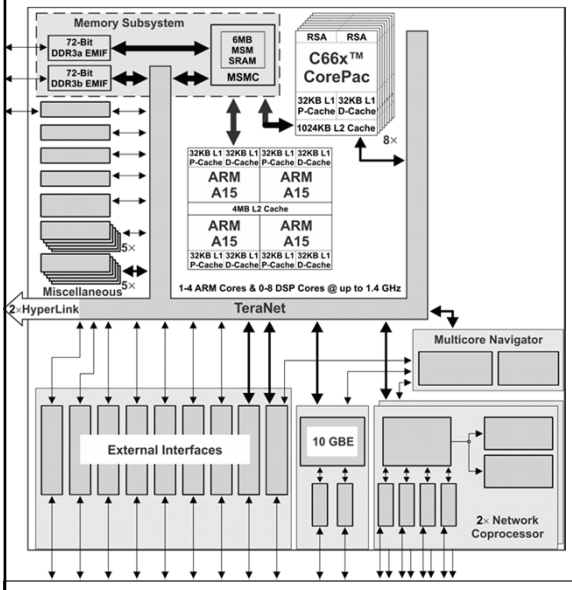
- Single, Dual, or Quad-ARM A15 CorePac operating at up to 1.4 GHz.
  - Full implementation of ARMv7-A architecture instruction set
  - Integrated Neon and Vector Floating-Point Unit
- L1 Memory: 32KB L1 per ARM A15 for caching program and data
- L2 Memory:
  - Shared L2 Cache Memory with full cache coherency using Snoop Control Unit (SCU)
  - 4 MB L2 Cache is shared between the 1 to 4 ARM A15 core(s).
- The AMBA 4.0 AXI Coherency Extension (ACE) master port is connected directly to the MSMC2 for short-path access to shared MSMC SRAM.
- The ACE also provides IO-coherent access to the shared memory and external memory connected through the EMIF.
- Cluster-level and core-level power management and low-power standby modes (also known as WFI/WFE modes)

KeyStone II Memory Subsystem: MSM/MSMC



- Multicore Shared Memory (MSM SRAM)
  - 2-6 MB shared among the C66x and ARM A15 CorePacs.
  - May contain program and data
- Multicore Shared Memory Controller (MSMC version 2.0)
  - Arbitrates access of C66x and ARM A15 CorePac and SoC masters to shared and external memory through DDR3 EMIF
  - Provides error detection and correction for all shared memory
  - Memory protection and address extension to 64 GB (36 bits)
  - Provides multi-stream pre-fetching capability
  - Support for ARM coherency with EDMA/peripheral masters in DDR3A and MSMC SRAM space
  - 8 SRAM banks
  - Runs at the DSP frequency, thereby increasing memory access by fourfold compared to previous MSMC v1.0

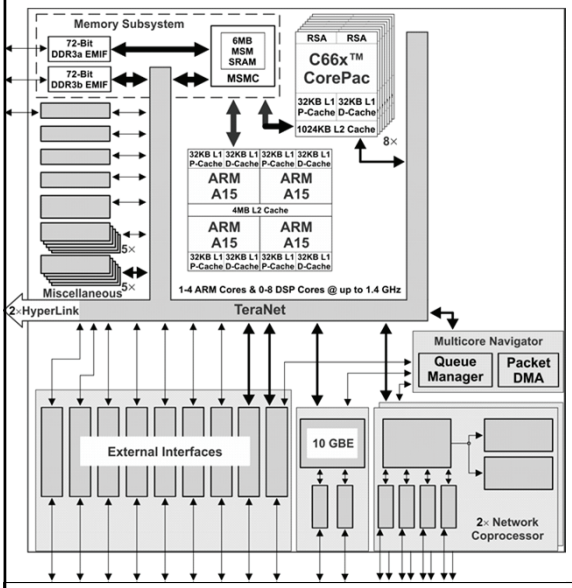
KeyStone II Memory Subsystem: DDR3



Up to two DDR3 subsystem(s) per device:

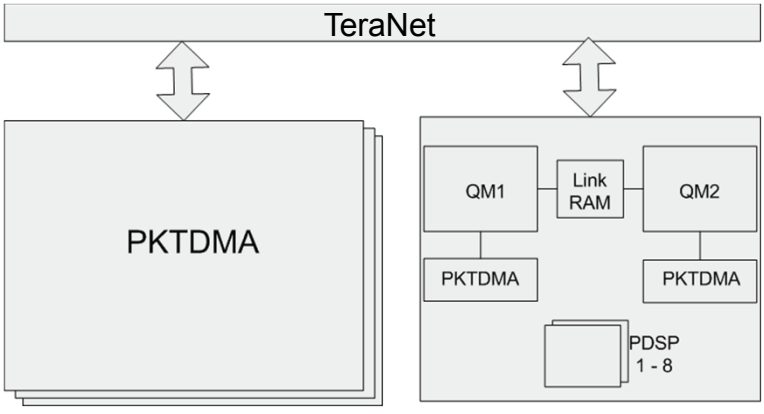
- The first DDR3 subsystem (DDR3A) supports up to 8 GB memory addresses and is connected to the CorePac(s) through the MSMC.
- When present, the second DDR3 subsystem (DDR3B) supports up to 2GB memory address and is connected directly to the TeraNet.
- Each DDR consists of a 64b/72b EMIF controller:
  - Supports 16-bit, 32-bit, and 64-bit modes .
  - **Operates at up to 1600 MT/s**
  - Supports power down of unused pins when using 16-bit or 32-bit width

KeyStone II Multicore Navigator

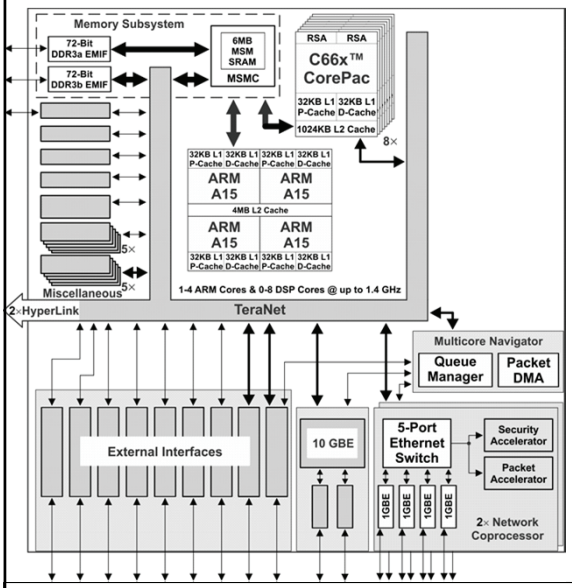


- Consists of the following:
  - 2x Queue Manager
  - Multiple, dedicated Packet DMA engines
  - 2x infrastructure DMAs
- Provides seamless inter-core communications (messages and data exchanges) between cores, IP, and peripherals. “Fire and forget.”
- Low-overhead processing and routing of packet traffic to and from peripherals and cores
- Supports dynamic load optimization
- Data transfer architecture designed to minimize host interaction while maximizing memory and bus efficiency
- Supports up to 16K hardware queues and 1M descriptors (32K internal).

KeyStone II Multicore Navigator Architecture

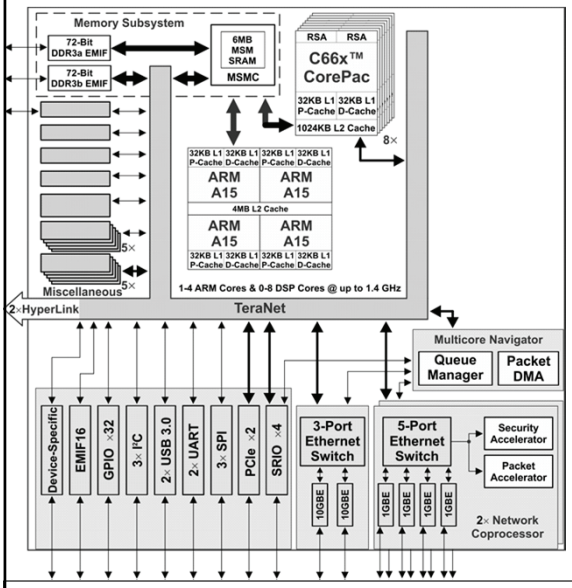


KeyStone II Network Coprocessor (NETCP)



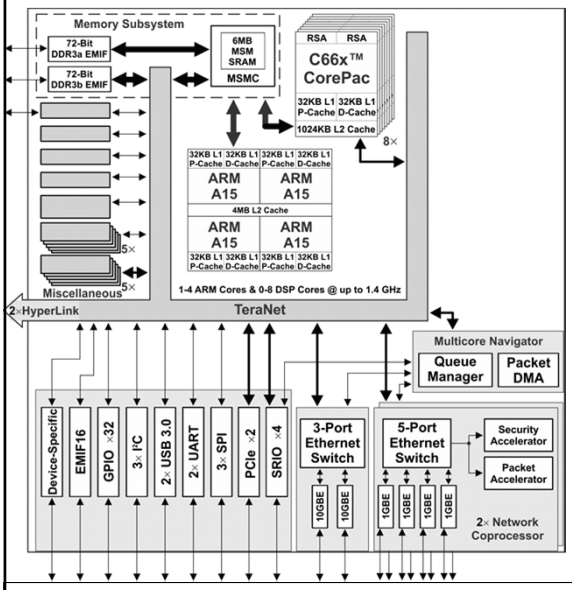
- Consists of one or two Network Coprocessor(s)
- Provides hardware accelerators to perform L2, L3, and L4 processing and encryption that was previously done in software
- Packet Accelerator (PA)
  - Single IP address option
  - UDP (and TCP) checksum and selected CRCs
  - L2/L3/L4 support
  - Quality of Service (QoS)
  - Multicast to multiple queues
  - Timestamps
- Security Accelerator (SA)
  - Hardware encryption, decryption, and authentication
  - Supports IPsec ESP, IPsec AH, SRTP, and 3GPP protocols
- 2x 5-port Ethernet switches (depending on number of instances of NETCP) with 4-8 ports connecting to 4-8 SGMII ports and one port connecting to the Packet and Security Accelerators.

KeyStone II External Interfaces



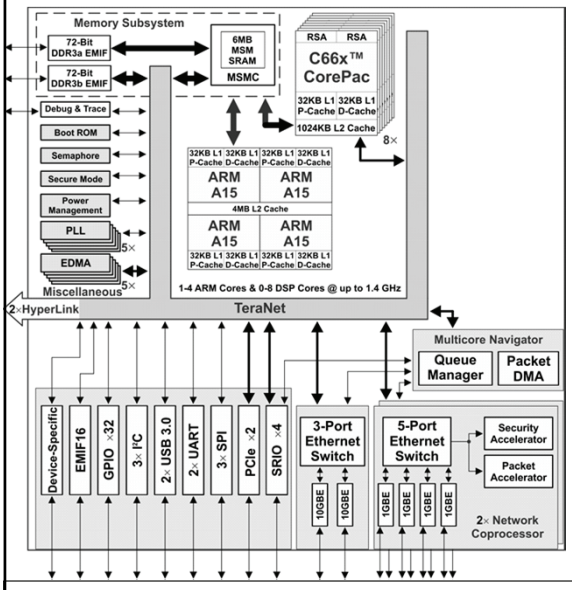
- **8x SGMII ports support 10/100/1000M Ethernet through 1-2x 5-port Ethernet switch(es).**
- **2x XGMII ports support up to 10G Ethernet through a 3-port Ethernet switch.**
- 4x high-bandwidth Serial RapidIO (SRIO v2.1) lanes for inter-DSP applications
- **2x PCIe at 5 Gbps**
- **3x SPI modules with up to four chip selects per module.**
- **2x UART for development/testing**
- **2x USB 3.0**
- **3x I2C at 400 Kbps**
- **32 GPIO pins**
- EMIF 16
- Device-specific interfaces

KeyStone II HyperLink Bus



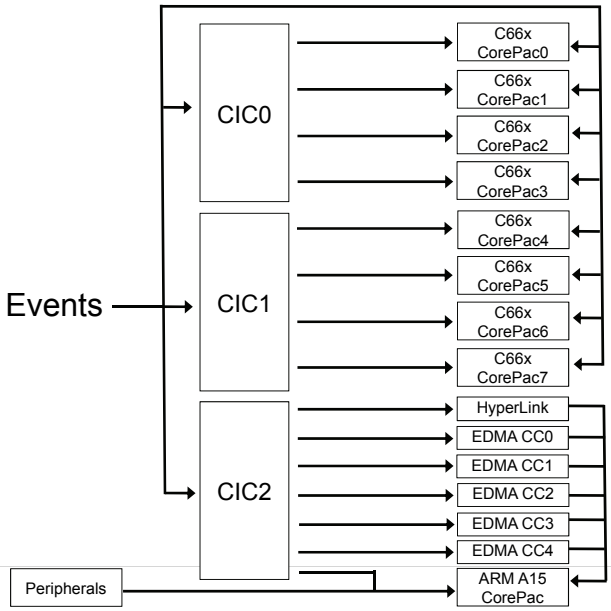
- Provides TI-propriety, high-speed interconnects termed HyperLink.
- **Up to 2x HyperLink modules with 4 lanes each.**
- Provides the capability to expand the device to include hardware acceleration or other auxiliary processors
- Supports up to 12.5 Gbaud per lane

KeyStone II Miscellaneous Elements



- **ARM- and DSP-driven Boot ROM:**
  - **C66x CorePacs support booting from SRIO, PCIe, I2C Master, I2C Slave, SPI, Ethernet, XIP, and HyperLink.**
  - **ARM CorePacs support booting from UART, NAND, XIP, SPI, Ethernet, PCIe, I2C, SRIO and HyperLink.**
  - **Support varies by peripheral availability**
- Semaphore module provides atomic access to shared chip-level resources.
- **Secure Mode (1-time burn security key)**
- **Power Management:**
  - **Manages power- and clock-switching of individual IPs and CorePac(s).**
  - **Supports Dynamic Power Switching (DPS):**
    - **Power-state hibernation modes 1 and 2**
    - **Manages each C66x CorePac, each ARM core, and/or the entire ARM CorePac**
  - **Reset isolation capability on select peripherals**
  - **SmartReflex Class 0 and Class 3**
- **Up to 5 on-chip PLLs:**
  - **One Main PLL**
  - **One PLL for DDR3A**
  - **One PLL for DDR3B**
  - **One PLL for ARM CorePac**
  - **One PLL for Packet Accelerator**
- **5x EDMA controllers**
- 20x 64-bit timers
- Inter-Processor Communication (IPC) Registers

KeyStone II Central Interrupt Controller

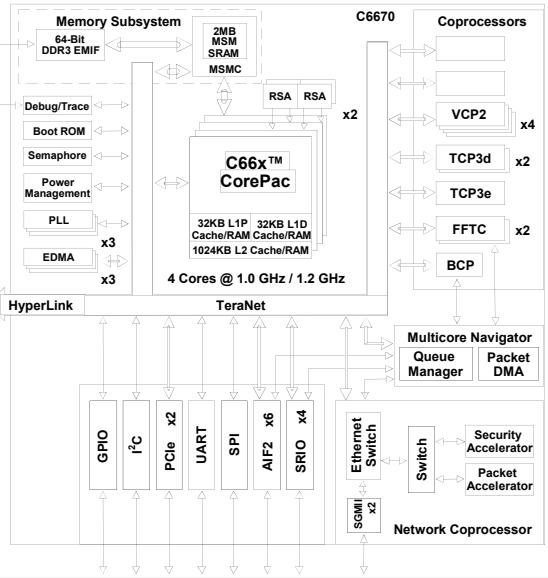


KeyStone Platform

Device-Specific Offerings

Texas Instruments

Device-Specific: C6670 for Wireless Apps



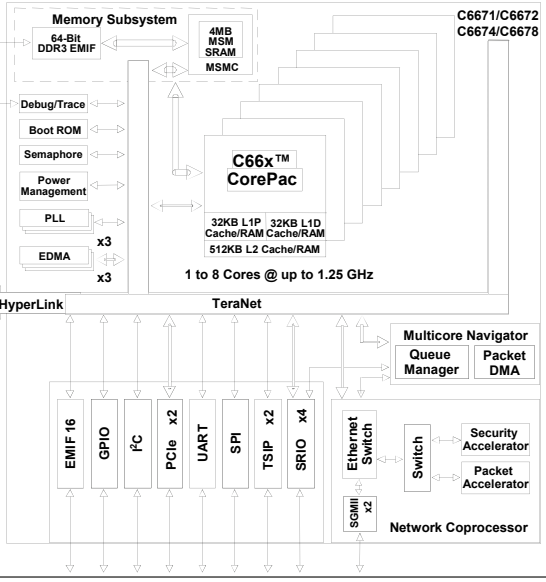
Device-specific Coprocessors:

- 2x FFT Coprocessor (FFTC)
- Turbo Decoder/Encoder Coprocessor (TCP3d/3e)
- 4x Viterbi Coprocessor (VCP2)
- Bit-rate Coprocessor (BCP)
- 2x Rake Search Accelerator (RSA)

Device-specific Interfaces:

- 6x Antenna Interface 2 (AIF2)

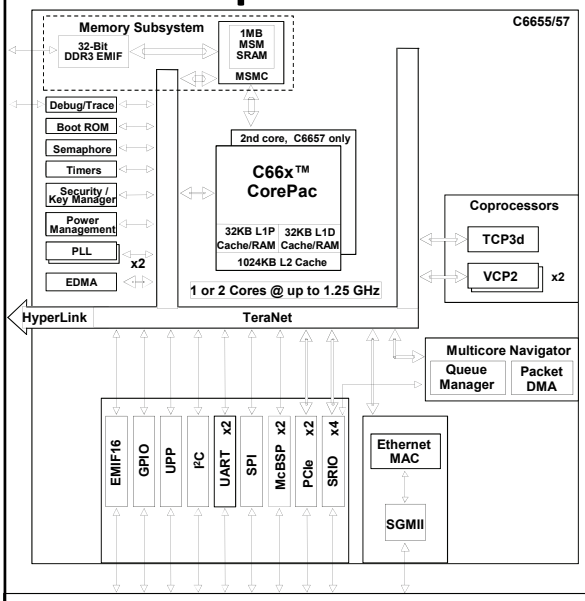
Device-Specific: C667x General Purpose



Device-specific Interfaces:

- 2x Telecommunications Serial Port (TSIP)
- Asynchronous Memory Interface (EMIF16):
  - Connects memory up to 256 MB
  - Three modes:
    - Synchronized SRAM
    - NAND flash
    - NOR flash

Device-Specific: C665x General Purpose



Device-specific Coprocessors:

- Turbo Decoder Coprocessor (TCP3d)
- 2x Viterbi Coprocessor (VCP2)

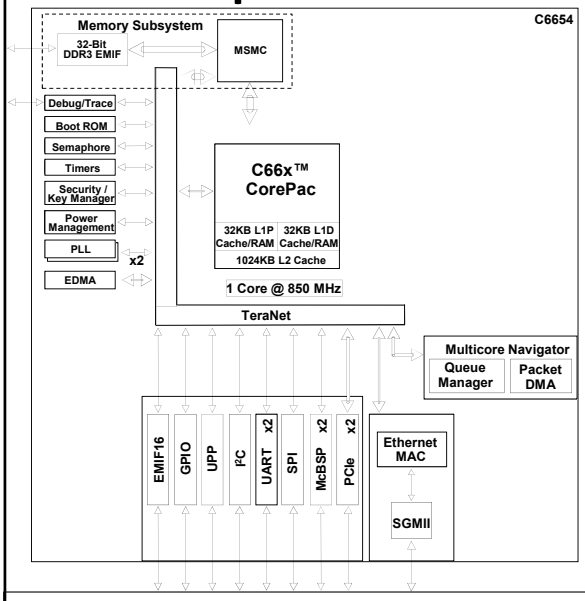
Device-specific Interfaces:

- Asynchronous Memory Interface (EMIF16)
- Universal Parallel Port (UPP)
- 2x Multichannel Buffered Serial Ports (McBSP)

Device-specific Memory:

- 1 MB Multicore Shared Memory (MSM SRAM)
- 32-bit DDR3 Interface

Device-Specific: C665x Power Optimized



Device-specific Interfaces:

- Asynchronous Memory Interface (EMIF16)
- Universal Parallel Port (UPP)
- 2x Multichannel Buffered Serial Ports (McBSP)

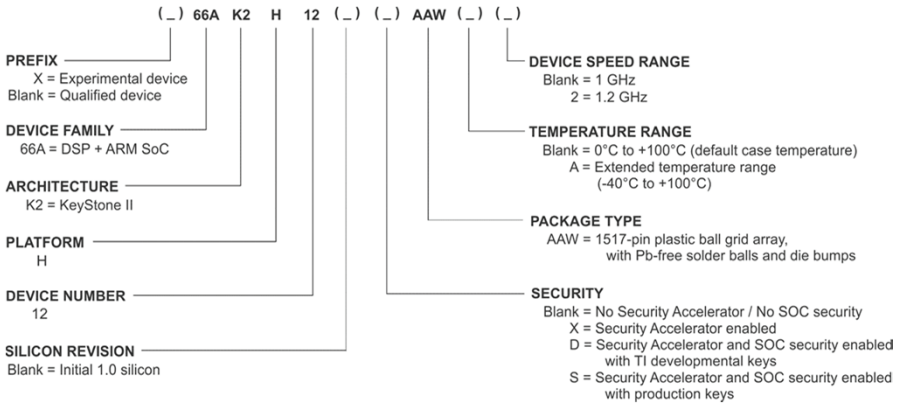
Device-specific Memory:

- 32-bit DDR3 Interface

KeyStone C665x: Key HW Variations

HW Feature	C6654	C6655	C6657
CorePac Frequency (GHz)	0.85	1 @ 1.0, 1.25	2 @ 0.85, 1.0, 1.25
Multicore Shared Memory (MSM)	No	1024KB SRAM	
DDR3 Maximum Data Rate	1066	1333	
Serial Rapid I/O Lanes	No	4x	
HyperLink	No	Yes	
Viterbi Coprocessor (VCP)	No	2x	
Turbo Coprocessor Decoder (TCP3d)	No	Yes	
Network Coprocessor (NETCP)	No	No	

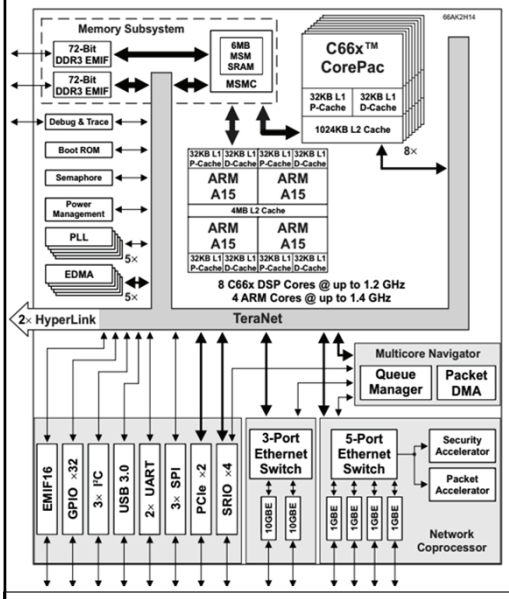
KeyStone II Part Numbering



K2H Compared to K2E

Platform	C66x DSP	ARM A15	Max Clock Ghz	MSMC Shared Memory – MB	Navigator Queues	DDR3 EMIF 72-bit 1600 MT/s	5-Port 1GB Switch	3-Port 10GB Switch	USB 3.0	HyperLink	SRIO x4	PCIe x2	TSIP
K2E	0x to 1x	1x to 4x	ARM = 1.4 DSP = 1.4	2	8K	1x	1x to 2x	1x	2x	1x	--	2x	1x
K2H	4x to 8x	2x to 4x	ARM = 1.4 DSP = 1.2	6	16K	2x	1x	1x	1x	2x	1x	1x	--

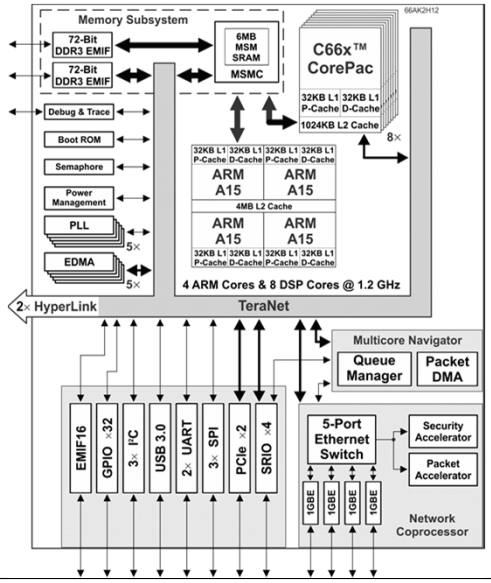
K2H Platform Device Variations



The K2H platform has two variations:

- 66AK2H14
  - 8x C66x CorePacs
  - Quad-ARM A15 CorePac
  - 2x Queue Managers support up to 16K queues
  - 1x 5-port Network Coprocessor (NETCP)
  - 1x USB3.0 to support solid state drive
  - 1x 3 port 10GBE Switch Subsystem

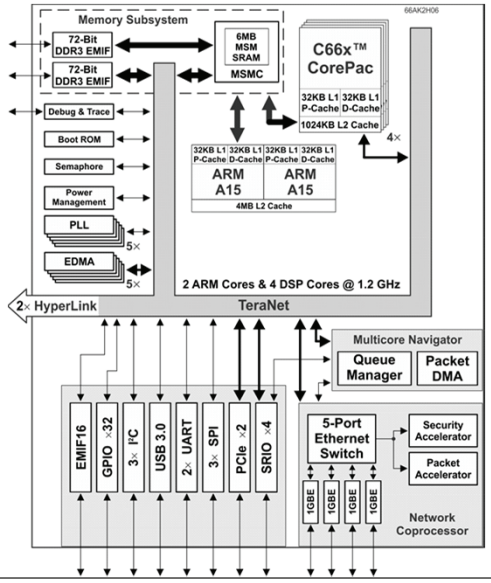
K2H Platform Device Variations



The K2H platform has two variations:

- 66AK2H14
  - 8x C66x CorePacs
  - Quad-ARM A15 CorePac
  - 2x Queue Managers support up to 16K queues
  - 1x 5-port Network Coprocessor (NETCP)
  - 1x USB3.0 to support solid state drive
  - 1x 3 port 10GBE Switch Subsystem
- 66AK2H12
  - Scaled-down version of 66AK2H14
  - 10GBE interface is NOT available.

K2H Platform Device Variations



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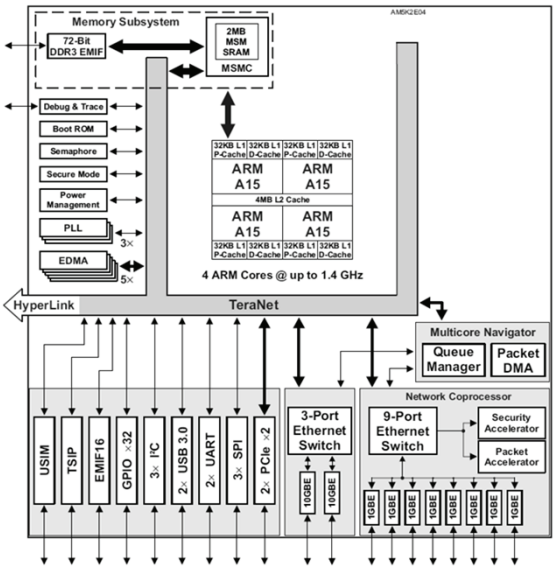
  - 2x Queue Managers support up to 16K queues
  - 1x 5-port Network Coprocessor (NETCP)
  - 1x USB3.0 to support solid state drive
  - 1x 3 port 10GBE Switch Subsystem
- 66AK2H12
  - Scaled-down version of 66AK2H14
  - 10GBE interface is NOT available.
- 66AK2H06
  - Scaled-down version of 66AK2H12
  - 4x C66x CorePacs
  - Dual-ARM A15 CorePac

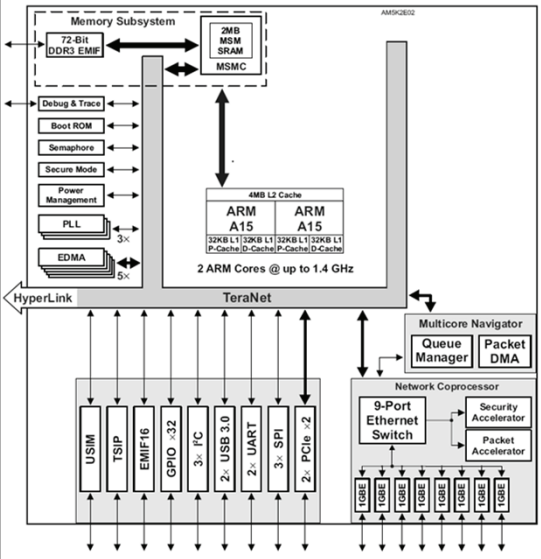
K2E Platform Device Variations



The K2E platform has four variations:

- AM5K2E04
  - First ARM-only TI multicore device
  - Quad-ARM A15 CorePac
  - 1x Queue Manager supports up to 8K queues
  - 1x 9-port Network Coprocessors (NETCP)
  - 1x 3 port 10GBE Switch Subsystem
  - 2-port PCIex2
  - Telecommunications Serial Port (TSIP)
  - 2x USB 3.0 to support solid state drive
  - No SRIO

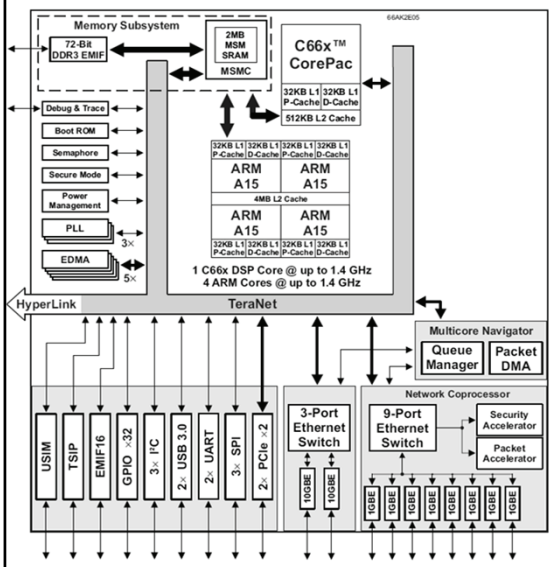
K2E Platform Device Variations



The K2E platform has four variations:

- AM5K2E04
  - First ARM-only TI multicore device
  - Quad-ARM A15 CorePac
  - 1x Queue Manager supports up to 8K queues
  - 1x 9-port Network Coprocessors (NETCP)
  - 1x 3 port 10GBE Switch Subsystem
  - 2-port PCIex2
  - Telecommunications Serial Port (TSIP)
  - 2x USB 3.0 to support solid state drive
  - No SRIO
- AM5K2E02
  - Scaled-down version of AM5K2E04
  - Dual-ARM A15 CorePac
  - 10GBE not included

K2E Platform Device Variations



The K2E platform has four variations:

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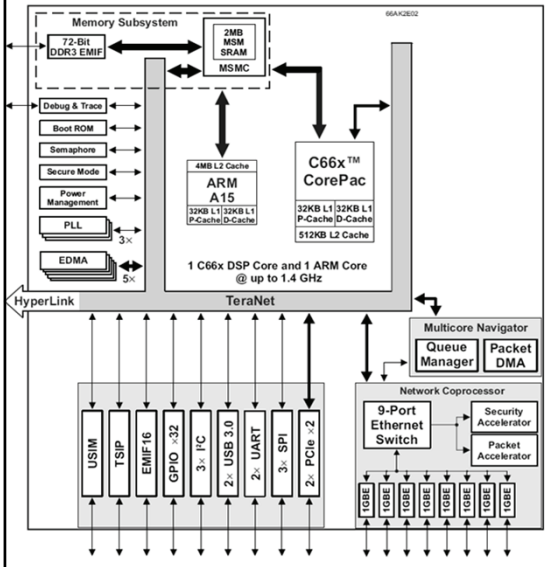
  - 1x 3 port 10GBE Switch Subsystem
  - 2-port PCIex2
  - Telecommunications Serial Port (TSIP)
  - 2x USB 3.0 to support solid state drive
  - No SRIO
- AM5K2E02
  - Scaled-down version of AM5K2E04
  - Dual-ARM A15 CorePac
  - 10GBE not included
- 66AK2E05
  - Same as AM5K2E04 with a single C66x CorePac added

K2E Platform Device Variations



The K2E platform has four variations:

- AM5K2E04
  - First ARM-only TI multicore device
  - Quad-ARM A15 CorePac
  - 1x Queue Manager supports up to 8K queues
  - 1x 9-port Network Coprocessors (NETCP)
  - 1x 3 port 10GBE Switch Subsystem
  - 2-port PCIex2
  - Telecommunications Serial Port (TSIP)
  - 2x USB 3.0 to support solid state drive
  - No SRIO
- AM5K2E02
  - Scaled-down version of AM5K2E04
  - Dual-ARM A15 CorePac
  - 10GBE not included
- 66AK2E05
  - Same as AM5K2E04 with a single C66x CorePac added
- 66AK2E02
  - Same as AM5K2E02 with a single-ARM A15 CorePac and a single C66x CorePac added

KeyStone I Compared to KeyStone II

IP block	KeyStone I	KeyStone II
ARM Cortex-A15 core	No	4x
MSMC	Ver1.0	Ver2.0
DDR3 EMIF (64-bit)	1x	2x
MSMC SRAM	2 Mbytes	6 Mbytes
DDR3A memory (max)	8 Gbytes	8 Gbytes
DDR3B memory (max)	No	2 Gbytes (for ARM and DSP cores) 512 Mbytes (system masters)
ARM Boot ROM	No	256 Kbytes
OTP memory	No	4 Kbits
Queue Manager Subsystem + PKTDMA	1x	2x
EDMA3CC	3x	5x
EDMA3TC	10x	14x
HyperLink	1 x 4	2 x 4
10 Gigabit Ethernet (10GBE)	No	1 x 2
UART	1x	2x
SPI	1x	3x
I2C	1x	3x
GPIO	1x 16	1x 32
Timer64	8x	20x
USB3	No	1x to 3x
PLL controller + On-chip PLLs	3x	5x
ARM Subsystem ETB (16 KB)	No	1x
DSP TETB (4 KB)	4x	8x
Tracer	16x	32x
MPU	6x	15x
Security Manager	No	1x

For More Information

- Device-specific Data Manuals for the KeyStone SoCs can be found at TI.com/multicore.
- Multicore articles, tools, and software are available at Embedded Processors Wiki for the KeyStone Device Architecture.
- View the complete C66x Multicore SOC Online Training for KeyStone Devices, including details on the individual modules.
- For questions regarding topics covered in this training, visit the support forums at the TI E2E Community and Deyisupport website.

TI Catalog Processor IDH & Solution Introduction

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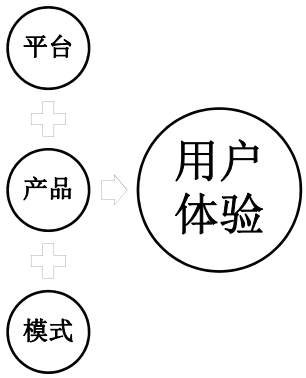
☺ 风向标核心理念：

- ✓ 第三方开放云平台
- ✓ 合作伙伴智能硬件
- ✓ 多方共赢模式



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◆ 监测报警
◆ 自动录制
◆ 实时流媒体监控

安全

◆ 提升空气质量
◆ 调节湿度
◆ 控制温度

健康

◆ 设备监控
◆ 电量监测
◆ 能源管理

能源

◆ 远程控制、监测
◆ 一键模式、情景模式
◆ 客制化联动模式

模式

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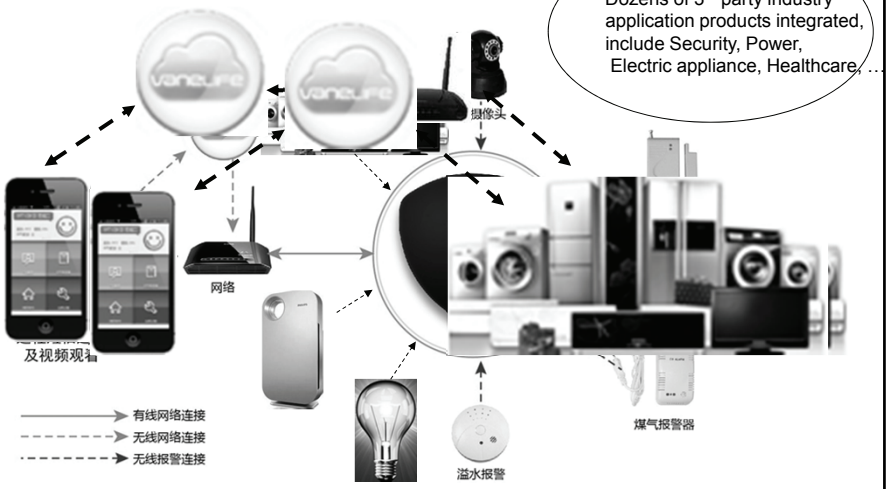
Vanelife Platform

Dozens of 3rd party industry application products integrated, include Security, Power, Electric appliance, Healthcare, …



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Vanelife 风向标开放平台

Features：

- ➢支持 iOS，Android
- ➢远程控制，监测
- ➢客制化 一键模式，情景模式
- ➢客制化 联动模式
- ➢大数据收集，分析，提案

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Vanelife 风向标开放平台优势

- ✓ 近四年第三方开放 云+硬件 平台持续投入
- ✓ 与智能硬件厂家完全互补合作
- ✓ 云-平台-终端-PCBA-BOM 灵活的接入方式
- ✓ 更快速产品化，导入量产
- ✓ 更具性价比
- ✓ 更好的用户体验

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风向标科技官网　风向标科技官方微博　风向标科技微信公众平台　风向标科技天猫旗舰店

浙江风向标科技有限公司
地址：上海市徐汇区龙华中路596号绿地中心东楼1701-03室
电话：+86 (021) 6433-3233
传真：+86 (021) 5186-2723
邮编： ZIP.200032

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Embest

About Embest

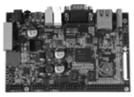
Embest is a leading global solution provider for easy-to-use development tools, industrial control boards and design services based on the ARM Technology. The products and design services will make electronics development faster and more reliable, so that customers can save development time and process and improved product quality with an obvious cost down.

Embest was established in China since year 2000, with 150 staffs now, among them there are 80 experienced engineers in software, hardware design and testing. The company was acquired by Premier Farnell in June, 2012, a listed company in UK with a history of more than 70 years in electronics distribution business. Embest is the strategic partner of ARM and TI.

Embest products based on TI Technology

element14 BeagleBone Black(Rev C)
Based on TI AM3358 ARM Cortex-A8 processor, 1GHz, 512MByte DDR3, 4GB eMMc with OS Debian7.4

SBC8600B
Core board based on TI AM3359 ARM Cortex-A8 MPU @720 MHz, 512MByte DDR3 SDRAM, 512MByte NAND Flash



Devkit 8600
Evaluation board Based on TI AM3359 ARM Cortex-A8 MPU @720MHz, 512MByte DDR3 SDRAM, 512MByte NAND Flash

Design Service

Embest provides comprehensive services to specify, develop and produce products and help customer to implement innovative technology and product features. Progressing from prototyping to the final product within a short timeframe and thus shorten the time to market, and to achieve the lowest production costs possible.

Embest provides customized design service based on TI technology for global customers. Embest can help customer on:

- Design files
- Image files
- Software source codes
- Relevant documents
- PCB/PCBA

Contacts of Custom Services::

globalsales@embest-tech.com

Serial Design

TI Cortex-A8
SD-AM3358-EVM/SD-AM3358-SOM

Ethernet接口：2个，千兆
LCD接口：1个，16/24bit
RS232接口：2个
RS485接口：1个
CAN接口：1个
USB Host接口：1个
USB OTG接口：1个

Linux
Linux v3.12.10
AM335xSDK 07_00_00

MMC接口：2个
ADC接口：4个，12bit
RTC：1个
JTAG接口：1个，14-Pin
GPMC总线接口：1个，8bit
外设接口：UART、SPI、McASP、I2C、PWM

Android
Android Jelly Bean v4.2.2
Linux Kernel v3.2
SDK：v4.1.1

Starterware
V2.00.01.01

开发调试仿真器

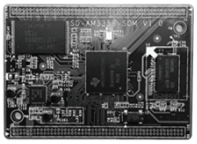
开发系统自带隔离，可靠性更高，可以满足工业调试
支持TI全系列DSP、ARM处理器
支持Code Composer Studio v4和以上版本

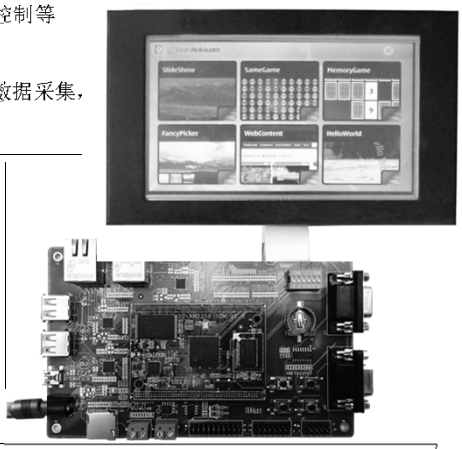
TI AM335x参考设计

HMI：电梯招呼板，热电厂控制系统，双彩LED控制等
EPOS机：手持终端（无线/有线），台式终端（无线/有线）
医疗终端：生化分析仪，黄胆分析仪，血液分析仪等
智能家居：智能遥控器，智能家居中央控制，门禁控制等
家用电器：冰箱，洗衣机，空调，热水器等
消费类产品：GPS，PDA，PAD等
工业控制：PLC，机器人，工控机，工业以太网，数据采集，运动伺服等

物流扫码机：

最小系统定制板（SOM）





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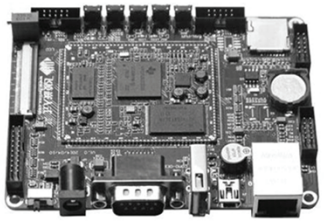
A8的性能 ♦ ARM9的价格

飞凌嵌入式携手 TI 引领 A8 进入普及时代

强大的真工业级开发板——OK335xS-II

800MHz	1600	硬件3D	-40℃~+85℃
主频	Dmips	图形加速	运行温度



- Cortex-A8 TI AM3354处理器
- 多总线，双网口支持，6路串口
- 真工业级开发板，运行温度-40℃~+85℃

海量测试程序和应用例程

Linux 用户使用手册　　Wince 用户使用手册

惊爆价 **298** 元

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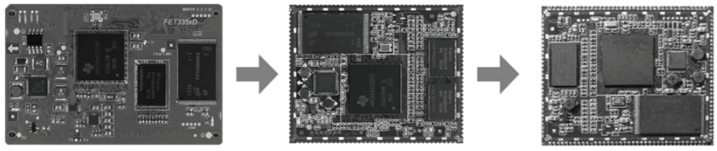
飞凌嵌入式 FORLINX EMBEDDED

Forlinx专注嵌入式领域20年

ARM核心控制板卡制造专家　　嵌入式解决方案专业提供商



FET335xD　　FET335xS　　FET335xS-II

应用案例

矿井信息采集系统　医疗标签打印机设备　汽车仪表盘　智能家居中央控制系统

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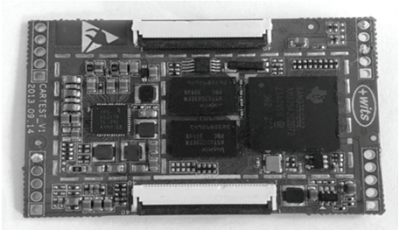
南京九能科技有限公司

南京九能科技有限公司成立于2004年,长期从事智能数码产品开发和生产。其核心团队由海外留学高级学术人才，国家重点实验室研发人员，以及在国际大型科技企业长期工作的高级专家组成。团队不仅具备强大的产品研发能力，也具备丰富的企业管理经验。

九能科技和美国德州仪器公司（TI）在内嵌式平台进行长达5年深入的战略合作，成功的推出了基于DM3730和AM335 的整体解决方案平台。该平台业已被各行业众多客户成功应用于工业级智能物流终端，智能家居，智能旅游等领域。

放眼未来，智能型生活已经朝我们大步走来。九能科技将以科技为基础，人才为框架，充分借助金融，互联网的翅膀，凭借优质产品和经营诚信，在智能设备领域做出重要贡献。

产品简介：



基于AM335X核心板

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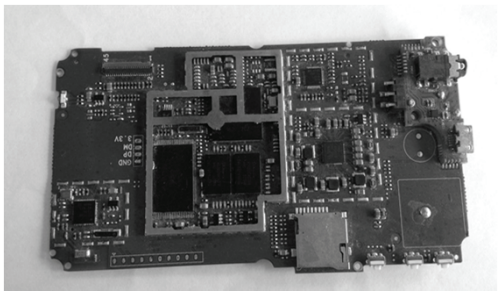

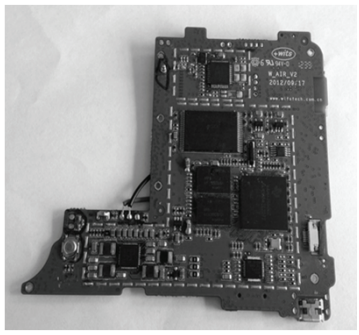

基于AM335X智能终端主板
基于AM335X人机界面主板

- 地址：南京市秦淮区公园路42号体育大厦1803室
- 电话：025-83115162
- Email:support@jiunengtech.com

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EMA

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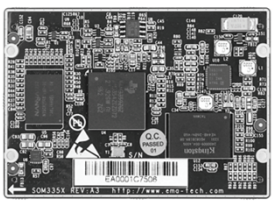
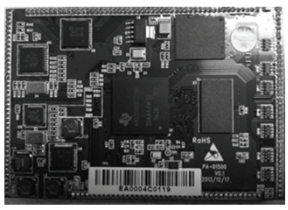
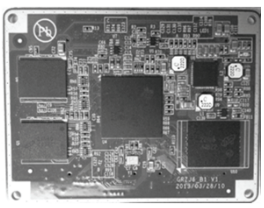
EMA SOM335x 核心板

SOM335x是基于TI AM335x系列处理器的低功耗嵌入式核心板。相比beagle bone等模块，更具产品化，更稳定，资源更丰富；

工业级设计，工作温度-40℃~85℃，通过盐雾试验，适用于工业应用；

提供产品级的Linux 3.2 + QT4.5+SQLite、工业级Android 4.0系统支持；

EMA 提供多种规格核心板，适合不同场合的应用;

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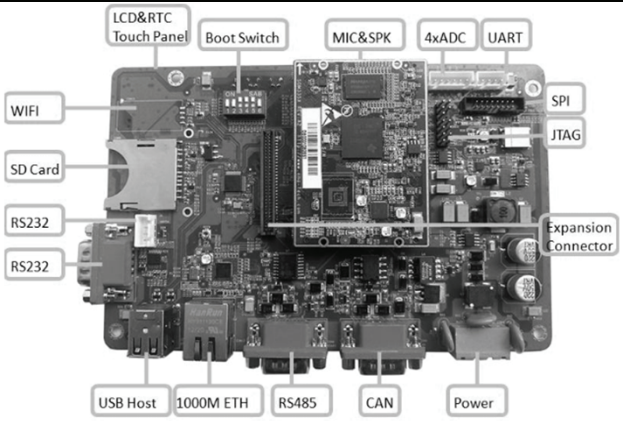
基于AM335x的工业级主板HMI335x

基于SOM335x核心板，通过EMC/EMI测试，低成本、低功耗、功能齐全

9～24V宽压输入，提供HMI应用常用接口：CAN、RS485、RS232

支持Linux3.2 + QT4.5 + SQLite软件方案，或Android4.0 + EMA-IO方案

典型案例：家庭中央空调控制器、工业HMI、银行等行业自助终端



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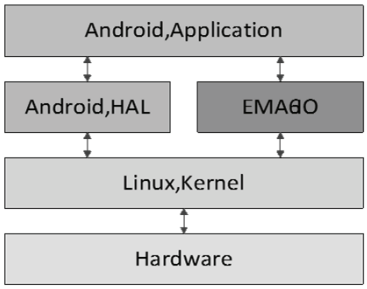
SOM335x Android软件 - EMA-IO

- EMA-IO Android系统中间件软件，突破了标准Android系统的资源接口限制,使得应用程序访问底层设备成为现实。从而填补了Android系统在专用领域发展中的空白局面。
- 标准 Android 系统在加载 EMA-IO 后,应用程序只需通过简单的编程实现,即可安全地访问所需底层设备,为用户节省大量开发成本。
- EMA-IO 涵盖CAN、GPIO、I2C 以及各类基于UART的设备。



TEXAS INSTRUMENTS

Embedsky

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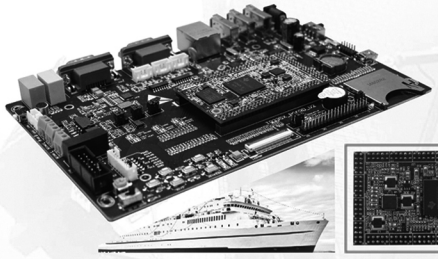
公司及产品简介

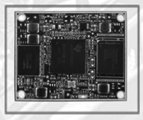
广州天嵌计算机科技有限公司是一家专业提供嵌入式开发和解决方案的高科技企业，在行业内有很高的知名度。雄厚的研发实力和优质的售后服务，让您的产品研发更简单！更快捷！更有保障！

TQ_335x是基于TI-AM335x（Cortex-A8核心架构）系列芯片设计的一款性能稳定的开发平台。产品适用于：工业控制系统、HMI人机界面、医疗电子、智能仪表、智能家居控制……。

TQ 3358工控系列



TQ 3358 Core A



TQ 3358 Core B

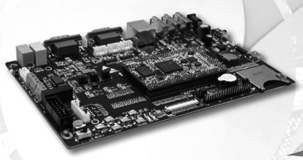
TQ 3358 Core C

天嵌科技 www.embedsky.com 您身边的嵌入式专家
广州天嵌计算机科技有限公司

TQ 3358 成功案例

工业控制—HMI

商业消费—智能检测仪



智能家居—智能网关

医疗电子 — 6通道荧光仪

TEXAS INSTRUMENTS

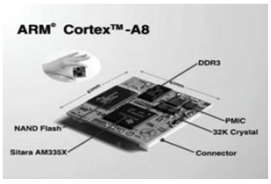
StrongKiwi

TEXAS INSTRUMENTS

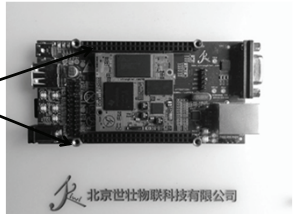
StrongKIWI Product

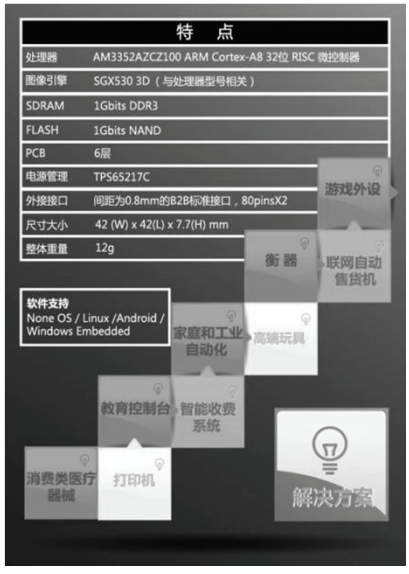
- Cortex – A8 Core Board

To be the authorized 3rd design party of TI, StrongKIWI released the core board with the Cortex-A8 minimum system.



配套底板：
扩展槽和
Beaglebone Black
完全兼容。





TEXAS INSTRUMENTS

StrongKIWI's Service

TI 第三方合作研发机构 -
北京世社物联科技有限公司（StrongKIWI）
电话：010-67857759
邮箱：Marketing@strongkiwi.com

TEXAS INSTRUMENTS

Assem

TEXAS INSTRUMENTS

Beijing Assem Technology LTD.,Co.

1. 在行业专用设备领域，有着领先技术和自主知识产权的系统软件设计

- 对嵌入式Linux内核进行了深度优化
- 针对长期使用的特点，对外围设备的驱动程序进行了大量的优化

2. 在行业专用设备领域，有着领先技术的硬件设计

- 能够灵活运用特有的技术手段发挥产品的性能，同时又能减少成本
- 十分熟悉可与ARM产品匹配使用的外围器件，保证产品的稳定性

3. 从研发到量产成品的全过程经验与技术

- 针对ARM系列处理器有丰富的工业产品设计经验
- 有多年整机成品批量生产的经验，充分了解产品的整个生产过程
- 十分了解产品在生产过程中的问题，在产品设计时即以满足大批量生产和苛刻使用为目标

Beijing Assem Technology LTD.,Co.

- **海尔集团物联网家电核心合作伙伴，量产智能家电信息化模块唯一供应商**
- 卡萨帝冰箱/洗衣机物联网模块产品，海尔空调物联网模块产品
- 海尔医疗设备智能控制产品
- 海尔云平台技术服务方
- 海尔智能家居对讲系统设计和制造方
  - 基于TI Sitara AM335X 处理器
  - CORTEX-A8处理器完美替代ARM9，HMI操作友好速度快
  - 回声消除、安防、按键、音频播放/录音、MMC系统更新、网络等模块
  - 通过各类电气特性测试的工业级平台
- **世界最大金融机具公司VeriFone针对国内市场研发的第一个产品的嵌入式操作系统技术提供商**
- **国家信息中心政务虚拟化系统桌面终端**

ENEA

TEXAS INSTRUMENTS

Enea (瑞典宜能) 公司简介

- Enea (宜能)是全球领先的嵌入式软件提供商，1968年在瑞典成立，1989年上市。解决方案包括：多核芯片RTOS软件平台、分布式通讯中间件(IPC)、CGL实时Linux等。客户产品如：基站、雷达、声纳、电子对抗、航空航天、网络设备等。
- Enea 是 TI 的全球白金 (Platinum) 合作伙伴，提供针对 TI 多核 DSP/SoC(如 C6678/K2/66AK) 整套的高性能基础软件开发平台，包括：

  ☐RTOS软件平台 ☐分布式中间件 ☐开发调试工具

- Enea 部分客户列表:

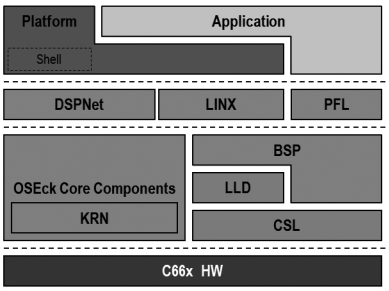
ERICSSON, HUAWEI, Nokia Siemens Networks, ZTE中兴, 大唐电信, Potevio 中国普天, Alcatel·Lucent, NASA, BOEING, AIRBUS, LOCKHEED MARTIN, EADS DEFENCE & SECURITY, ALSTOM, ABB, AEP AMERICAN ELECTRIC POWER, CETC, CASIC 中国航天科工集团, CSIC 中船重工, 中国航天, 中航工业, 理工雷科 RACH, 中国科学院, 中国兵器工业集团公司

info_china@enea.com

TEXAS INSTRUMENTS

OSEck软件平台针对 C6678 平台模块

- RTOS, 中间件, 工具



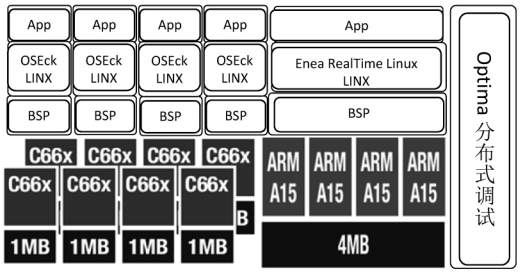
- OSEck专门针对TI C66优化模块
- TI 软件模块

1. 针对TI KeyStone Multicore Navigator优化的OSEck 实时操作系统。
2. 针对核间通讯优化的进程间通讯模块－LINX IPC
   - ✓ DSP内核间 LINX CDMA通讯
   - ✓ DSP间/板卡间LINX Rapid/IO通讯(Message和DIO)
   - ✓ DSP间/板卡间的LINX Ethernet通讯
3. 针对各种外设优化的BSP驱动，包括CDMA, Ethernet, Rapid/IO等。
4. DIO 高性能SRIO通讯机制
5. 高性能的DSPNet TCP/IP协议
6. Shell 用户界面
7. 针对 UDP包优化的网络加速软件模块 – PFL。
8. 系统死后分析工具－Core Dump
9. Eclipse系统极调试工具－内存、CPU Profile等。
10. Log Analyzer- 离线日志分析工具

info_china@enea.com

Enea异构SoC软件平台- (RTOS, 实时Linux, 中间件, 工具)

1. OSEck – 多核DSP软件平台
   - ✓ OSEck实时稳定的内核，
   - ✓ OSEck LINX －支持多DSP核无缝通讯的进程间通讯模块
2. Enea Linux – 实时商业Linux
   - ✓ 基于Yocto的图形Linux开发调试环境
   - ✓ Enea 实时Linux优化
3. LINX IPC – ARM核(Linux) 到DSP核(OSEck)的无缝 进程间通讯模块
   - ✓ 支持多芯片，多板卡的无缝通讯
   - ✓ RapidIO, Ethernet, 共享内存等。
4. Optima/CDA – 优化调试工具
   - ✓ 开发、调试
   - ✓ 死后分析
   - ✓ 性能调优工具。
5. DSP BootLoading
   - ✓ Enea Linux下载DSP映像并启动DSP.

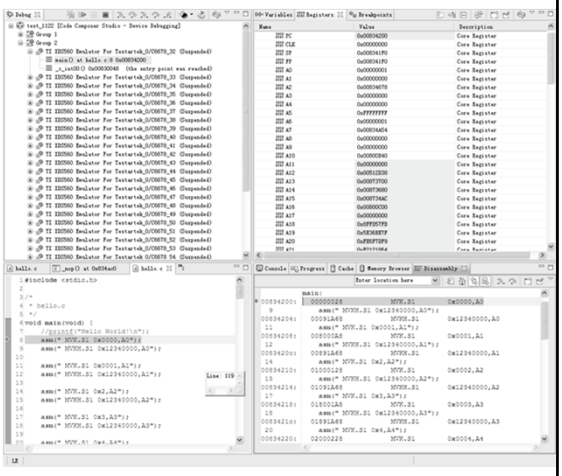


info_china@enea.com

Testartek(泰星达)

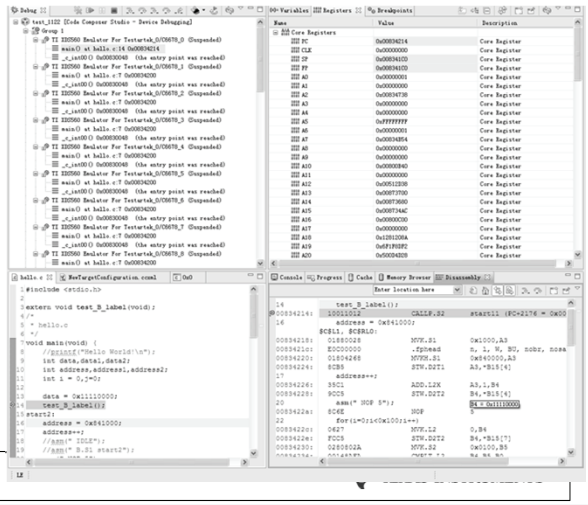
泰星达C6678 综合调试平台

- Testartek TI C667X 系列综合调试平台，可以在不用硬件仿真器情况之下对C 6678芯片进行各种调试。降低了开发、测试、整合及维护应用程序的难度，满足于单核及多核心、海量处理器的超级应用。尤其是大量DSP的调试十分方便。
- 满足跨板卡，不同处理器之间的调试。
- 与CCS无缝兼容，用户界面仍是CCS，CCS版本升级对其无影响。
- 能够实现大数量处理器的同时调试和监测。
- 便于海量运算的处理器管理，通信调度。
- 可以通过不同的接口来进行调试，比如：PCI-E，以太网等。
- 无需硬件仿真器实现下载，运行，断点，单步，观察内存等调试功能



泰星达C6678 综合调试平台

- 针对DDR3，EDMA，IDMA，SRIO，GE等，开发了更高效的通信模块，非常适用于视频算法、大数据处理等每秒钟上万次通信的算法。

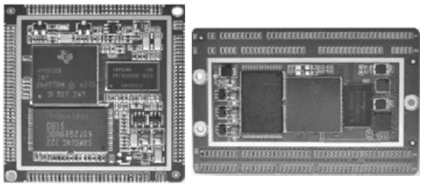


- 泰星达（北京）科技有限公司
- 王寿龙 13301197747

Lierda

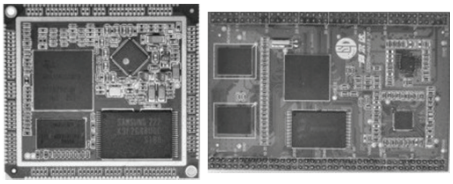
TEXAS INSTRUMENTS

➢ AM1808标准核心板



ARM926EJ-S内核，最高主频达到456MHZ。本核心板带有128MB的DDR2、256MB的Nand Flash。

➢ AM335x标准核心板



Cortex-A8内核，最高主频达到720MHZ。本核心板带有256MB的DDR2、256MB的Nand Flash。

TEXAS INSTRUMENTS

EA

➢ 智能HMI显示终端

HMI-显示板

产品简介

本方案的目的在于满足物联网时代智能家电追求高用户体验，高可扩展性的人机交互界面的要求。使用AM335X A8处理器，搭载Android4.2.2操作系统，配置10点超灵敏电容触摸屏，通过谷歌免费提供的SDK可以方便地设计出功能强大且体验上佳的人机界面，同时预留wifi、以太网等接口，可轻松实现联网等扩展应用。

性能特点

- Android4.2.2操作系统
- 1GHz cortex-A8 cpu
- 预留1路USB host模式和1个OTG接口
- 100M/10M以太网、WIFI802.11 b/g/n
- 支持6个uart，支持SPI、CAN、i2c总线扩展
- 支持音频输出及录音功能

技术参数

- 输入电压：5V-42V
- 操作系统：Android4.2.2
- 处理器：AM3358(1GHz Cortex-A8)
- 运行内存:512MB DDR3
- 显示屏：7inch 800*480 1670万色 电容屏

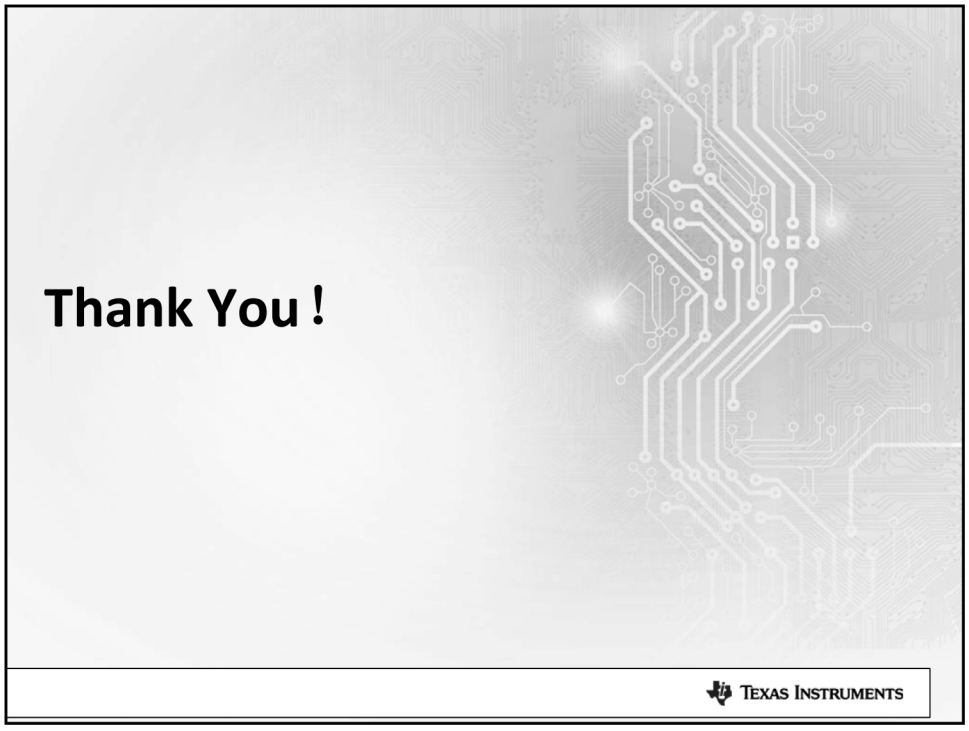
TI main device

AM335X
TPS65910
TLV320AIC3106

Business Model

- system solutions

TEXAS INSTRUMENTS


Thank You !
Texas Instruments

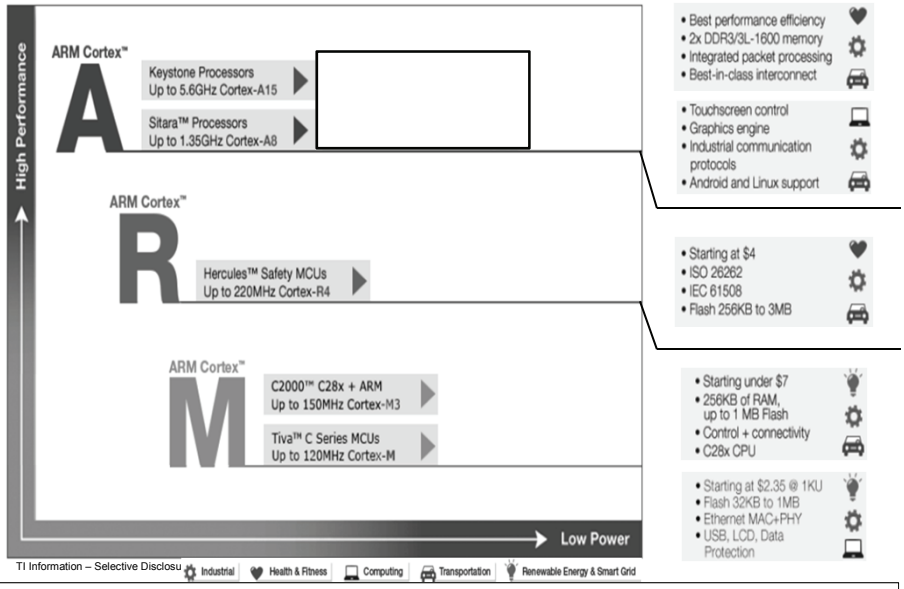
TI Keystone II ARM Subsystem Intro

KeyStone Training

TI Keystone II ARM Subsystem Introduction

- **ARM Overview and Basics**
  - ARM Architecture and Categories
- **ARM Cortex-A15 in TI Keystone II Devices**
- **Software Provided of TI Keystone II ARM Parts**

TI's ARM Products



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  - Cortex-A15 Features in TI Keystone II Devices
  - Basic Benchmark Comparison
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  - ARM Interrupt Sub-modules
  - SoC Boot with ARM Master
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Why Cortex-A15?

Wild Application Fields
- High performance computing
- Low power server
- Wireless infrastructure
- High-end digital home
- Mobile computing

Open Software Ecosystem
- Linux and Ubuntu
- Java SE, Java FX
- Android
- Microsoft Windows Embedded

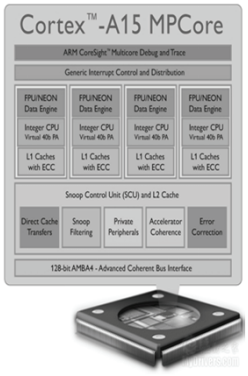
Why Cortex-A15

Advanced Architecture
- Full ARMv7-A Architecture Instruction Set
- Up to 4MB low-latency L2 cache
- Up to 1.4-GHz Processor Core Speed
- AMBA 4.0 AXI ACE Master Port
- Support NEON, VFP V4, and Thumb V2

Popular Features Support
- Up to 4 Core SMP
- Support LPAE for more than 4GB DDR3
- Virtualization support for virtual machine
- Trust Zone support with Monitor mode
- Java and Jazelle environment support

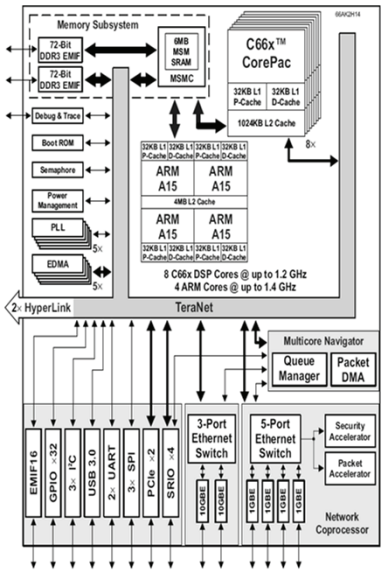
Cortex-A15 Features in TI Keystone II Devices

- Cortex A15 MPCore processor
  - Cortex A15 MPCore version **R2P4**, 1, 2, 4 cores in one cluster
  - **Standard** ARM v7-A architecture
  - Full support of **Trust Zone** and **Virtualization** features
  - **Multi-issue**, **out-of-order**, **superscalar pipeline**
  - **Dynamic branch prediction** with BTB and GHB, a return stack, and an indirect predictor
  - Per core **NEON** (SIMDv2) and **VFP** (VFPv4)
  - L1 instruction and data cache of **32 KB, 2-way**, **16 word line** with **128 bit interface**
  - Integrated L2 cache **up to 4MB, 16-way**, **16 word line**, **128-bit interface** to L1 along **with ECC/parity**
  - **128-bit AMBA4** AXI with ACE protocol, 32-bit APB



Flexible Configurations in TI Keystone II Devices

Keystone II Multicore DSPs			
	1 Cortex - A15	2 Cortex - A15	4 Cortex - A15
0 TMS320C66x DSP		**AM5K2E02**	**AM5K2E04**
1 TMS320C66x DSP	**66AK2E02**		**66AK2E05**
4 TMS320C66x DSP		**66AK2H06**	
8 TMS320C66x DSP			**66AK2H12 66AK2H14**



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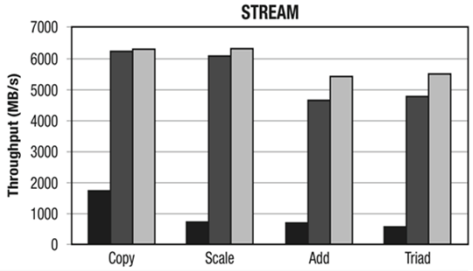
Benchmarks – Core, Memory Latency

- Dhrystone, DMIPS/MHz, CPU core and L1 only
  - **3.5DMIPS/MHz** (highly dependant on compiler)
  - **19600DMIPS** with KeyStone II Quad-ARM Cortex-A15 CorePac at 1.4GHz
- Floating point
  - Quad single-precision IEEE-754 FMAC per cycle
- Memory Latency, load-to-use latency
  - 4cc L1D hit, typically hidden by A15 micro architecture
  - 20cc L2 hit (4MB)
  - MSMC2 SRAM: ~50cc
  - External Memory: ~100ns (~140 cycles) L2 miss to DDR page that is open

Benchmark Comparison – Bandwidth

- STREAM benchmark is the industry-standard benchmark for the measurement of sustainable memory bandwidth.
- It including:
  - COPY: floating-point loads and stores
  - SCALE: floating-point multiply
  - SUM: floating-point add
  - TRIAD: floating-point multiply and add



	Copy	Scale	Add	Triad
A8 - 1 core	1744	728	711	589
A15 - 1 core	6228	6073	4633	4753
A15 - 2 core	6280	6291	5390	5488

Cortex-A8: 1 GHz, 64-bit DDR2-1333 memory, Codesourcery GCC v4.6.3 compiler;
Cortex-A15: 1.4 GHz, 64-bit DDR3-1600 memory, Linaro GCC v4.6.3 compiler

- These results represent substantial improvements resulting from the Cortex-A15 processor's VFPv4 floating-point processing and from Keystone II's MSMC-based path to memory.
- http://www.ti.com/lit/wp/spry223/spry223.pdf

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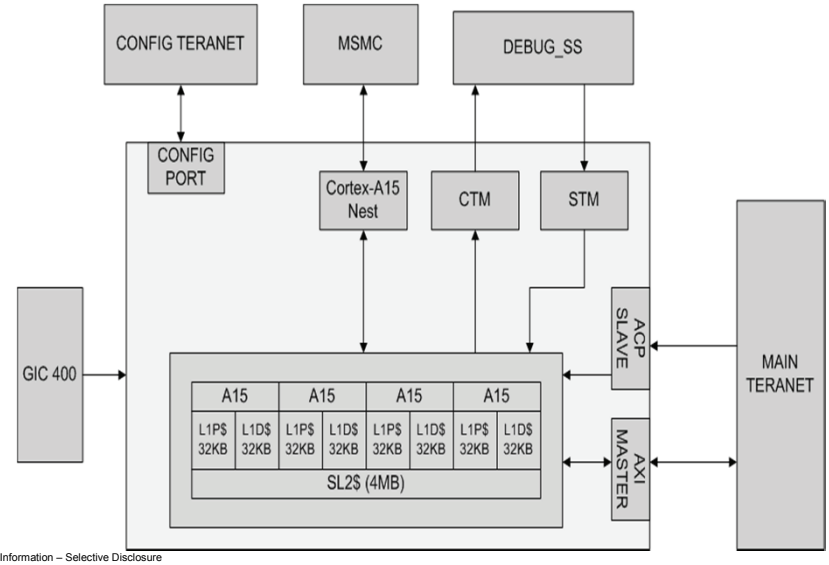
Functional Diagram on 66AK2H12



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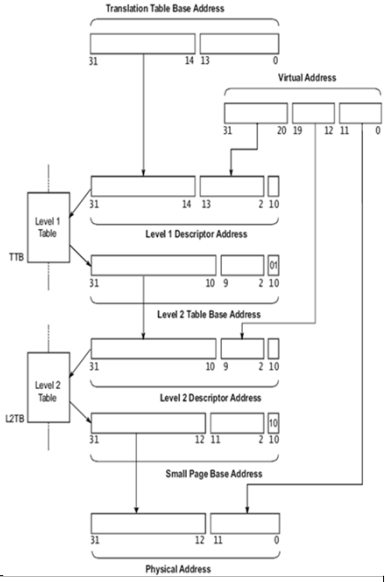
Cortex-A15 Memory Management Unit (MMU)

- Logical-to-Physical memory translation:
  - User protected
  - Hardware manages the actual memory
- Large physical addressing up to 40-bit (1TB)
- Up to 3-level data structure for virtual 4kB page:
  - Two levels for virtual 2MB pages (Linux huge pages)
  - Translation Look-aside Buffers (TLB) cache one page of address translations per entry to speed up the translation process:
    - L1 instruction access
    - L1 data access
    - L2 TLB

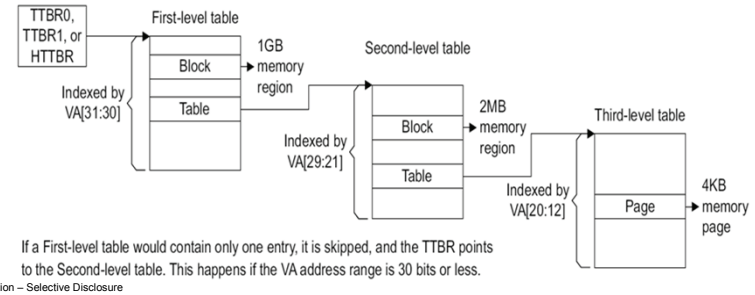
Cortex-A15 Memory Management Unit (MMU)

- The core performs MMU to translate virtual addresses generally as follow steps:
  - Core issues a 32-bit virtual address
  - MMU uses several bit-fields of virtual address to index TLBs, or perform translation table walk if missed in TLBs
  - MMU combines the physical address MSBs from the page table entry with previous LSBs to the actual physical address with the page table defined memory attributes



Cortex-A15 MMU - LPAE

- Cortex-A15 support Large Physical Address Extensions (LPAE) for connecting physical memory larger than 4GB
- LPAE provides:
  - New translation table format – long descriptor format
  - 32-bit virtual addresses, with 40-bit physical addresses
  - New memory attributes added

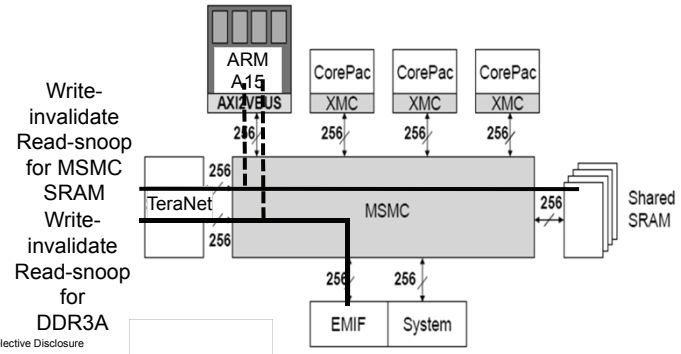


Cortex-A15 Cache

- Cortex-A15 implements with **fixed 32KByte L1** instruction and data cache per core
- Cortex-A15 implements with **up to 4MByte L2** shared cache per cluster
- Cortex-A15 can **automatically maintain data coherency across other L1/L2 caches** if:
  - Configure with correct memory type(normal, shared, etc)
  - CPUs are in the same domain
- MMU uses translation tables to control which memory area are cached
- Caches handle data in lines (64 bytes per line)

I/O Coherency

- Keystone II devices support memory coherency accesses between A15 core(s) and other non-core master peripherals (Ex: EDMA) in the DDR3A and MSMC SRAM space.(not for DDR3B, each DSP cores or between A15 cores and DSP cores)
- Non-core master can recognize and access the A15 core L1D and L2 cache to maintain the coherency through AMBA-4 ACE

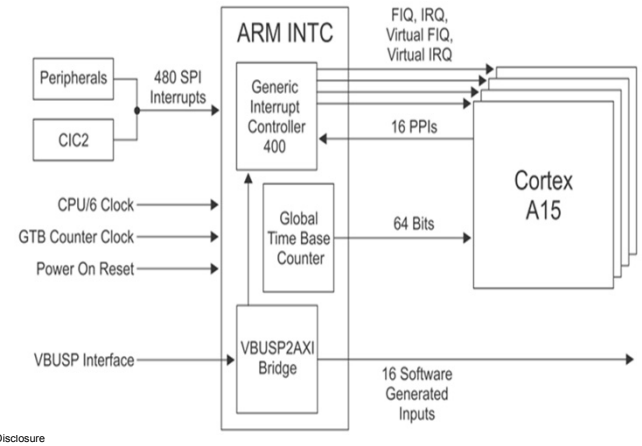


TI Keystone II ARM Subsystem Introduction

- **ARM Overview and Basics**
- **ARM Cortex-A15 in TI Keystone II Devices**
  - Cortex-A15 Features in TI Keystone II Devices
  - Basic Benchmark Comparison
  - Interconnections and Buses
  - Memory Architectures
  - ARM Interrupt Sub-modules
  - SoC Boot with ARM Master
  - ARM Communication with DSP
- **Software Provided of TI Keystone II ARM Parts**

ARM INTC on Keystone II Devices

- ARM INTC (AINTC) subsystem includes the GIC-400 with a Global time base counter and a VBUSP2AXI interface for registers' configuration



GIC-400 on Keystone II Devices

- Keystone II devices integrate GIC-400 (**r0p0rel1**) for ARM INTC
- GIC-400 provides a scalable solution for up to **480 peripheral interrupts** with 1-to-n broadcast capability
- Each interrupt can be steered to **nFIQ or nIRQ with individual priority**
- GIC-400 allows software to configure each interrupt line to be **level-sensitive or edge-sensitive** by configuring GICD_ICFGR
- GIC-400 on Keystone II devices support:
  - **16 SGIs** (Software Generated Interrupts) (per each A15 core)
  - **6 external PPIs** (Private Peripheral Interrupts) (per each A15 core)
  - **1 internal PPI** (per each A15 core)
  - **480 SPIs** (Shared Peripheral Interrupts) (for A15 4 cores cluster)

Cortex-A15 Exceptions – Handling

- When the exception asserts, the following steps should be processed for this exception:
  - **1. Save processor status**
    - Copy CPSR to SPSR_<mode>
    - Store the return address in R14 LR_<mode>
  - **2. Change the processor status for exceptions**
    - Mode field bits, ARM or Thumb status
    - Interrupt disable bits, set PC to vector address
  - **3. Execute the exception handler**
  - **4. Return to main application**
    - Restore CSPR from SPSR_<mode>, clear interrupt disable bit
    - Restore PC from R14 LR_<mode> with adjustment offset
- Step 1&2 are performed by processor automatically, step 3&4 are responsible by software

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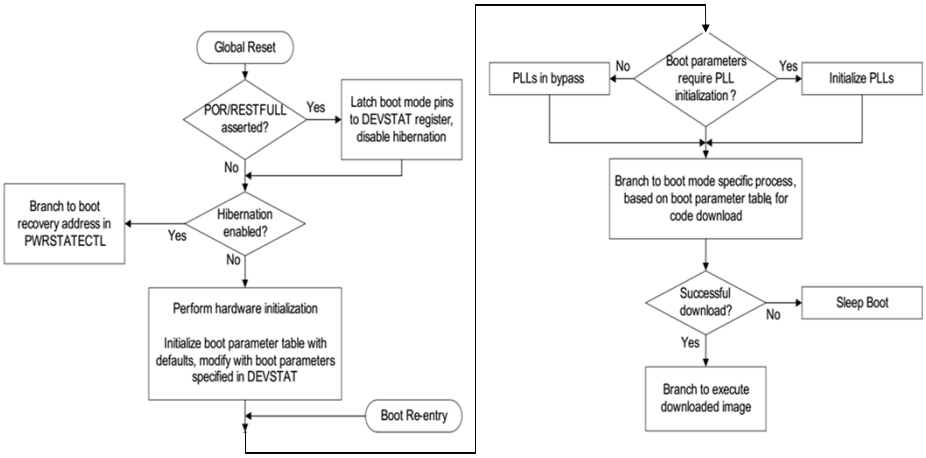
Boot mode when ARM as boot master

- Keystone II devices support several boot modes for boot master is ARM Core0
- Boot mode is selected by 16 Pins mapped to relative 16 bits in DEVSTAT register
- Supported boot mode and Pins configuration on 66AK2H12 is as follow

DEVSTAT Boot Mode Pins ROM Mapping

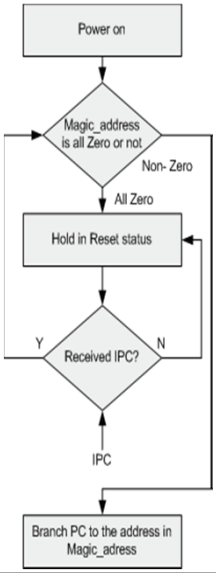
16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Mode
X	X	0	ARMEN	SYSEN	ARM PLL CONFIG			Boot Master	SYS PLL CONFIG			Min	0	0	0	SLEEP
SlaveAddr		1	Port										0	0	0	I^2C SLAVE
X	X	X	Bus Addr		Param Idx				X	Port			0	0	1	I^2C MASTER
Width	Csel		Mode						Npin				0	1	0	SPI
0	Base Addr		Wait	Width	ARM PLL CONFIG				SYS PLL CONFIG			0	0	1	1	EMIF (ARM Master)
					X	Chip Sel										EMIF (DSP Master)
1	First Block			Clear	ARM PLL CONFIG							Min				NAND (ARM Master)
					X	Chip Sel										NAND (DSP Master)
Lane	Ref Clock		Data Rate		ARM PLL CONFIG								1	0	0	SRIO (ARM Master)
X					Lane Setup											SRIO (DSP Master)
PA clk	Ref clk		Ext Con		ARM PLL CONFIG								1	0	1	Ethernet (ARM Master)
					Rsvd	Lane Setup										Ethernet (DSP Master)
Ref clk	Bar Config				ARM PLL CONFIG							0	1	1	0	PCIe (ARM Master)
					SerDes Cfg											PCIe (DSP Master)
Port	Ref clk		Data Rate		ARM PLL CONFIG							1	1	1	0	HyperLink (ARM Master)
					SerDes Cfg											HyperLink (DSP Master)
X	X	X	X	Port	ARM PLL CONFIG							Min	1	1	1	UART (ARM Master)
X	X	X	X		X	X	X									UART (DSP Master)

ARM Boot High Level Flow



ARM Boot Related Info

- ARM initial status on Keystone II Devices
  - Only ARM core 0 is powered on when the device is up, the rest ARM cores are powered off by default
  - ARM core is in supervisor mode by default after power on
  - All the interrupts except IPC are disabled, MMU and Cache are disabled
- Boot secondary ARM cores
  - Please refer the flow chart on the right side



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ARM Communication with DSP

- Hardware Queue
  - Use hardware queue (general propose) as the media
  - Use descriptor to transfer the message between Cores
  - Can pending the queue or use interrupts.
- Hardware IPC
  - Use hardware IPC to generate interrupt to dedicate Core(s)
  - Support up to 28 different Source IDs per Core

0x02620240	0x02620243	4B	IPCGR0	IPC Generation Register for C66x CorePac0
0x02620244	0x02620247	4B	IPCGR1	IPC Generation Register for C66x CorePac1
0x02620248	0x0262024B	4B	IPCGR2	IPC Generation Register for C66x CorePac2
0x0262024C	0x0262024F	4B	IPCGR3	IPC Generation Register for C66x CorePac3
0x02620250	0x02620253	4B	IPCGR4	IPC Generation Register for C66x CorePac4
0x02620254	0x02620257	4B	IPCGR5	IPC Generation Register for C66x CorePac5
0x02620258	0x0262025B	4B	IPCGR6	IPC Generation Register for C66x CorePac6
0x0262025C	0x0262025F	4B	IPCGR7	IPC Generation Register for C66x CorePac7
0x02620260	0x02620263	4B	IPCGR8	IPC Generation Register for ARM CorePac0
0x02620264	0x02620267	4B	IPCGR9	IPC Generation Register for ARM CorePac1
0x02620268	0x0262026B	4B	IPCGR10	IPC Generation Register for ARM CorePac2
0x0262026C	0x0262026F	4B	IPCGR11	IPC Generation Register for ARM CorePac3
0x02620270	0x0262027B	12B	Reserved	Reserved
0x0262027C	0x0262027F	4B	IPCGRH	IPC Generation Register for Host
0x02620280	0x02620283	4B	IPCAR0	IPC Acknowledgement Register for C66x CorePac0
0x02620284	0x02620287	4B	IPCAR1	IPC Acknowledgement Register for C66x CorePac1
0x02620288	0x0262028B	4B	IPCAR2	IPC Acknowledgement Register for C66x CorePac2
0x0262028C	0x0262028F	4B	IPCAR3	IPC Acknowledgement Register for C66x CorePac3
0x02620290	0x02620293	4B	IPCAR4	IPC Acknowledgement Register for C66x CorePac4
0x02620294	0x02620297	4B	IPCAR5	IPC Acknowledgement Register for C66x CorePac5
0x02620298	0x0262029B	4B	IPCAR6	IPC Acknowledgement Register for C66x CorePac6
0x0262029C	0x0262029F	4B	IPCAR7	IPC Acknowledgement Register for C66x CorePac7
0x026202A0	0x026202A3	4B	IPCAR8	IPC Acknowledgement Register for ARM CorePac0
0x026202A4	0x026202A7	4B	IPCAR9	IPC Acknowledgement Register for ARM CorePac1
0x026202A8	0x026202AB	4B	IPCAR10	IPC Acknowledgement Register for ARM CorePac2
0x026202AC	0x026202AF	4B	IPCAR11	IPC Acknowledgement Register for ARM CorePac3

Figure 8-23 IPC Generation Registers (IPCGRx)

31	30	29	28	27 – 8	7	6	5	4	3 – 1	0
SRCS27	SRCS26	SRCS25	SRCS24	SRCS23 – SRCS4	SRCS3	SRCS2	SRCS1	SRCS0	Reserved	IPCG

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  - TI Keystone II U-Boot & Linux Kernel Versions and Features

Compiler and CCS support

- Linaro GCC cross compiler
  - Released by the Linaro organization, **open source** under the GPL license
  - Bases on GNU GCC baseline and has both versions to **support both bare-metal** (Launchpad) **and Linux ABI** (Linaro) compilations
  - **Better support Cortex-A15** pipeline and optimizations since GCC 4.7
  - TI and ARM are major members, recommend to use Linaro compiler
- Linaro GCC bare-metal cross compiler are integrated in CCS since V5.4.0.00091
  - Started with GCC v4.7.3
- Linaro GCC Linux ABI cross compiler are available in the following link
  - https://launchpad.net/gcc-linaro/4.7/4.7-2013.03/+download/gcc-linaro-4.7-2013.03.tar.bz2

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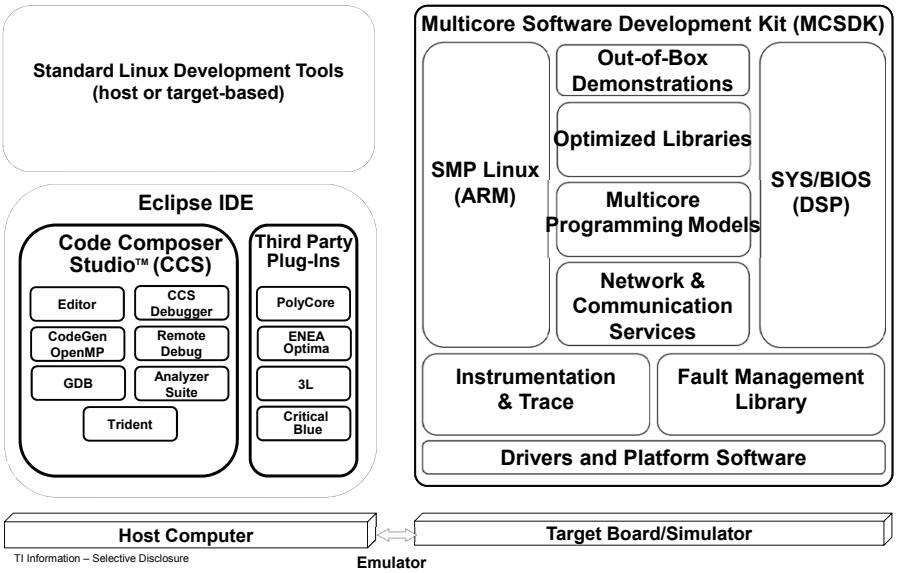
Development Ecosystem



Linux Development Support

- Linux-based software platform for development, deployment, and execution of ARM A15 on KeyStone II.
- Actively upstreaming Keystone II support to the open-source community
- Source code and prebuilt images of u-boot and kernel
- Open-source Linaro tool-chain for compilation (GCC) and debug (GDB)
- Load-and-run Linux kernel using Code Composer Studio
- Telnet into device to view console print as device boots and to mount root filesystem

TI Open Source Presence

- Active member of Linux Foundation
- Founding member of Linaro
- Sponsor of BeagleBoard and PandaBoard
- Top open hardware and open embedded software projects
- Top 10 contributor to kernel, leads embedded-processing industry contributions

Most active 3.4 employers

By changesets			By lines changed		
(None)	1156	10.8%	(None)	108509	15.5%
Intel	1138	10.6%	Intel	67464	9.7%
Red Hat	960	9.0%	Red Hat	65966	9.4%
(Unknown)	688	6.4%	(Unknown)	50900	7.3%
Texas Instruments	428	4.0%	IBM	36800	5.3%
IBM	381	3.6%	Oracle	26617	3.8%
Novell	372	3.5%	Texas Instruments	25687	3.7%
(Consultant)	298	2.8%	Samsung	24966	3.6%
Wolfson Microelectronics	286	2.7%	NVidia	20604	2.9%
Samsung	234	2.2%	Linux Foundation	16917	2.4%
Google	222	2.1%	ST Ericsson	15792	2.3%
Oracle	188	1.8%	Novell	15185	2.2%
Freescale	175	1.6%	Wolfson Microelectronics	14039	2.0%
Qualcomm	161	1.5%	(Consultant)	13495	1.9%
Linaro	143	1.3%	AMD	10151	1.5%
Broadcom	140	1.3%	Freescale	10102	1.4%
NetApp	133	1.2%	Linaro	9360	1.3%
MiTAC	133	1.2%	Google	9070	1.3%
AMD	132	1.2%	Qualcomm	8972	1.3%

THE LINUX FOUNDATION Linaro beagleboard.org

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Baseline Versions and Features

- TI Keystone II Linux kernel Baseline
  - Based on **Linux Kernel v3.8.4** in community (latest has **v3.10.10**)
  - Have **both regular and PREEMPT_RT** branches
  - Fully support **FDT** (Flat Device Tree) for hardware description
  - Fully support **LPAE** for **up to 36-Bit physical address**
  - Integrated frequently used **BSP&Drivers for Keystone II EVM**
  - Support most **popular file system** such as ramfs, ubifs
- TI Keystone II U-Boot Baseline
  - Based on **2013.01** version U-Boot
  - Support **both Tags and FDT** for passing kernel parameters
  - Integrated **daily used function command** such as EVM POST, DSP core Power OFF, image generation tools with SPL, image burning tools, etc
- Cross Compiler Baseline
  - Based on Linaro GCC v4.7.3 (20130313), better support Cortex-A15 features

To Get the Source Code and MCSDK Prebuilt Image

- Prebuilt Images in MCSDK 3.x
  - Including prebuilt U-Boot images (bin & gph format), boot monitor, DTB, uImage, file systems of ramfs (cpio) and ubifs (ubi image and ubifs format) for both regular and RT versions
  - MCSDK GA and updated versions are available
  - Integrated daily used PDK test images in the prebuilt root filesystem
  - Latest version download links:
  - http://software-dl.ti.com/sdoemb/sdoemb_public_sw/mcsdk/latest/index_FDS.html
- Source Code on Git.TI site
  - U-Boot:
  - http://git.ti.com/cgit/cgit.cgi/keystone-linux/u-boot.git/
  - Linux Kernel:
  - http://git.ti.com/cgit/cgit.cgi/keystone-linux/linux.git/
  - Boot Monitor:
  - http://git.ti.com/cgit/cgit.cgi/keystone-linux/boot-monitor.git/

Thank You!

TI Keystone Networking Coprocessor Introduction

KeyStone Training

Texas Instruments

Why Network Co Processor (NetCP):

Motivation behind NETCP:

- Use firmware based PDSP (Packet Descriptor Processors) to do processing and encryption.

Goals for both Packet Accelerator and Security Accelerator:

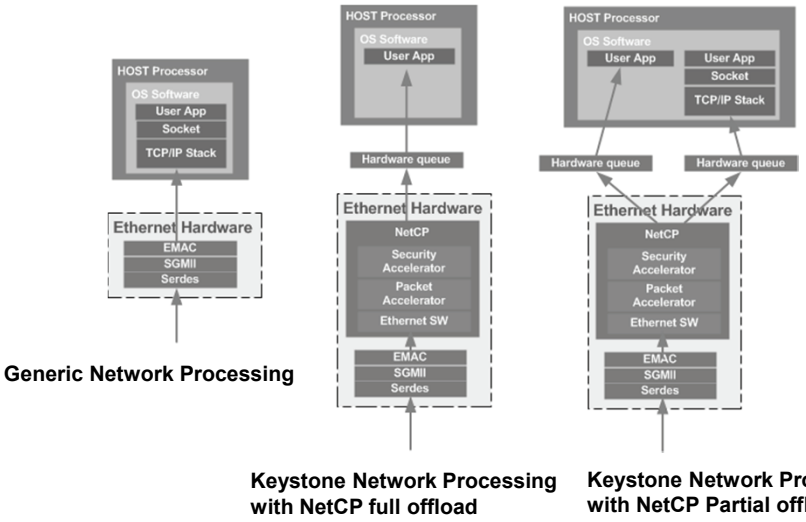
- Offload processing from the cores
- Improve system integration
- Allow cost savings at the system level

Security Key applications:

- IPSec tunnel endpoint (e.g. LTE eNB, ...)
- Secure RTP (SRTP)
- Air interface (2G/3G/4G) security processing

Texas Instruments

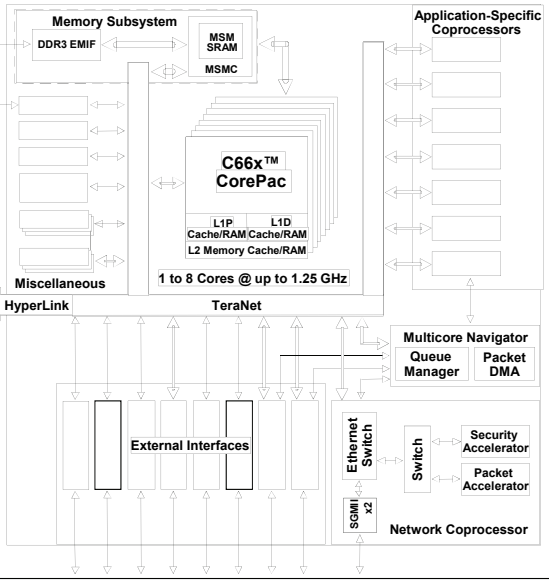
Why Network Co Processor (NetCP)



Agenda

- KeyStone I/NetCP1.0
  - Overview
  - Typical Application
  - PA 1.0
- KeyStone II/ NetCP1.5
  - Overview
  - Typical Application
  - PA 1.5
  - NetCP QMSS/PDSP Firmware/RA
- NetCP 1.0 Vs NetCP1.5
- Security Accelerator
  - Overview
  - Channel Configuration
  - Data Process

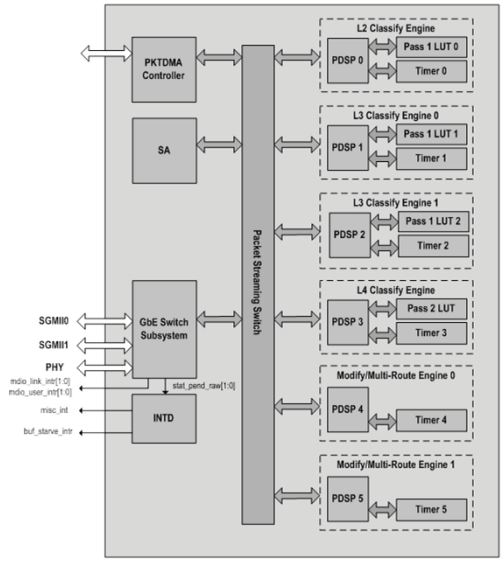
KeyStone I Network Coprocessor



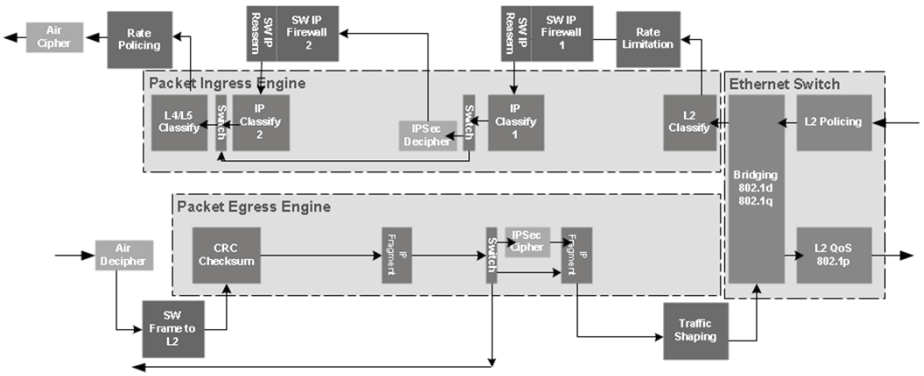
- Provides hardware accelerators to perform L2, L3, and L4 processing and encryption that was previously done in software
- Packet Accelerator (PA)
  - Single or multiple IP address option
  - UDP (and TCP) checksum and selected CRCs
  - L2/L3/L4 support
  - Quality of Service (QoS)
  - Multicast to multiple destinations inside the device
  - Timestamps
- Security Accelerator (SA)
  - Hardware encryption, decryption, and authentication
  - Supports IPsec ESP, IPsec AH, SRTP, and 3GPP protocols

Packet Accelerator 1.0 Block Diagram

- Provides hardware accelerators to perform the packet classification for Ethernet L2, L3, and L4
  - Hardware Lookup table (LUT1 64 entry/table, LUT2 8K entry/table)
- Based on use case firmware can be redefined/developed
- Engines for modification (IP header/UDP header checksum, IP fragmentation, update PPPoE header)
- Multi routing (same packet can be copied and routed to 8 different queue)



NetCP1.0 Typical Application



- Software for IP reasembly
- Software IP Firewall
- Software for Packet Framing on to-network direction

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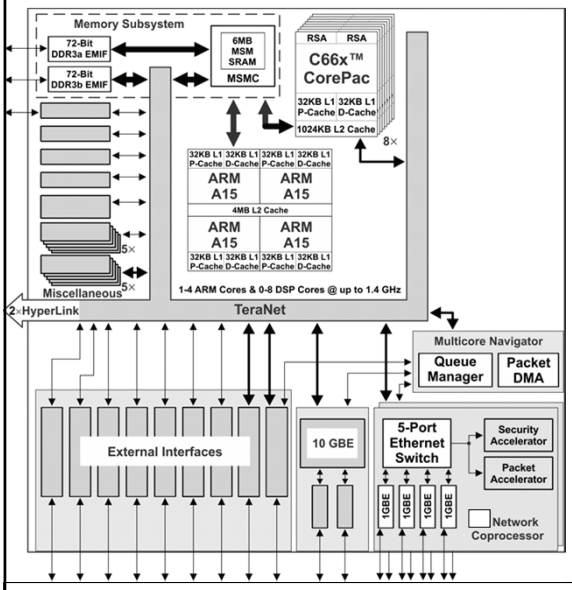
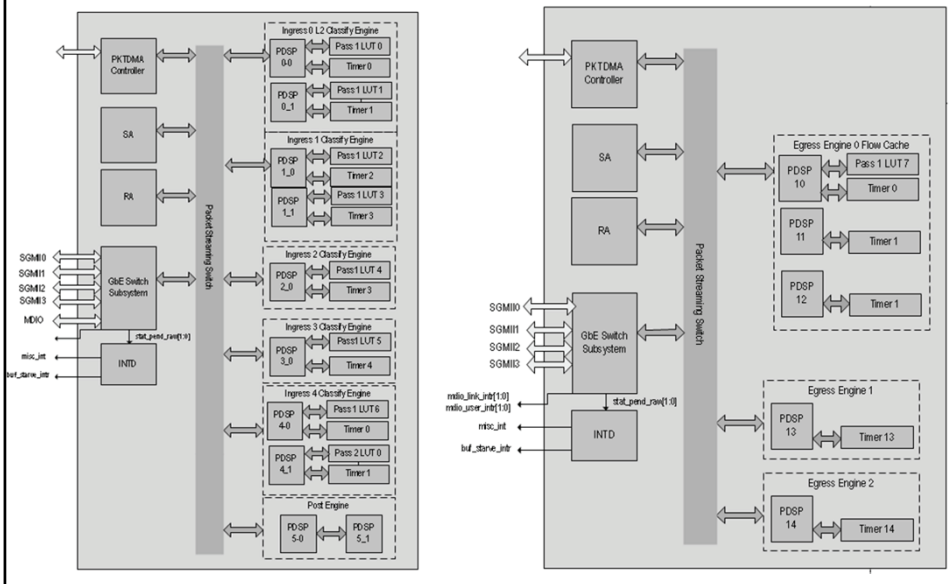
KeyStone II Network Coprocessor (NETCP)



- Consists of one or two Network Coprocessor(s)
- Provides hardware accelerators to perform L2, L3, and L4 processing and encryption that was previously done in software
- Packet Accelerator (PA)
  - Single IP address option
  - UDP (and TCP) checksum and selected CRCs
  - L2/L3/L4 support
  - Quality of Service (QoS)
  - Multicast to multiple queues
  - Timestamps
- Security Accelerator (SA)
  - Hardware encryption, decryption, and authentication
  - Supports IPsec ESP, IPsec AH, SRTP, and 3GPP protocols
- 2x 5-port Ethernet switches (depending on number of instances of NETCP) with 4-8 ports connecting to 4-8 SGMII ports and one port connecting to the Packet and Security Accelerators.

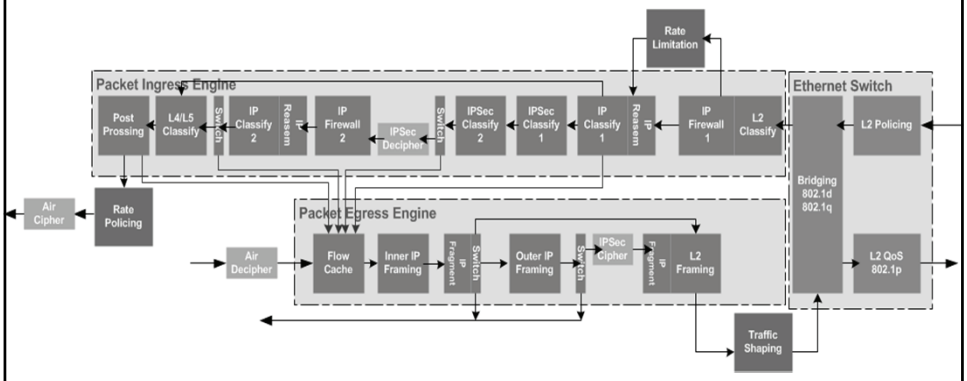
Packet Accelerator 1.5 Block Diagram



Packet Accelerator 1.5

- PA LLD interface and features are compatible with NetCP1.0
- Provides hardware accelerators to perform the packet classification for Ethernet L2, L3, and L4
  - Hardware Lookup table (LUT1 256 entry/table, LUT2 3K entry/table) with mask/range configuration
- Each PDSP can do more complex processing (MAX to 3K instructions)
- Egress direction has capability to modify a packet as configuration and route it to Ethernet directly

NetCP1.5 Typical Application

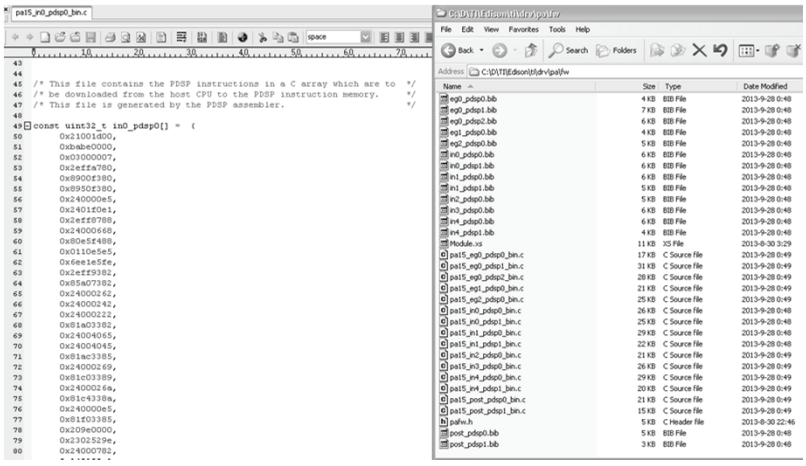


- Hardware accelerators to do L2, L3, and L4 processing, packet classify
- Hardware accelerators for IPSec/air cihper encryption
- Hardware QoS for PQ/WRR
- Hardware accelerators for IP reasembly
- Hardware accelerators for Flow Cache
- Hardware accelerators for IP Firewall

NetCP QMSS

- The primary use case is for handling CDMA based packet flows between PA and the Security Accelerator (SA) and Reassembly (RA) engines.
- Using the PA1.5 queue management subsystem offloads DMA and queue operations from the global PA CDMA and chip-level QMSS.
- Provides support for 128 total queues (2 Queue Managers supporting 64 queues each)
  - Supports up to 16K descriptors
  - Supports 16 memory regions for storage of descriptors with each region storing up to 16K descriptors
- Provides support for monitoring 21 queues (queues 0 through 20 of Queue Manager 0) by exporting hardware signals indicating queue status to a local CPPI DMA engine.
- Provides a 128KB memory region for fast local storage of packet descriptors and/or buffers

PDSP firmware



- Each PDSP has dedicated firmware file with array and binary format

Reassembly Engine

- The Reassembly engine is a hardware accelerator block for reassembling fragmented IPv4 and IPv6 Packets
- Supports reassembly at 10Gbps rate for up to 1K concurrent contexts
- There will be 2 in the system
  - Pre-SA decrypt
  - Post-SA decrypt
- The timeouts will be from 100 to $2^{32} * 2^{10}$ clock cycles@400MHz

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NetCP 1.0 Vs 1.5

Applications	1.0	1.5
Maximum IP packet size	9KB	64KB
PDSP	PA 6 PDSPs 8KB IRAM/PDSP	PA 15 PDSPs 12KB IRAM/PDSP
LUT	3 LUT1 with 64 entries 1 LUT2 with 8K entries(32 bit each)	8 LUT1 (256 entries), mask/range supported 1 LUT2 with 3K entries (64 bit each), range supported
Hardware Firewall	No	256 entries/ACL for outer IP & 256 entries/ACL for Inner IP
Hardware IP Reassembly	No	Outer IP and inner IP reassembly by hardware
Flow cache	No	Yes
IPSec	Replay widows 128	Replay widows 1024 Performance 2x 1.0
Air Cipher	Separate Air Ciphering and Authentication No ZUC F8/F9 and Snow3G F9	Simultaneous Air Ciphering and Authentication Support ZUC F8/F9 and Snow3G F9
Internal memory ECC	No	Yes
Internal QMSS	No	Yes
PKT DMA	9 Tx channels 24 Rx channels	21 Tx channels 91 Rx channels
QoS	PQ+WRR	PQ+WRR Performance 4x 1.0

Agenda

- KeyStone I/NetCP1.0
  - Overview
  - Typical Application
  - PA 1.0
- KeyStone II/ NetCP1.5
  - Overview
  - Typical Application
  - PA 1.5
  - NetCP QMSS/PDSP Firmware/RA
- NetCP 1.0 Vs NetCP1.5
- Security Accelerator
  - Overview
  - Channel Configuration
  - Data Process

Security Accelerator Overview

Motivation
- Hardware Encryption, Decryption, and Authentication
- Faster than software

Supported Protocols
- IPsec ESP
- IPsec AH
- SRTP
- 3GPP

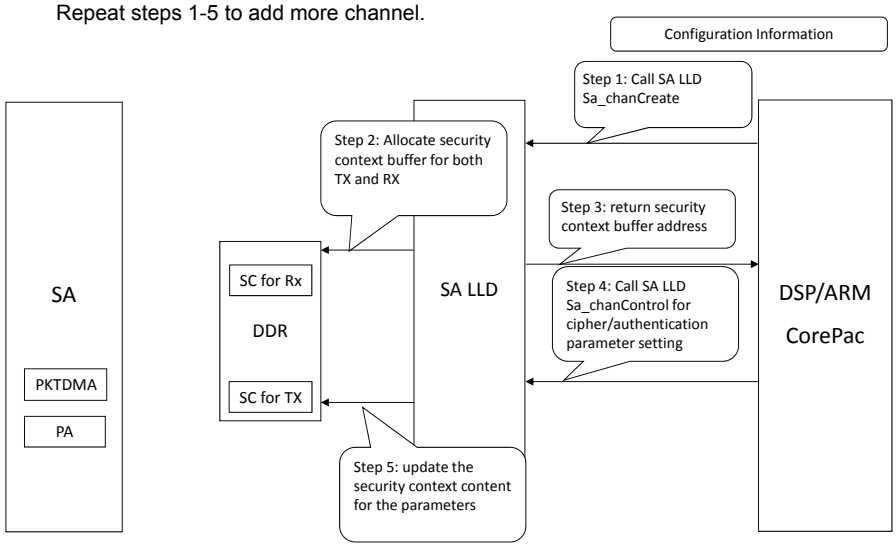
Each security accelerator supports:
- Loosely coupled accelerator at 1.5M packets per second
- Authentication and replay protection at Gigabit Ethernet wire rate
- Pre- and post- algorithm packet header processing and security association maintenance
- Context caching for security associations (SW or HW managed)
- Can be used by NetCP without host intervention and by SW in parallel

Module Name	Block size (Bits)	Throughput (Mbits/sec)	Remark
AES modes	128	3x 2,800.0	AES 256-bit key numbers, worst case for modes other than CCM
3DES modes	64	2x 1,493.3	3DES 3 key numbers, worst case
Galois Multiplier	128	2x 8,960.0	Galois multiplier core used for GCM mode
AES modes 128 bit key	128	3x 3,200.0	AES 128-bit key numbers, worst case for modes other than CCM
AES -CCM - 256 bits AES Key	128	3x 1,400.0	In CCM mode, AES is run twice for same block.
Kasumi	64	1244.4	Kasumi in F8 mode
Snow3G	320	1154.6	SNOW 3G in F8 mode. 40 bytes in one block, for 1500 byte blocks the throughput is above 5Gbit/s
HMAC- SHA1	512	2x 2,185.4	SHA 1 core
HMAC- MD5	512	2x 2,715.2	MD5 core
HMAC-SHA2	512	2x 2,715.2	SHA 2 core(max 256 bit hash)

TEXAS INSTRUMENTS

SA LLD: Channel Configuration

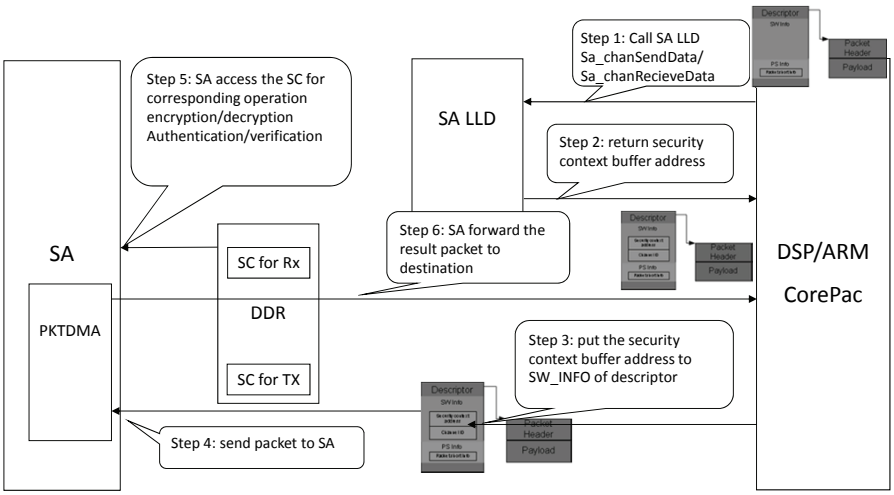
Repeat steps 1-5 to add more channel.



TEXAS INSTRUMENTS

SA LLD: Packet Process (Air Cipher)

Repeat steps 1-6 send more packet.



For More Information

- Device-specific Data Manuals for the KeyStone SoCs can be found at TI.com/multicore.
- Multicore articles, tools, and software are available at Embedded Processors Wiki for the KeyStone Device Architecture.
- View the complete C66x Multicore SOC Online Training for KeyStone Devices, including details on the individual modules.
- For questions regarding topics covered in this training, visit the support forums at the TI E2E Community and Deyisupport website.

Keystone Design Consideration

KeyStone Training

Texas Instruments

Agenda

- **Marketplace Challenges and KeyStone Solutions**
- KeyStone SoC Hardware Design
- Software Development

Texas Instruments

Common Usage Cases

- Network gateway, speech/voice processing
  - Typically hundreds or thousands of channels
  - Each channel consumes about 30 MIPS
- Cloud computing
- Server and Storage
- Large, complex, floating point FFT
- Video processing
- Medical imaging
- LTE, WiMAX, other wireless physical layers
- Scientific processing (Oil explorations)
  - Large complex matrix manipulations
- Your applications?

Marketplace Challenges

- Increase of data rate
  - Think about Ethernet, from 10Mbps to 10Gbps
- Increase in algorithm complexity
  - Think about typical face recognition, finger prints, cloud computing
- Increase in development cost
  - Hardware and software development
- **KeyStone SOC devices are a solution**
  - Fast peripherals part of the device
  - High performances, fixed point and floating point processing power. Parallel data movement.
  - Off-the-shelf devices
  - Elaborate set of software tools

To Fulfill Large Data Transmission

- Fast peripherals are needed to:
  - Receive high bit-rate data into the device
  - Transmit the processed HBR data out of the device
- KeyStone devices have a variety of high bit-rate peripherals, including the following:
  - 10/100/1000 Mpbs Ethernet
  - 10G Ethernet
  - SRIO
  - PCIe
  - AIF2
  - TSIP

Enable Complex Algorithms

- 8 functional units of the C66x CorePac provide:
  - Fixed- and Floating-point native instructions
  - Many SIMD instructions
  - Many Special Purpose Powerful instructions
  - Fast (0 wait state) L1 memory
  - Fast L2 memory
- ARM Core provides
  - Fixed- and Floating-point native instructions
  - Many SIMD instructions
  - Fast (0 wait state) private L1 cache memory for each A15
  - Fast shared coherent L2 cache memory

Inter-Processor Communication

- Shared memory
  - Very fast and large external DDR interface(s).
  - DSP Core provides 32- to 36-bit address translation enables access of up to 10GB of DDR. ARM core uses MMU to translate 32 bits logical address into 40 bits physical address
  - Fast, shared L2 memory is part of the sophisticated and fast MSMC.
- Hardware provides ability to move data and signals between cores with minimal CPU resources.
  - Powerful transport through Multicore Navigator
  - Multiple instances of EDMA
- Other hardware mechanisms that help facilitate messages and communications between cores.
  - IPC registers, semaphore block

Minimizing Resource Contention

- Each DSP CorePac has a dedicated port into the MSMC.
- MSMC supports pre-fetching to speed up loading of data.
- Shared L2 has multiple banks of memory that support concurrent multiple access.
- ARM core uses AMBA bus to connect directly to the MSMC, provide coherency and efficiency
- Wide and fast parallel Teranet switch fabric provides priority-based parallel access.
- Packet-based HyperLink bus enables the seamless connection of two KeyStone devices to increase performance while minimizing power and cost.

Multicore SOC Design Challenges

- Hardware design
  - Specific design requirements
  - high-speed interface design
  - Reference design solution
- Software development
  - Multicore work allocation and load balance
  - Multicore communication
  - Low level hardware driver
  - Application library

Agenda

- Marketplace Challenges and KeyStone Solutions
- **KeyStone SoC Hardware Design**
  - ***Minimum System Design***
  - ***Peripherals Design***
  - ***Reference Design - EVM***
- Software Development

Minimum System Design

- Power Supplies
- Clocking
- DDR3 Design
- Boot Design
- JTAG

Power Supplies - KI

- Power Types
  - AVS for CVDD
    - Interface VCNTL[3:0]: 4-pin 6-bit dual-phase
    - with initial voltage **1.1v**;
    - Two classes solutions
      - » LM10011: P7256, P7303
      - » UCD92xx: Refer to EVM Schematic
  - Fixed power: 1.0/1.5/1.8V

Design Details see section 2 of "Hardware design guide SPRABI2C".

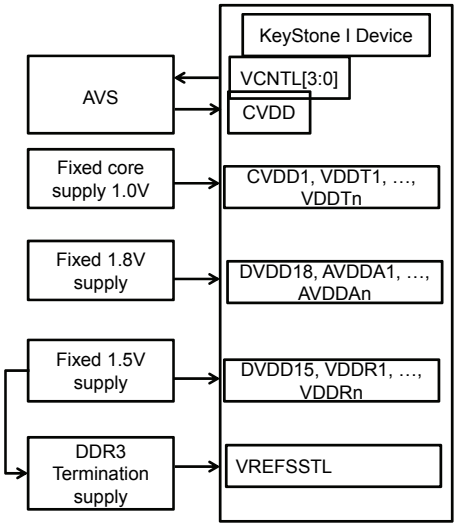
- Available tools to calculate the DSP power consumption and current value.

The data is application-dependent and the model is used to get the accurate results.
Power Consumption Model download link:

http://www.ti.com/product/tms320c66xx (Software & Tools -> Models)

- Power Supply Sequence
  - Core voltage start before IO voltage
    - CVDD -> CVDD1 -> DVDD18 -> DVDD15
  - IO voltage start before core voltage
    - DVDD18 -> CVDD -> CVDD1 -> DVDD15

Details requirement refer to the device data manual.



Power Supplies - KII

- Power Types
  - AVS for CVDD
    - Interface VCNTL[5:0]: 4-pin 6-bit dual-phase or 6-pin 6-bit single phase
    - with initial voltage **1.0v**;
    - Two classes solutions
      - » LM10011: P7256, P7303, EVMK2E Schematic
      - » UCD92xx: EVMK2H Schematic
  - Fixed power: 0.95/0.85/1.5/1.8V/3.3

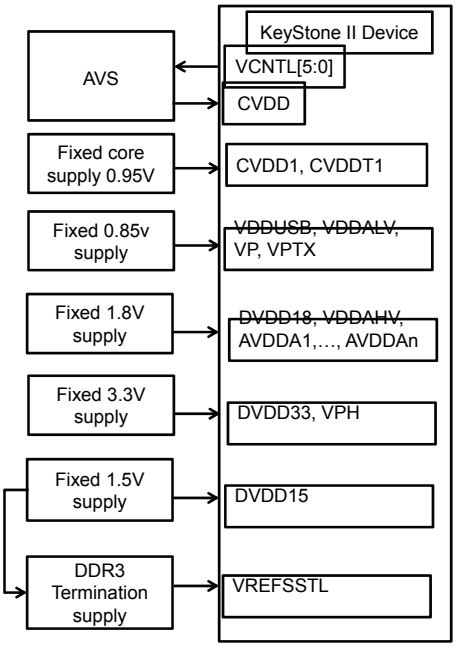
Design Details see section 2 of "Hardware design guide SPRABV0".

- Available tools to calculate the DSP power consumption and current value.

The data is application-dependent and the model is used to get the accurate results.

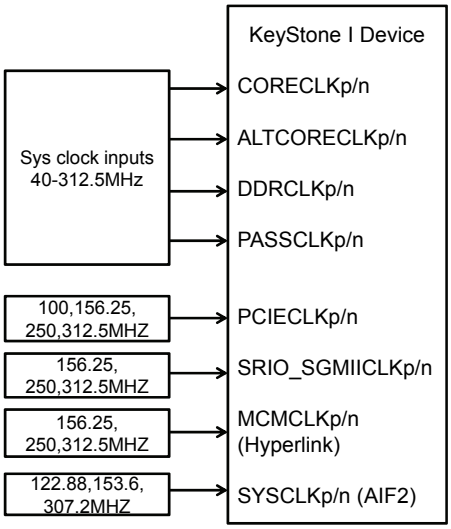
- Power Supply Sequence
  - Core voltage start before IO voltage
    - CVDD -> CVDD1, DVDD18, VDDAHV, AVDDAx-> DVDD15->VDDALV, VDDUSB, VP, VPTX->DVDD33
  - IO voltage start before core voltage
    - DVDD18, VDDAHV, AVDDAx->CVDD->CVDD1-> DVDD15->VDDALV, VDDUSB, VP, VPTX->DVDD33

Details requirement refer to the device data manual.



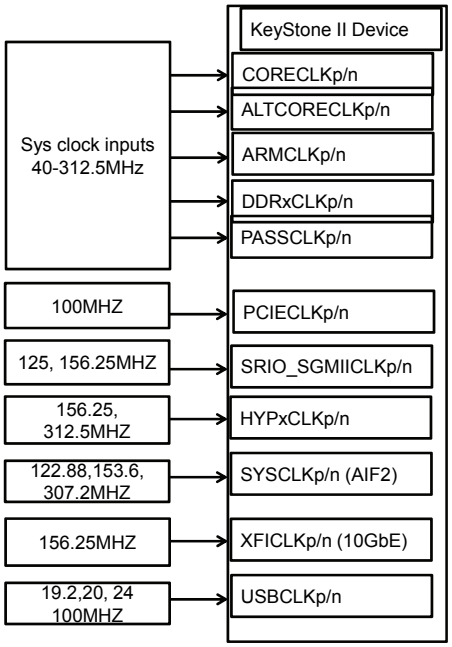
Clocking - KI

- Clock Types
  - Necessary: Clock for Main PLL (CORECLK or ALTCORECLK).
  - Selective: Clock for peripherals(depend on design)
- Design Requirements
  - Should satisfy with the jitter requirements;
  - Should select the valid input frequencies;
  - Unused clock inputs should be connected as figure 13 in SPRABI2C.
- Reference Design Guide
  - See the "Clock Design guide (SPRABI4)" and section 3 of "Hardware design guide(SPRABI2C)" for clock design details.
  - See the EVM schematic and PCB layout for reference.
- Recommend Clock Parts
  - CDCM6208
  - CDCE62005
  - CDCE62002



Clocking - KII

- Clock Types
  - Necessary: Clock for Main PLL (CORECLK or ALTCORECLK).
  - Selective: Clock for peripherals(depend on design)
- Design Requirements
  - Should satisfy with the jitter requirements;
  - Should select the valid input frequencies;
  - Unused clock inputs should be connected as figure 15 in SPRABV0.
- Reference Design Guide
  - See the “Clock Design guide (SPRABI4)” and section 3 of “Hardware design guide(SPRABV0)” for clock design details.
  - See the EVM schematic and PCB layout for reference.
- Recommend Clock Parts
  - CDCM6208
  - CDCE62005
  - CDCE62002



DDR3 Design

- Design Guide
  - See the “DDR3 Design Requirement for Keystone Devices(SPRABI1A)” for information regarding supported topologies and layout guidelines.
  - See the section “Input clock requirements” of the “Hardware design guide for KI devices (SPRABI2C)” and SPRABV0 for KII devices for the input reference clock and unused pin requirements.
- Available tools to generate DDR3 configuration values

  The DDR3 configuration registers’ value depend on board layout and the selected SDRAM.

  Refer to the “Keystone I DDR3 Initialization SPRABL2B” for the DDR3 initialization sequence and use the DDR3 spreadsheet to generate your value, then update the DDR3 initial value of the demo code STK.

Boot Design

- Boot Modes
  - Memory boot: EMIF, SPI, and I2C master boot.
  - Host Boot: UART, SRIO, PCIe, EMAC, Hyperlink and I2C slave boot.

  For boot details, see the SPRUGY5B for KI, SPRUGY9C for KII DSP bootloader, and SPRUHJ3 for KII ARM bootloader.
- Boot Configuration Pins
  - Boot mode and configurations are chosen using bootstrap pins on the device, and Pins are latched and stored in the DEVSTAT register during POR. To determine the boot configuration, BOOTMODE[13:0] are used for KI, BOOTMODE[15:0] are used for KII.
  - See the device data manual for details of the pins configuration.
- See the **RBL** source code for detailed boot sequence.

JTAG

- Design Guide
  - All JTAG pins are 1.8v IO, a voltage converter is needed if the selected emulator doesn't support 1.8v IO levels.
  - For JTAG connection design guide refer to: http://processors.wiki.ti.com/index.php/XDS_Target_Connection_Guide
  - Details about trace emulator design, see the "Emulator and Trace Headers Technical Reference Manual (SRPU655H)"
- JTAG Emulator Selection

  http://www.ti.com/lsds/ti/tools-software/emulators.page

JTAG Probes and Trace Receivers

XDS100v2/v3 | XDS200 | XDS510 | XDS560v2 STM | XDS560v2 Pro Trace

- Emulation header selection
  - 14-pin and 20-pin can satisfy with the general debug
  - 20-pin can support export of system trace data
  - 60-pin can support export of core trace, and it can also support export of system trace data.

  notes: For DSP device has on chip trace buffer, the XDS560 14pin/20pin generation emulator support core trace too.
- For JTAG problems, refer to:

  http://processors.wiki.ti.com/index.php/Debugging_JTAG_Connectivity_Problems

Peripherals Design

- General Peripherals
  - I2C/SPI/EMIF16/UART/uPP/TSIP/GPIO
- High Speed Peripherals
  - USB
  - EMAC
  - 10GbE
  - PCIe
  - SRIO
  - Hyperlink
  - AIF2

General Peripherals

- Design Requirements
  - All the interfaces operate at 1.8v, voltage level translator is needed to tolerant other voltage such as 2.5v or 3.3v.
  - Requirement of external resistor is interface-dependent, suggest select the recommended resistor values in the hardware design guide, or maybe need to use the IBIS module to determine the best resistor.
  - Unused pins requirements are interface-dependent, it can be left unconnected if with internal pull-up or pull-down resistors.
- Reference Design Guide
  - For detail design requirements of each interface, see the related section of file “Hardware design guide for KI devices(SPRABI2C)” and SPRABV0 for KII devices.
- Throughput Performance
  - For theory and measurement throughput performance refer to the “Throughput performance guide(SPRABK5A)”.

High Speed Peripherals – USB/EMAC/10GbE/PCIe/SRIO/Hyperlink/AIF2

- Reference Design Guide
  - For the input reference clock requirements see the section “Input clock requirements” of the “Hardware design guide for KI devices (SPRABI2C)” and “SPRABV0 for KII devices”.
  - See the “SerDes Implementation Guide for Keystone I Devices (SPRABC1)” and “SPRUHO3 for KII devices” for serdes layout rules constraints and the serdes registers configuration.
  - See the respective section of “Hardware design guide for KI devices(SPRABI2C)” and “SPRABV0 for KII devices” for the unused pins requirement.
  - See the EVM schematic and PCB layout for reference design.
- Throughput Performance
  - For theory and measurement throughput performance see the “Throughput performance guide(SPRABK5A)”.

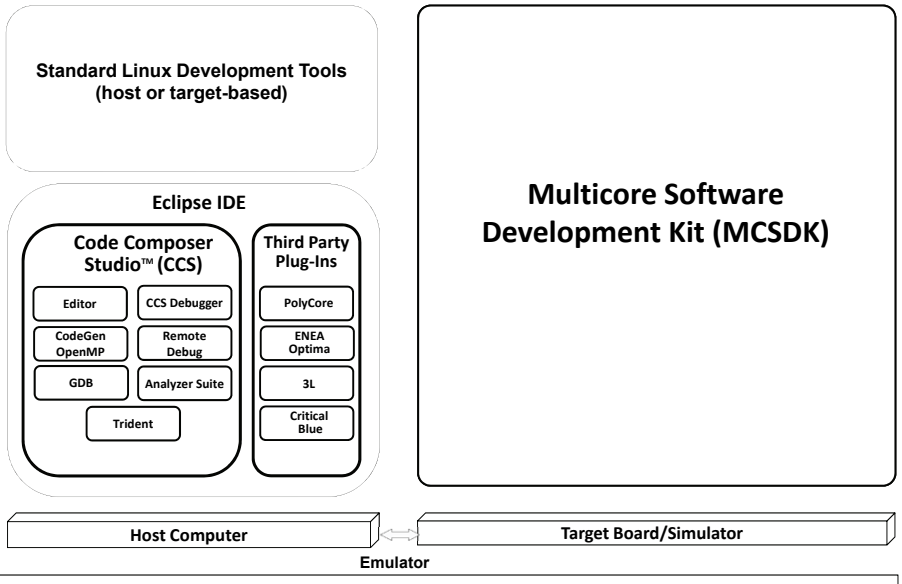
Reference Design - EVM

- EVM Types
  - EVM6678L/LE
  - EVM6657L/LE
  - EVM6670L/LE
  - EVMK2H/K2HX
- Click the above EVM link, you can find the below EVM information
  - EVM Quick Setup Guide.
  - Technical Reference Guide.
  - Schematic.
  - PCB Layout.
  - EVM Firmware such as the UCD file for power and FPGA file.
  - ……
- In all, the EVM is a good reference design guide for startup.

Agenda

- Marketplace Challenges and KeyStone Solutions
- KeyStone SoC Hardware Design
- **Software Development**
  - ***Software Development Ecosystem***
  - ***CCS Eclipse IDE v5***
  - ***Multicore Software Development Kit (MCSDK)***
  - ***Multicore Program***
  - ***Application Software***

Multicore SW Development Ecosystem



CCS Eclipse IDE v5

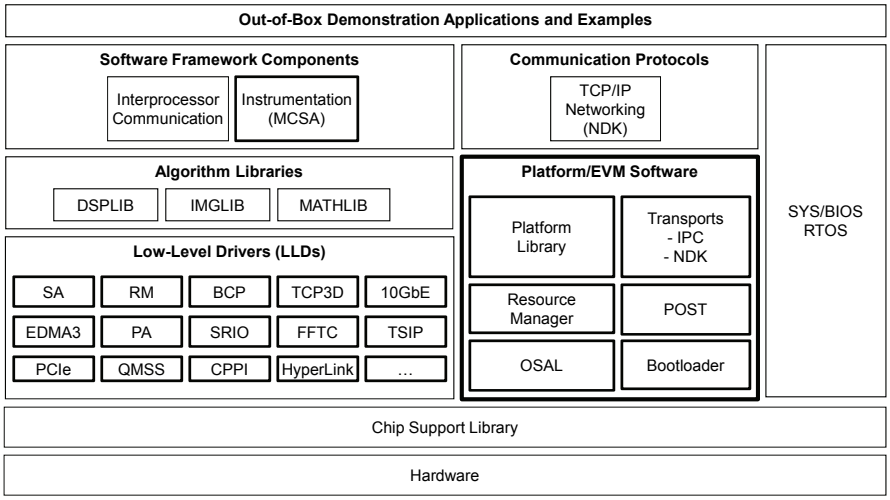
- Code Composer Studio (CCS) is an Eclipse-based IDE that supports application development on multiple cores/devices:
  - Support simulator, debug/emulation, remote Debug, instrumentation and visualization.
  - Integrated compiler tools with support for OpenMP.
  - Allows developers to integrate third-party software tools assisting for multicore programming, profiling and analysis capabilities.

  CCSv5 details see: http://processors.wiki.ti.com/index.php/Category:Code_Composer_Studio_v5
- Download CCS and the compiler.
- CCS License:
  - Free for 90days for CCSv5,
  - free license file for C66x EVMs here (under "Keystone EVM Info" section of the download page)
  - more about CCS-License.

MCSDK: Overview

- Set of software building blocks to facilitate development of applications
- DSP and ARM platform software, low-level drivers, high-level APIs and other utilities
- Source and prebuilt libraries are included
- Embedded OS: SYS/BIOS RTOS on C66; Linux on ARM
- Development OS: Windows and Linux PC support
- Free to download with all components in one installer

C66x MCSDK Overview



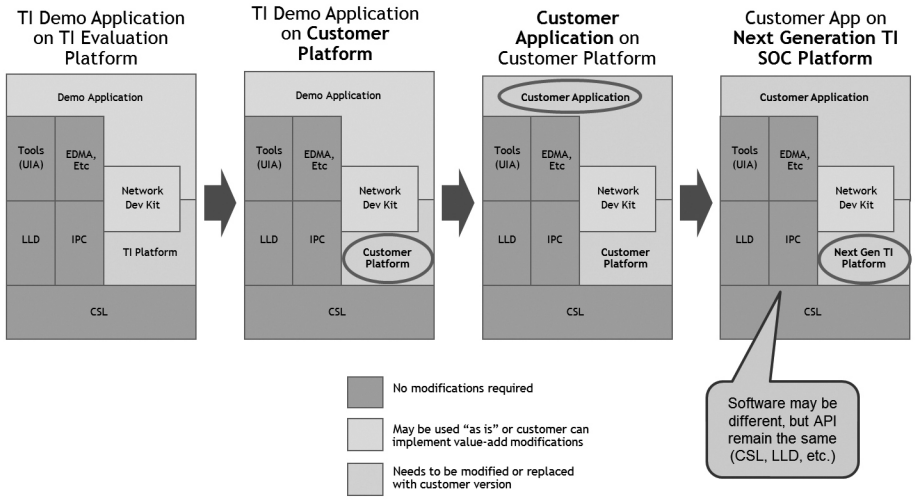
ARM Linux Perspective: Overview

- Linux-based software platform for development, deployment, and execution of ARM A15 on KeyStone II.
- Actively upstreaming Keystone II support to the open-source community
- Source code and prebuilt images of u-boot and kernel
- Open-source Linaro toolchain for compilation (gcc) and debug (gdb)
- Load-and-run Linux kernel using Code Composer Studio
- Telnet into device to view console print as device boots and to mount root filesystem

Drivers & Platform Software: Summary

Module	DSP (CSL)	DSP (LLD)	ARM (CSL)	ARM (User Mode LLD)	ARM (Linux kernel)
Timer64	x		x		
ARM Arch Timer					x
ARM Intc (GIC)			x		x
CPINTC	x		x		
CPSW (5-port 10G)	x		x		x
USB 3.0	x		x		x
GPIO	x		x		x
EMIF16 - NAND	x		x		x
I2C	x		x		x
USIM	x		x		x
UART	x		x		x
SPI	x		x		x
AIF2	x	x			
SRIO	x	x	x		x
PCIe	x	x	x		x
PA	x	x	x	x	x
SA	x	x	x	x	x
CPSW (5-port 1G)	x		x		x
QMSS + PktDMA	x	x	x	x	x
RAC	x				
TAC2	x				
VCP2	x				
TCP3D	x	x			
BCP	x	x			
FFTC	x	x			
EDMA	x	x			
HyperLink	x	x	x	x	
HW Semaphore	x				x
PSC					x

Getting Started: Development Flow



Getting Started: Algorithm Libraries

Algorithm libraries contain C66x C-callable, hand-coded, assembly-optimized functions for specific usage:

- **Fundamental Math & Signal Processing Libraries**
  - **DSPLIB**: Signal-processing math and vector functions
  - **MathLIB:** Floating-point math functions
- **Image & Video Processing Libraries**
  - **IMGLIB:** Image/video processing functions
  - **VLIB:** Video analytics and vision functions
- **Telecommunication Libraries**
  - **VoLIB:** Voice over IP application related functions
  - **FaxLIB:** FAX application related functions
- **Medical Libraries**
  - **STK-MED:** Ultrasound and optical coherence tomography algorithms

More info: http://processors.wiki.ti.com/index.php/Software_libraries

Getting Started: Out-of-Box Demos

Keystone I & II demos:

- **Utility Application Demo**
  - Provides system information (OS version, CPU info, network interfaces), System statistics (mem/cpu usage, TX/RX pkts), Flash NAND/EEPROM, etc.
- **Image Processing Demo**
  - Image edge detection demo

Keystone II demos:

- **IPC Demo**
  - Load DSP out file from ARM and perform ARM-DSP communication
- **Transport Net Demo**
  - NetCP capabilities including PA, SA and Ethernet Switch Subsystem

Multicore Program

- For basic multicore program knowledge, see “Multicore Program Guide (SPRAB27B)”.
- Program Model
  - See the Hua and Image processing demos in the MCSDK.
  - See the multicore video infrastructure demo for multicore software demo.
  - See OpenMP for its usage in multicore program.
- Below table lists the basic IPC engines comparison between traditional and keystone devices.

	Traditional Solution	**Keystone Solution**
Inter-Processor Communication	EDMA ISR	EDMA ISR, IPC, Hardware Semaphore, Navigator, SRIO
Data Transfer Engines	EDMA, Ethernet, SRIO, AIF	EDMA, Ethernet, SRIO, AIF; Navigator, Hyperlink, 10GbE
Shared Resource Management	Global Flag	Global Flag, Hardware Semaphore, IPC

Application Software

- MCSDK Video Demos: Provides multiple video demos to demonstrate capability of C66x multi-core DSPs on computation intensive video processing.
- Industrial Image Demo: Focuses on the natural ability to parallelize image processing algorithms with employing open-source packages such as OpenMP and OpenCV.
- Medical Imageing Demo: Illustrates the system-level integration of key medical imaging algorithm modules on multicore DSPs, currently focuses on the Ultrasound and Optical Coherence Tomography(OCT) application domains.
- For more other application software see the Target End Equipments here.

Keystone I Development Tool Availability

- Keystone I Evaluation Modules: Available
  - http://www.ti.com/tool/tmdxevm6678
  - http://www.ti.com/tool/tmdxevm6670
  - http://www.ti.com/tool/tmdxevm6657
- MCSDK 2.x: Available
  - http://www.ti.com/tool/bioslinuxmcsdk
- EVM Materials and Support:
  - http://www.advantech.com/Support/TI-EVM/
  - http://www.einfochips.com/index.php/partnerships/texas-instruments/tms320c6657-evm#5-resources

Keystone II Development Tool Availability

- Keystone II Evaluation Modules: Available
  - http://www.ti.com/tool/evmk2h
- EVM Materials and Support:
  - http://www.advantech.com/Support/TI-EVM/
- MCSDK 3.0: Available
  - http://www.ti.com/tool/bioslinuxmcsdk
- Toolchain: Now
  - Linaro GCC bare-metal cross compiler are integrated in CCS since V5.4.0.00091
    - Started with GCC v4.7.3
  - Linaro GCC Linux ABI cross compiler are available in the following link
    - https://launchpad.net/linaro-toolchain-binaries/trunk/2013.03/+download/gcc-linaro-arm-linux-gnueabihf-4.7-2013.03-20130313_linux.tar.bz2
- Linux:
  - Uboot: http://arago-project.org/git/projects/?p=u-boot-keystone.git;a=summary
  - Kernel: http://arago-project.org/git/projects/?p=linux-keystone.git;a=summary
  - Boot Monitor: http://arago-project.org/git/projects/?p=boot-monitor.git;a=summary

For More Information

- Multicore Program Guide
- Multicore articles, tools, and software are available at Embedded Processors Wiki for the KeyStone Device Architecture.
- View the complete C66x Multicore SOC Online Training for KeyStone Devices, including details on the individual modules.
- For questions regarding topics covered in this training, visit the support forums at the TI E2E Community and 德州仪器中文社区.

Sitara™ PRU-ICSS Traning

Agenda

- **Introduction to the PRU Subsystem (PRU-ICSS on AM335x)**
- Getting Started Programming
  - PRU Assembler (PASM)
  - PRU Development Support Integrated in CCS&C Compiler
  - Linux PRU Application Loader
- PRU Application
- Other Resources

Introduction to the PRU SubSystem

- What is PRU SubSystem?
  - **P**rogrammable **R**eal-time **U**nit **S**ub**S**ystem
  - Dual 32bit RISC processors
  - Local instruction and data RAM; access to SoC resources.

- What devices include PRU SubSystem?
  - Legacy PRUSS: OMAPL137/ AM17x, OMAPL138/ AM18x, C674x
  - PRU-ICSS* (PRUSSv2): AM335x

- Why PRU SubSystem?
  - Full programmability allows adding customer differentiation
  - Efficient in performing embedded tasks that require manipulation of packed memory mapped data structures
  - Efficient in handling of system events that have tight real-time constraints.

* PRU-ICSS = **P**rogrammable **R**eal-time **U**nit and **I**ndustrial **C**ommunication **S**ub**S**ystem.

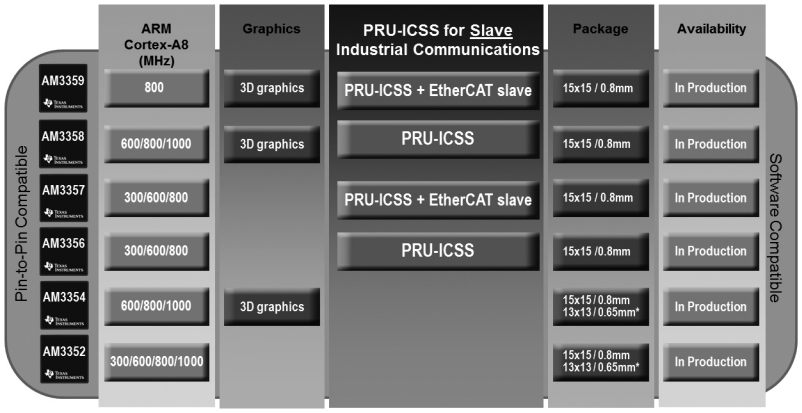
PRU Subsystem Is / Is-Not

IS	IS-Not
Dual 32-bit RISC processor specifically designed for manipulation of packed memory mapped data structures and implementing system features that have tight real time constraints	In not a H/W accelerator to speed up **algorithm computations**.
Simple RISC ISA - Approximately 40 instructions - Logical, arithmetic, and flow control ops all complete in a single cycle	Is **not a general purpose RISC processor** - No multiply hardware/instructions - No cache - No pipeline
Could be used to enhance the existing peripheral feature set or implement new peripheral capability with software bit bang	Is not a stand alone configurable peripheral and will need some hardware assist for configurable peripheral implementation
Includes example code to demonstrate various features. Examples can be used as building blocks.	No Operating System or high level application software stack

PRU Value

- Extend connectivity and peripheral capability
  - Implement Industrial Communications protocols (like EtherCAT®,PROFINET, EtherNet/IP™, PROFIBUS, POWERLINK, SERCOS III)
  - Implement special peripherals and bus interfaces (like soft UARTs interfaces)
  - Digital IOs with latency in ns
  - Implement smart data movement schemes (especially useful for audio algorithms like reverb, room correction, etc.)
- Reduce system power consumption
  - Allows switching off both ARM and DSP clocks
  - Implement smart power controller by evaluating events before waking up DSP and/or ARM. Maximized power down time.
- Accelerate system performance
  - Full programmability allows custom interface implementation
  - Specialized custom data handling to offload CPU

PRU-ICSS Subsystem on AM335x

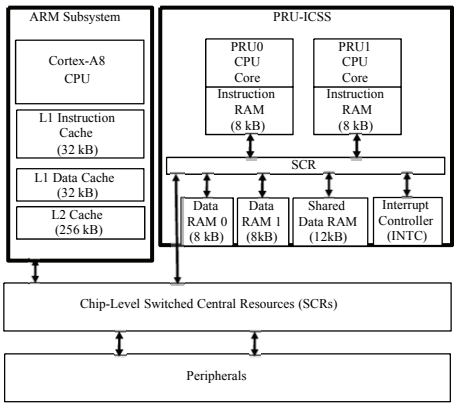


✓PRU-ICSS is used for slave industrial communication protocols such as Profibus, Profinet, Powerlink & Ethernet/IP

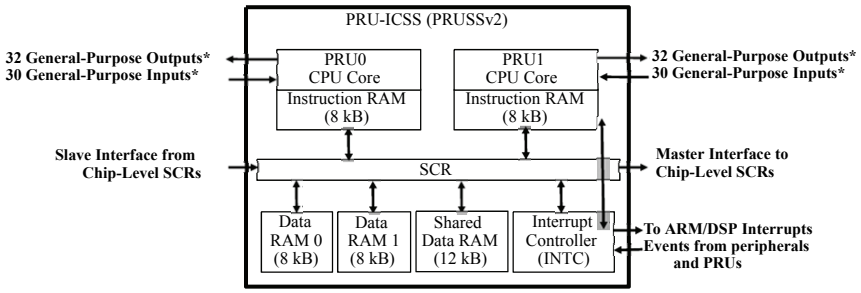
Package	15x15mm (ZCZ)	*13x13mm (ZCE)
ARM speed	Up to 1000 MHz	Up to 600 MHz
USB 2.0 OTG + PHY	x2	x1
EMAC	2-port switch	Single port

Chip-level Integration of the PRU-ICSS (PRUSSv2)

- ARM has access to PRU-ICSS memory
- PRU-ICSS has access to its own local memories and other chip-level memory resources and peripherals



PRU-ICSS (PRUSSv2) Block Diagram

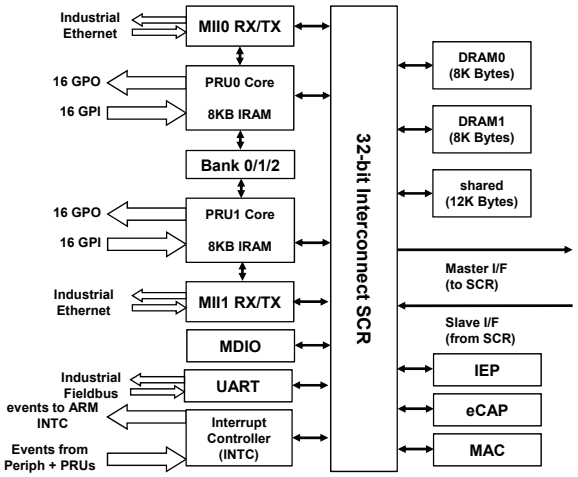


* On AM335x, only 15 General-Purpose Outputs and 16 General-Purpose Inputs are pinned out.

PRU-ICSS Subsystem

- Provides two independent programmable real-time (PRU) cores
  - 32-Bit Load/Store RISC architecture
  - no pipeline
  - 200MHz / 5ns
  - 8K Byte instruction RAM (2K instructions) per core
  - 8K Bytes data RAM per core
  - 12K Bytes shared RAM
- Includes Interrupt Controller for system event handling
- Fast I/O interface
  - 16 inputs and 16 outputs on external pins on AM335x via R30/R1
  - EDIO via IEP SYNC unit
- Power management via single PSC

PRUv2 Subsystem Functional Block Diagram



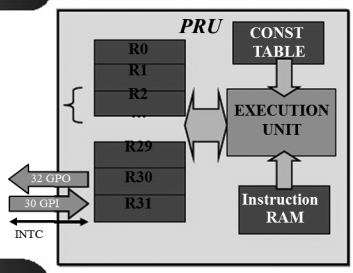
Enhancements in PRU-ICSS compared to Legacy PRUSS

- Memory
  - Additional data memory (8K Bytes vs 512 Bytes)
  - Additional instruction memory (8K Bytes vs 4K Bytes)
  - 12 KB Shared RAM
  - All memories within PRU-ICSS support parity
- PRU Resources
  - Enhanced GPIO (EGPIO), adding serial, parallel, and MII capture capabilities
  - Multiplier with optional accumulation (MAC)
  - Scratch pad (SPAD) with broadside interface
- Internal peripheral modules
  - UART
  - eCAP
  - MII_RT
  - MDIO
  - IEP
- Operating frequency
  - Legacy PRUSS: ½ CPU frequency
  - PRU-ICSS: 200 MHz

PRU Functional Block Diagram

General Purpose Registers
- All instructions are performed on registers and complete in a single cycle
- Register file appears as linear block for all register to memory operations

Constant Table
- Ease SW development by providing freq used constants
- Peripheral base addresses
- Few entries programmable



Execution Unit
- Logical, arithmetic, and flow control instructions
- Scalar, no Pipeline, Little Endian
- Register-to-register data flow
- Addressing modes: Ld Immediate & Ld/St to Mem

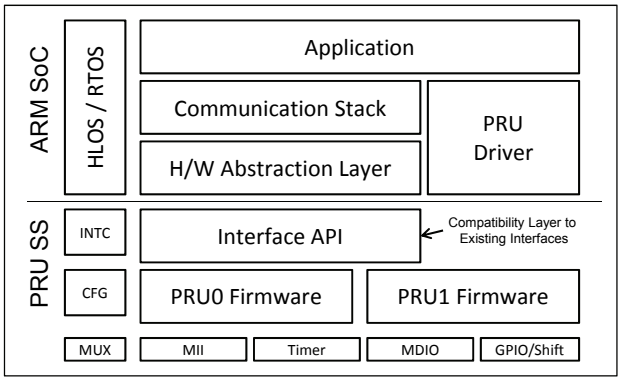
Special Registers (R30 and R31)
- R30
  - Write: 32 GPO (AM335x: 16 GPO pinned out)
- R31
  - Read: 30 GPI + 2 Host Int status (AM335x: 17 GPI pinned out)
  - Write: Generate INTC Event

Instruction RAM
- 8KB in size; 2K Instructions
- Can be updated with PRU reset

Agenda

- Introduction to the PRU Subsystem (PRU-ICSS on AM335x)
- Getting Started Programming
  - **PRU Assembler (PASM)**
  - PRU Development Support Integrated in CCS&C Compiler
  - Linux PRU Application Loader
- PRU Application
- Other Resources

Generic PRU Programming Model



PASM Overview

- PASM is a command-line assembler for the PRU cores
  - Converts PRU assembly source files to loadable binary data
  - Output format can be raw binary, C array (default), or hex
    - The C array can be loaded by host processor (ARM or DSP) to kick off PRU
  - Other debug formats also can be output
- Command line syntax:
  pasm_2 –V3 [-bcmldxz] SourceFile [-Dname=value] [-CArrayname]
- The PASM tool generates a single monolithic binary
  - No linking, no sections, no memory maps, etc.
  - Code image begins at start of IRAM (offset 0x0000)

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PRU Development Support Integrated in CCS

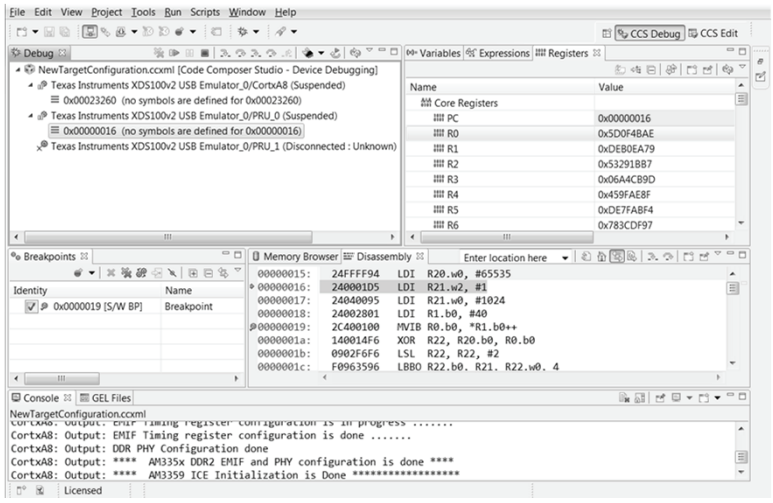
		CCS 5.x
pasm (PRU assembler)		No
AM335x PRU Debug Tools	Disassembly window	Yes
	Memory windows	Yes
	Register windows	Yes
	Execution controls	Yes
	Soft reset control	Yes
	Sleep control	Yes

Download the CCS 5.x here:
http://processors.wiki.ti.com/index.php/Download_CCS

Summary of PRU Debug Capabilities

- Disassembly window to show PRU assembly code
- Memory windows to show PRU program and data memory contents
  - Ability to load/fill memory contents
  - Ability to save memory contents
  - Ability to load PRU code binaries
- Register windows to show PRU subsystem control, data and status registers
  - View and modify PRU subsystem registers
- Execution controls
  - Run/Halt
  - Single-stepping through assembly instructions
  - Breakpoint control
- PRU soft reset control

Execution Control Screenshot



C Compiler

- Developed and maintained by TI CGT team
  - Remains very similar to other TI compilers
- Full support of C/C++
- Adds PRU-specific functionality
  - Can take advantage of PRU architectural features automatically
  - Contains several intrinsics
    - List can be found in Compiler documentation
- Full instruction-set Assembler for hand-tuned routines

TI PRU CGT Assembler vs PASM

- **Advantages of using TI PRU Assembler over PASM**
  - **The biggest advantage is that the TI PRU linker produces ELF files that enable source-level debugging within CCS. No more debugging in disassembly window!!**
  - **The TI PRU assembler uses the same shell as other TI compilers. Customers only need to learn one set of conventions, directives, etc.**
  - **TI PRU assembler will be maintained in the future, while PASM will not be updated anymore.**
  - **The TI PRU assembler uses the powerful TI linker which allows more flexibility then PASM and facilitates linking PRU programs with host CPU image for runtime loading and symbol sharing.**
- **Disadvantages of using TI PRU Assembler over PASM**
  - **Have to learn new directives if already used to PASM**
  - **TI PRU assembler requires more command line options and a linker command file.**
  - **Some porting effort required for reusing legacy PASM projects.**

There are some differences in the instructions and directives supported TI PRU Assembler versus PASM. Theses are listed in the TI PRU Compiler package release notes which is located at the root of the install folder.

TI PRU CGT Assembly vs C

- Advantages of coding in Assembly over C
  - Code can be tweaked to save every last cycle and byte of RAM
  - No need to rely on the compiler to make code deterministic
  - Easily make use of scratchpad
- Advantages of coding in C over Assembly
  - More code reusability
  - Can directly leverage kernel headers for interaction with kernel drivers
  - Optimizer is extremely intelligent at optimizing routines
    - "Accelerating" math via MAC unit, implementing LOOP instruction, etc.
  - Not mutually exclusive - inline Assembly can be easily added to a C project

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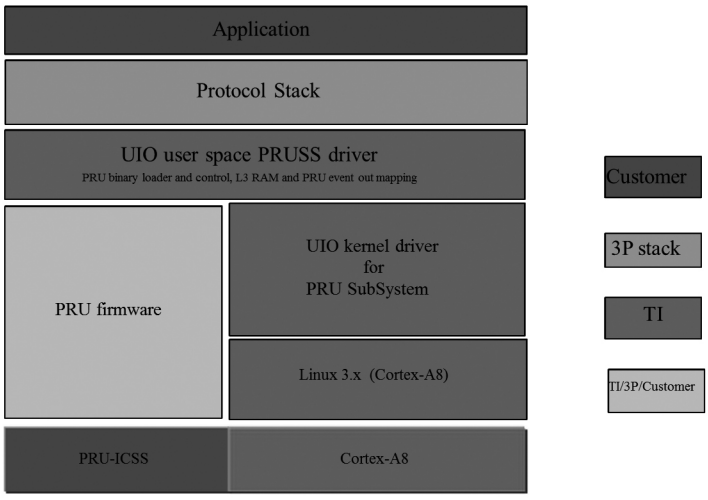
- PRU Application
- Other Resources

PRU Linux Loader

- Host processor of SoC must load code to a PRU and initiate its execution
- ARM processor can load code to PRU instruction memory and interact with PRU from user space using the application loader
- Application loader is available in open-source
- Application PRU Loader
  - API's allow ARM to interact with PRU in user space
  - Supports BSD licensing
  - Can be used for protocol emulation and user space applications

Application Loader S/W Architecture



Application Loader Examples

AM1808 SDK

- AM335x PRU package includes several basic PRU application example code. These examples use the Linux application loader.
  - Additional PRU examples can be found in the AM1808 SDK.
  - The AM18x PRUSS to AM335x PRU-ICSS Software Migration Guide provides reference of how these examples can be ported to AM335x.
- PRU example code demonstrates:
  - Memory transfers
  - Accessing constant tables *
  - Interrupts
  - Toggling GPIOs *
  - eDMA configuration *
- AM1808 SDK can be downloaded at:
  http://software-dl.ti.com/dsps/dsps_public_sw/sdo_sb/targetcontent/sdk/AM1x/latest/index_FDS.html

* Only included in AM1808 examples.

Steps to use develop code

- To Use,
  - Build UIO kernel driver as module
  - Build User space API's, link to application code
  - Compile application code using API
  - Compile PRU binaries using PASM
  - On file system, install UIO kernel driver, application executables, PRU binaries

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PRU (Programmable Real-time Unit) For Configurable Logic
Enabling real-time Ethernet** Slave **communications

Architecture

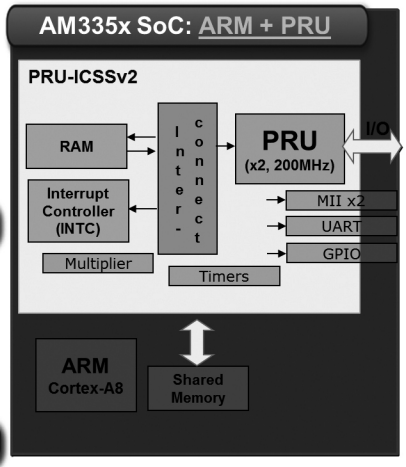
- Real-time oriented – 100% Deterministic
- Two 32-bit RISC cores for real-time functions each running at 200MHz
- 8KB IRAM, 8KB DRAM, 12KB Shared RAM
- Single-cycle execution & Direct I/O interface sampling at ~5ns
- Very easy to program
- Logic, Control and arithmetic instructions
- 32-bit MULT and Interrupt controller

Capabilities

- Implement Real-time communication interfaces : PROFIBUS, EtherCAT, PROFINET & Ethernet/IP
- Implement custom IP (such as EnDAT 2.2, SINC3 decimation, PWMs, DP Memory, Manchester Coding, 9 bit UART or a Backplane bus)

Advantages

- Easy to program & completely Flexible
- Reduce system cost & complexity



Popular Industrial Communication Protocols

Preliminary – Future dates are Subject to change

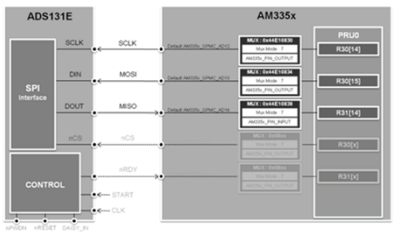
Protocol	Configuration	SW Availability	3rd party Stack Partners
Profibus	Slave (AM1810 & AM335x)	SDK Release (AM1810): Now Certification (AM1810): Now GA SDK release (AM335x) – Now	TMG
EtherCAT	Slave only (AM335x)	Beta SDK release – Now GA SDK Release – Now Certification: Now	ETG Koenig, Acontis, Port
Ethernet/IP (w/ Gb switch)	Slave only (AM335x)	EA SDK Release: Now Certification: 2Q14 GA SDK Release: 3Q14	Molex
Ethernet/IP (w/ PRU)	Slave only (AM335x)	EA SDK Release: Now Certification: 2Q14 GA SDK Release: 3Q14	Molex
PROFINET-RT/IRT	Slave only (AM335x)	EA SDK Release: NOW Certification: NOW; 2Q14 (IRT) GA SDK release: 3Q14	Molex
OpenMAC for Powerlink	Slave only (AM335x)	Available from 3P (Port)	Port
Sercos-3	Slave Only (AM335x)	Available from 3P (Automata)	Automata
IEC61850	Client/Server (AM335x)	Available from 3P (TriangleMicroWorks)	TMW

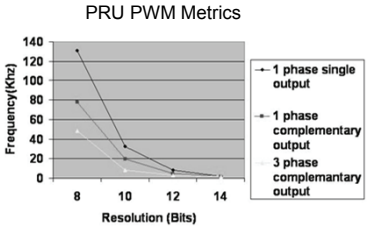
SDK: Software Development Kit

TEXAS INSTRUMENTS

PRU – Simple Coding Examples

Project	Scale	Comment
SPI Interface with ADS131E0	Scale up to 8 SPIs	eliminates 4 x STM32
3 Phase PWM	8 kHz compl 3 phase	overcome pin-mux
SINC3 Filter for Sigma Delta Modulator	2 channel 10MHz	
Soft-UART	up to 115200 baud	Two full duplex Soft-UARTS per PRU





TEXAS INSTRUMENTS

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- **Other Resources**

PRU-ICSS Documentation and Resources

- CCS External Download at
  http://processors.wiki.ti.com/index.php/Download_CCS
- AM335x PRU-ICSS Documentation is available in the
  AM335x PRU-ICSS package

Backup

IA-SDK Links

- Download:
  - http://www.ti.com/tool/sysbiossdk-ind-sitara
- **Getting Started Guide** (generic):
  - http://processors.wiki.ti.com/index.php/AM335x_SYSBIOS_Industrial_SDK_Getting_Started_Guide
- **Release Notes** (release dependent):
  - http://processors.wiki.ti.com/index.php/AM335x_SYSBIOS_Industrial_SDK_01.00.00.08_Release_Notes
- **User Guide** (release dependent):
  - http://processors.wiki.ti.com/index.php/AM335x_SYSBIOS_Industrial_SDK_01.00.00.08_User_Guide
- Default install path:

  <drive>:/ti/am335x_sysbios_ind_sdk_x.x.x.x
  - Should be aligned with CCS and Sys/Bios paths

Communication Slave Architecture

TI Software

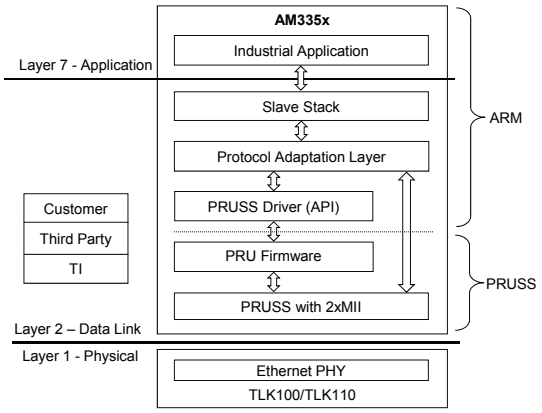
- SYS/BIOS based IA-SDK
- Starterware device drivers
- Protocol adaptation layer
- PRU-ICSS firmware implementing commuication protocol HW layer

Third Party Software

- Slave stack source code

Customer Software

- Industrial Application
- Sample application provided by TI



Example: EtherCAT Slave

TI Software

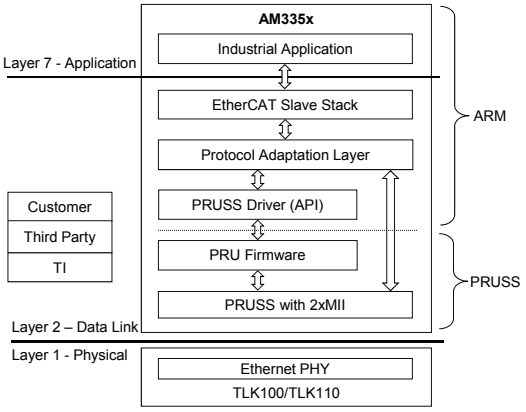
- SYS/BIOS based SDK
- Sitaraware device drivers
- Protocol adaptation layer for EtherCAT
- PRUSS EtherCAT firmware

Third Party Software

- Fully validated evaluation version of Beckoff Slave stack included in Software Development Kit
- Free production license for ETG members (ETG membership is free)
- Compatible with other third party EtherCAT stacks

Customer Software

- Industrial Application
- Sample application provided by TI



IA-SDK contents

[docs]	- main documentation
[drivers]	- PRUSS, LED, MMU and UART drivers for ICS/IDK
[examples]	
…[ethercat_slave]	- EtherCAT example (to be used with SSC)
…[powerlink_slave]	
…[profibus_slave]	
…[uartecho]	
[platform]	- generic AM335x drivers (based on Starterware)
[protocols]	- PRU firmware and API libs
…[EtherCAT_slave]	
…[Powerlink_slave]	
[starterware]	- base SoC code, drivers and tools
[tools]	- GEL, post build and FLASH tools

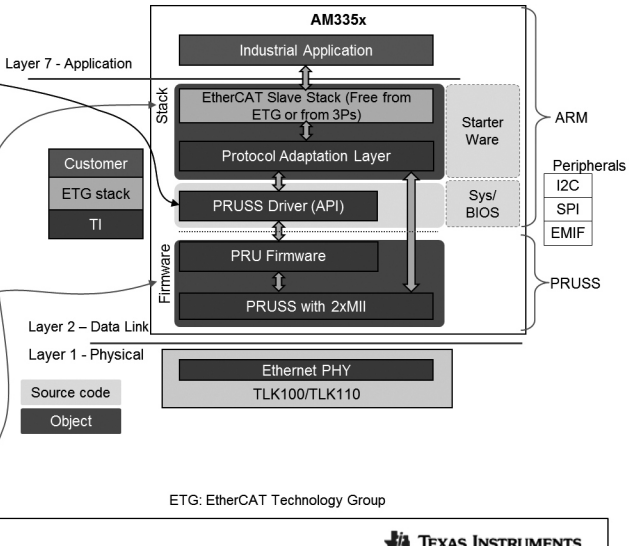
EtherCAT Protocol

[docs]	- EtherCAT Firmware/API docs
[firmware]	- PRUSS binary as header files for PRUSS driver usage
[ecat_appl]	- EtherCAT example to be patched on SSC 5.0.1 sources
[include]	- header files for EtherCAT slave controller (ESC) API and Slave Sample Code
[stack]	- pre-compiled library of Beckhoff SSC (proprietary sw)

- SSC source code is available for free from Beckhoff for all ETG members.
- SSC source required to modify stack options and/or change EtherCAT application
- Future IA-SDK to be based on latest SSC release at the time

IA-SDK File Structure

```
|--- sdk
|   |--- docs
|       |---AM335x Industrial SDK User G
|       |---AM335x Industrial SDK Releas
|       |---AM335x Industrial SDK Gettin
|   |--- drivers
|       |--- include
|       |--- lib
|       |--- src
|   |--- examples
|       |--- ethercat
|       |--- i2c_led
|       |--- uart_echo
|    |--- platform
|       |--- am335x
|           |--- evmam335x
|               |--- include
|               |--- lib
|               |--- src
|   |--- protocols
|       |--- ethercat
|           |--- docs
|           |--- firmware
|           |--- include
|           |--- stack
```



ETG: EtherCAT Technology Group