

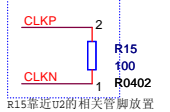
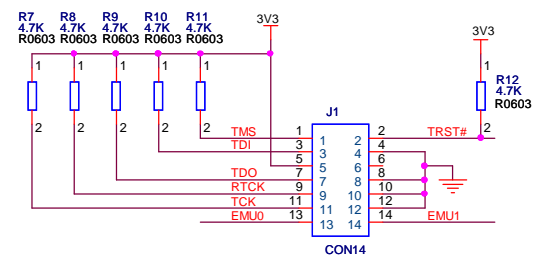
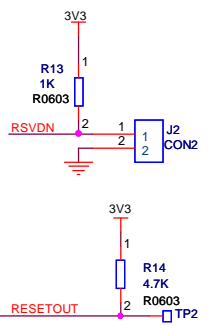
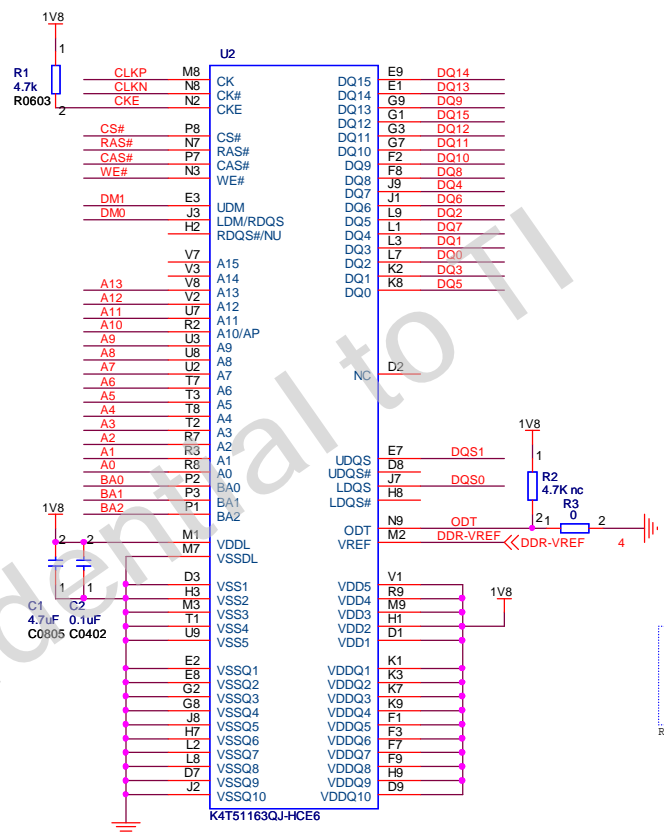
Note5
其它信号请参考SPRS710A文档
5.11.3.3--5.11.3.12

Note1
DDR2数据线需要作等长控制

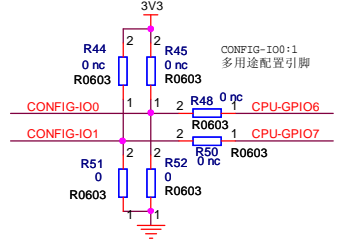
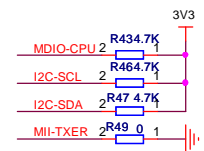
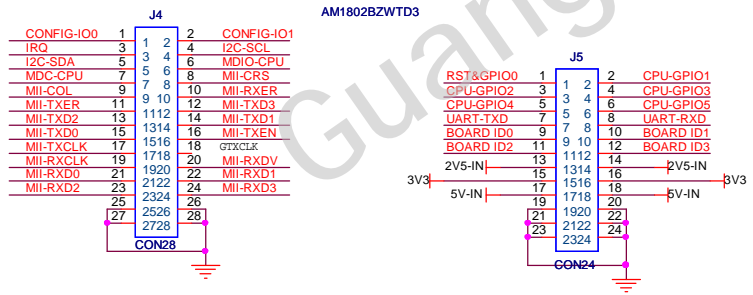
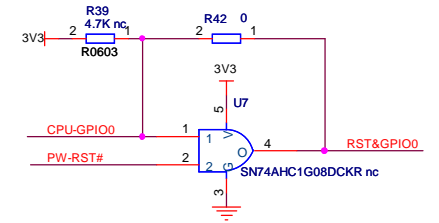
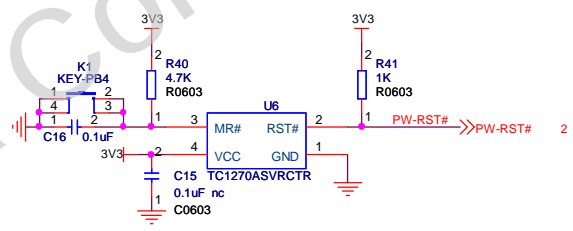
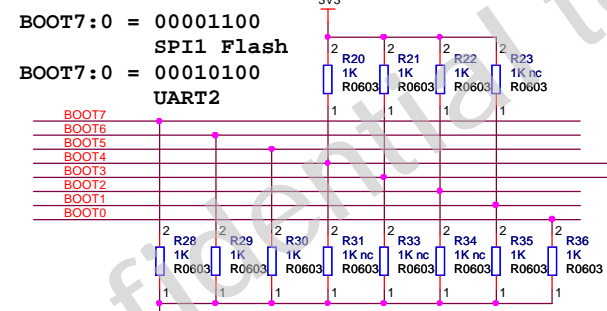
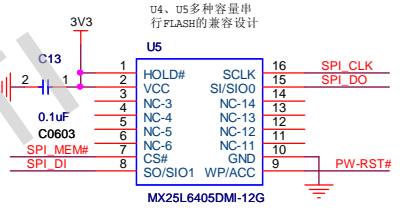
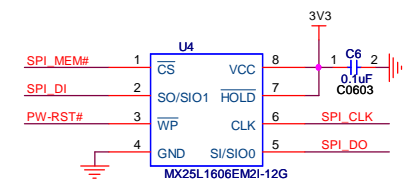
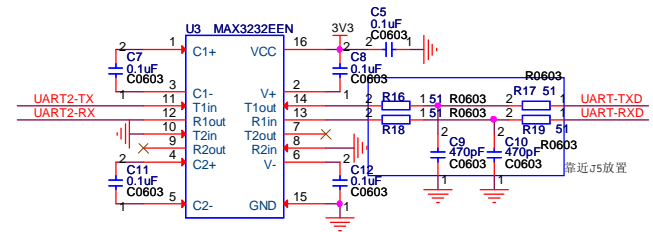
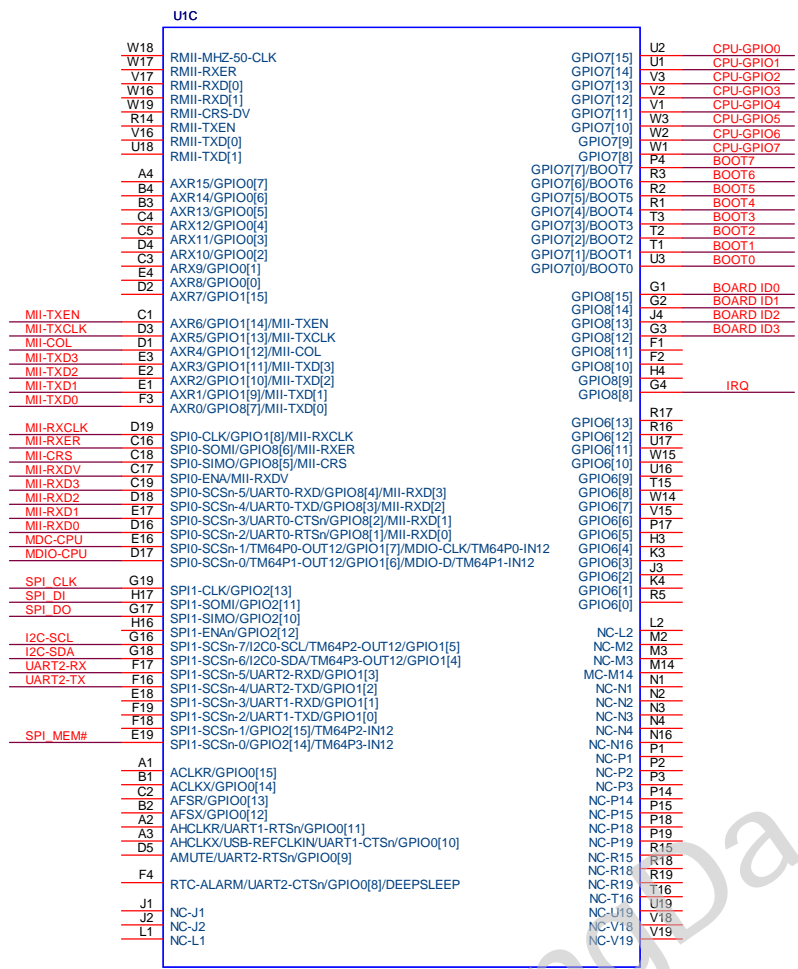
Note2
差分信号，信号线长度尽可能与数据线等长

Note3
信号线长度尽可能与数据线等长

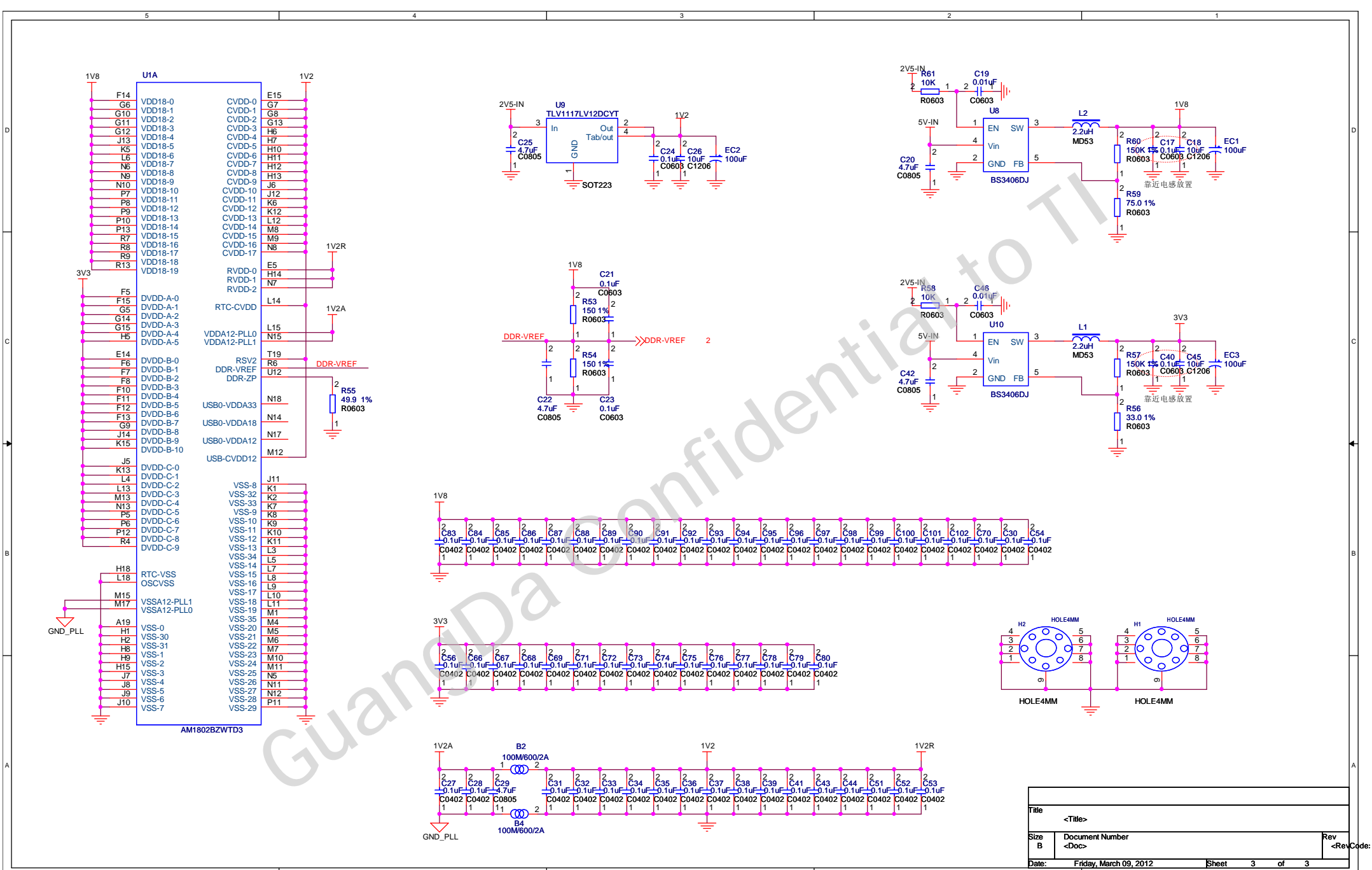
Note4
DDR-DQGATE-0、DDR-DQGATE-1 二信号线需要作等长控制，同时二信号需要与DDR2数据线等长。



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