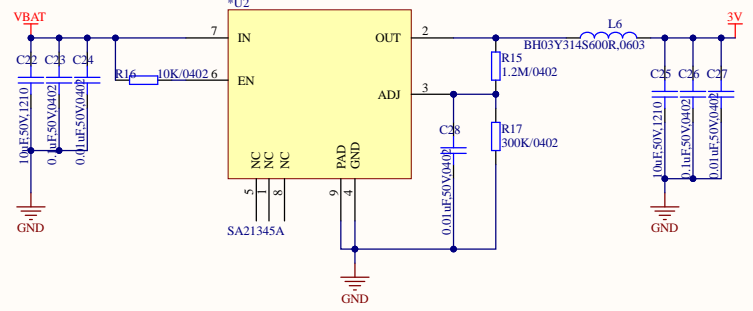
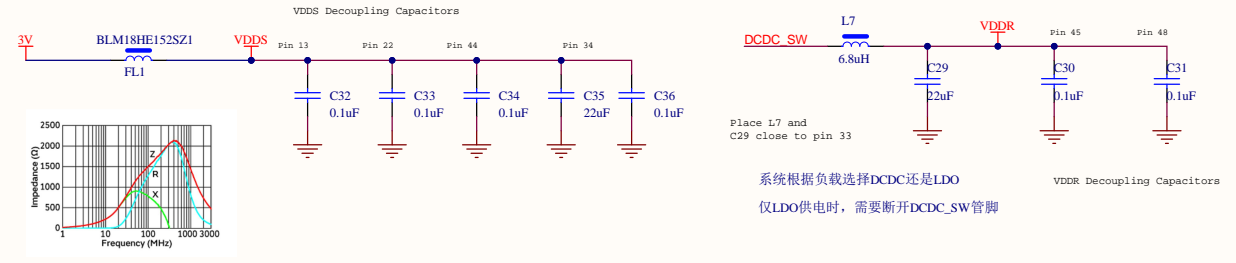


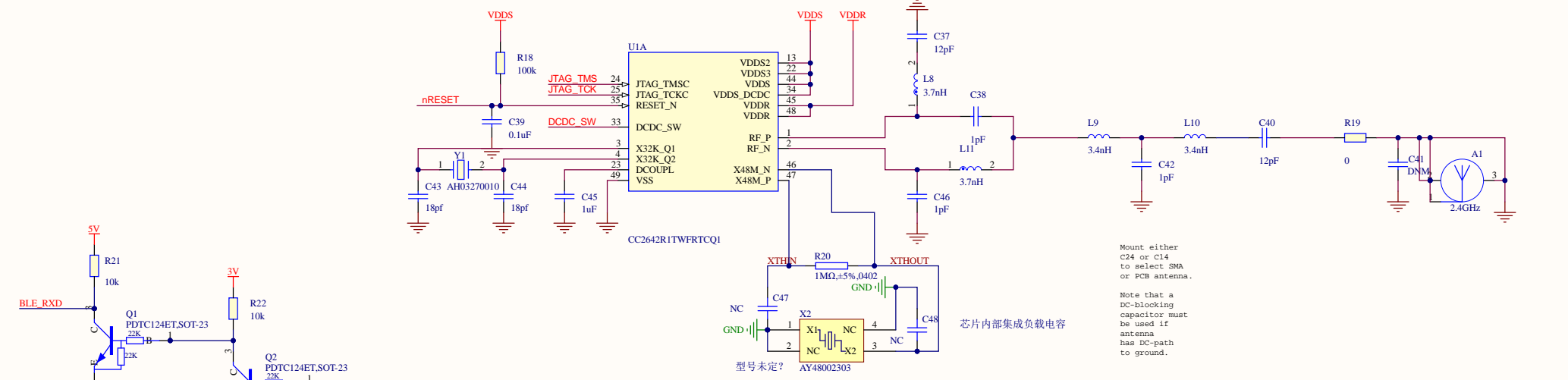
3V输出



VDDS, VDDR设计

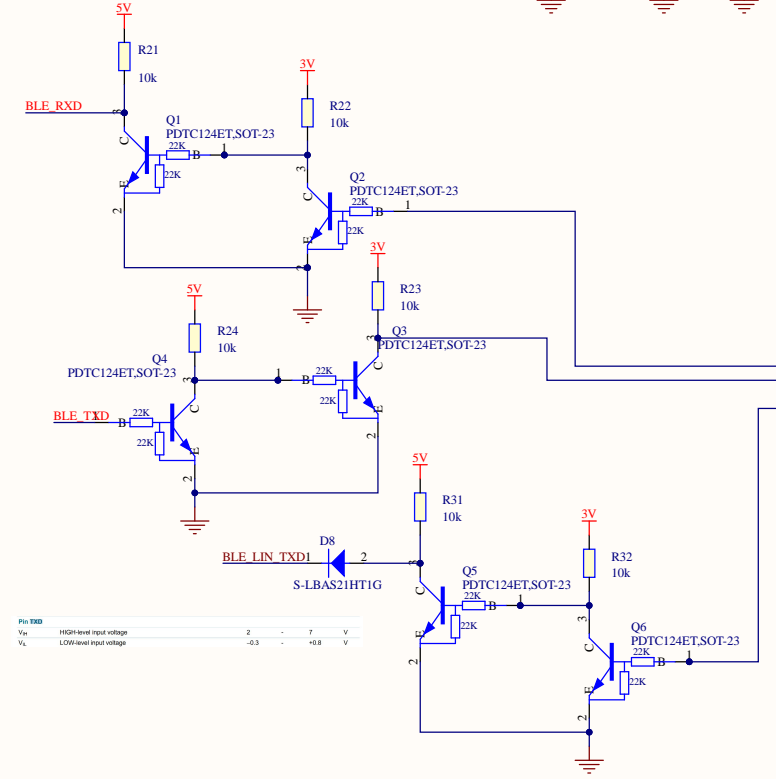


系统根据负载选择DCDC还是LDO
仅LDO供电时，需要断开DCDC_SW管脚



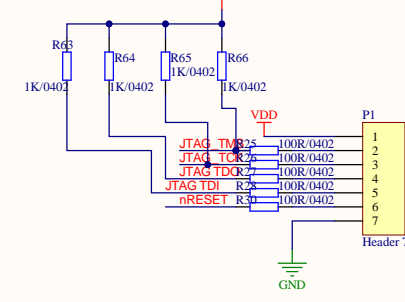
Mount either C24 or C14 to select SMA or PCB antenna.
Note that a DC-blocking capacitor must be used if antenna has DC-path to ground.

芯片内部集成负载电容



V _{IO_TXD}	HIGH-level input voltage	2	7	V
V _{IO}	LOW-level input voltage	-0.3	+0.8	V

JTAG下载电路



Title		
Size	Number	Revision
A3		
Date:	11/09/2022	Sheet of
File:	D:\I\工作\BLE\PCB_Project\BLE_SchDown By:	

