AFE77xx: RX & TX DSA Gain/Phase Calibration

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RX DSA – Gain/Phase Calibration

- The RX DSA Gain/Phase Calibration has two modes of operation.
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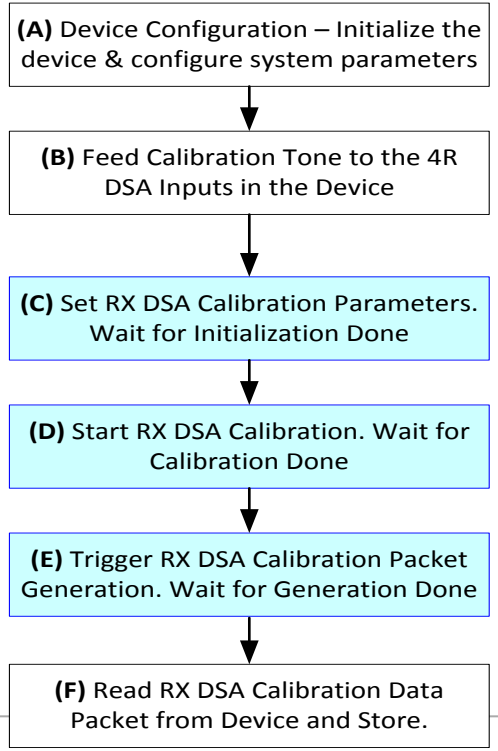
- Gain/Phase Calibration Mode: The calibration mode operation is performed once for each device, as part of factory calibration.
  - During the calibration mode, test tones are injected to enable the device to estimate the gain and phase error as a function of the RX DSA gain steps.
  - The gain/phase parameters are computed for the RX DSAs in each of the 4 receivers.
  - The estimated gain/phase parameters are to be read by the host and stored in a non-volatile memory.
- Calibration Packet Load Mode: The calibration packet load mode operation is performed once during every power up.
  - During the calibration packet load mode, the gain/phase parameters stored by the host in a non-volatile memory are configured in to the device.
  - The configured parameters are used, internally in the device, to compensate for gain/phase errors as the RX DSA gain steps are changed during normal operation.

RX DSA – Calibration Mode

- Requirement on the Test Tone:
  - The tone frequency should be selected to be in the desired band of operation, i.e., should be within about ±40% of interface rate (e.g., ±100 MHz for 245.76 MSPS).
  - The input tone frequency should be an integer multiple of fs/256, where “fs” is the ADC sampling rate.
  - There should be no frequency error between the reference clock provided to the source generating the test tone & AFE77xx. Hence, the references should be tied together.
  - The tone level at the input of the device should nominally be around -16 dBm.
  - One test tone should be injected in the band of interest.
  - The test tone can be simultaneously injected to all the receivers with the same band of interest.
    - For instance, if the receiver frequency in the two sets of 2R (in a 4T4R) would be configured to the same frequency band, then the same test tone can be simultaneously injected to all 4R.
- Calibration Mode Configuration
  - The specific frequency band of interest for the DSA and the decimation factor (e.g., interface rate) need to be used during the calibration mode.
  - After calibration, the gain/phase error parameters are expected to hold only for the frequency band of interest.

RX DSA – Calibration Flowchart (1)

- The RX DSA calibration mode flowchart is illustrated.
  - Additional details on the states of the flowchart are provided in the following slides.



Macro command – Check for status/error [Status register]

RX DSA – Calibration Flowchart (2)

- State A: The device is brought out of reset by setting the appropriate SPI registers. The device needs to be configured in to the appropriate state with the desired system parameters (LO frequency, interface rate, etc.)

- State B: The calibration tone corresponding to desired frequency band is to be fed to all the 4R inputs in the device.

- State C: The initialization parameters for RX DSA calibration needs to be programmed.
  - An SPI register bit indicating initialization done (“Macro done”) event needs to be monitored. When the “Macro done” bit is 1 proceed to State D.

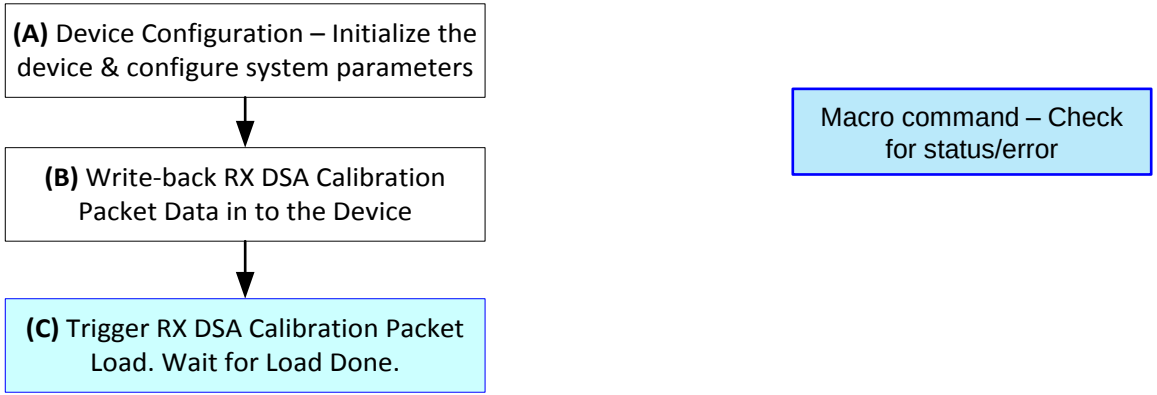
RX DSA – Calibration Flowchart (3)

- State D: The appropriate set of SPI registers corresponding to the RX DSA calibration macro needs to be programmed to start the RX DSA calibration procedure.
  - An SPI register bit indicating calibration done (“Macro done”) event needs to be monitored. When this bit is 1, check the Error bit.
  - Read the Error bit in the status byte. If it is 1, then record the ‘Error_Status’. [Status register]
    - Take appropriate action based on the ‘Error_Status’ (e.g., Signal power too low, Tone frequency incorrect, etc.) and then repeat the step to start RX DSA calibration (State D).
  - Otherwise, proceed to State E.

- State E: Trigger the generation of the RX DSA gain/phase calibration packet with SPI writes
  - An SPI register bit indicating packet generation done (“Macro done”) event needs to be monitored. When this bit is 1, check the Error bit.
  - Read the Error bit in the status byte. If it is 1, then record the ‘Error_Status’. [Status register]
    - In case the ‘Error_Status’ indicates an error, then exit to an “Error State” and record error status indicators. If no error, then proceed to State F.

- State F: Read the RX DSA calibration data packet from the device and store it in non-volatile memory.

RX DSA – Calibration Packet Load Mode



- State A: The device is brought out of reset by setting the appropriate SPI digital registers. The device needs to be configured in to the appropriate state with the desired system parameters (LO frequency, interface rate, etc.)
- State B: Write-back RX DSA calibration data, stored in a non-volatile memory, in to device.
- State C: Trigger (by SPI writes) load of RX DSA gain/phase calibration packet.
  - Monitor the “Macro done” bit in the Status byte [Status register]. When this bit is 1 proceed to the next step.
  - Read the “Error bit” in the status byte. If it is 1, then record the “Extended error code”
    - If the Extended error code indicates that the packet is corrupted, ensure that the packet is written correctly to the device.
    - Otherwise the calibration packet load mode is complete.

TX DSA – Gain/Phase Calibration

- The TX DSA Gain/Phase Calibration has two modes of operation.
  1. Gain/Phase Calibration Mode
  2. Calibration Packet Load Mode

- Gain/Phase Calibration Mode: The calibration mode operation is performed once for each device, as part of factory calibration.
  - During the calibration mode, a test tone is transmitted and looped-back to enable the device to estimate the gain and phase error as a function of the TX DSA gain steps.
  - The gain/phase parameters are computed for the TX DSA in each of the 4 transmitters.
  - Estimated gain/phase parameters are to be read by the host and stored in a non-volatile memory.

- Calibration Packet Load Mode: The calibration packet load mode operation is performed once during every power up.
  - During the calibration packet load mode, the gain/phase parameters stored by the host in a non-volatile memory are configured in to the device.
  - The configured parameters are used, internally in the device, to compensate for gain/phase errors as the RX DSA gain steps are changed during normal operation.

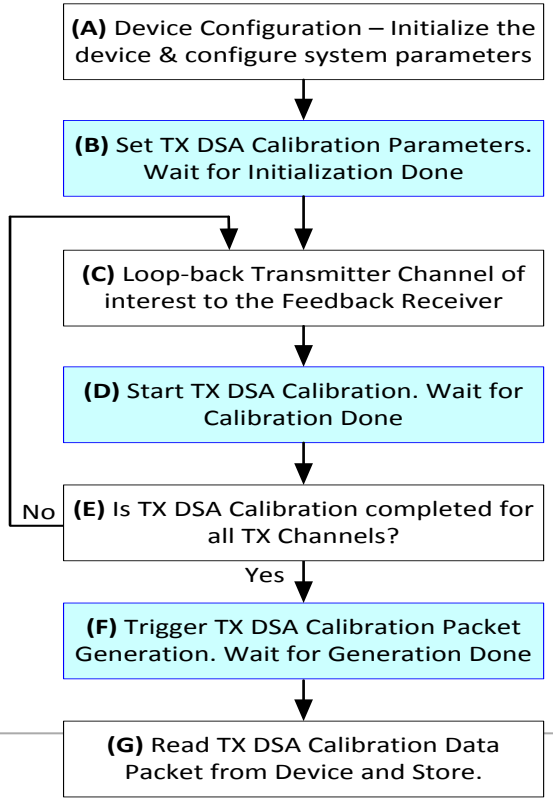
TX DSA – Calibration Mode

- <u>Requirement on TX Loop-back Configuration to FB Receiver:</u>
  - The test signal would be generated internally within the device from each of the transmitters.
  - The host needs to connect the transmit channel for which DSA gain/phase calibration needs to be performed to the feedback channel. This information needs to be provided to the device.
  - The TX DSA gain/phase calibration would be performed sequentially for each of the transmitters.

- Calibration Mode Configuration
  - The specific frequency band of interest for the TX DSA and the interpolation factor (e.g., correct interface rate) need to be used during the calibration mode.
  - After calibration, the gain/phase error parameters are expected to hold only for the frequency band of interest.

TX DSA – Calibration Flowchart (1)

- The TX DSA calibration mode flowchart is illustrated.
  - Additional details on the states of the flowchart are provided in the following slides.



Macro command – Check for status/error

TX DSA – Calibration Flowchart (2)

- State A: The device is brought out of reset by setting the appropriate SPI registers. The device needs to be configured in to the appropriate state with the desired system parameters (LO frequency, interface rate, etc.)

- State B: The initialization parameters for TX DSA calibration needs to be programmed.
  - An SPI register bit indicating initialization done (“Macro done”) event needs to be monitored. If the “Macro done” bit is 1, then proceed to State C.

- State C: The transmitter channel of interest needs to be looped back to the appropriate feed-back channel.

- State D: The appropriate set of SPI registers corresponding to the TX DSA calibration macro needs to be programmed to start the TX DSA calibration procedure.
  - An SPI register bit indicating calibration done (“Macro done”) event needs to be monitored. If this bit is 1, check the Error bit.
  - Read the Error bit in the status byte. If it is 1, then record the ‘Error_Status’. [Status register]
    - Take appropriate action based on the ‘Error_Status’ (e.g., Signal power too low, Signal power too high, etc.) and then repeat the step to start TX DSA calibration (State D). Otherwise, proceed to State E.

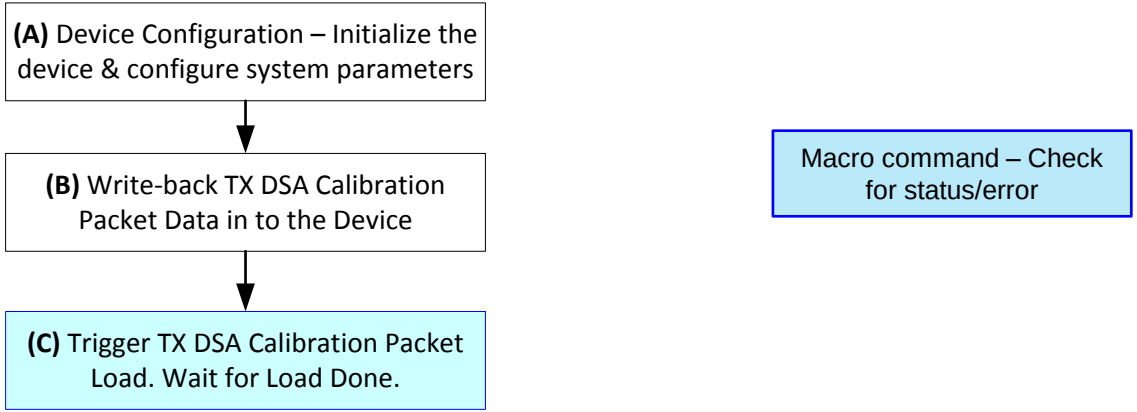
TX DSA – Calibration Flowchart (3)

- State E: Check if TX DSA gain/phase calibration has been completed for all TX channels. If yes, the proceed to State F. Otherwise, proceed to State C.

- State F: Program appropriate SPI registers to trigger the generation of the TX DSA gain/phase calibration packet.
  - An SPI register bit indicating packet generation done (“Macro done”) event needs to be monitored. If this bit is 1, check the Error bit.
  - Read the Error bit in the status byte. If it is 1, then record the ‘Error_Status’. [Status register]
    - In case the ‘Error_Status’ indicates an error, then exit to an “Error State” and record error status indicators. If no error is indicated, then proceed to State G.

- State G: Read the TX DSA calibration data packet from the device and store it in non-volatile memory.

TX DSA – Calibration Packet Load Mode



- State A: The device is brought out of reset by setting the appropriate SPI digital registers. The device needs to be configured in to the appropriate state with the desired system parameters (LO frequency, interface rate, etc.)
- State B: Write-back TX DSA calibration data, stored in a non-volatile memory, in to device.
- State C: Trigger (by SPI writes) load of TX DSA gain/phase calibration packet.
  - Monitor the “Macro done” bit in the Status byte [Status register]. When this bit is 1 proceed to the next step.
  - Read the “Error bit” in the status byte. If it is 1, then record the “Extended error code”
    - If the Extended error code indicates that the packet is corrupted, ensure that the packet is written correctly to the device.
    - Otherwise the calibration packet load mode is complete.

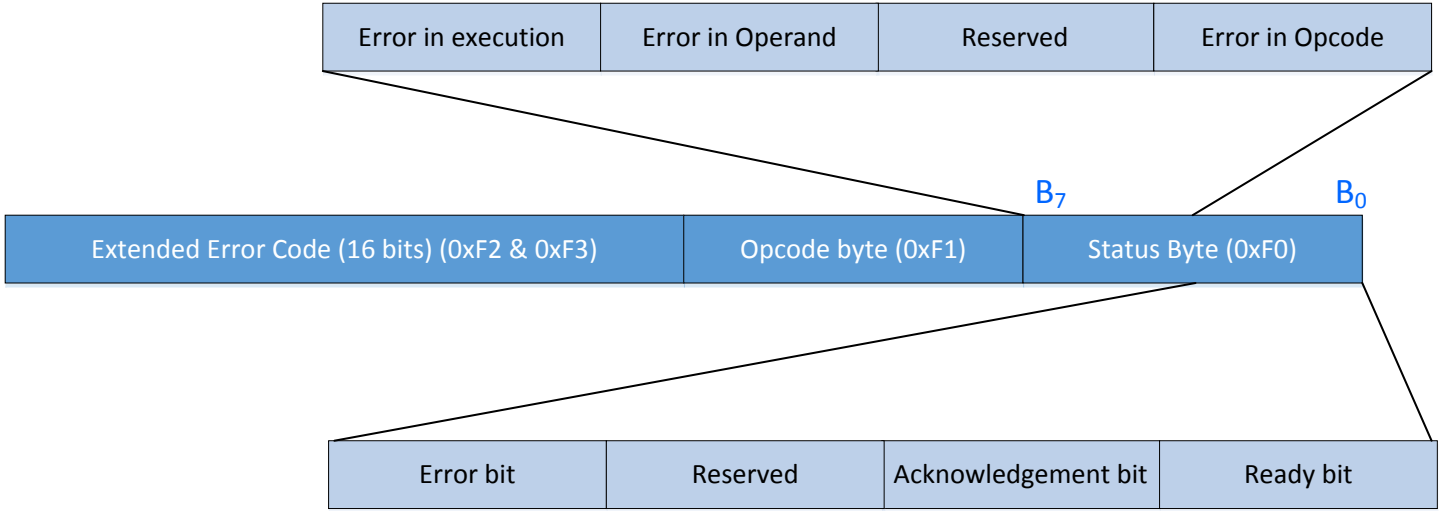
RX & TX DSA Calibration Data Packet Size

- RX DSA Calibration Packet: The size of the data packet that needs to be stored for the RX DSA calibration depends on whether it also needs to handle external LNA or not.
  - RX DSA only: 987 bytes for 4 RX channels.
  - RX DSA & External LNA: 1019 bytes for 4 RX channels.

- TX DSA Calibration Packet: The size of the data packet that needs to be stored for the TX DSA calibration is 712 bytes for 4 TX channels.

Status register description (1/2)

- AFE77xx status register can be used to determine
  - If device is ready to take a macro command
  - Execution state of the previously issued macro command
- Status register is 4 bytes long (0xF0 to 0xF3 in the customer macro page)



Status register description (2/2)

- First byte consists of 6 status & error indicator bits
  - Ready Bit – AFE77xx is ready for a macro
  - Acknowledgement Bit – AFE77xx has acknowledged the recently issued macro
  - Reserved bit
  - Error bit – Recently exceuted macro command encountered an error
  - If Error bit is set –the following bits indicate the type of error
    - Next 4 bits are interpreted as follows
      - Error In opcode – Opcode not supported. Check the opcode
        - » Read byte at address 0xF1 and compare with the opcode from document
      - Reserved bit
      - Error in Operand – Operands are in error. Check the operands.
      - Error in execution bit
        - » If error in execution bit is set, read the extended error code (bytes 0xF2 and 0xF3) and check against the table

Extended error information (1/2)

Opcode = 0x12	Extended error code	Cause / debug information
Factory Calibration data load step	0x0	Packet was applied correctly
	0x1	Operands are wrong
	0xB	DSA packet corrupted

Opcode = 0x41	Extended error code	Cause / debug information
Factory calibration: Initialization step	0x0	Initialization was successful

Opcode = 0x41	Extended error code	Cause / debug information
Factory Calibration :	0x0	Calibration step was successful.
Calibration step	0x1	Calibration operand is wrong
	0x2	RX DSA reliability condition is hit -- High signal power
	0x3	Calibration tone frequency is out of band (±40% of interface rate)
	0x4	Signal Power level is too low for calibration
	0x5	For internal debug only. Not expected to happen
	0x6	Internal module error. Not expected to happen
	0x7	Internal signal overflow happened or TDD toggle error
	0x8	Either tone is not an integer multiple of fs/256 or spur level is too high

Extended error information (2/2)

Opcode = 0x41	Extended error code	Cause / debug information
Factory Calibration : Packet generation step.	0x0	DSA packet generation successful
	0x9	In DSA calibration gain error observed is higher than threshold (±2 dB) Check for tone coherency.
	0xA	DVGA Gain is higher than expected range (40 dB)
	0xC	In DSA calibration phase error s observed is higher than threshold (typically, 40°)