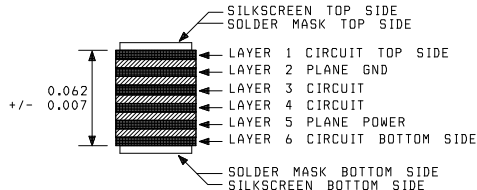


- NOTE:
1. MATERIAL SELECTION:
6 LAYER, EPOXY GLASS, NEMA GRADE FR-4, 0.062 +/- 0.007 THICK,
1 1/2 OZ. FINAL COPPER EXTERNAL LAYERS, 1/2 OUNCE INTERNAL.
SOLDERABLE SURFACES TO BE ENIG (ELECTROLESS NICKEL IMMERSION GOLD).
 2. SOLDER RESIST: THE USE OF SOLDER RESIST COATING SHALL BE IN
ACCORDANCE WITH THE REQUIREMENTS OF IPC-SM-840. ALL SOLDERABLE
SURFACES ARE TO BE FREE OF SOLDER RESIST. COLOR - GREEN.
USE LIQUID PHOTOIMAGEABLE RESIST.
 3. SILKSCREEN: USE WHITE NON-CONDUCTIVE INK. ALL COMPONENT AND
TESTPOINT LANDS ARE TO BE FREE OF INK.
 4. MANUFACTURER'S IDENTIFICATION: ADD IN ETCH OR TO SILKSCREEN.
 5. ELECTRICAL BARE BOARD TEST REQUIRED.
 6. DRILL SIZES ARE FINISHED SIZE AFTER PLATING.
 7. FABRICATE TO MEET EU RoHS DIRECTIVE.
 8. BOARD SHALL MEET THE REQUIREMENTS OF UL796
WITH A FLAMMABILITY RATING OF 94V-0.
 9. BOARD VENDOR MAY REMOVE THERMALS FOR VIA'S ON PLANE LAYERS.
 10. BOARD VENDOR MAY REMOVE NON FUNCTIONAL PADS ON INNER LAYERS.
 11. BOARD VENDOR MAY ADD TEAR SHAPING TO INNER LAYERS.
BOARD VENDOR TO ADD TEAR SHAPING TO OUTER LAYERS.
 12. BOARD TO BE SCORED AT DESIGNATED LINE. SCORING TO BE 30 DEG.
AND A MINIMUM OF 0.015 INCHES BOARD MATERIAL IN CHANNEL.
 13. THIEVING STRUCTURES MAY BE ADDED TO COMPENSATE FOR VARIATIONS
IN COPPER DENSITIES ACROSS THE PWB. SPACING BETWEEN THIEVING AND
CONDUCTIVE PATTERN TO BE 0.020" MINIMUM.
 14. 0.0048", 0.0049", and 0.005" WIDE TRACES TO BE IMPEDANCE CONTROLLED.
50 OHM +/-10% SINGLE ENDED 0.005" TRACE WIDTH.
90 OHM +/-10% DIFFERENTIAL (0.0048" TRACE WIDTH)
100 OHM +/-10% DIFFERENTIAL (0.0049" TRACE WIDTH)

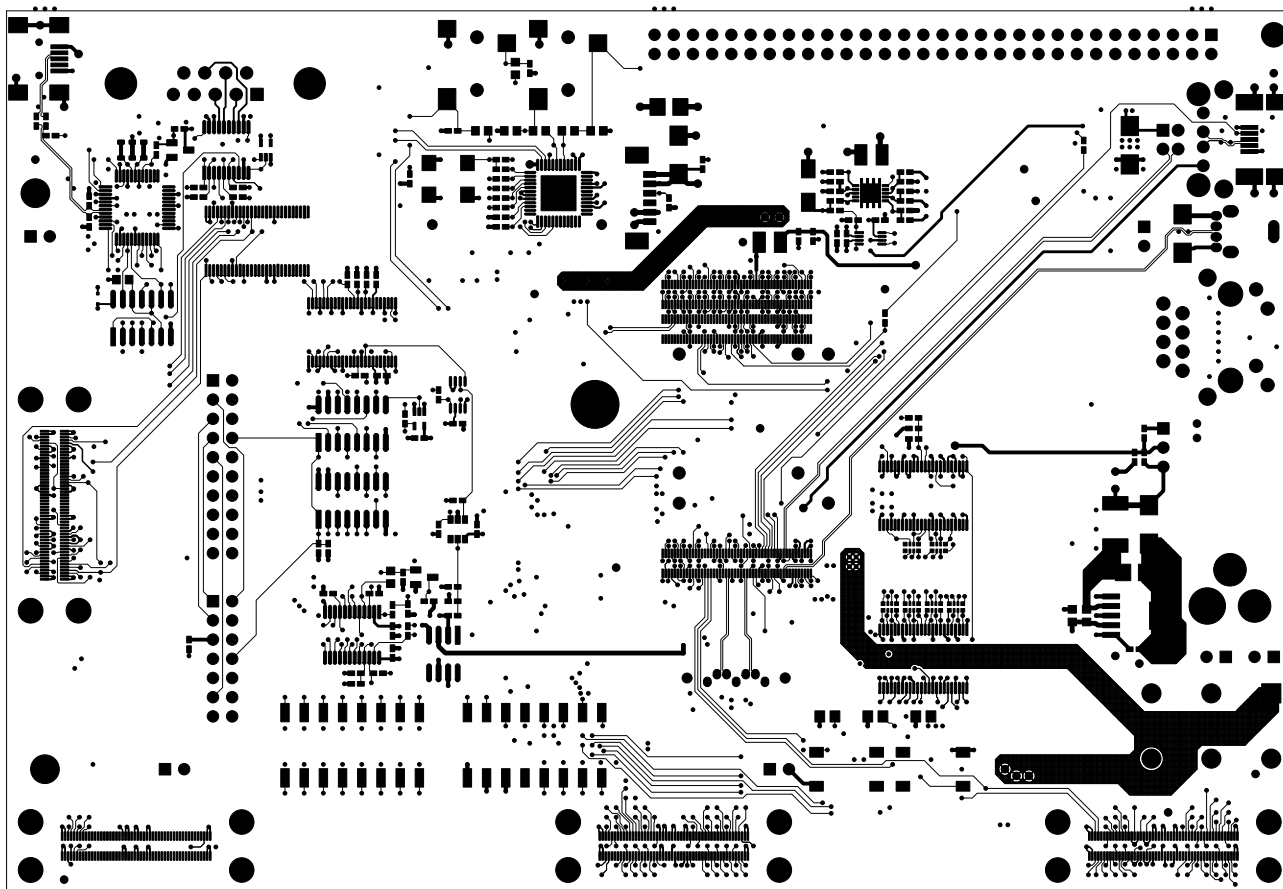


6 LAYER STACK-UP

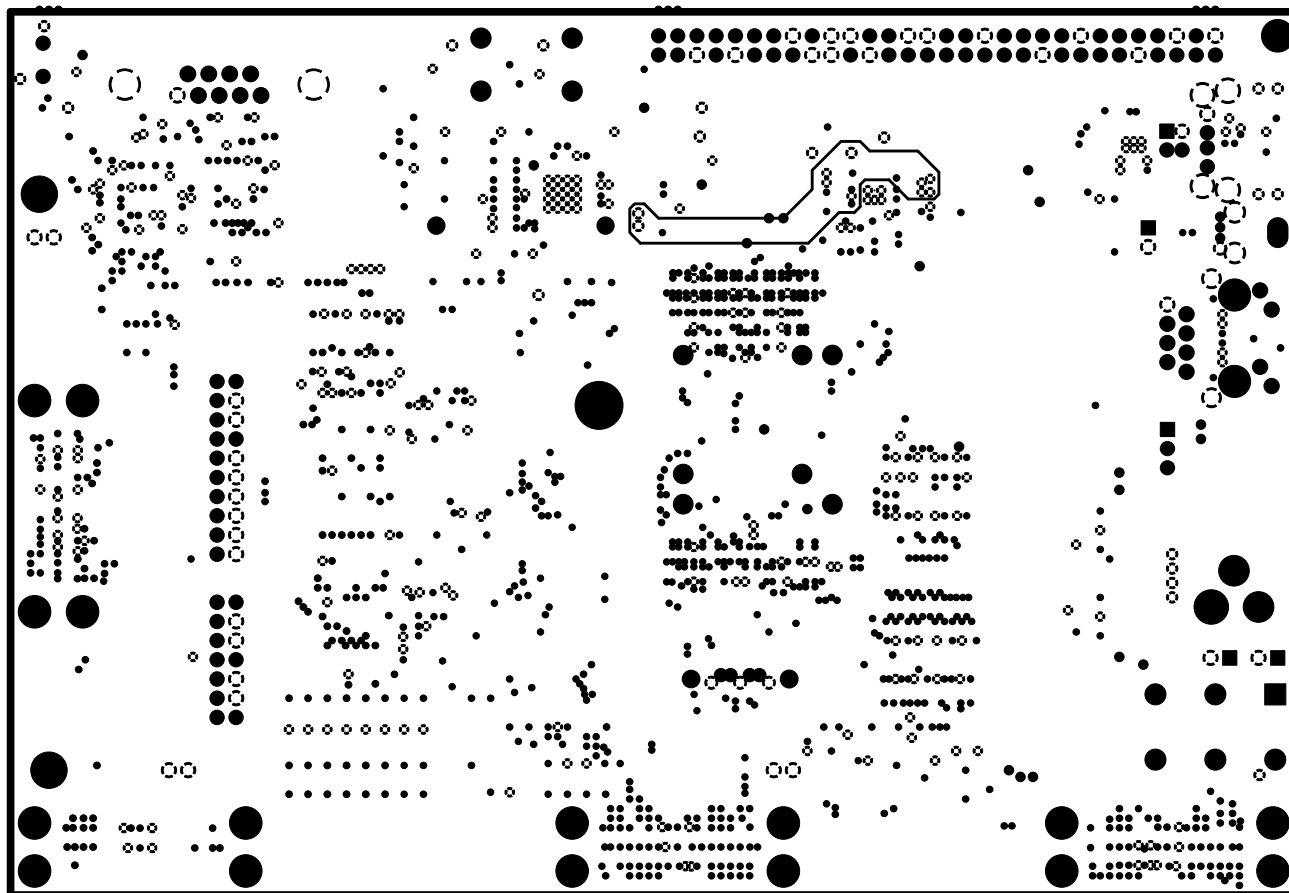
REVISION CHANGES			
PART NO.	REV	DATE	CHANGES
1012939	A	04-09-2009	--
1013126	A	06-30-2009	SEE BELOW

1. ADDED MTG HOLES RIGHT OF J29 AND LEFT OF J13
2. ROTATED 180 DEGREES: S2, S7, J22, J23
3. SHIFTED J13 LEFT 0.25" TO PREVENT INCORRECT DAUGHTERCARD MATING
4. ADDED MTG HOLE TO UPPER RIGHT CORNER
5. BOARD DIMENSIONS CHANGED FROM 4.6" X 6.1" TO 4.6" X 6.725"
6. ARRAY CHANGED FROM 1-UP TO 2-UP

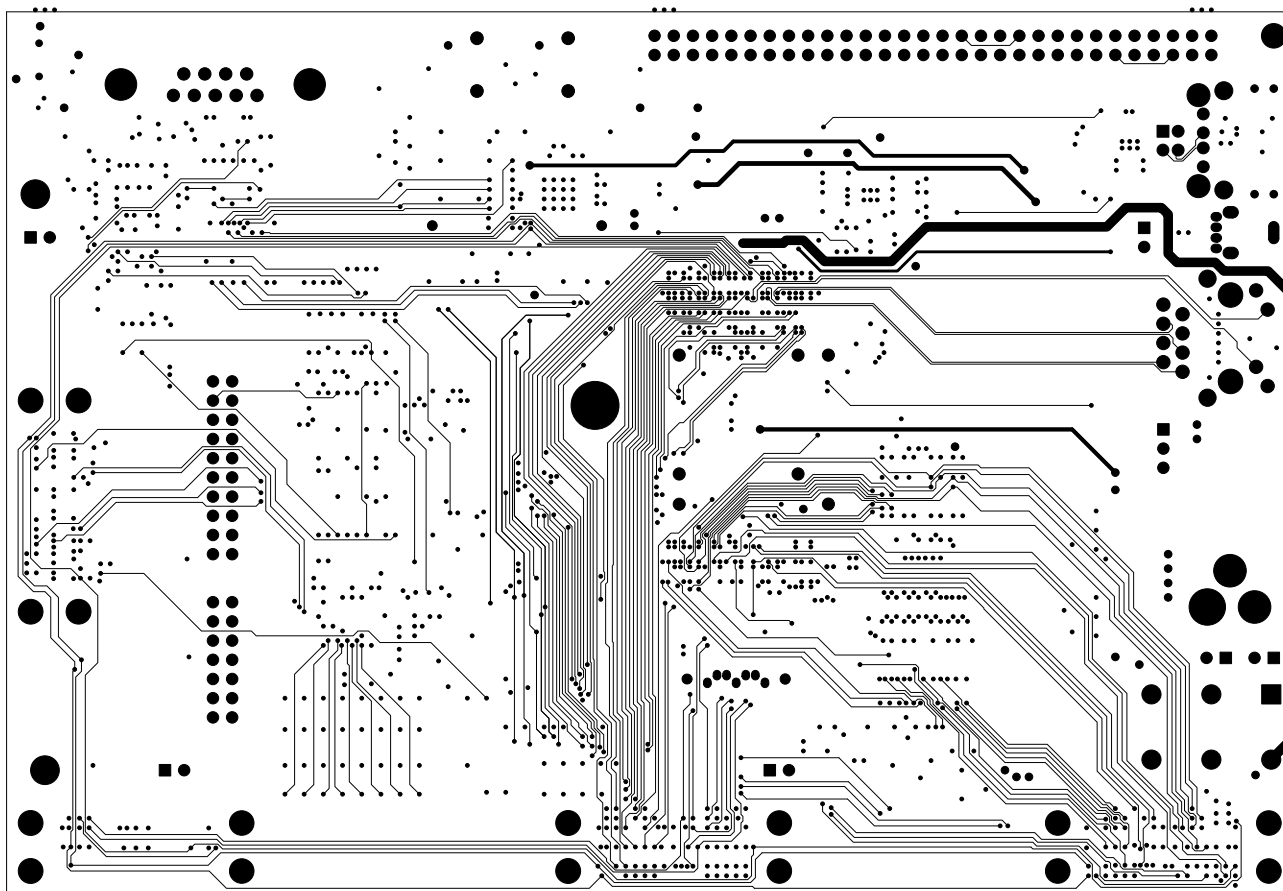
DRILL CHART				
SYM	DIAM	TOL	QTY	NOTE
⋈	0.010	+/- 0.003	1260	PLATED
#	0.020	+/- 0.003	44	PLATED
+	0.020	+/- 0.003	18	NON-PLATED
◇	0.029	+/- 0.003	7	PLATED
⊠	0.032	+/- 0.003	4	PLATED
⊞	0.035	+/- 0.003	2	NON-PLATED
○	0.036	+/- 0.003	3	PLATED
⊗	0.040	+/- 0.003	126	PLATED
⊗	0.043	+/- 0.003	9	PLATED
+	0.051	+/- 0.003	2	NON-PLATED
◇	0.053	+/- 0.003	2	PLATED
#	0.063	+/- 0.003	7	NON-PLATED
△	0.064	+/- 0.003	2	PLATED
⊠	0.067	+/- 0.003	4	PLATED
⊞	0.040X0.074	+/- 0.003	2	PLATED SLOT
⊞	0.075	+/- 0.003	6	PLATED
⊞	0.091	+/- 0.003	2	NON-PLATED
⊞	0.094	+/- 0.003	2	NON-PLATED
⊠	0.033X0.096	+/- 0.003	1	PLATED SLOT
△	0.120	+/- 0.003	2	PLATED
⊗	0.125	+/- 0.003	2	PLATED
⊞	0.125	+/- 0.003	1	NON-PLATED
⊞	0.128	+/- 0.003	2	NON-PLATED
⊞	0.129	+/- 0.003	17	NON-PLATED
⊞	0.140	+/- 0.003	1	PLATED
×	0.150	+/- 0.003	2	NON-PLATED
TOTAL			1530	



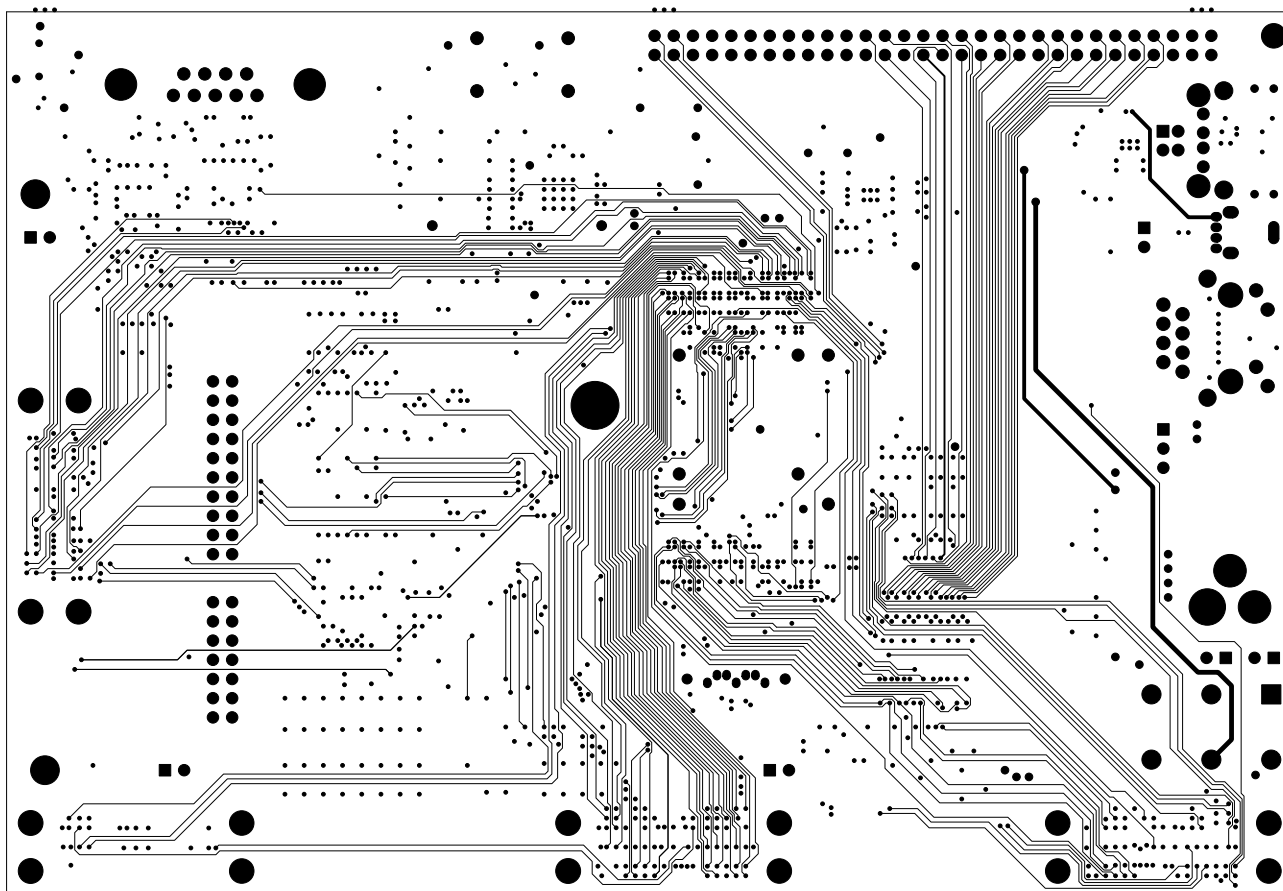
LOGIC PRODUCT DEVELOPMENT
LAYER 1 TOP



LOGIC PRODUCT DEVELOPMENT
LAYER 2 GND

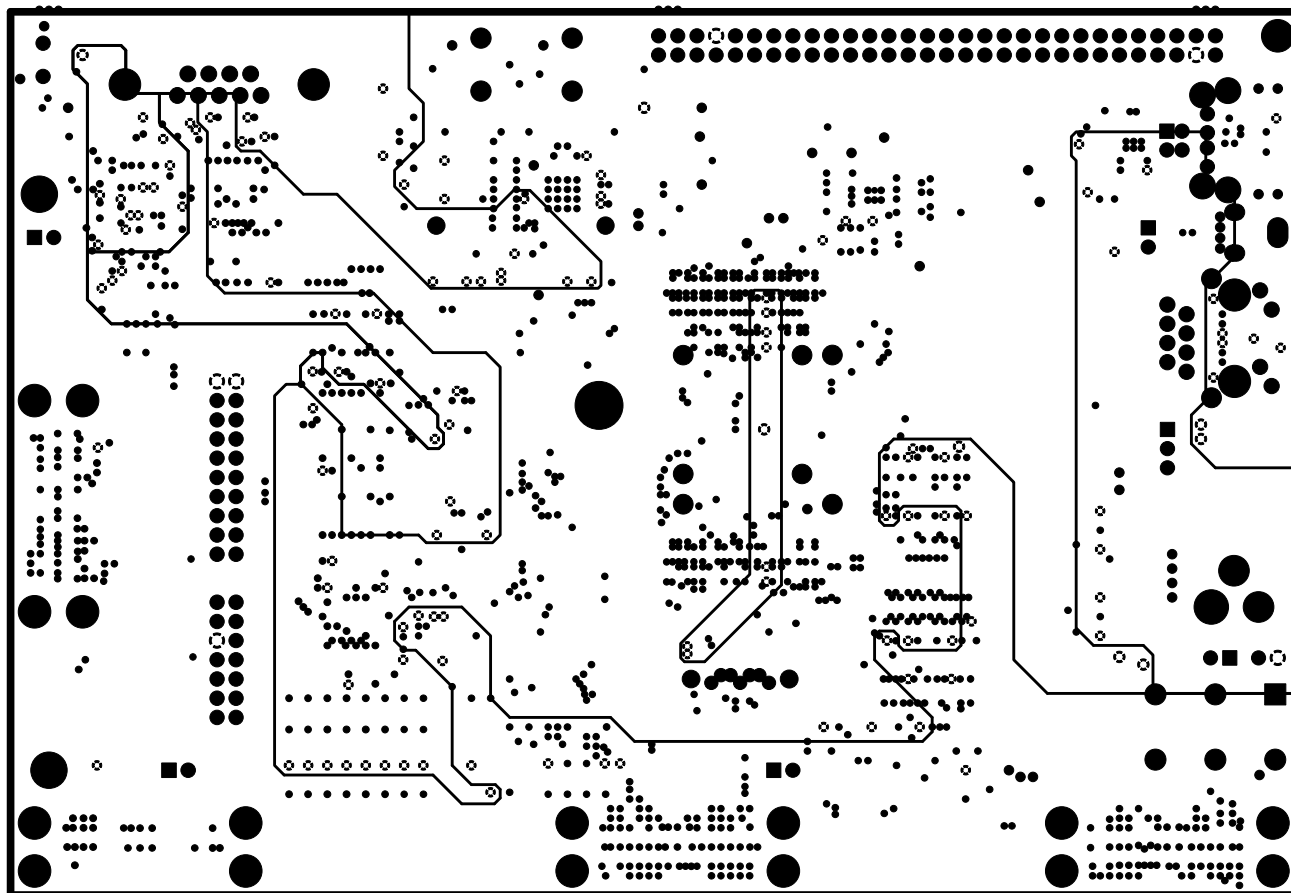


LOGIC PRODUCT DEVELOPMENT
LAYER 3



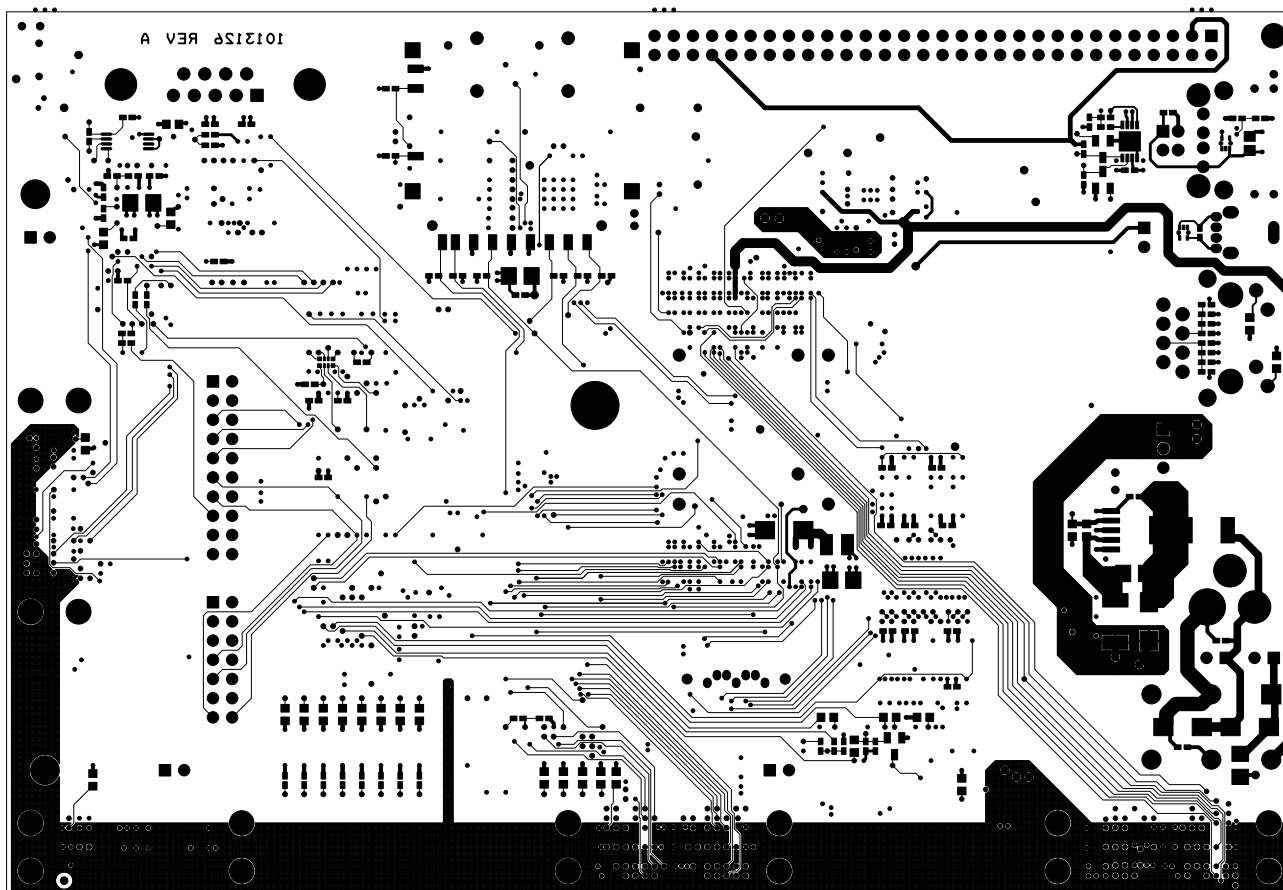
LOGIC PRODUCT DEVELOPMENT

LAYER 4



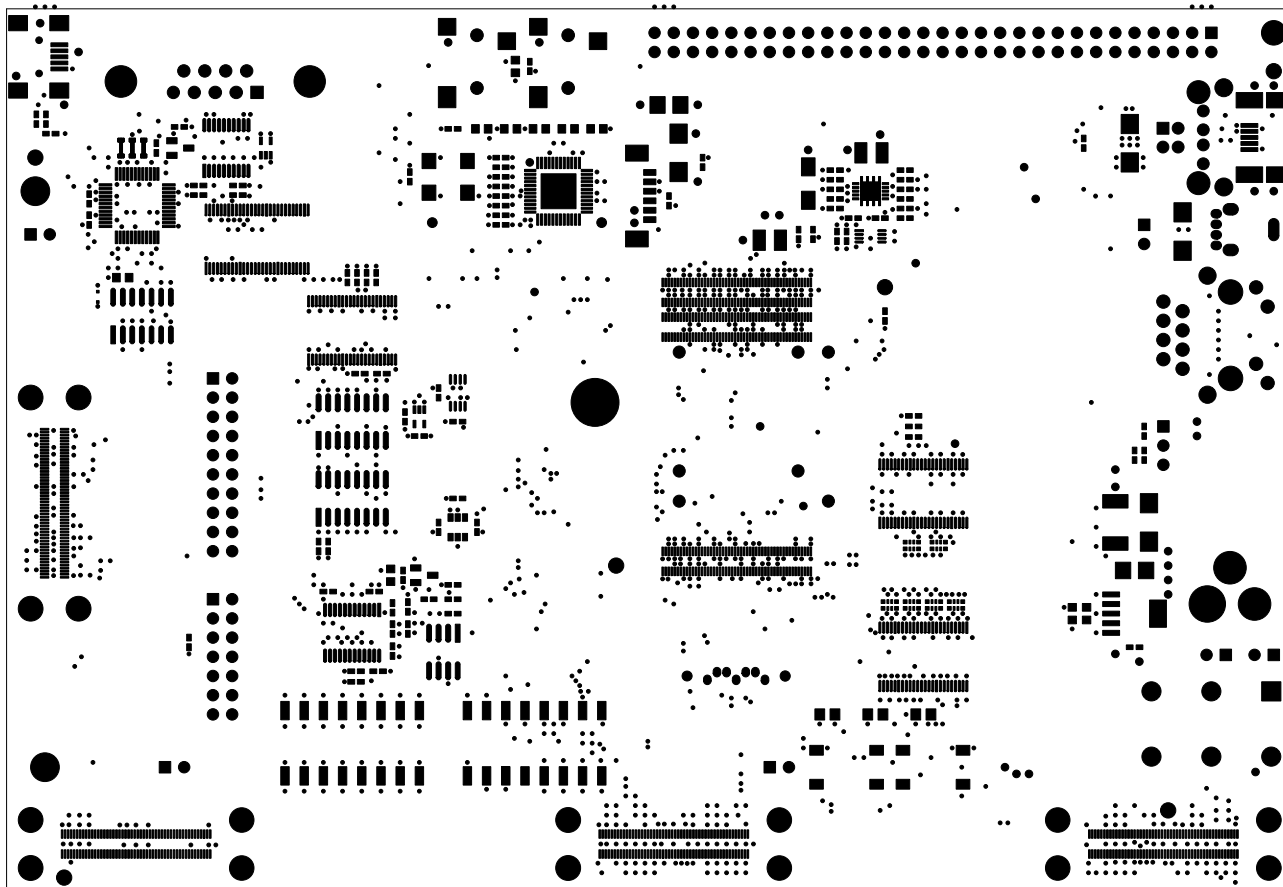
LOGIC PRODUCT DEVELOPMENT

LAYER 5 PWR

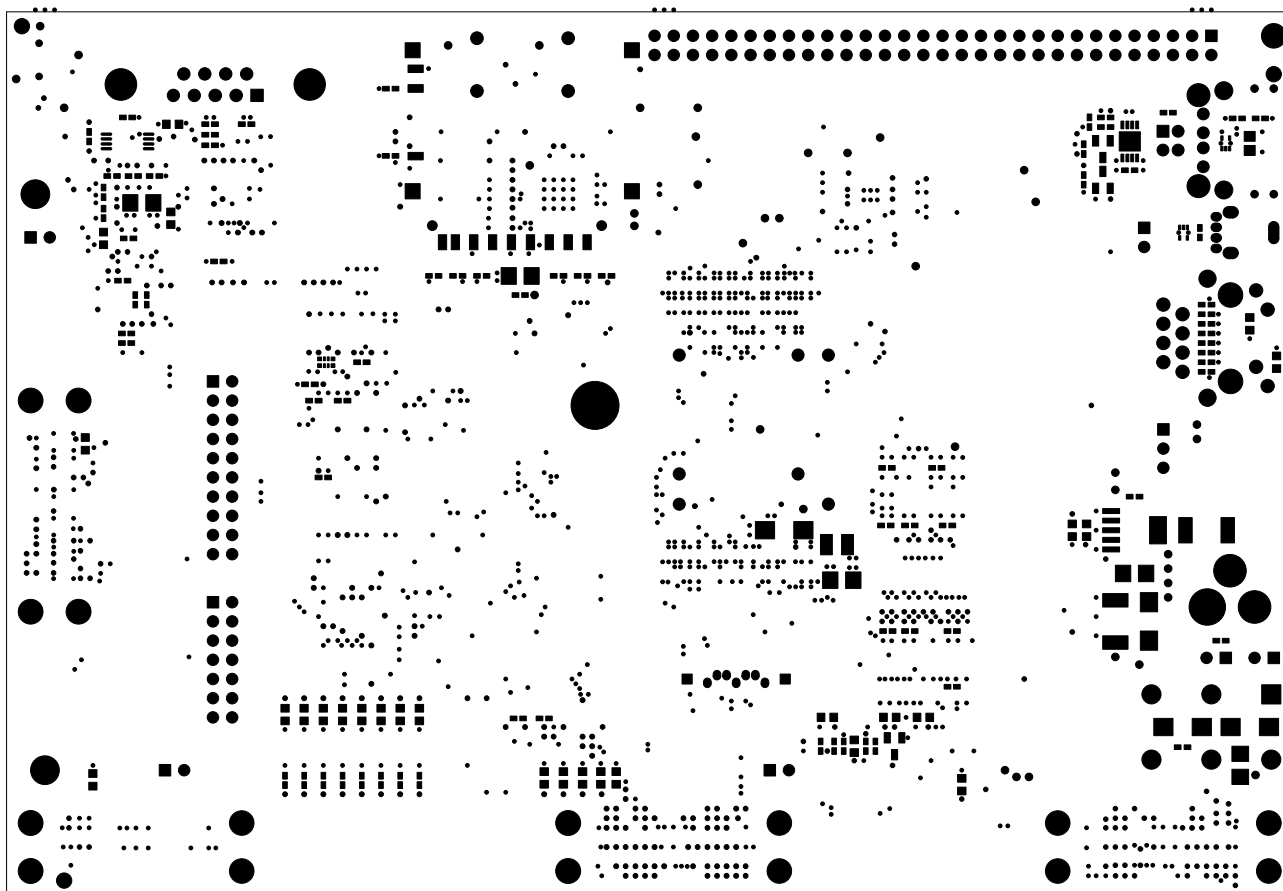


LOGIC PRODUCT DEVELOPMENT

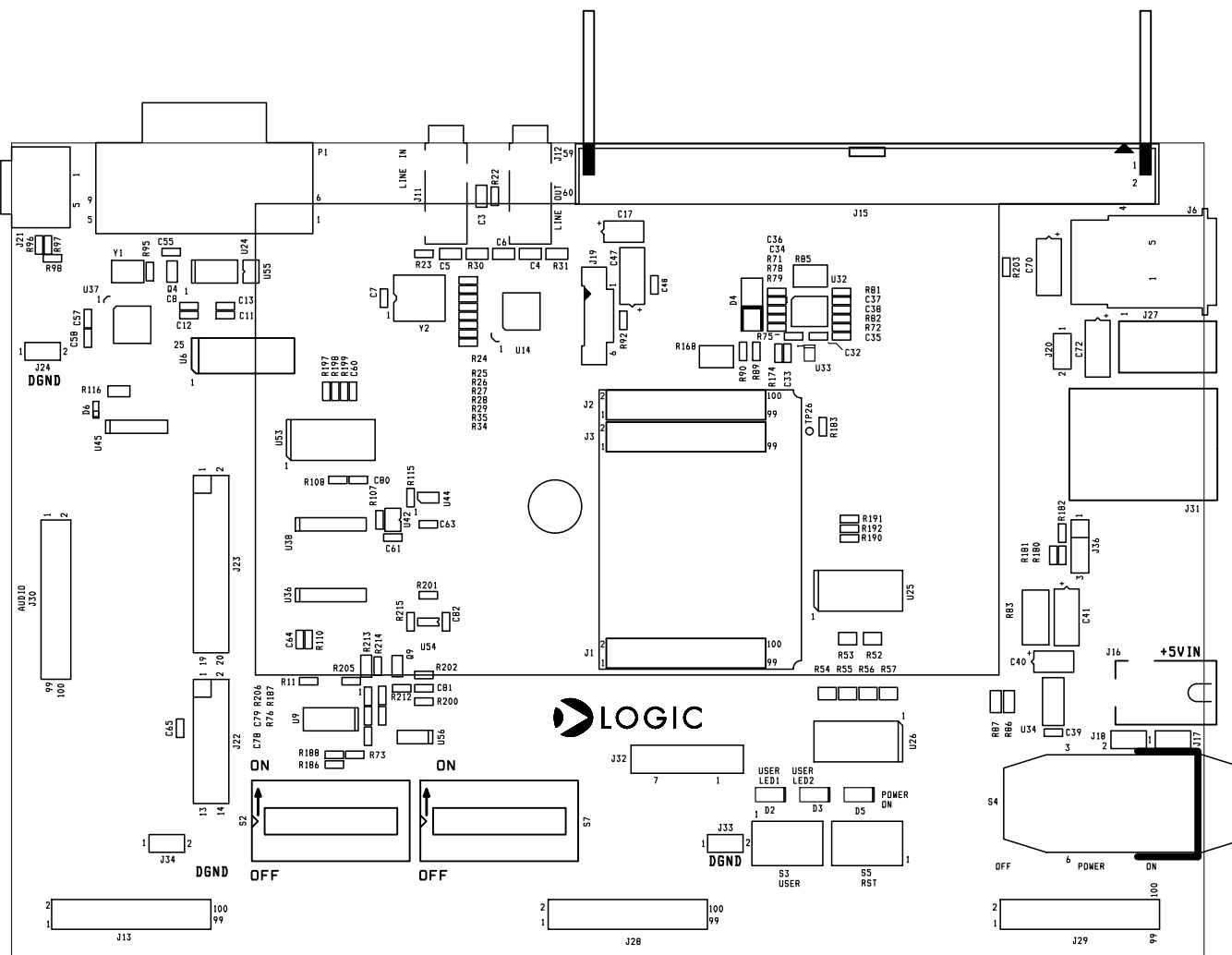
LAYER 6 BOTTOM



LOGIC PRODUCT DEVELOPMENT
SOLDERMASK TOP

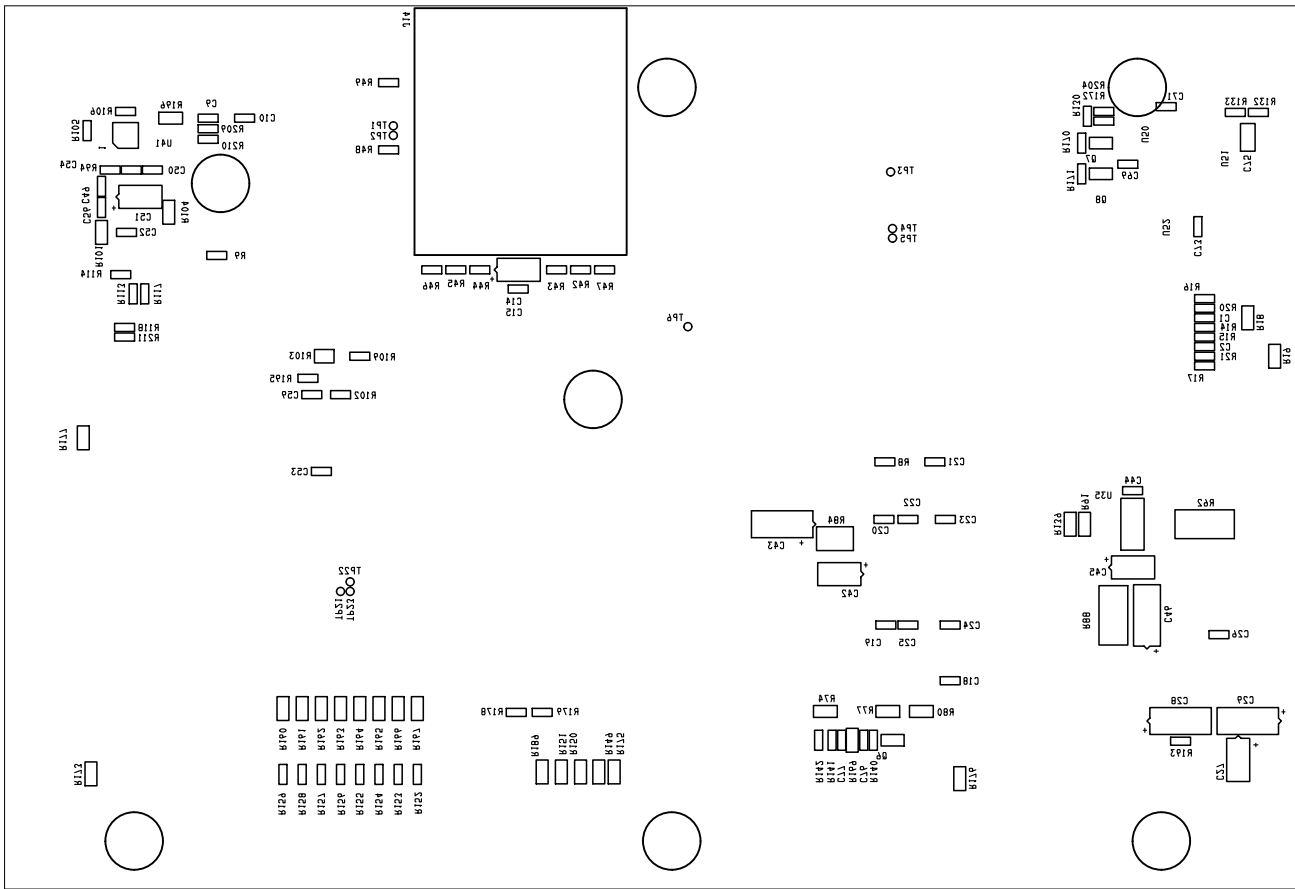


LOGIC PRODUCT DEVELOPMENT
SOLDERMASK BOT



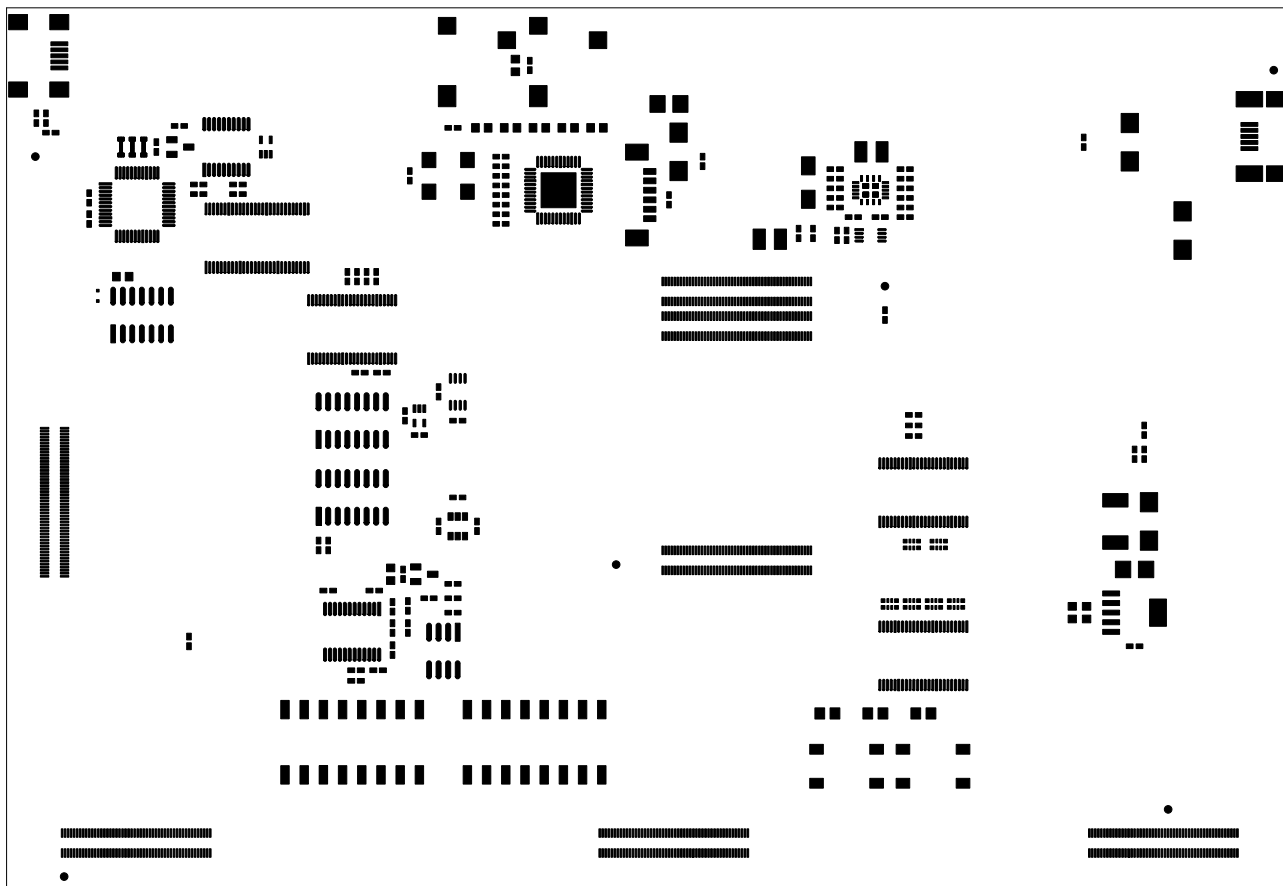
LOGIC PRODUCT DEVELOPMENT

SILKSCREEN TOP



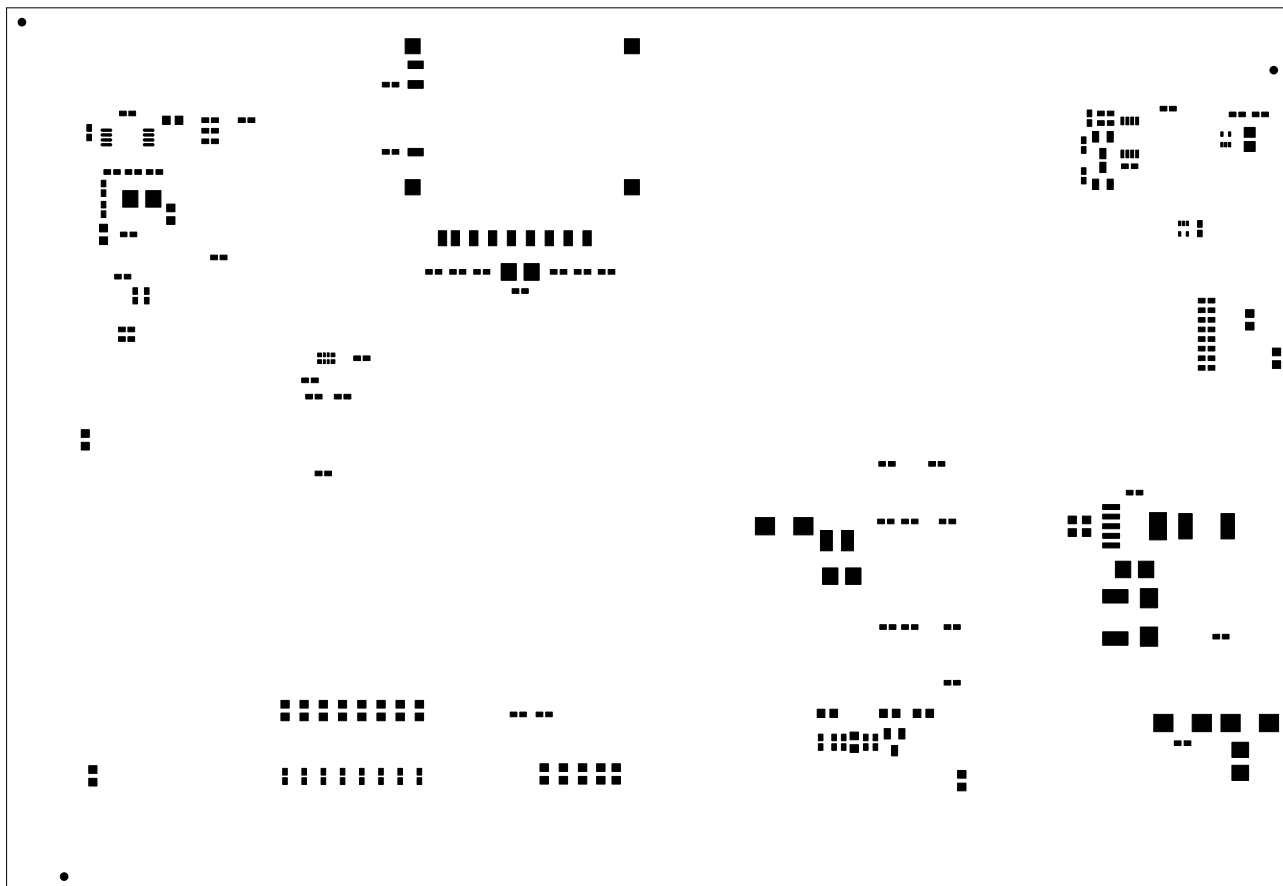
LOGIC PRODUCT DEVELOPMENT

SILKSCREEN BOT



LOGIC PRODUCT DEVELOPMENT

SOLDERPASTE TOP



LOGIC PRODUCT DEVELOPMENT

SOLDERPASTE BOT