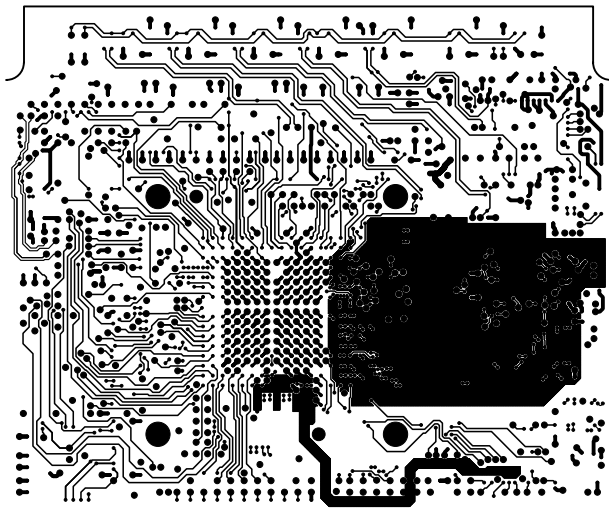
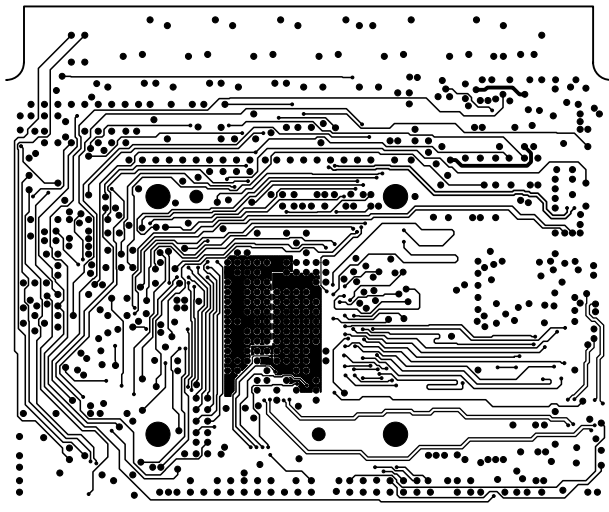


LOGIC PRODUCT DEVELOPMENT
1014606 REV A OMAP L138 PM SOM
11-18-2009
LAYER 1 TOP

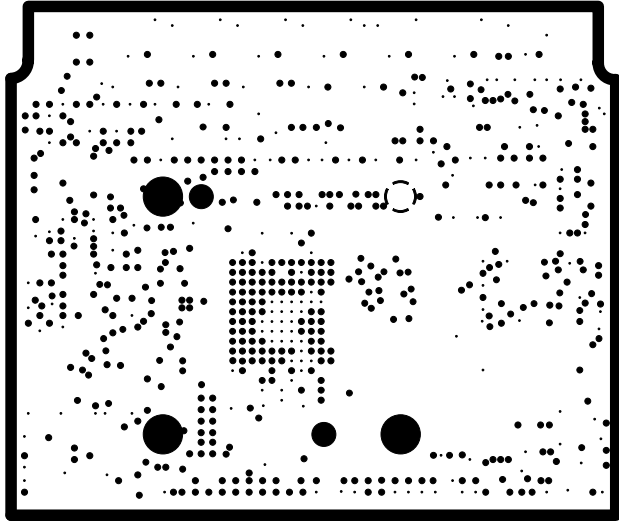


LOGIC PRODUCT DEVELOPMENT
1014606 REV A OMAP L138 PM SOM
11-18-2009
LAYER 2 SIGNAL



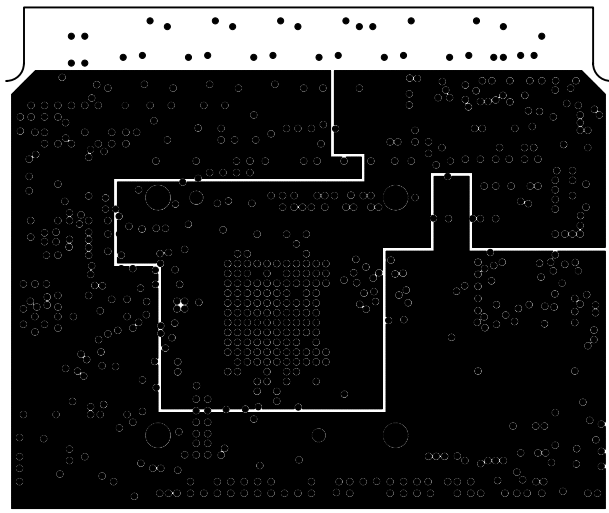
LOGIC PRODUCT DEVELOPMENT
1014606 REV A OMAP L138 PM SOM
11-18-2009

LAYER 3 SIGNAL



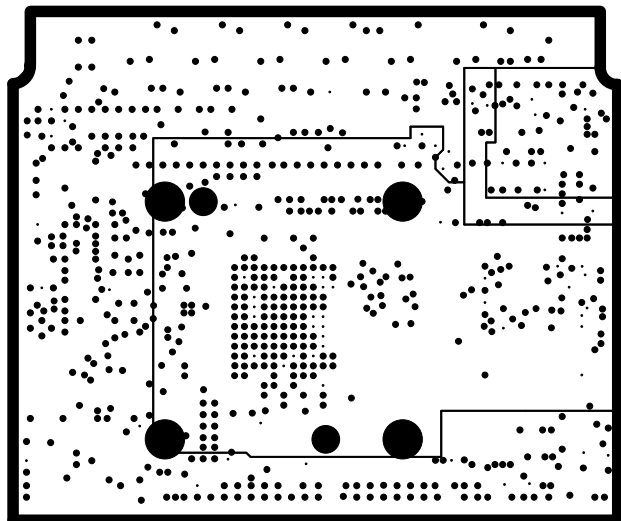
LOGIC PRODUCT DEVELOPMENT
1014606 REV A OMAP L138 PM SOM
11-18-2009

LAYER 4 GROUND



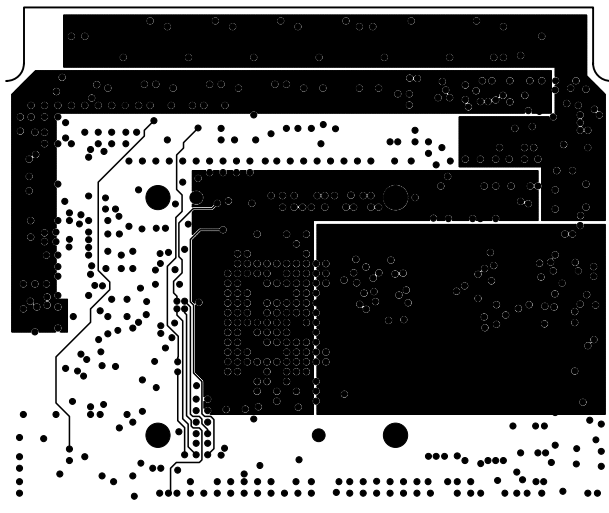
LOGIC PRODUCT DEVELOPMENT
1014606 REV A OMAP L138 PM SOM
11-18-2009

LAYER 5 SIGNAL



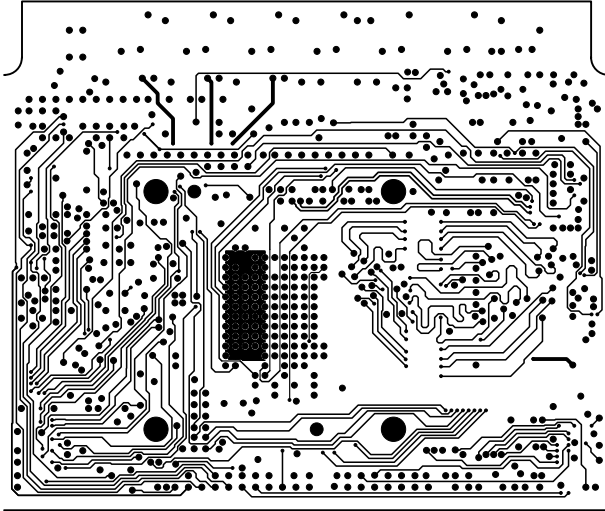
LOGIC PRODUCT DEVELOPMENT
1014606 REV A OMAP L138 PM SOM
11-18-2009

LAYER 6 POWER



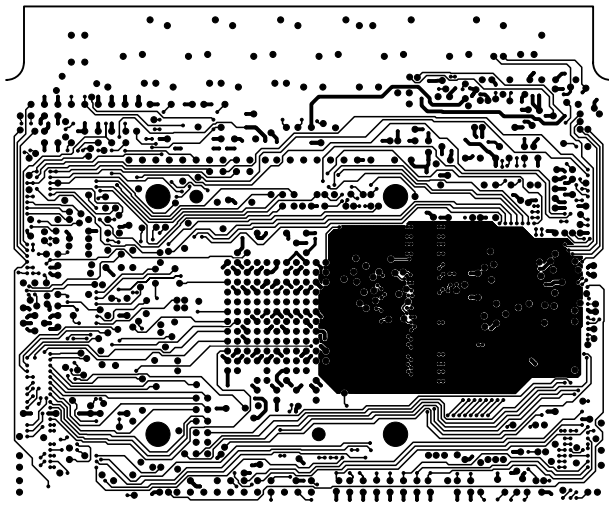
LOGIC PRODUCT DEVELOPMENT
1014606 REV A OMAP L138 PM SOM
11-18-2009

LAYER 7 SIGNAL



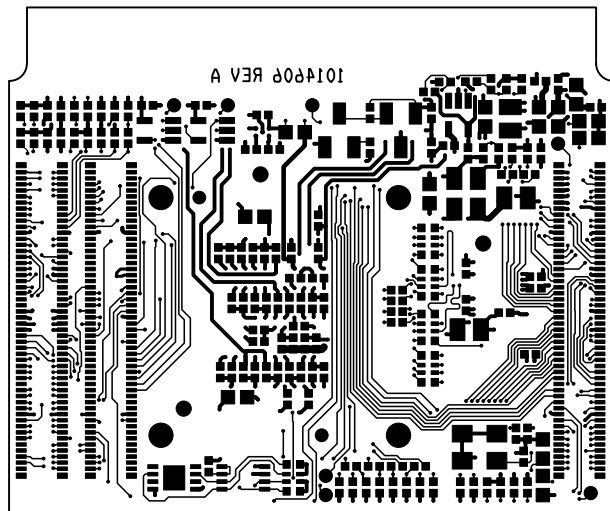
LOGIC PRODUCT DEVELOPMENT
1014606 REV A OMAP L138 PM SOM
11-18-2009

LAYER 8 SIGNAL



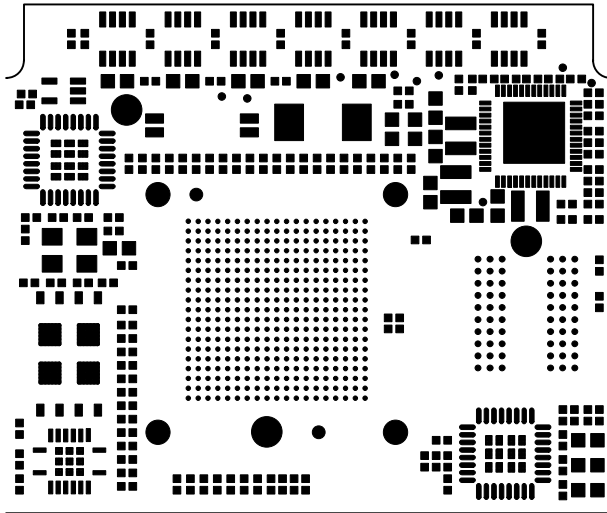
LOGIC PRODUCT DEVELOPMENT
1014606 REV A OMAP L138 PM SOM
11-18-2009

LAYER 9 SIGNAL



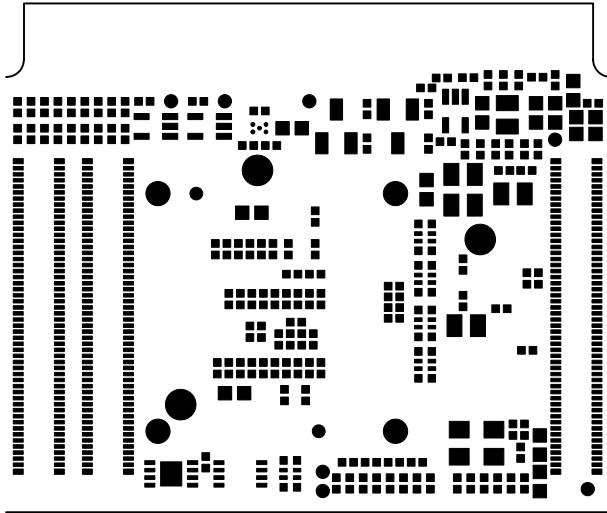
LOGIC PRODUCT DEVELOPMENT
1014606 REV A OMAP L138 PM SOM
11-18-2009

LAYER 10 BOTTOM



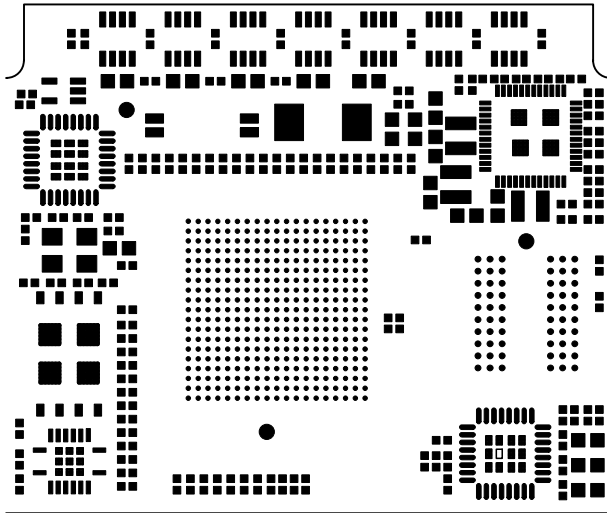
LOGIC PRODUCT DEVELOPMENT
1014606 REV A OMAP L138 PM SOM
11-18-2009

SOLDERMASK TOP



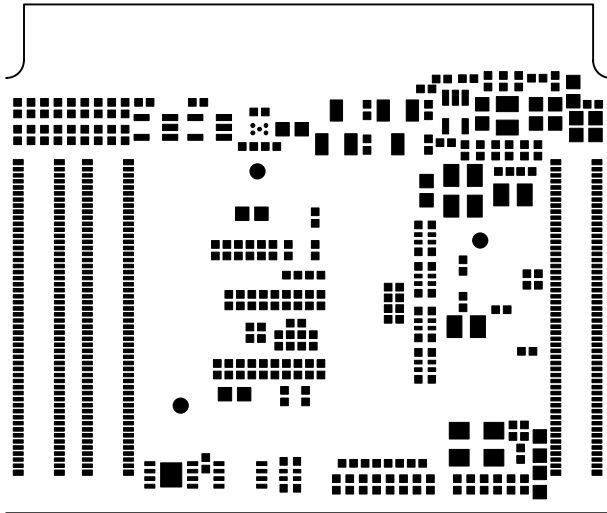
LOGIC PRODUCT DEVELOPMENT
1014606 REV A OMAP L138 PM SOM
11-18-2009

SOLDERMASK BOTTOM



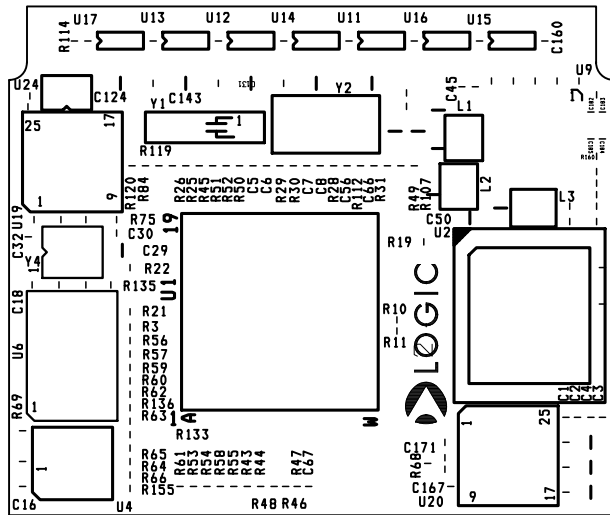
LOGIC PRODUCT DEVELOPMENT
1014606 REV A OMAP L138 PM SOM
11-18-2009

SOLDERPASTE TOP



LOGIC PRODUCT DEVELOPMENT
1014606 REV A OMAP L138 PM SOM
11-18-2009

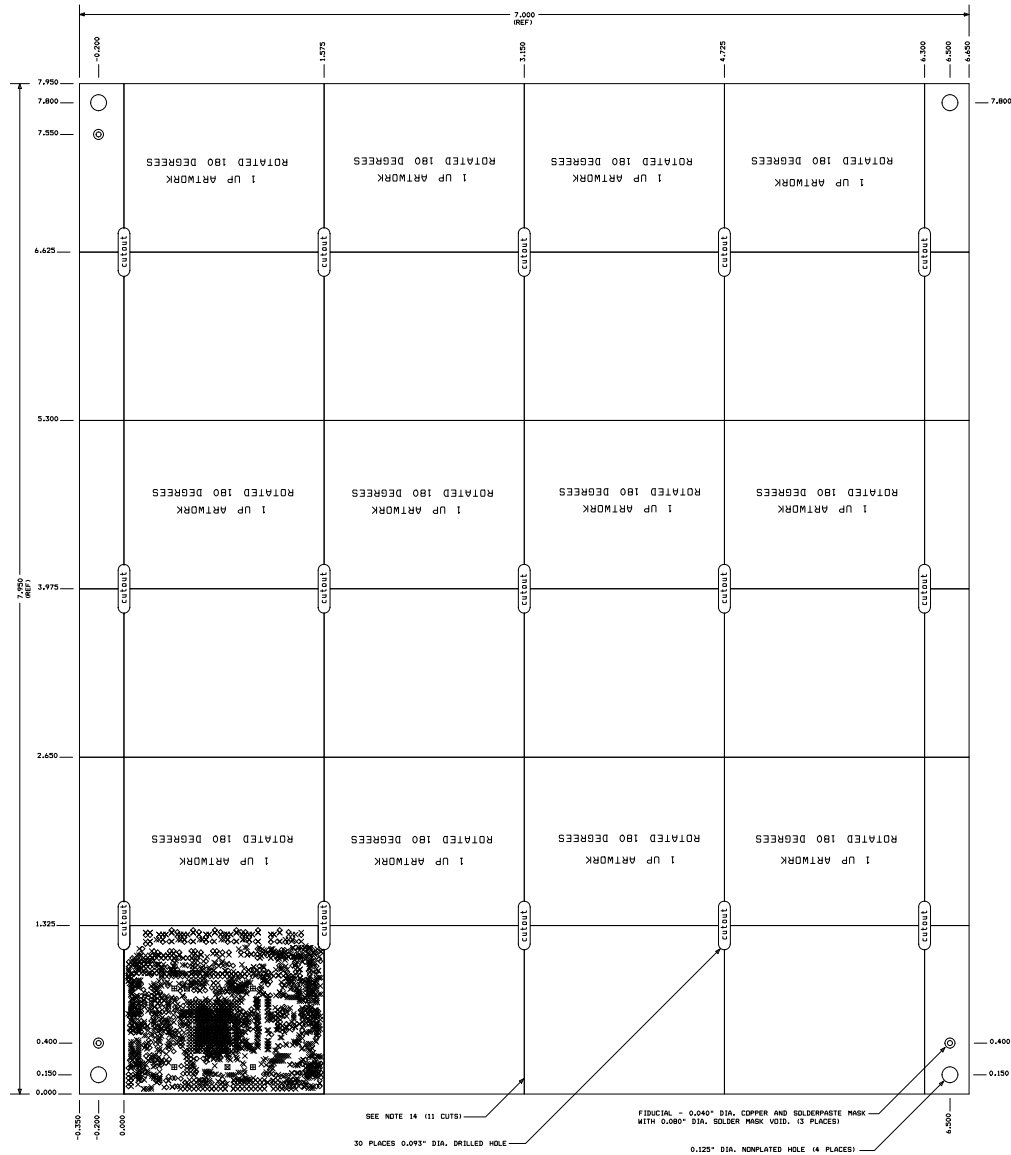
SOLDERPASTE BOTTOM



LOGIC PRODUCT DEVELOPMENT
1014606 REV A OMAP L138 PM SOM
11-18-2009

SILKSCREEN TOP





NOTE:

1. MATERIAL SELECTION:
10 LAYER, EPOXY GLASS, NEMA GRADE FR-4, 0.062 +/-0.007 THICK.
0.5 OZ. MINIMUM COPPER WITH SMOBC.
THE PRINTED CIRCUIT BOARDS MANUFACTURED TO THIS DRAWING
MUST BE ROHS COMPLIANT.
ALTERNATIVE MATERIAL MUST BE APPROVED BY LOGIC PRIOR TO USE.
2. FINISH ON ALL SOLDERABLE SURFACES TO BE:
IMMERSION SILVER (18Ag)
3. DESIGN INCLUDES MICRO-VIA TECHNOLOGY L1-L2, L2-L3, L8-L9 AND L9-L10.
BURIED VIA TECHNOLOGY L2-L9
4. DRILL HOLE TOLERANCE TO FAB NOTES:
5. SOLDER RESIST: COLOR - GREEN (COLOR).
THE USE OF SOLDER RESIST COATING SHALL BE IN ACCORDANCE WITH
THE REQUIREMENTS OF IPC-SM-840.
USE LIQUID PHOTODIMAGEABLE RESIST APPLIED OVER BARE COPPER.
ALL SOLDERABLE SURFACES ARE TO BE FREE OF SOLDER RESIST.
SOLDER RESIST BRIDGES 0.003" OR LESS MAY BE REMOVED.
6. SILKSCREEN: USE WHITE NON-CONDUCTIVE INK. ALL COMPONENT AND
TESTPOINT LANDS ARE TO BE FREE OF INK.
7. MANUFACTURER'S IDENTIFICATION: ADD TO SILKSCREEN ON BOTTOM SIDE.
8. ELECTRICAL BARE BOARD TEST REQUIRED.
9. DRILL SIZES ARE FINISHED SIZE AFTER PLATING.
10. BOARD VENDOR MAY REMOVE THERMALS FOR VIA'S ON PLANE LAYERS.
11. BOARD VENDOR MAY REMOVE NON FUNCTIONAL PADS ON INNER LAYERS.
12. BOARD VENDOR MAY ADD TEAR SHAPING TO INNER LAYERS.
BOARD VENDOR TO ADD TEAR SHAPING TO OUTER LAYERS.
13. BOARD IS A 4x6 ARRAY.
14. BOARD TO BE SCORED AT DESIGNATED LINE. SCORING TO BE 30 DEG.
AND A MINIMUM OF 0.015 INCHES BOARD MATERIAL IN CHANNEL.
15. THEIVING STRUCTURES MAY BE ADDED TO COMPENSATE FOR VARIATIONS
IN COPPER DENSITY ACROSS THE PWB. SPACING BETWEEN THEIVING AND
CONDUCTIVE PATTERN TO BE 0.020" MINIMUM.
16. 0.0031, 0.0032, 0.0041 AND 0.0110" TRACE WIDTH TO BE IMPEDANCE CONTROLLED.
50 OHM +/-10% SINGLE ENDED (0.004" TRACE WIDTH).
90 OHM +/-10% DIFFERENTIAL:
0.0085 TRACE WIDTH ON LAYER 1 REFERENCED TO LAYER 4.
0.00425 TRACE WIDTH ON LAYER 2 REFERENCED TO LAYER 4.
0.0045 TRACE WIDTH ON LAYER 3 REFERENCED TO LAYER 4.
0.0045 TRACE WIDTH ON LAYER 8 REFERENCED TO LAYER 7.
100 OHM +/-10% DIFFERENTIAL:
0.0031 TRACE WIDTH ON LAYER 1 REFERENCED TO LAYER 2.
0.0031 TRACE WIDTH ON LAYER 2 REFERENCED TO LAYER 4.
0.00375 TRACE WIDTH ON LAYER 3 REFERENCED TO LAYER 4.
0.0031 TRACE WIDTH ON LAYER 9 REFERENCED TO LAYER 7.
0.0031 TRACE WIDTH ON LAYER 10 REFERENCED TO LAYER 9.
WIDTH OF TRACES ON SIGNAL LAYERS MAY BE ADJUSTED AS NECESSARY
TO ACHIEVE IMPEDANCE SPECIFIED.
17. MICRO VIAS ARE FROM LAYER 1-2, 2-3, 8-9, 9-10.
BLIND FIA IS FROM LAYER 2 TO 9.

IMPEDANCE CONTROLLED 10 LAYER STACKUP

LAYER #	THICKNESS (IN)	DESCRIPTION
SILKSCREEN TOP SIDE		
SOLDER MASK TOP SIDE		
LAYER 1 CIRCUIT TOP	0.0005/0.0007	SOLDERMASK
	0.0016	1 OZ. AFTER PLATING
	0.0028	PREPEG
LAYER 2 CIRCUIT / PLANE	0.0014	1 OZ. AFTER PLATING
	0.0027	PREPEG
LAYER 3 CIRCUIT	0.0006	3/8 OZ.
	0.0040	CORE
LAYER 4 PLANE GND	0.0006	3/8 OZ.
	0.0046	PREPEG
LAYER 5 CIRCUIT / PLANE	0.0006	3/8 OZ.
	0.0210	CORE
LAYER 6 PLANE PWR	0.0006	3/8 OZ.
	0.0046	PREPEG
LAYER 7 CIRCUIT / PLANE	0.0006	3/8 OZ.
	0.0040	PREPEG
LAYER 8 CIRCUIT	0.0006	3/8 OZ.
	0.0027	PREPEG
LAYER 9 CIRCUIT / PLANE	0.0014	1 OZ. AFTER PLATING
	0.0028	PREPEG
LAYER 10 CIRCUIT BOTTOM	0.0016	1 OZ. AFTER PLATING
	0.0005/0.0007	SOLDERMASK
SOLDER MASK BOTTOM SIDE		
SILKSCREEN BOTTOM SIDE		

DRILL CHART				
SYM	DIAM	TOL	QTY	NOTE
X	0.004	MICRO-VIA	1539	PLATED
C	0.008	+/-0.003	703	PLATED
W	0.033	+/-0.003	2	NON-PLATED
W	0.063	+/-0.003	4	NON-PLATED
TOTAL			2248	

REVISION CHANGES

PART NO.	REV	DATE	CHANGES
1012953	A	04-01-2009	--
1013333	A	04-30-2009	SEE BELOW #1,2
1013335	B	10-01-2009	SEE BELOW #3
1014406	A	11-18-2009	SEE BELOW #4

1. CHANGED STACKUP.
2. ADDED AND REMOVED COMPONENTS.
3. ADDED 2 0.095 MIL NP HOLES AND NOTE.
4. CHANGED CONNECTION ON U3, U4, U6 AND R133, ADDED C182-C185.