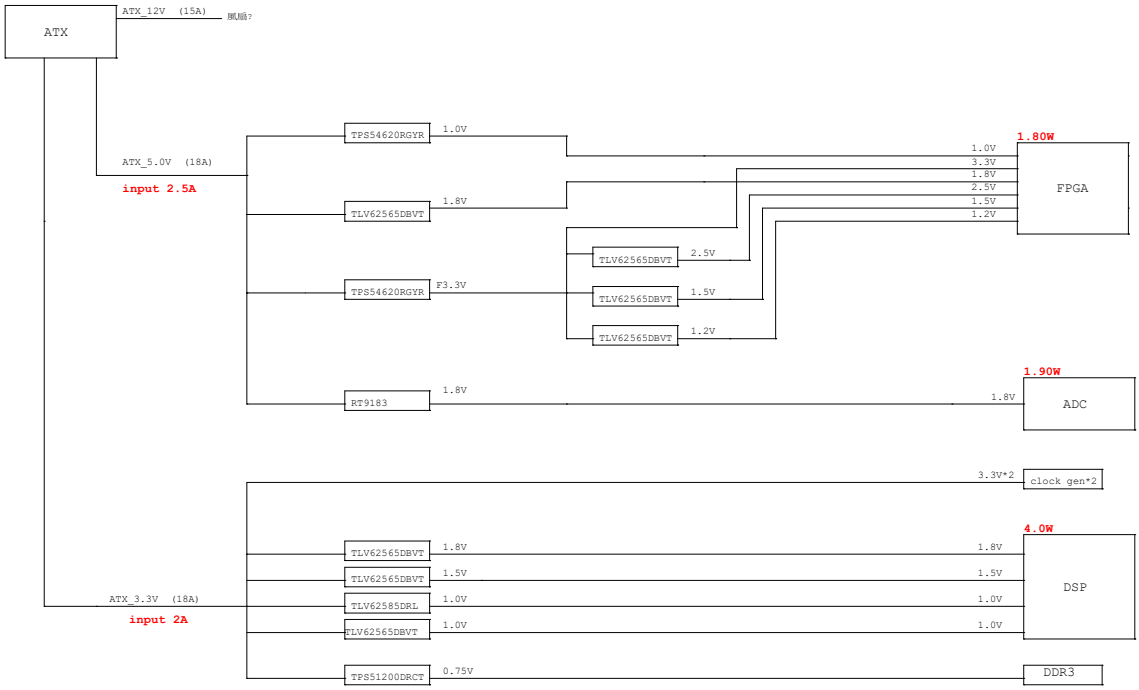

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Size: Document Number: Rev: <RevCode>
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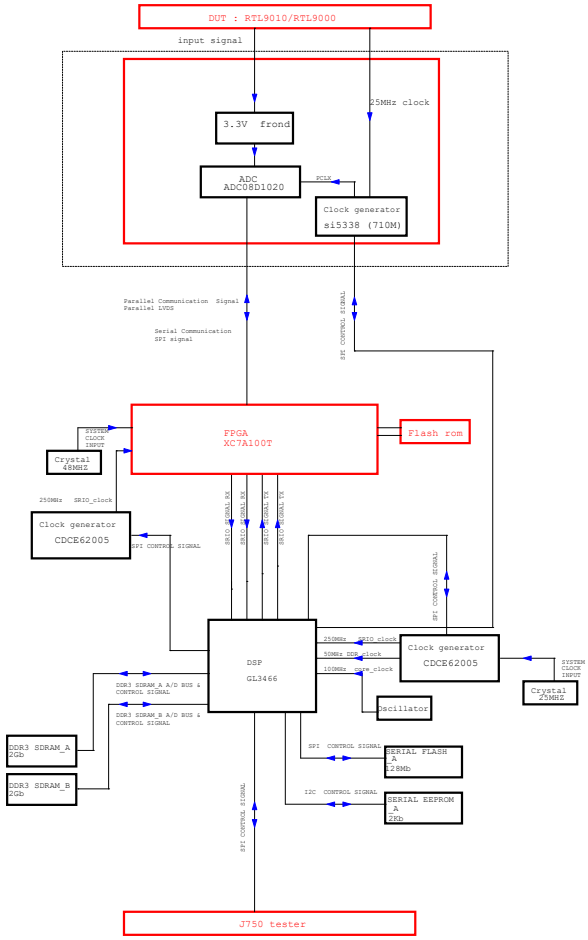
Date: Tuesday, January 07, 2020 Sheet 1 of 1

DSP TMS320C6657 System Block Diagram



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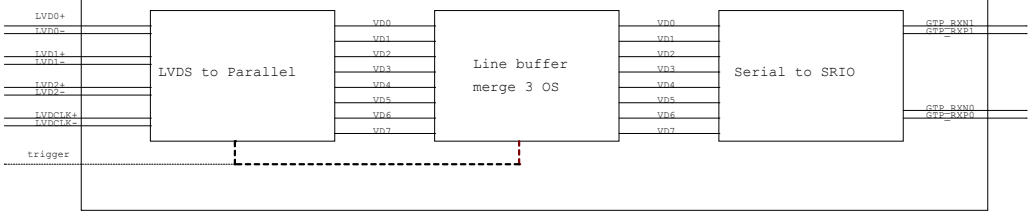
Size C	Document Number <Doc>	Rev <RevCode>
Date: Tuesday, January 07, 2020	Sheet 1 of 1	

To ADC (ADC08D1020)

FPGA BLOCK DIAGRAM

To DSP



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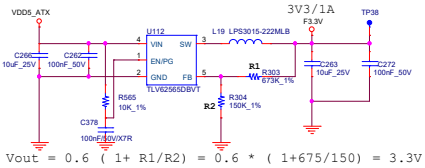
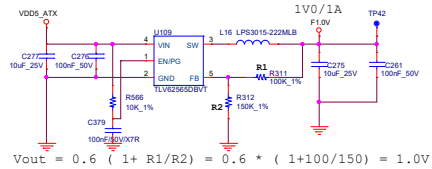
Date: Tuesday, January 07, 2020	Sheet 1 of 1	

B part

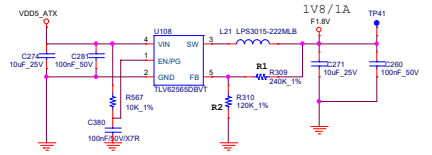
ATX POWER IN



Vout = 0.6 (1+ R1/R2) = 0.6 * (1+675/150) = 3.3V

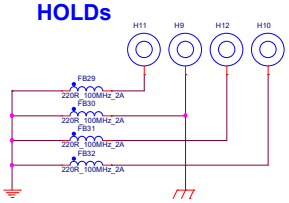


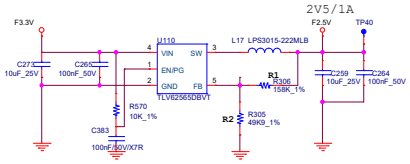
Vout = 0.6 (1+ R1/R2) = 0.6 * (1+100/150) = 1.0V



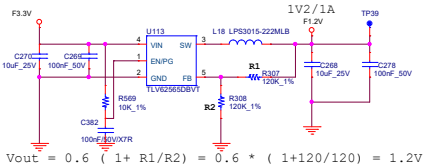
Vout = 0.6 (1+ R1/R2) = 0.6 * (1+240/120) = 1.8V

HOLDs

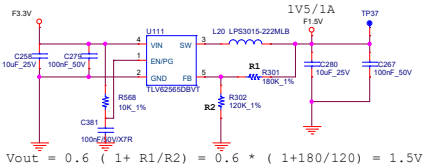




Vout = 0.6 (1+ R1/R2) = 0.6 * (1+158/49.9) = 2.5V



Vout = 0.6 (1+ R1/R2) = 0.6 * (1+120/120) = 1.2V



Vout = 0.6 (1+ R1/R2) = 0.6 * (1+180/120) = 1.5V

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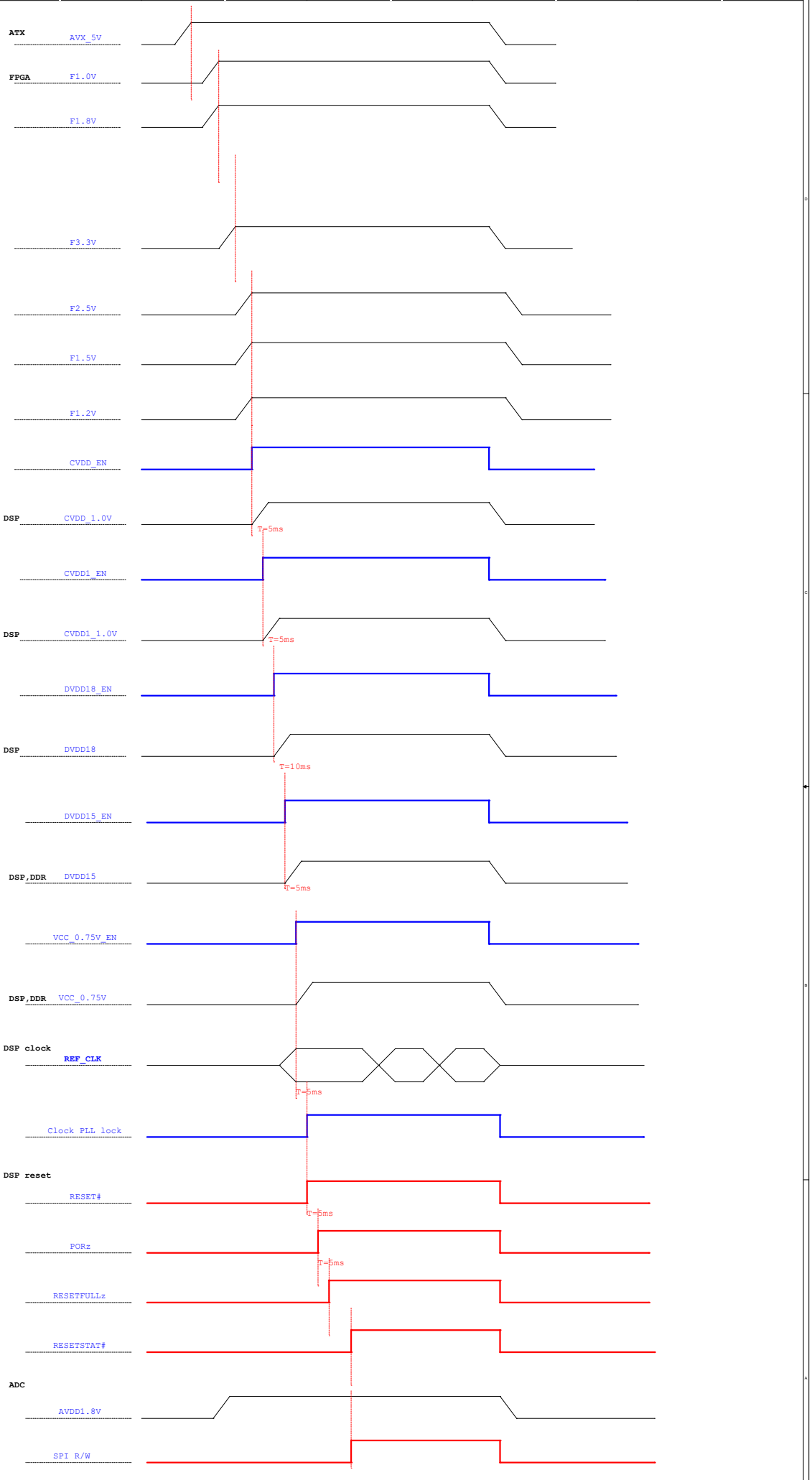

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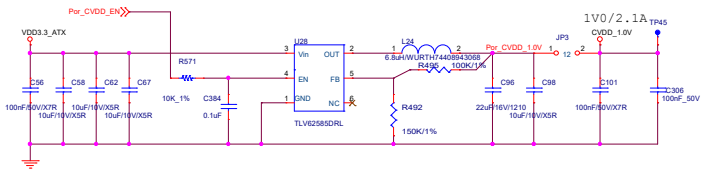
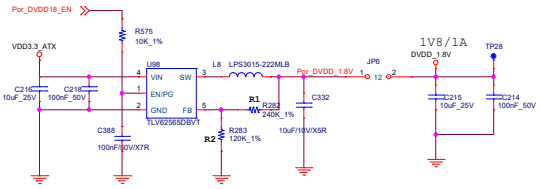
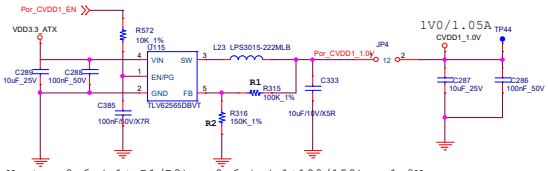
ATX POWER IN

Vout = 0.6 (1+ R1/R2) = 0.6 * (1+100/150) = 1.0V

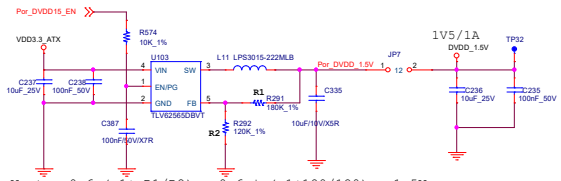




Vout = 0.6 (1+ R1/R2) = 0.6 * (1+240/120) = 1.8V

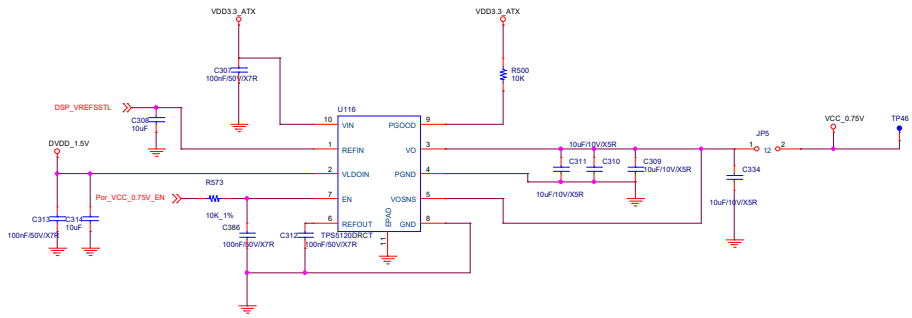


Vout = 0.6 (1+ R1/R2) = 0.6 * (1+100/150) = 1.0V



Vout = 0.6 (1+ R1/R2) = 0.6 * (1+180/120) = 1.5V

DDR Power Gen



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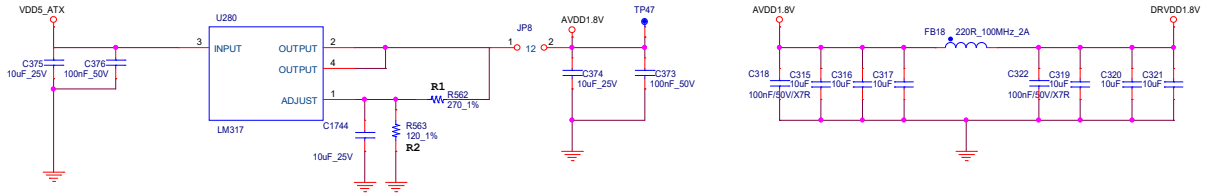

Vout = 1.25 (1+ R2/R1) = 1.25 * (1+110/210) = 1.9V

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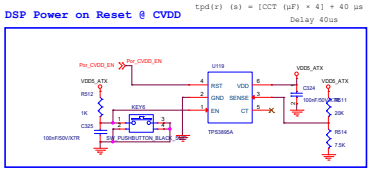
tpd(r) (s) = [CCT (µF) × 4] + 40 µs

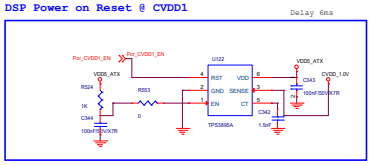
DSP Power on Reset @ CVDD

Delay 40us



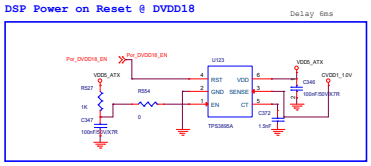
DSP Power on Reset @ CVDD1

Delay 6ms



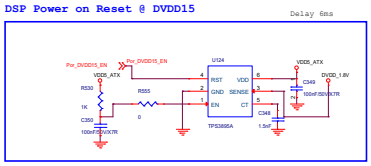
DSP Power on Reset @ DVDD18

Delay 6ms



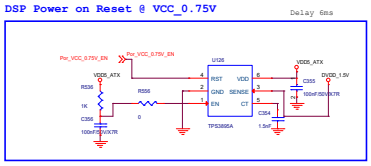
DSP Power on Reset @ DVDD15

Delay 6ms



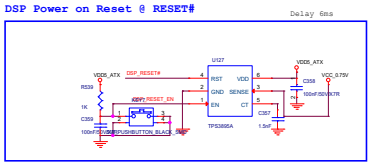
DSP Power on Reset @ VCC_0.75V

Delay 6ms



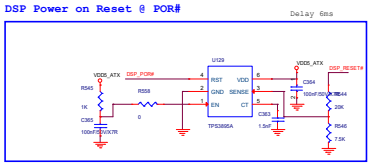
DSP Power on Reset @ RESET#

Delay 6ms



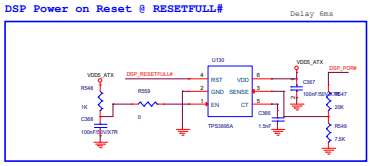
DSP Power on Reset @ POR#

Delay 6ms



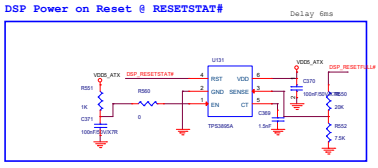
DSP Power on Reset @ RESETFULL#

Delay 6ms



DSP Power on Reset @ RESETSTAT#

Delay 6ms

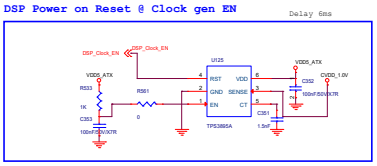


FPGA_Done

Status	Done
Right	V
Low	

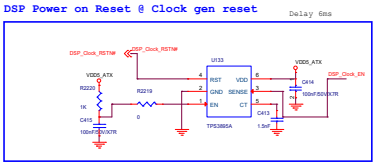
DSP Power on Reset @ Clock gen EN

Delay 6ms



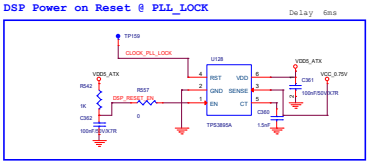
DSP Power on Reset @ Clock gen reset

Delay 6ms



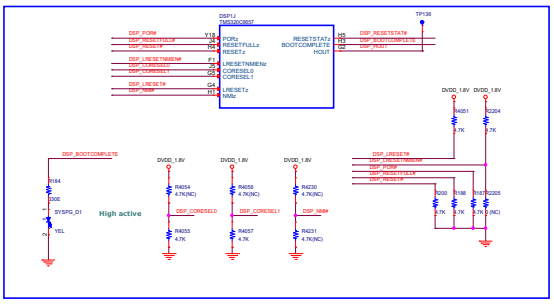
DSP Power on Reset @ PLL_LOCK

Delay 6ms

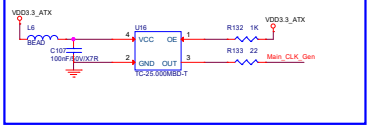


Reset Control

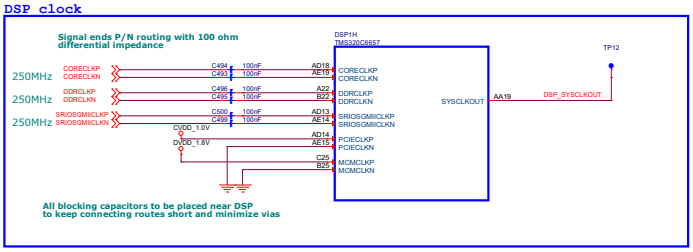
Default LRESETNMIEN tie high disable warm reset/NMI function



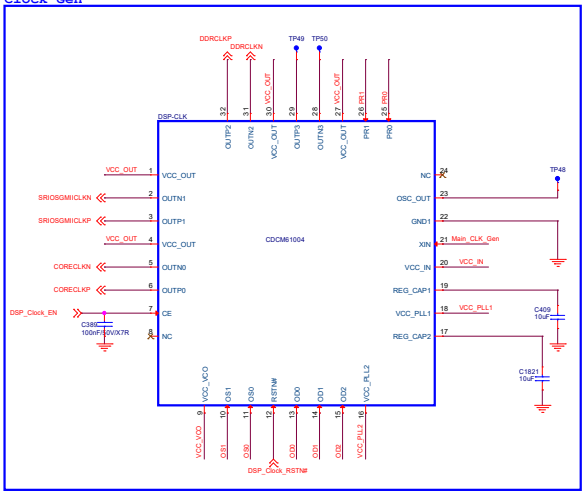
OSC Clock to clock gen



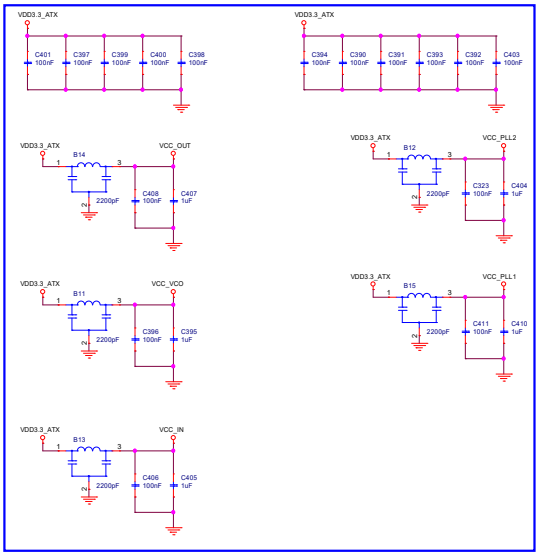
DSP clock



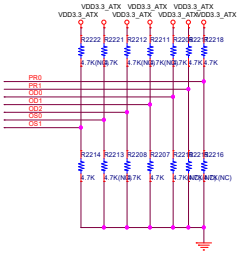
Clock Gen



Clock Gen Power



Clock Gen Configuration



SET Bit	Value(250MHz)	Description
PR 1:0	11	Prescaler Divider:4 | Feedback Divider:20
OD 2:0	001	Output Divider:2
OS 1:0	01	LVDS | OSC_OUT Off

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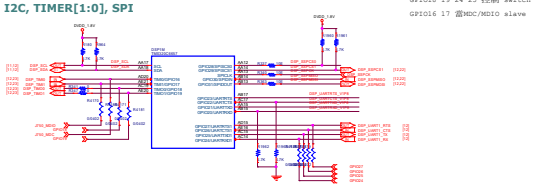
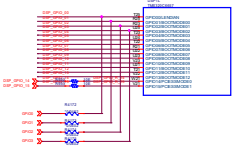
I2C, TIMER[1:0], SPI

GPIO18 19 24 25 控制 switch

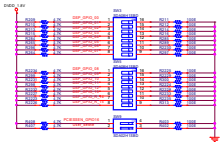
GPIO16 17 當MDC/MDIO slave



GPIO



BOOT STRAP CONFIGURATION



Boot Configuration

DIP Switch	DSP	BM_GPIO	Primary Function
BM_GPIO0	GPIO0	ENDIANESS	0 - Big Endian 1 - Little Endian
BM_GPIO[4:1]	GPIO[4:1]	BOOTMODE[3:0]	Boot Device
BM_GPIO[10:5]	GPIO[10:5]	BOOTMODE[9:4]	Boot Device Config
BM_GPIO[13:11]	GPIO[13:11]	BOOTMODE[12:10]	PLL Multiplier/I2C
BM_GPIO[15:14]	GPIO[15:14]	PCIESSMODE[1:0]	Endpt/RootComplex

Boot Device

BM_GPIO [4:1]	Boot Device	BM_GPIO [4:1]	Boot Device
0 0 0 0	Sleep/EMIF16	X 1 0 1	I2C Master
0 0 0 1	SRIO	0 1 0 1	I2C Slave
X 0 1 0	Ethernet	X 1 1 0	SPI
0 0 1 1	NAND	0 1 1 1	Hyperlink
0 1 0 0	PCIe	1 0 0 0	UART

Note: GPIO[10:5] bit definitions depend on the boot mode.

Boot PLL Settings

BM_GPIO [13:11]	Input Clock (in MHz)	BM_GPIO [13:11]	Input Clock (in MHz)
0 0 0	50.00	1 0 0	156.25
0 0 1	66.67	1 0 1	250.00
0 1 0	80.00	1 1 0	312.50
0 1 1	100.00	1 1 1	122.88

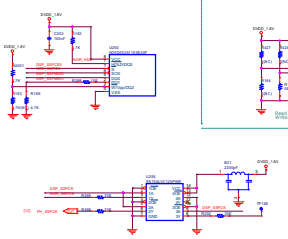
PCIe Mode Selection PCIESSMODE[1:0]

BM_GPIO [15:14]	PCIe Mode
0 0	End-point mode
0 1	Legacy End-point mode (support for legacy INTx)
1 0	Root complex mode
1 1	Reserved

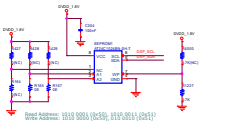
PCIESSEN

BM_GPIO16	PCIe Status
0	PCIe module disabled
1	PCIe module enabled

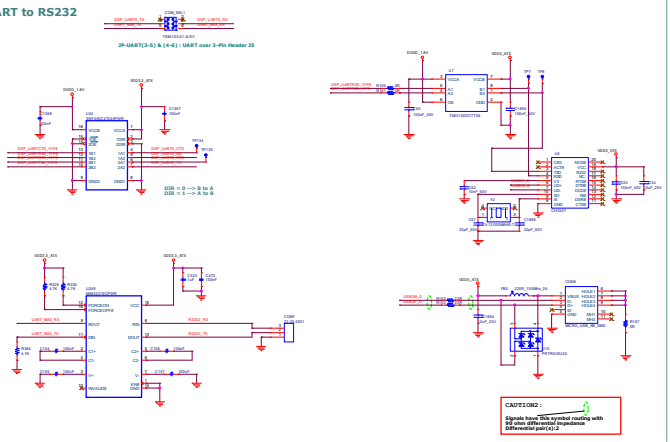
32Mb SPI NOR Flash



1Mb I2C EEPROM

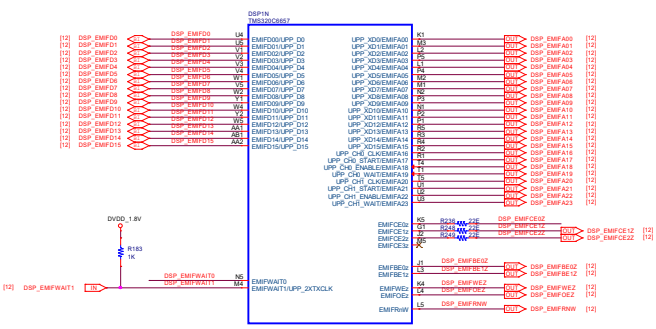


UART to RS232

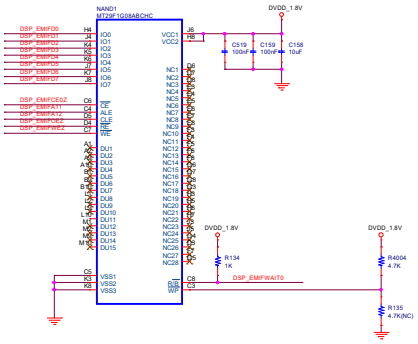


Reserved

C6657 - EMIF



NAND FLASH



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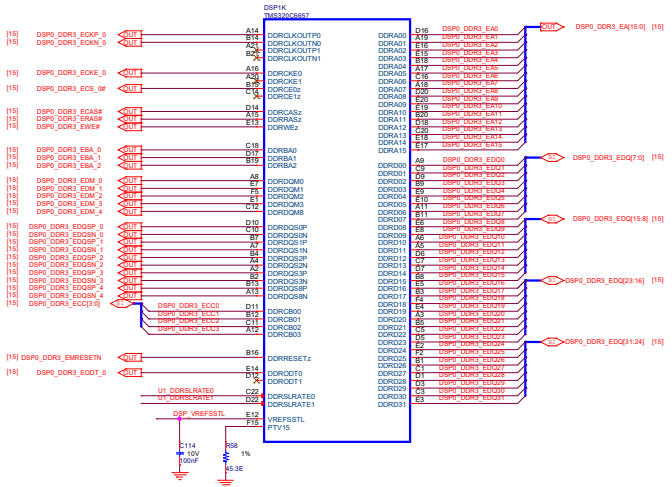
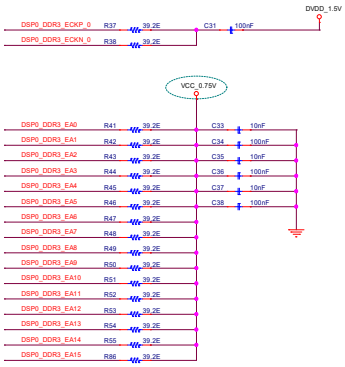
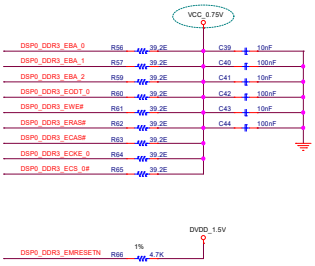
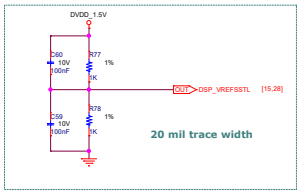
DDR3 INTERFACE

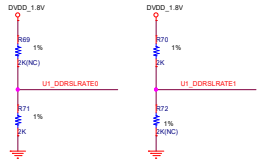




Place these resistors at the end of the trace.







DDR3 Slew-Rate Setting (DDRSLRATE[1:0]):

00 Fastest
01 Fast
10 Slow
11 Slowest

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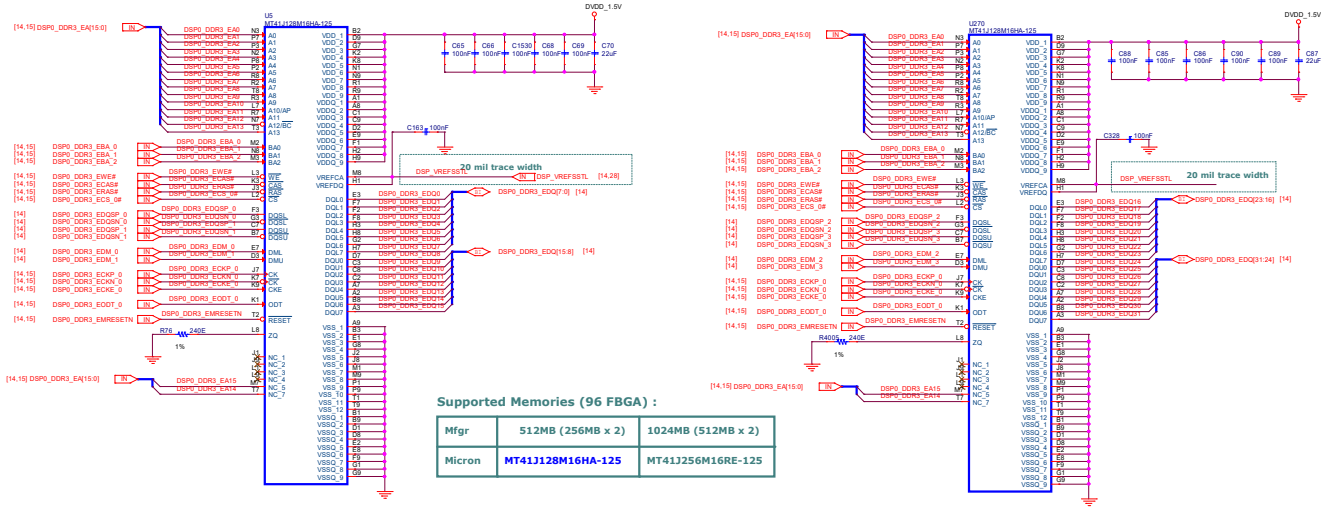
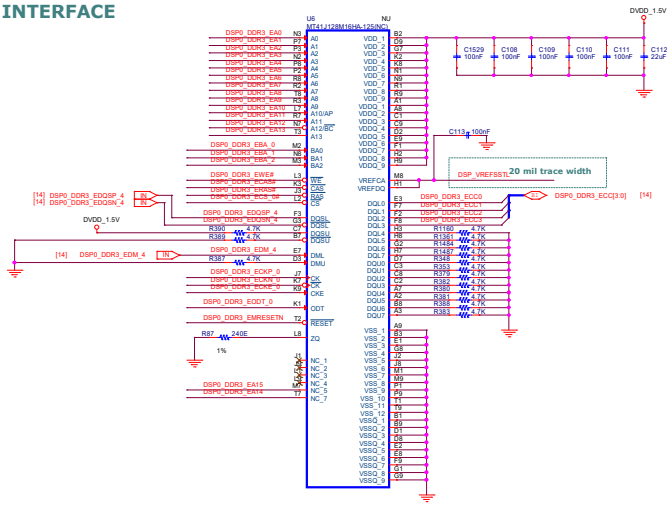
DDR3 MEMORY INTERFACE



Supported Memories (96 FBGA) :

Mfgr	512MB (256MB x 2)	1024MB (512MB x 2)
Micron	**MT41J128M16HA-125**	MT41J256M16RE-125

DDR3 ECC INTERFACE



- Data bits can be swapped within the byte lane to ease routing.

- Address/Command/Control/Clock routing must be Fly-By in byte order ECC, 0, 1, 2, 3.

Supported ECC Chip (96 FBGA) :

Mfgr	256MB	512MB
Micron	**MT41J128M16HA-125**	MT41J256M16RE-125

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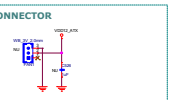
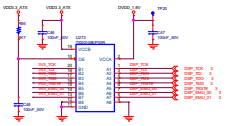
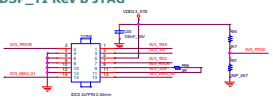
FAN CONNECTOR



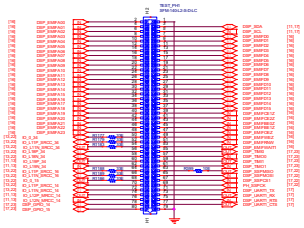
DSP_JTAG Voltage Converter



DSP_TI Rev B JTAG

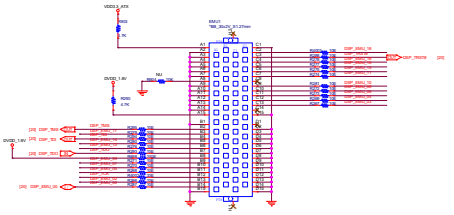


DEBUG HEADER

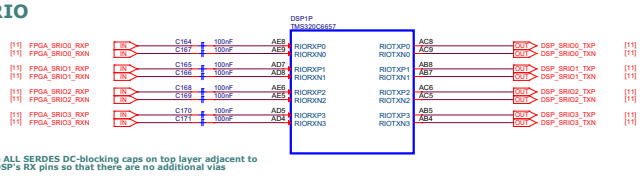


C6657 - JTAG & EMU

TI-60 Header

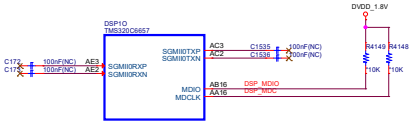


SRIO

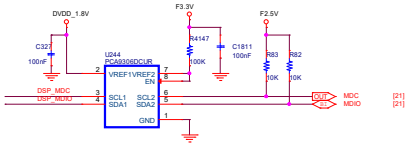


Place ALL SERDES DC-blocking caps on top layer adjacent to the DSP's RX pins so that there are no additional vias

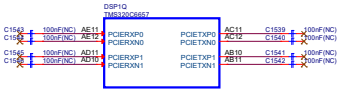
SGMII



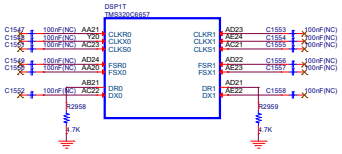
VOLTAGE LEVEL TRANSLATOR



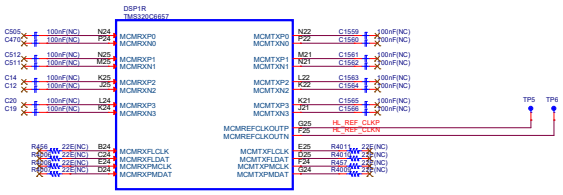
PCIE



McBSP



HYPERLINK



The HyperLink routes must have a max of 2 vias and no via stubs (Outer layer routing recommended)

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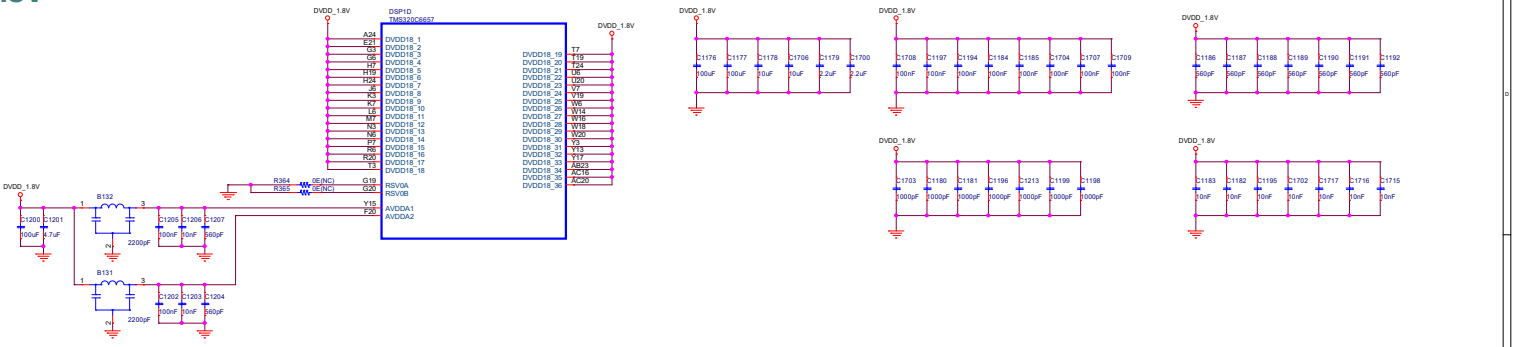
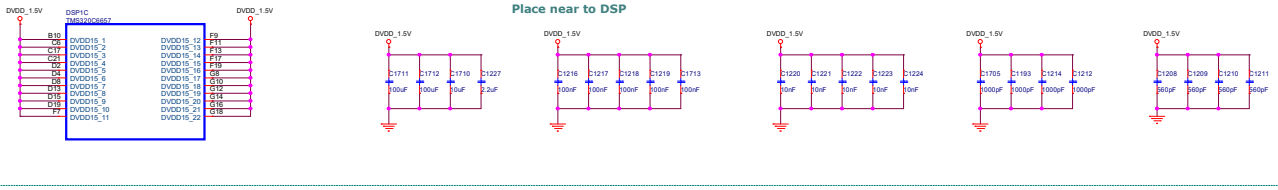
1.8V



1.5V



1.0V

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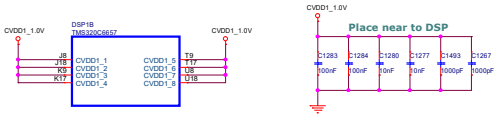
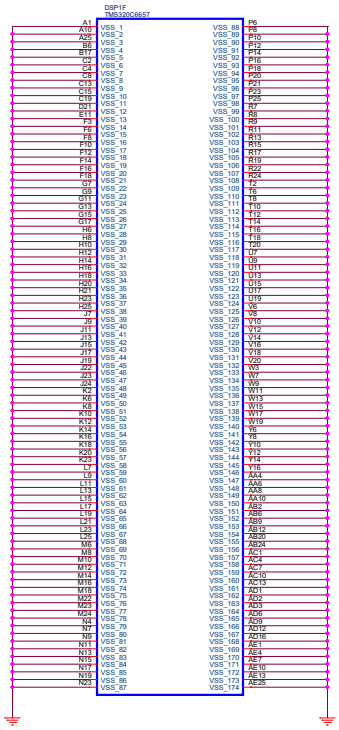
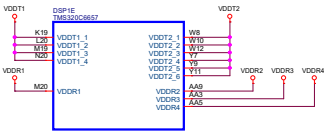
1.0V

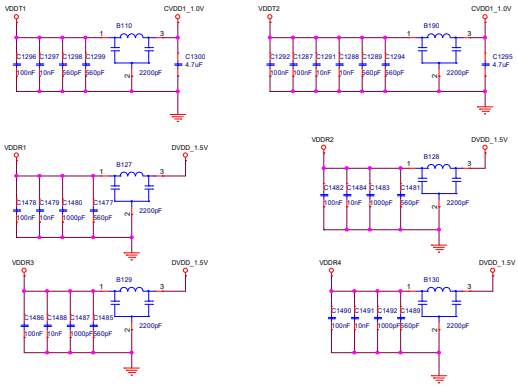


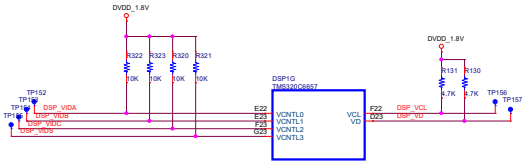
GROUND



1.0V & 1.5V for SERDES







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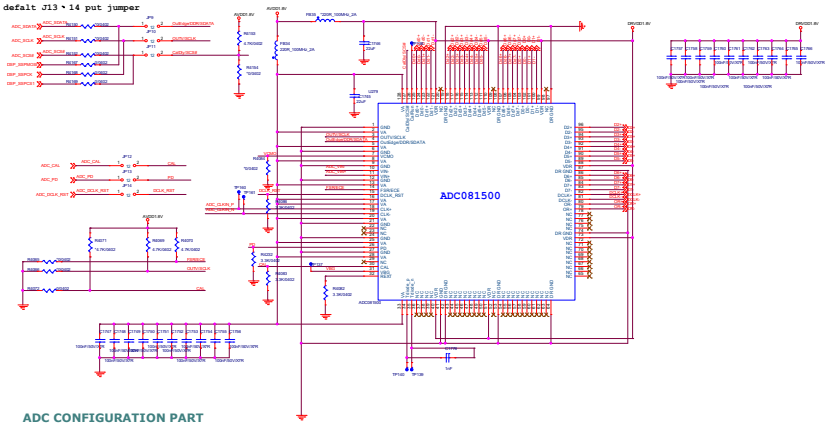
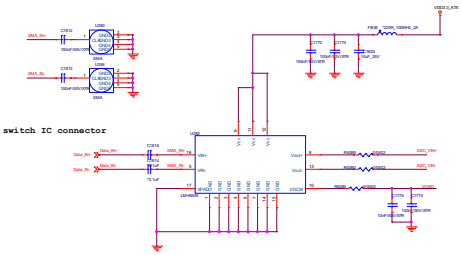
defalt J13、14 put jumper

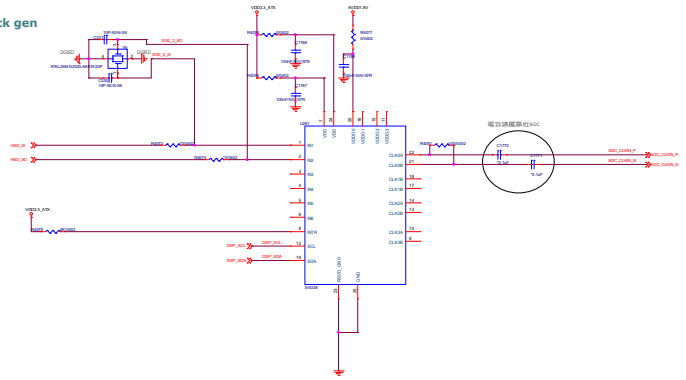


ADC CONFIGURATION PART



Front end

ADC Clock gen



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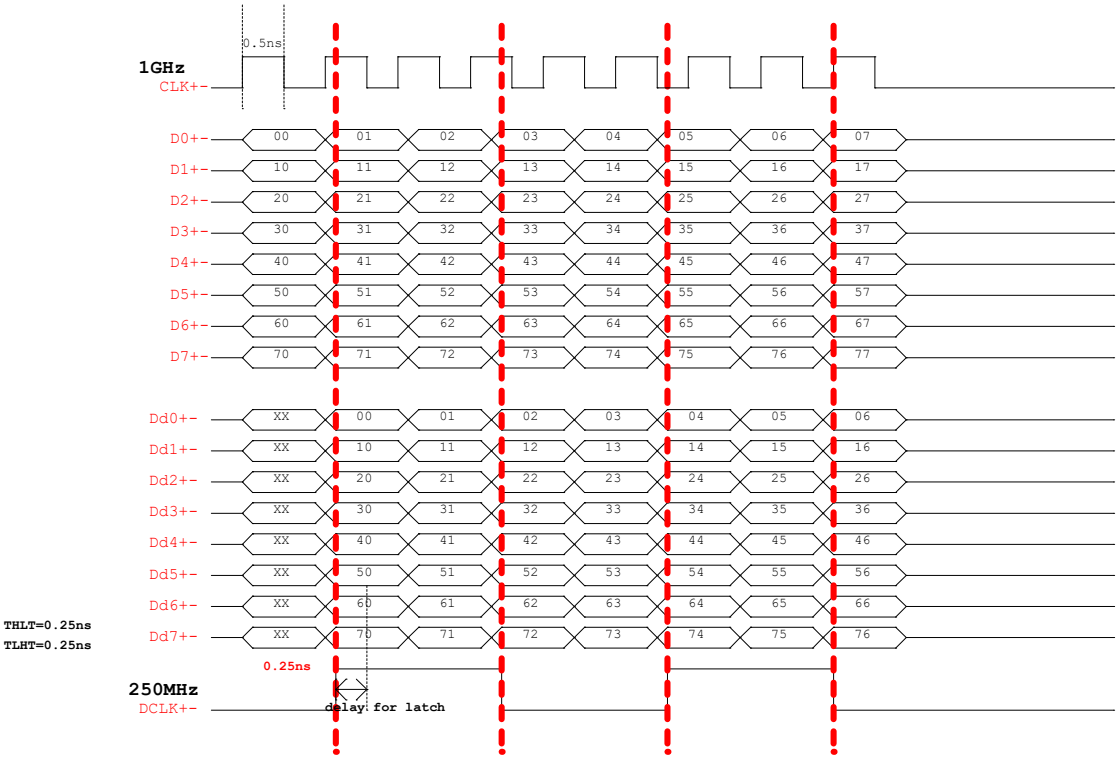

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GPIO18 19 24 25 控制 switch

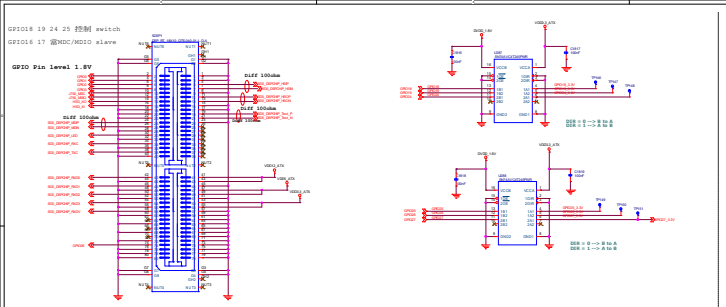
GPIO16 17 做MDC/MDIO slave

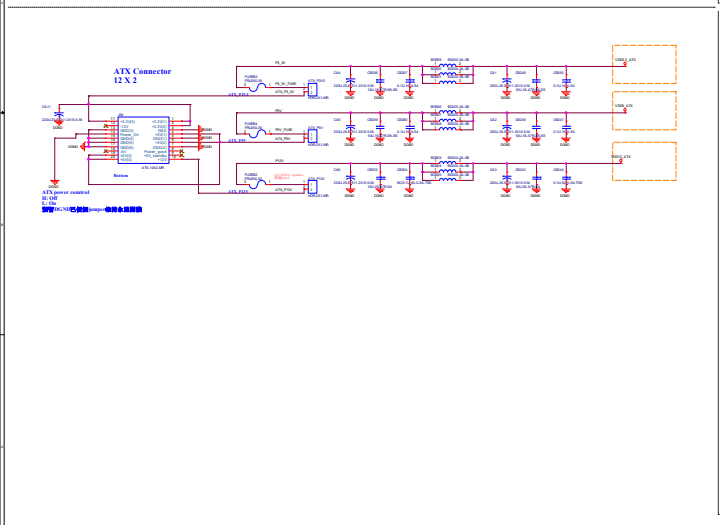
GPIO Pin level 1.8V

Diff 100ohm

Diff 100ohm

Diff 100ohm





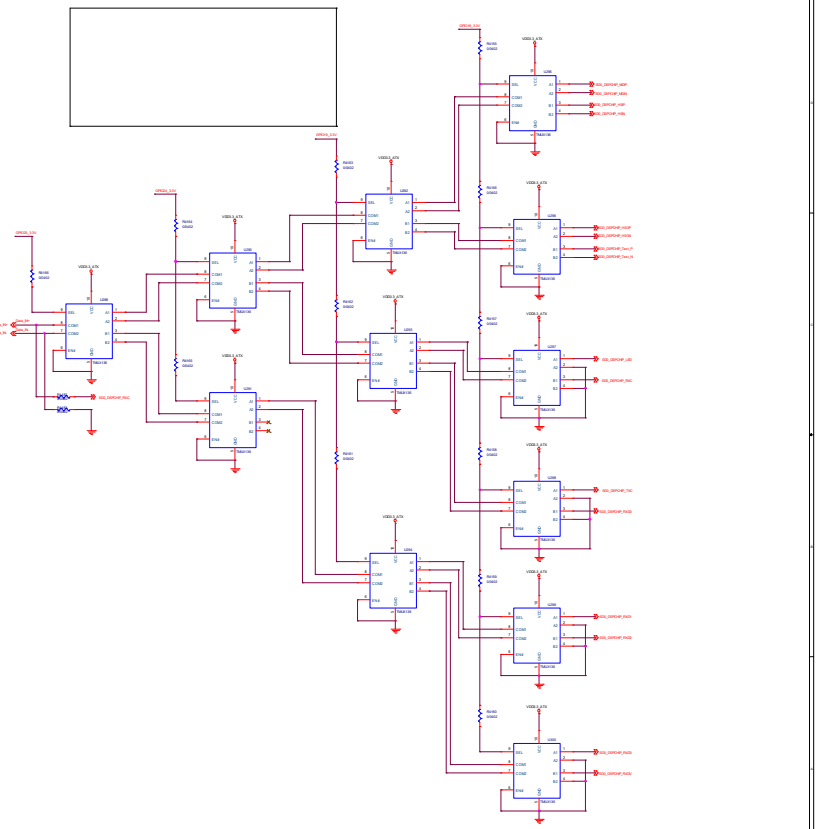
ATX Connector

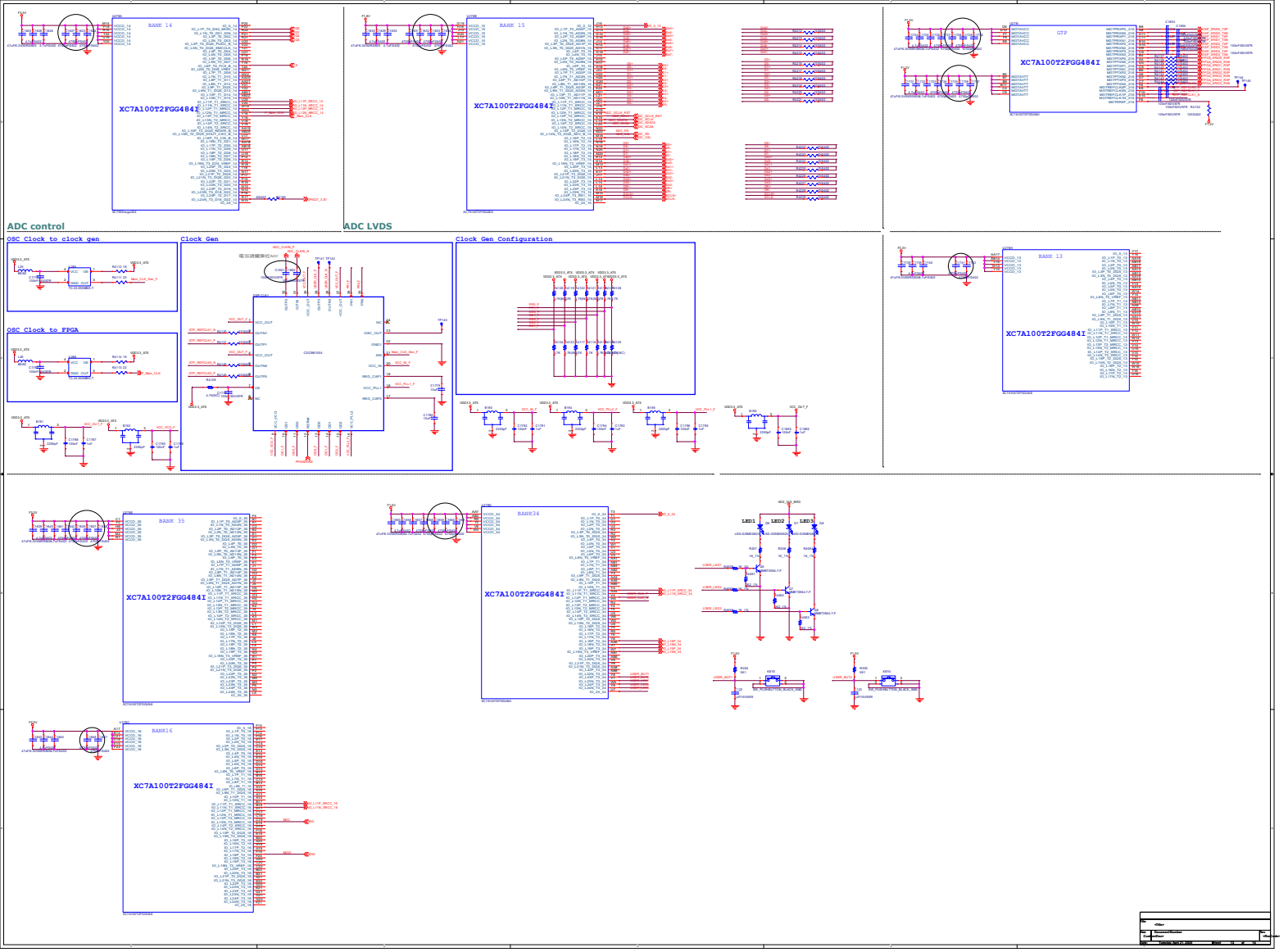
12 X 2

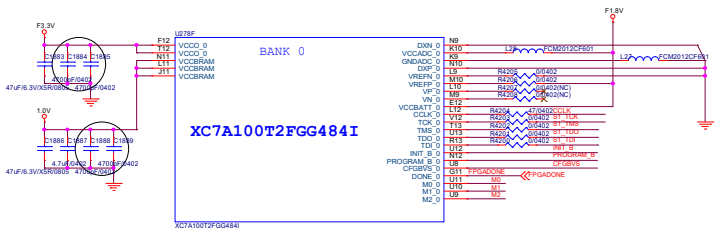
ATX power control

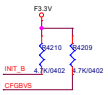
SI: I/O

SO: I/O

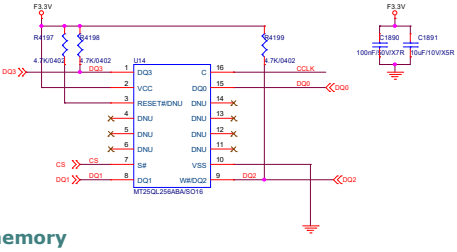



ADC control
ADC LVDS
OSC Clock to clock gen
Clock Gen
Clock Gen Configuration
OSC Clock to FPGA
XC7A100T2FGG484I
BANK 14
BANK 15
BANK 13
BANK 35
BANK34
BANK16
GTP
LED1
LED2
LED3

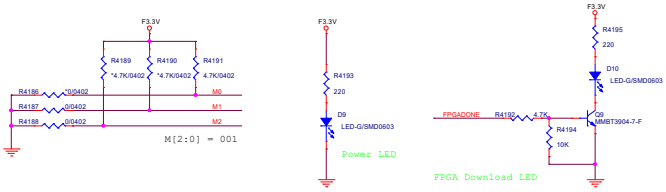




CHIP CONFIGURATION PART

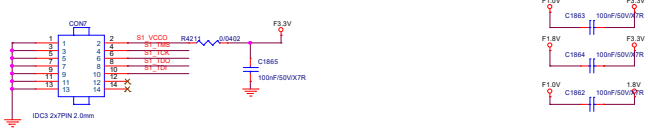


SPI Flash memory

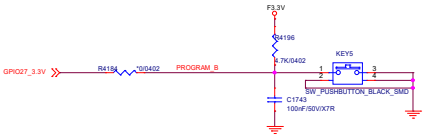


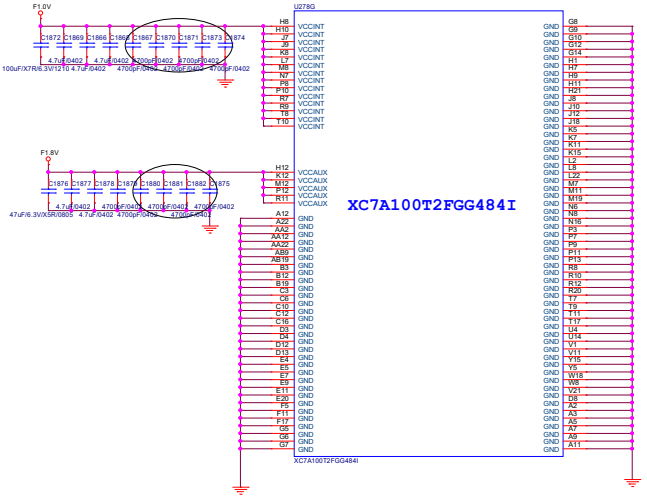
BOOT SET

JTAG



PRG RESET





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