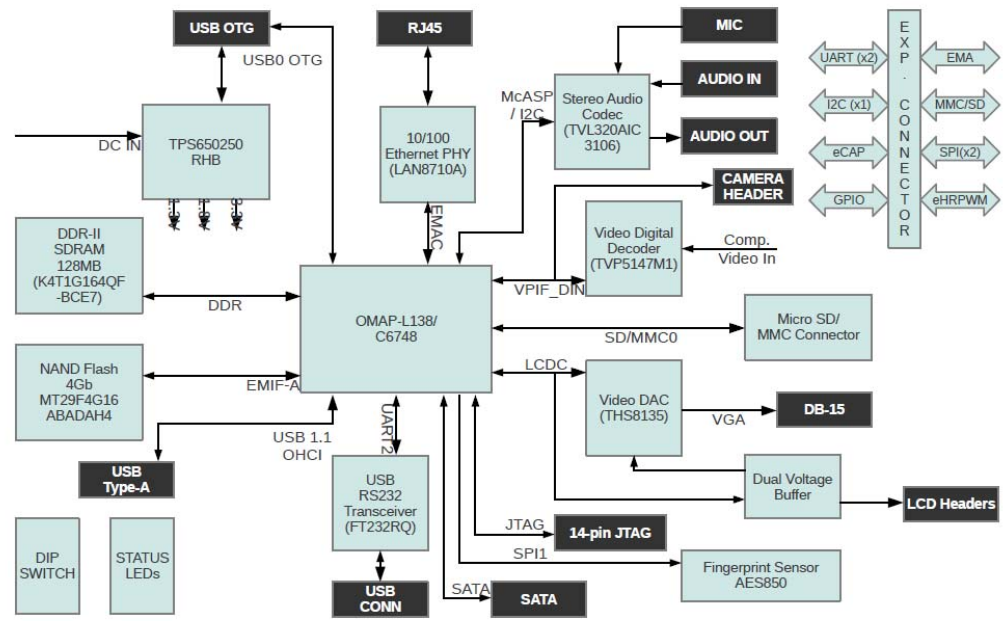
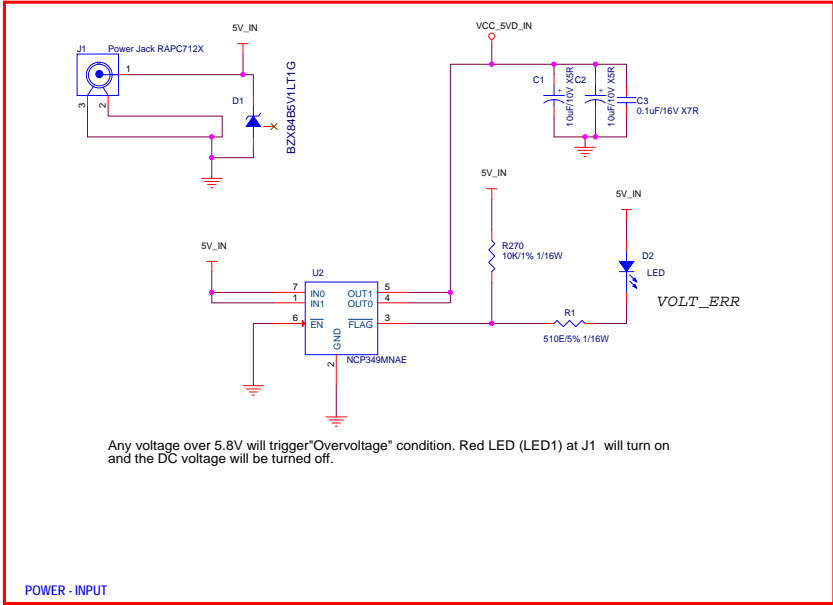


OMAP-L138/C6748 LC Dev Kit

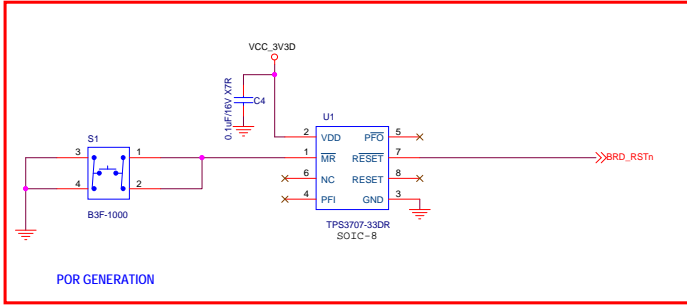
VER/REV #	DESCRIPTION	PREPARED BY	RELEASE DATE	APPROVED BY
A	Initial Release	CCO	17-Oct-2011	TI
A1	BOOT PIN PULLUPS CHNAGED TO 5.6K. DNI PARTS UPDATED	CCO	15-NOV-2011	TI
A2	Issue with U27 resolved. Added D8 in place of R269. Added a 10K pullup to U2-3.	CCO	04-DEC-2011	TI
A3	JTAG circuit changed	CCO	14-DEC-2011	TI
A4	LAN8710A symbol corrected. Added pullups.	CCO	16-DEC-2011	TI
A5	Connect RVDD0/I2 to VCC_1V3D instead of 1V2_LDO The capacitor C107 connected to VCC_3V3ADAC	CCO	22-FEB-2012	TI
A6	U26 is DNled	CCO	14-NOV-2012	TI
A6a	U8 part number corrected to MT29F4G16ABADAH4	CCO	06-MAR-2013	TI
A7E	J10 changed to CX3.5-1230-08, J14&J15 CHANGED TO 2254-501223G0ASUT , P1&P2 CHANGED TO 2127-431210G0CSUT	PTI	03-FEB-2015	TI

PAGE #	PAGE TITLE	PAGE DESCRIPTION
1	TITLE	TITLE OF THE SCHEMATICS
2	TABLE OF CONTENTS	TABLE OF CONTENTS
3	BLOCK DIAGRAM	TOP LEVEL BLOCK DIAGRAM OF THE SCHEMATICS
4	POWER & RESET	COMPLETE POWER SUPPLY CIRCUITRY ON BOARD AND REST CKT
5	DSP POWER AND RS232 IF	DSP POWER PART AND RS232 INTERFACE
6	DSP MEMORY IF & JTAG	DDR-2, FLASH INTERFACE TO THE DSP & JTAG CIRCUITARY
7	DSP PHERIPHERALS & VIDO DAC	DSP PHERIPHERALS & VIDO DAC CIRCUITARY
8	DDR-2 & FLASH	DDR-2 & FLASH DEVICES FOR DSP
9	VIDEO DIGITAL DECODER	VIDEO DIGITAL DECODER CIRCUITARY
10	AUDIO	AUDIO INTERFACE CIRCUITARY
11	ETHERNET	ETHERNET MII INTERFACE
12	EXPANSION CONNECTORS	EXPANSION CONNECTORS FOR PROVIDING EXTERNAL INTERFACE

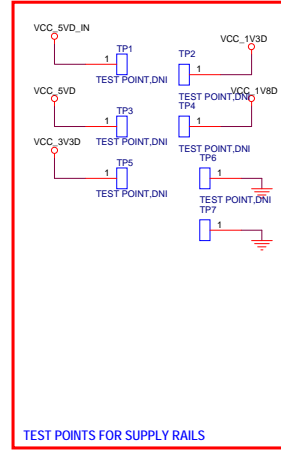




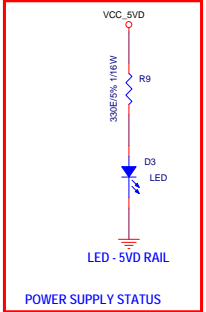
POWER - INPUT



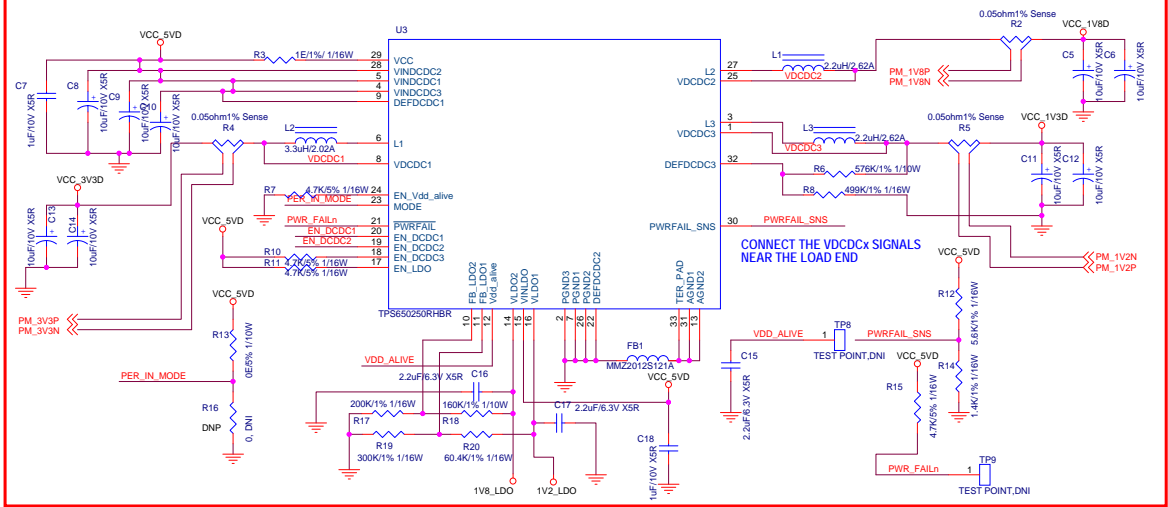
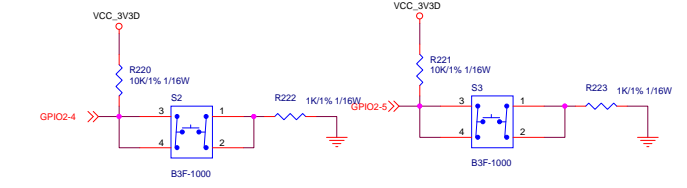
POR GENERATION



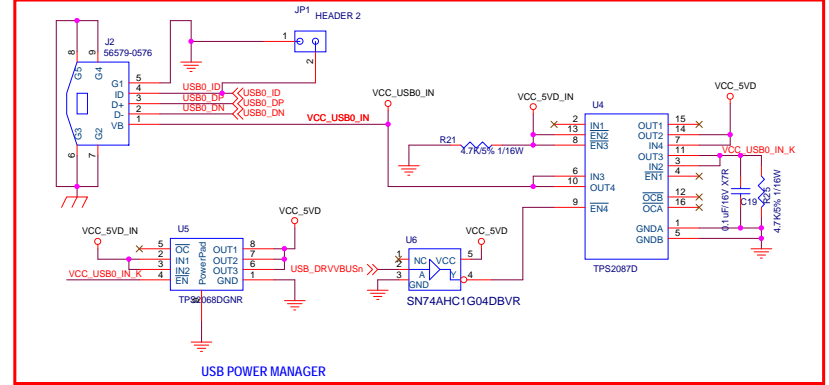
TEST POINTS FOR SUPPLY RAILS



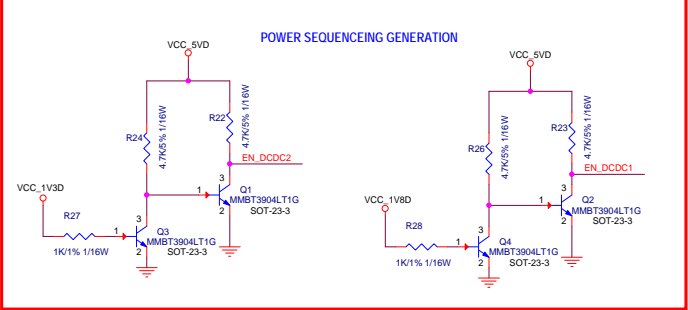
POWER SUPPLY STATUS



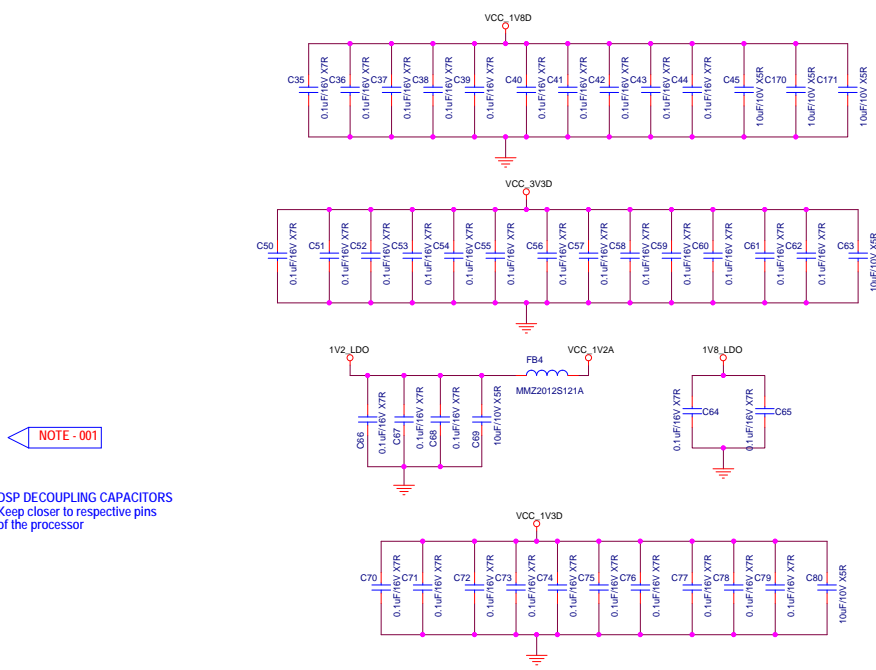
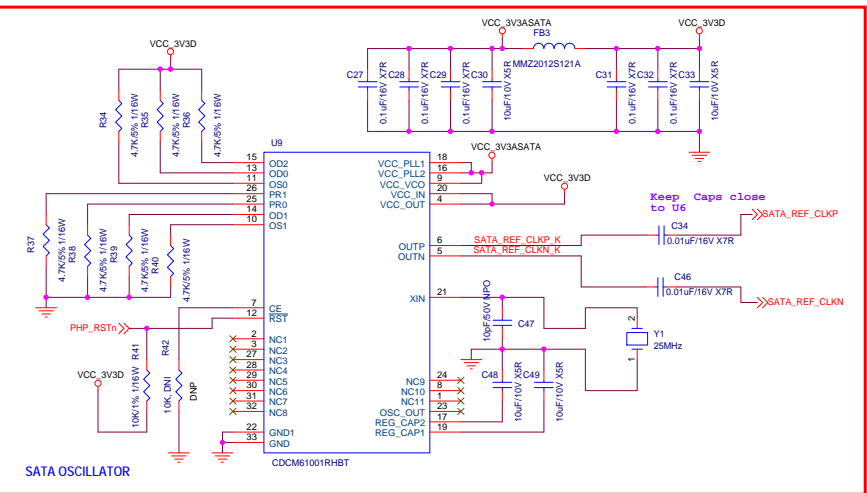
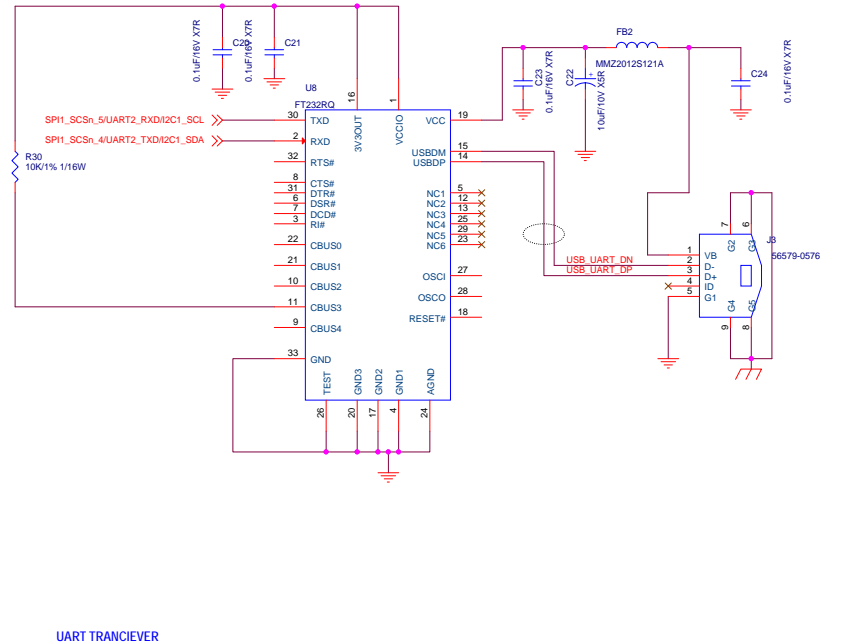
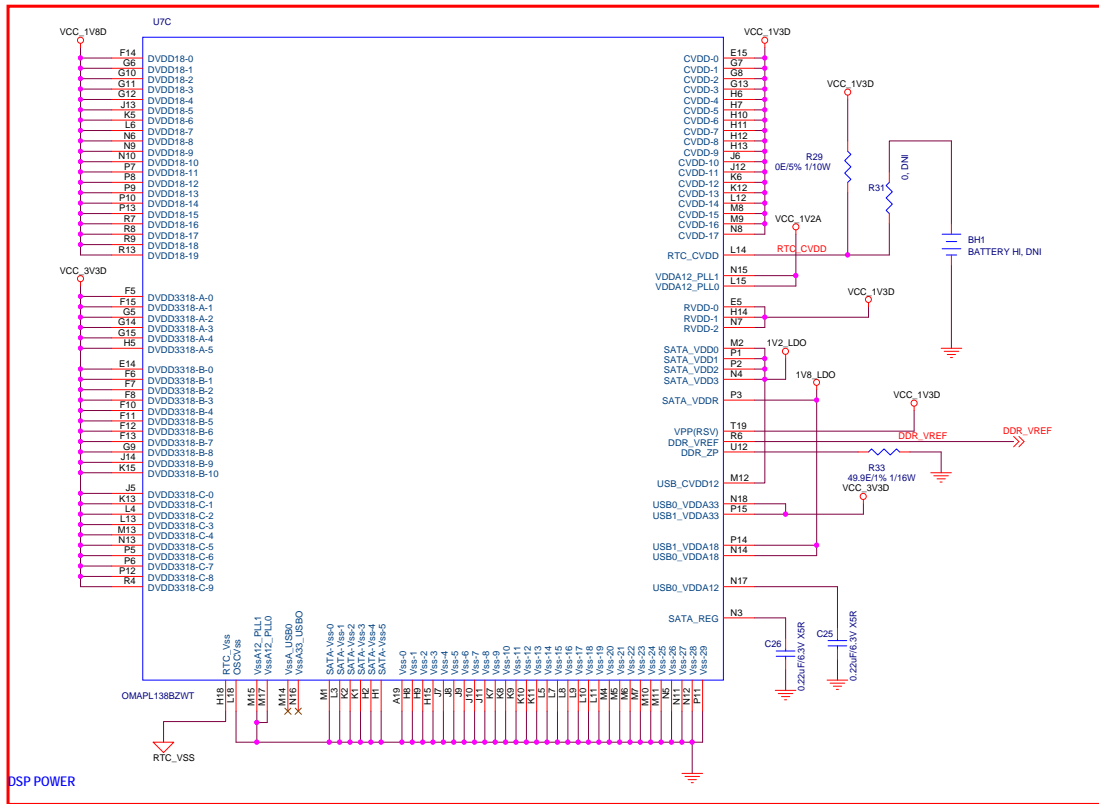
CONNECT THE VDDCCx SIGNALS NEAR THE LOAD END



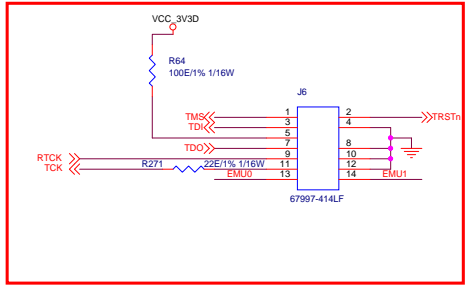
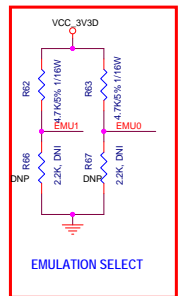
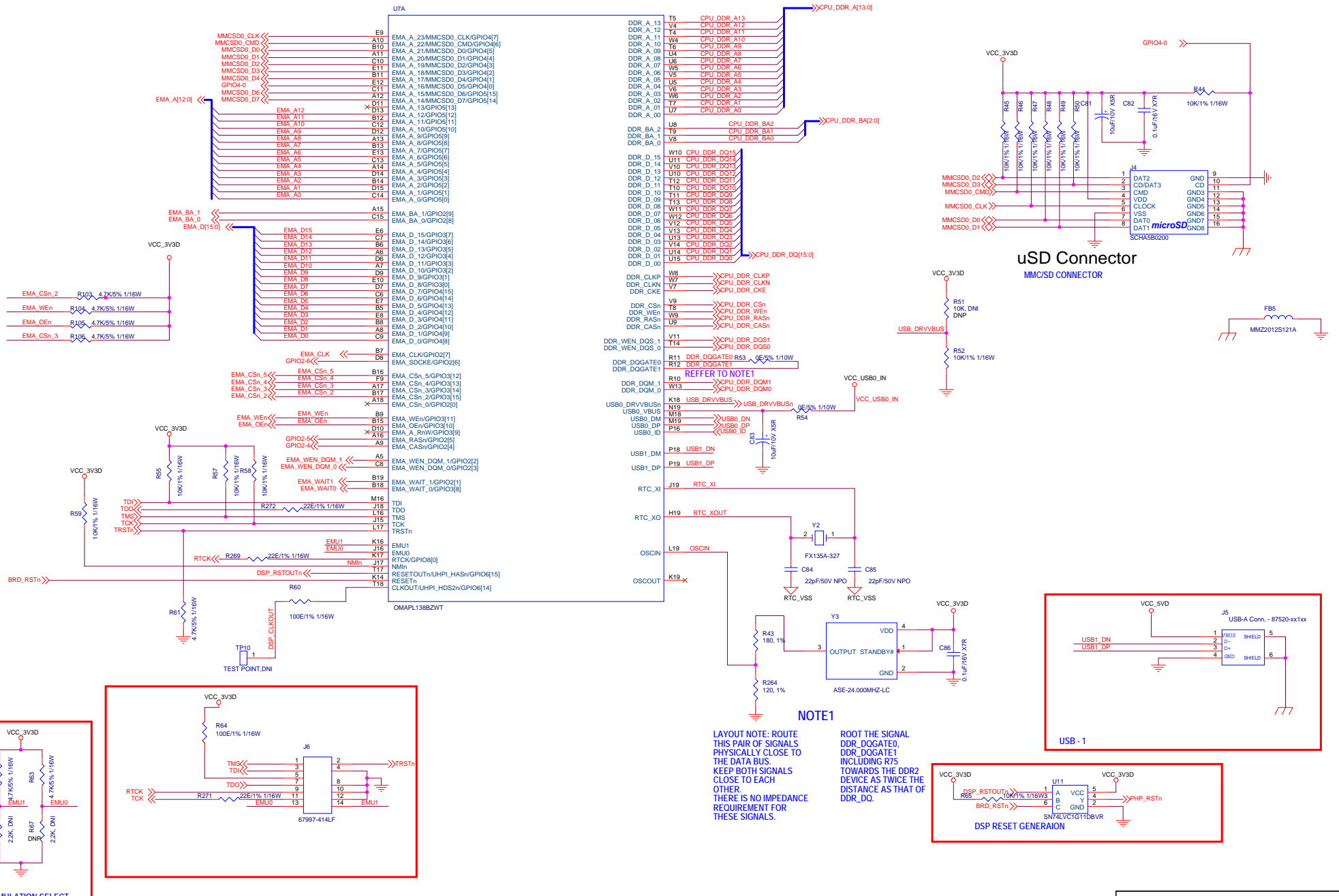
USB POWER MANAGER



POWER SEQUENCING GENERATION



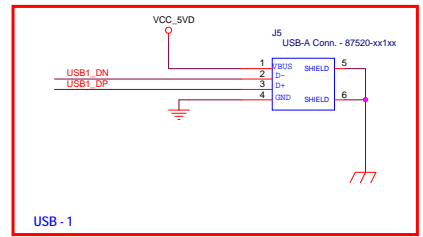
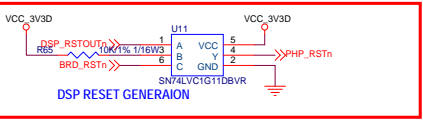
NOTE - 001 ALL DECAPS SHOULD BE PLACE WITHIN 1cm FROM EACH PIN

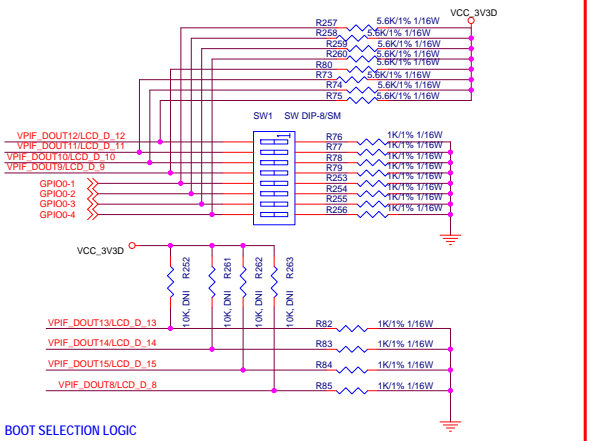
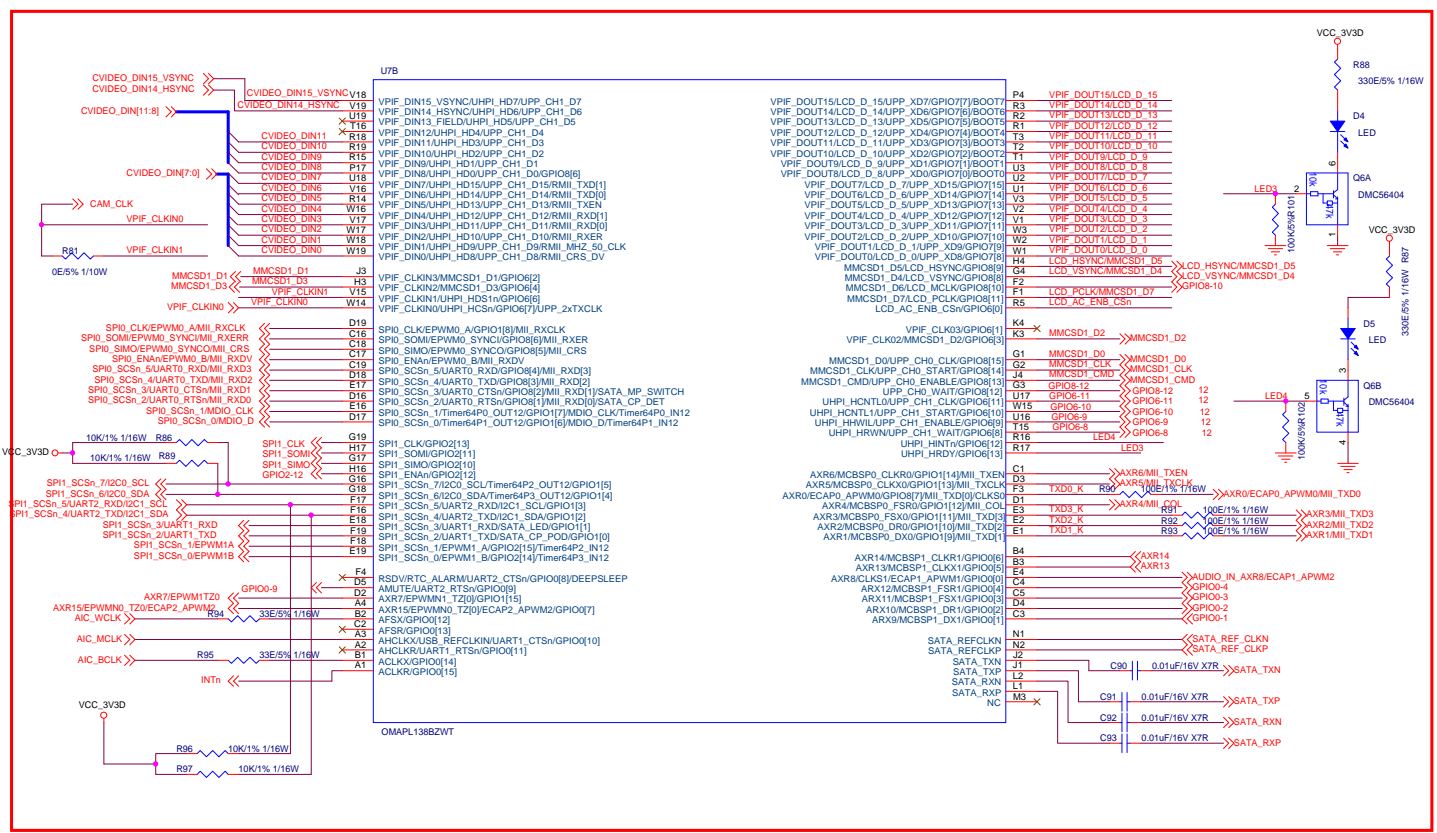


NOTE 1

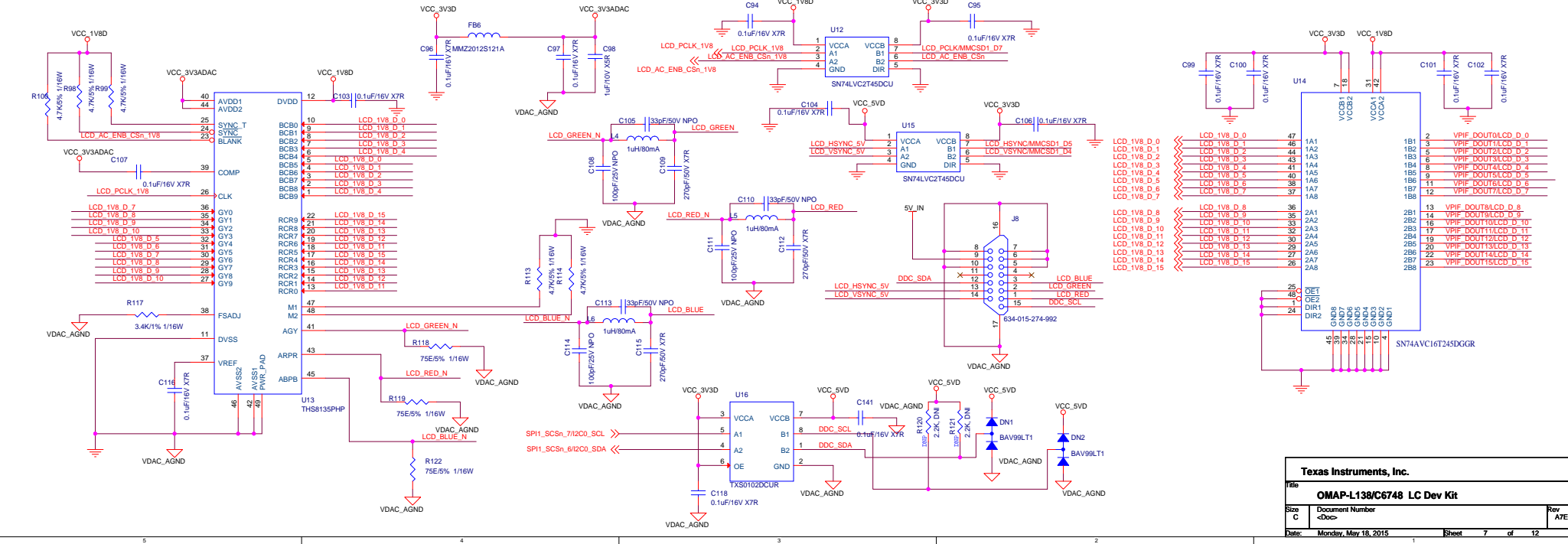
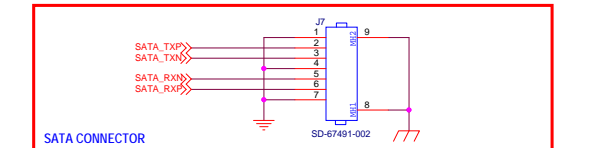
LAYOUT NOTE: ROUTE THIS PAIR OF SIGNALS PHYSICALLY CLOSE TO THE DATA BUS. KEEP BOTH SIGNALS CLOSE TO EACH OTHER. THERE IS NO IMPEDANCE REQUIREMENT FOR THESE SIGNALS.

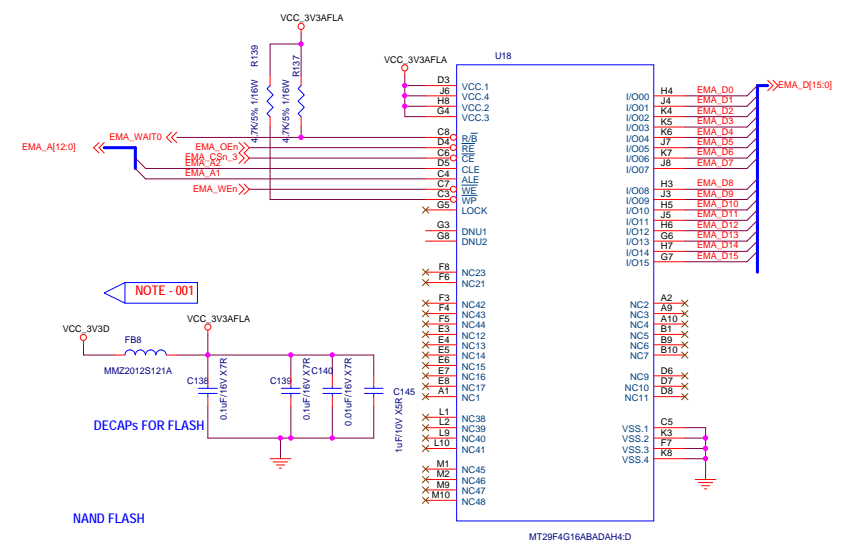
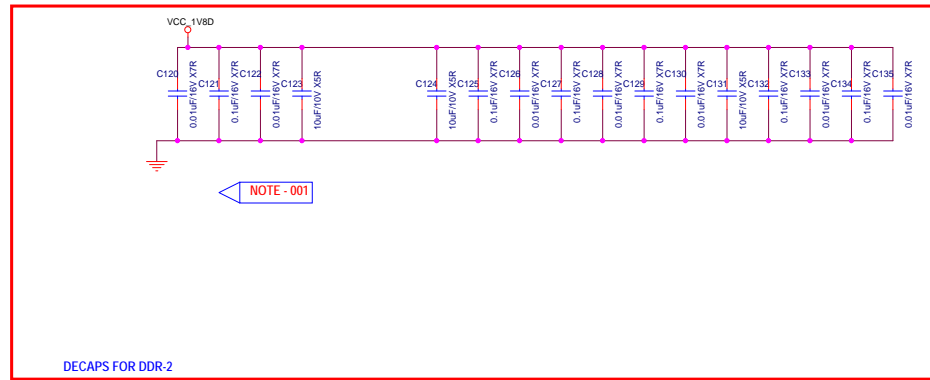
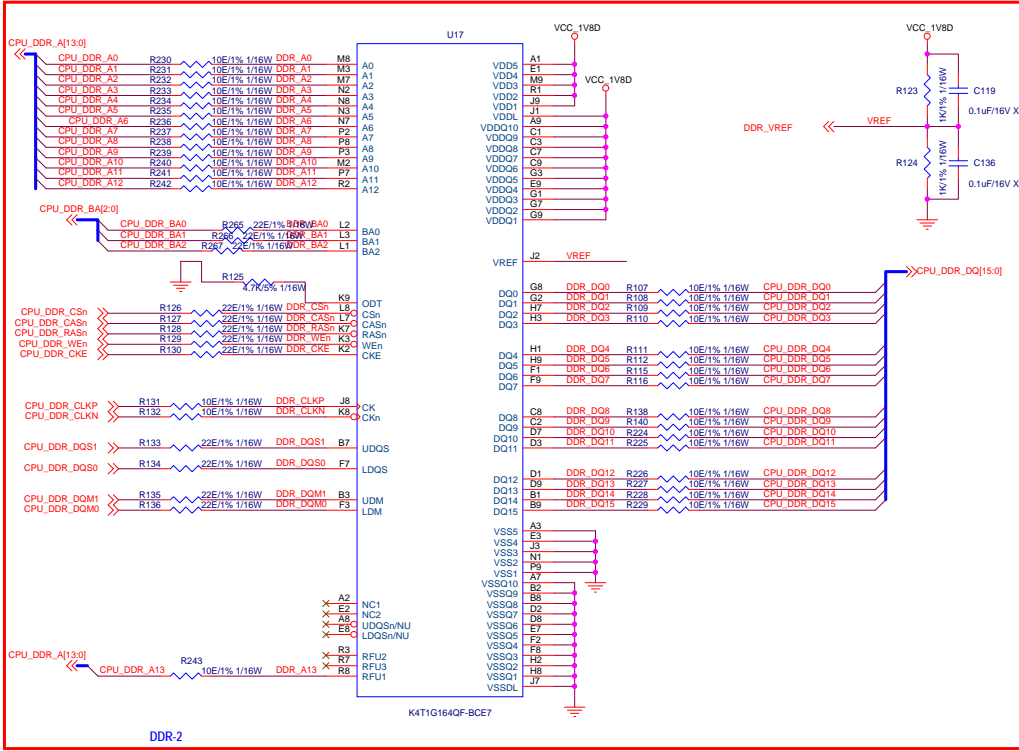
ROOT THE SIGNAL DDR_DQATE0, DDR_DQATE1 INCLUDING R75 TOWARDS THE DDR2 DEVICE AS TWICE THE DISTANCE AS THAT OF DDR_DQ.



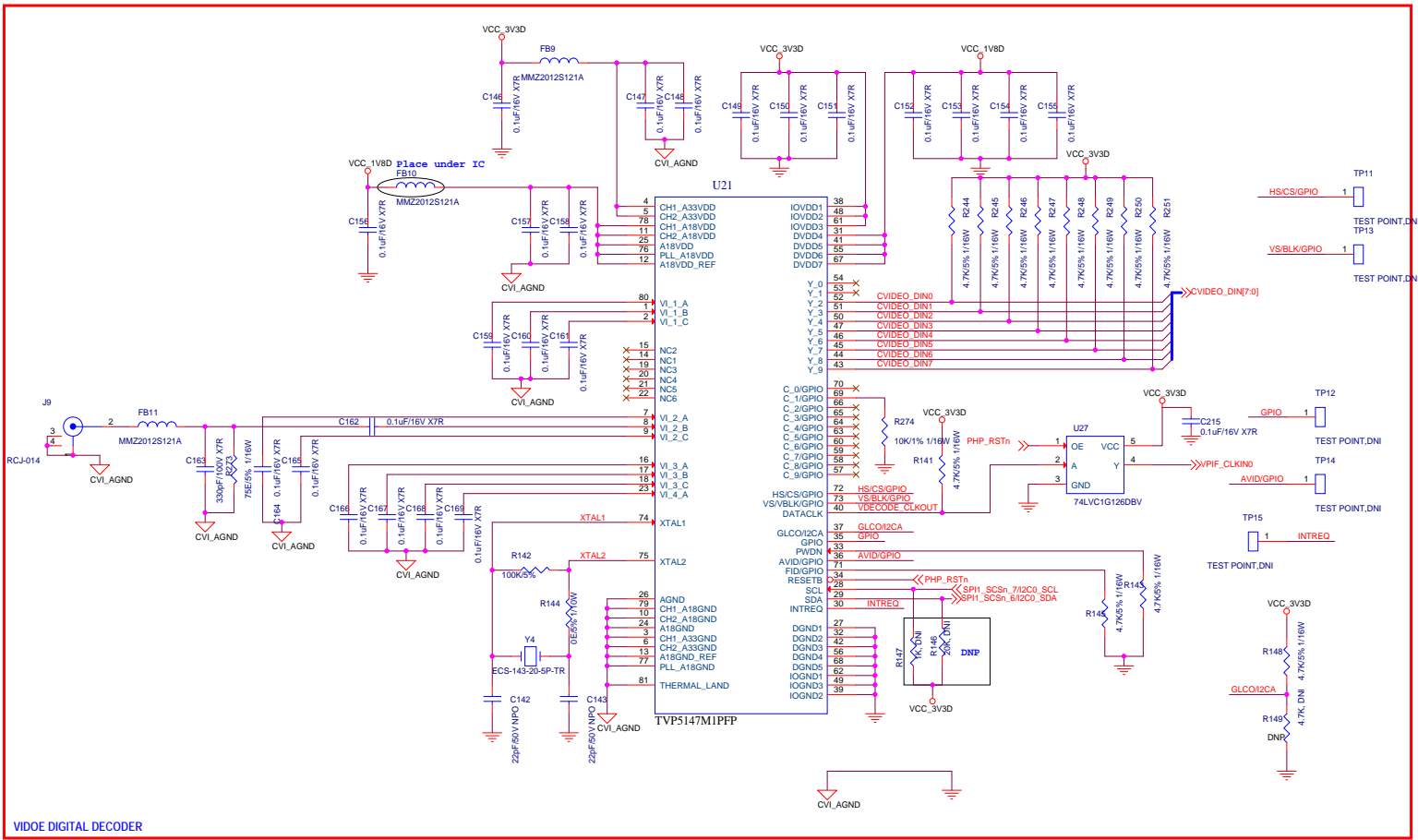


BOOT DEVICE	BOOT BITS [4:1]
NAND FLASH	0111
UART2	1010

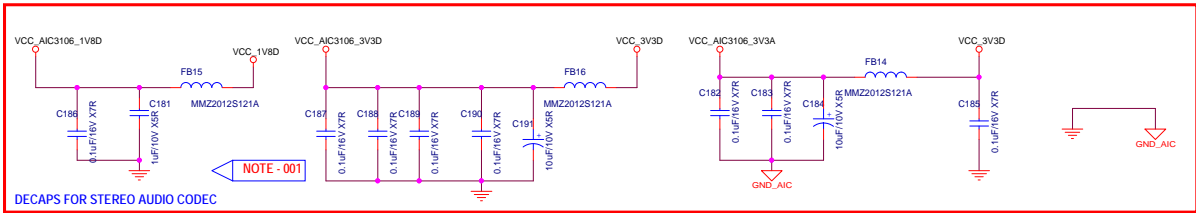
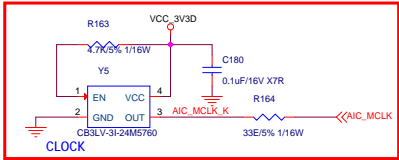
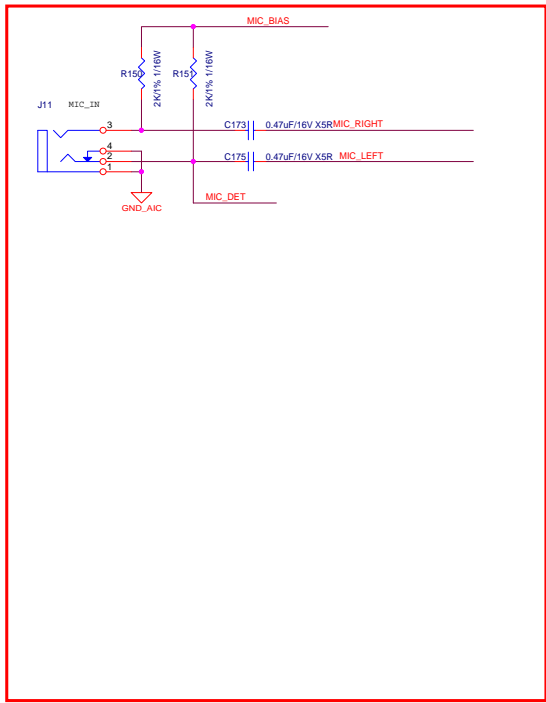
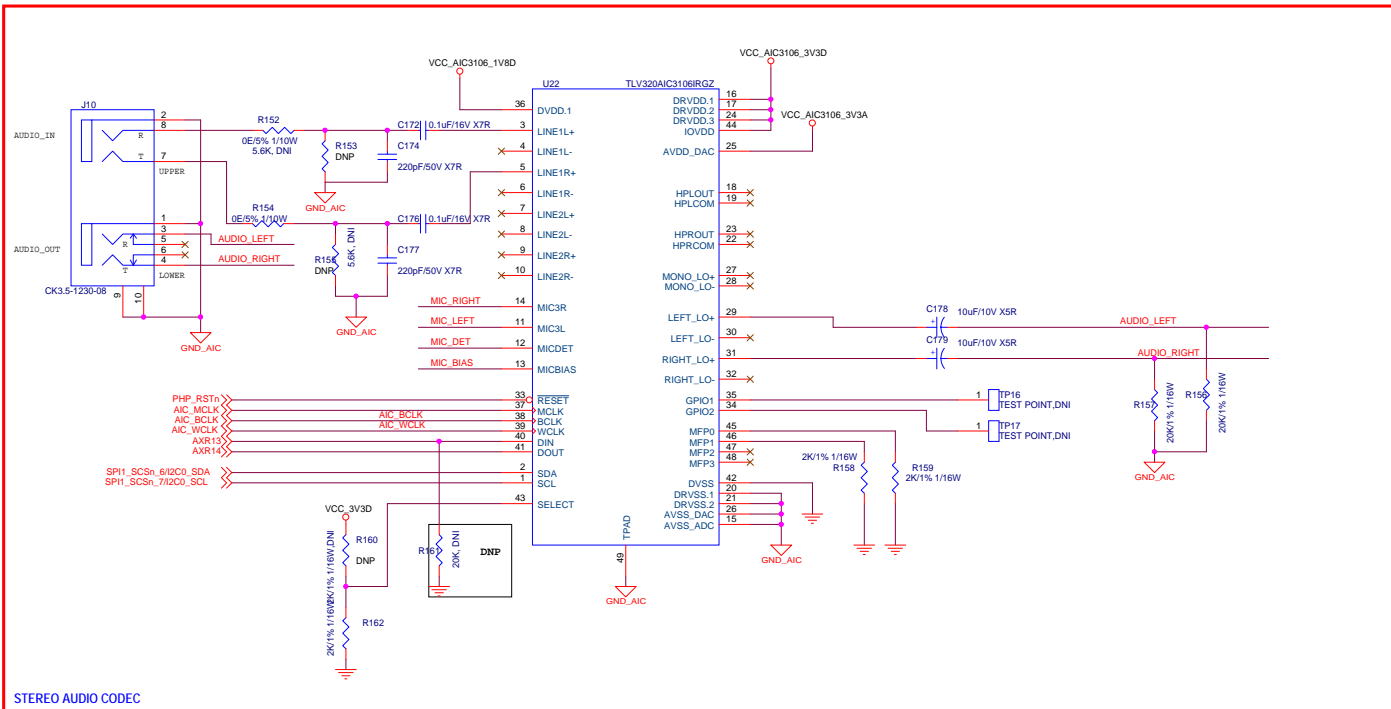




NOTE - 001 ALL DECAPS SHOULD BE PLACE WITHIN 1cm FROM EACH PIN

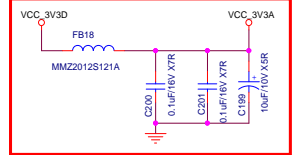
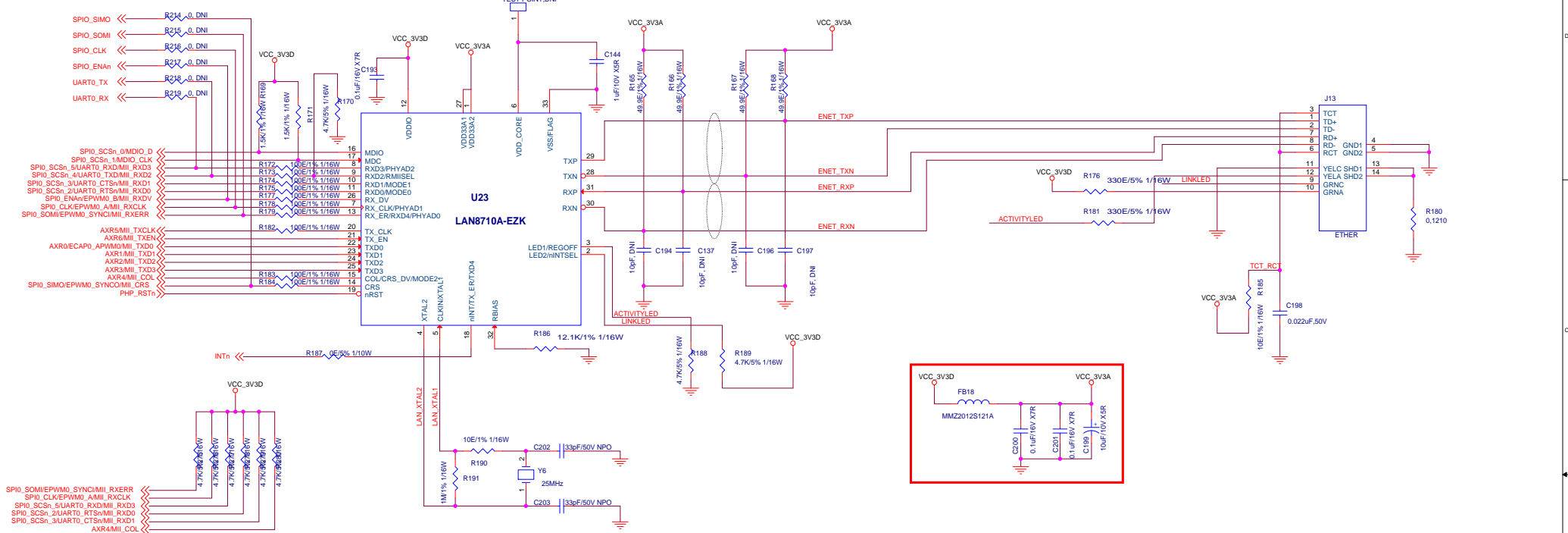


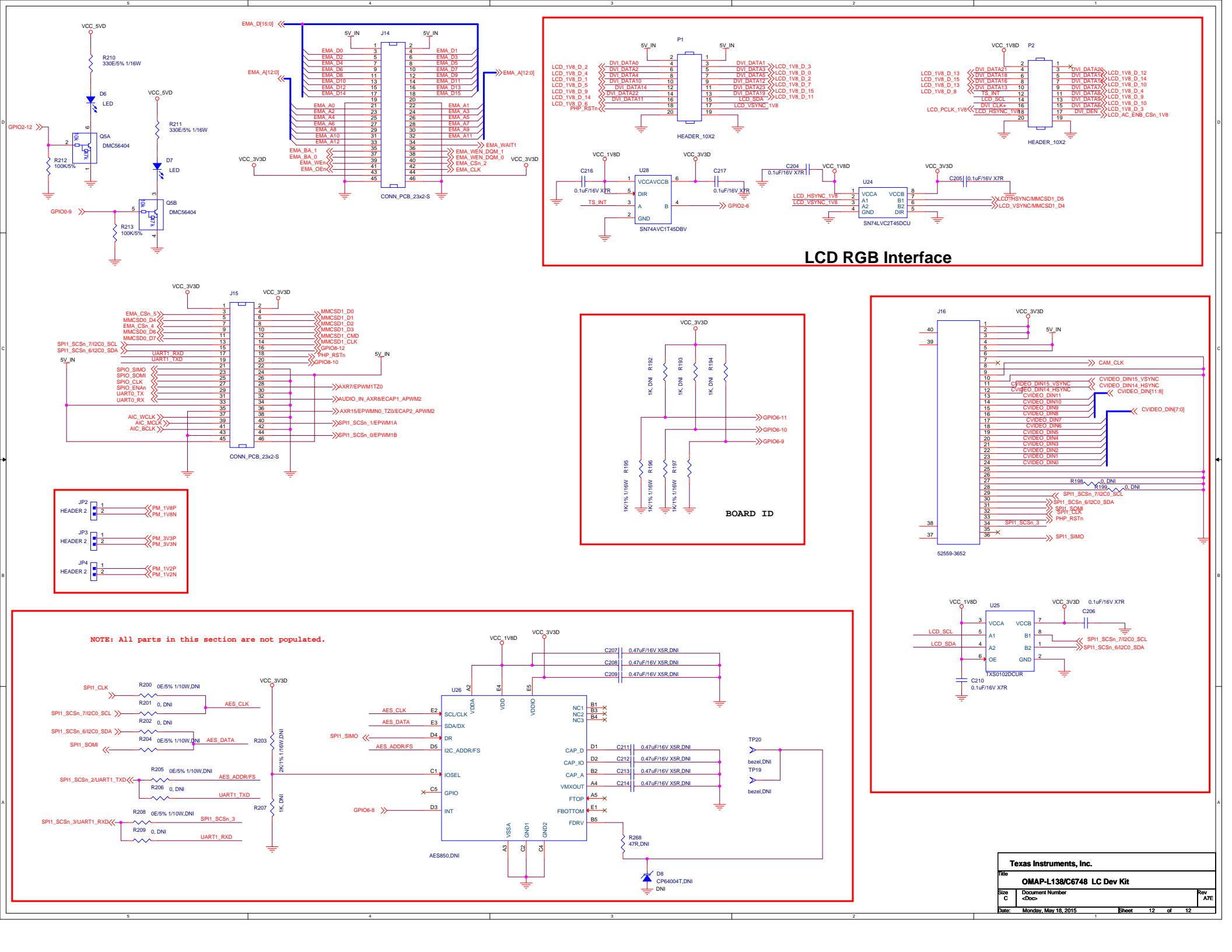
VIDOE DIGITAL DECODER



NOTE - 001 ALL DECAPS SHOULD BE PLACE WITHIN 1cm FROM EACH PIN

Differential Signals 100 Ohms





LCD RGB Interface

BOARD ID

NOTE: All parts in this section are not populated.

Texas Instruments, Inc.		
OMAP-L138/C6748 LC Dev Kit		
File		
Size	Document Number	Rev
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Date:	Monday, May 18, 2015	Sheet 12 of 12