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Preliminary

P21_0120_J721E_DRA829_TDA4VM_CAN_DL_Test_Report_r00d01

Date of Approval: 2021-Sept-20

Test Report

Device Under Test		**Customer**	
Device Name	Jacinto 7 Family	Order No.	P21_0120
Manufacturer	Texas Instruments	Name	Texas Instruments
Type / Version	MCAN v3.2.3	Address	Central expressway Dallas, TX 75243 USA
Sample marking	<sample marking>		

Number of Pages	28
Test Period	from 2021-Mai-20 until <yyyy-Mmm-dd>
Test Method / Test Requirement	CAN Conformance Test
Performed Tests and References	1 ISO CAN Conformance Tests according to "ISO 16845-1:2016 Road vehicles - Controller area network (CAN) - Conformance test plan" and C&S enhancement/corrections according to "C&S Conformance Test CAN – Data Link LayerSpecification C&S Enhancement Tests V06" 2 C&S Register Functionality Tests according to "C&S Register Functionality Test Specification V3.0" 3 C&S Robustness Tests according to "C&S Robustness Test Specification V2.1"

Conformance Test Results	The Test Results refer to the delivered device and the applicable test cases.
1 ISO CAN conformance tests	**Pass**
2 C&S Register Functionality tests	**In progress**
3 C&S Robustness tests	**Pass**

For detailed information see chapter Test List at the following pages.

 A detailed list of all executed test is available in separate document: P21_0120_TI_TDA4-DRA829-J7ES_MCAN_Test List_d00

Approved by	Test performed by
Lothar Kukla, Project Manager	Andreas Meitrodt, Project Engineer

Table of Content

Revision History

Old revision	New revision	Amendment Description	Editor
–	00	Initial version	AM
00	01	Add ROB-Test result	AM

1 Device Under Test (detailed)

General	
Date of Sample Arrival	19.04.2021
Manufacturer	Texas Instruments
Sample Marking	<sample marking>
Test performed with DUT no.	1

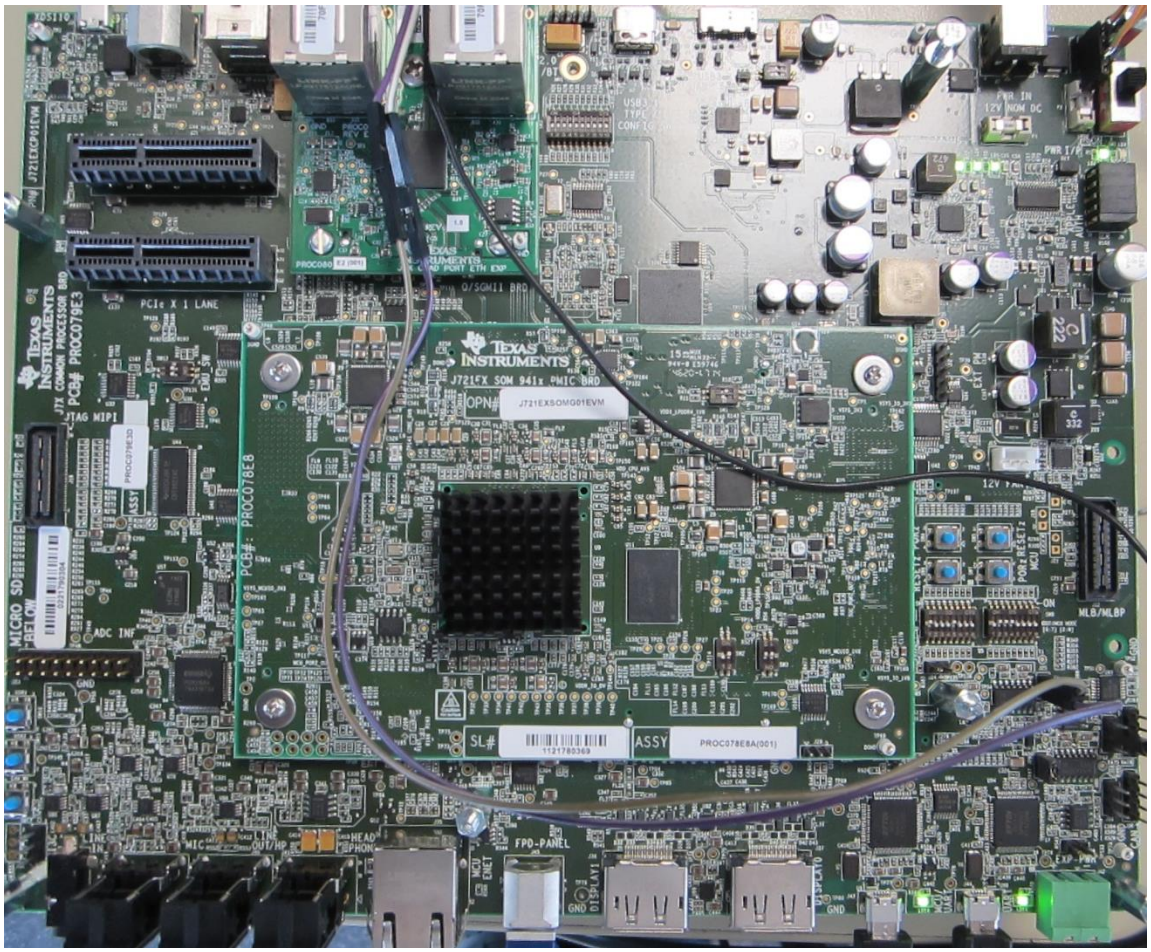
Device Specification	
Device Name	Jacinto 7 Family
Type / Version	MCAN v3.2.3
Design step	
HW-Version	
SW-Version	

Documentation	
Hardware manual	
User manual / datasheet	

Device Classification	
Evaluation board version	
Quartz / crystal oscillator with	<xxx> MHz
CAN clock bit timing	80 MHz
CAN clock ISO, RF, ROB	80 MHz
CAN clock tolerance	-

Software Specification	
Emulator version	XDS110
IDE version	Code Composer Studio Version: 10.3.1.00003
Compiler version	Code Composer Studio Version: 10.3.1.00003
Flash tool version	XDS110
UT name	csgwflr166
LT name	csgwflr162

2 Setup for Device Under Test



3 Test Equipment

The following test equipment and test system have been used.

No.	Component	Manufacturer	Version / Type	ID
1	C&S CAN Conformance Tester	C&S		
Test System 5				
2	Logic Analyzer System	Agilent	16702B	700046
3	Pattern Generator	Agilent	16720A	700048
4	Logic Analyzer Card	Agilent	16911A	700057
5	Clock-Pod	Agilent	10460A	500014
6	Data-Pod	Agilent	10462A	500038
7	CAN Card	Vector	CANboardXL	-
8	Coupler Box	C&S	Version 6.0	CSHW000045
9	CAN bus cable length	C&S	40cm	

4 Technical Correspondence

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5 Test List: ISO16845-1 TEST CLASSES 1 – 6

The ISO16845-1 pointed out a CAN Version for which a test case is applicable. CAN Implementations supporting CAN FD are often also support classical CAN. So the tests are performed in different IUT modes, for classical CAN and for CAN FD enabled. The resulting test combinations are:

- IUT in classical CAN mode and tests applied for classical CAN, in short "CC_CC".
- IUT in CAN FD mode and tests applied for classical CAN, in short "FD_CC".
- IUT in CAN FD mode and tests applied for CAN FD, in short "FD_FD".

The meaning of greyed fields in result Colum is that for the given IUT mode and Frame format combination is no test defined.

Following "Ref." numeration relates on the corresponding test specification ISO16845-1.

Ref.	Description	Result CC_CC	Result FD_CC	Result FD_FD	Comment
7	**Test type 1, Received frame**				
7.1	**Test class 1, valid frame format**				
7.1.1	Identifier and number of data test in base format	45 PASS	45 PASS	80 PASS	
7.1.2	Identifier and number of data test in extended format	45 PASS	45 PASS	80 PASS	
7.1.3	Reception after arbitration lost	6 PASS	6 PASS	4 PASS	
7.1.4	Acceptance of non-nominal Bit in base format frame	1 PASS		1 PASS	
7.1.5	Acceptance of non-nominal Bit in extended format frame	7 PASS	3 PASS	3 PASS	
7.1.6	Protocol exception behaviour on non-nominal Bit			2 PASS	
7.1.7	Minimum time for bus idle after protocol exception handling			6 PASS	
7.1.8	DLC greater than 8	7 PASS	7 PASS		
7.1.9	Absent bus idle – valid frame reception	2 PASS	2 PASS	2 PASS	
7.1.10	Stuff acceptance test in base format frame	10 PASS	10 PASS	10 PASS	

Ref.	Description	Result CC_CC	Result FD_CC	Result FD_FD	Comment
7.1.11	Stuff acceptance test in extended format frame	7 PASS	7 PASS	11 PASS	
7.1.12	Message validation	1 PASS	1 PASS	1 PASS	
7.1.13_cs	Form field tolerance test for FD frame format (C&S)			1 PASS	
7.2	**Test class 2, error detection**				
7.2.1	Bit error in data frame	1 PASS	1 PASS	1 PASS	
7.2.2	Stuff error for basic frame	64 PASS	59 PASS	40 PASS	
7.2.3	Stuff error for extended frame	91 PASS	86 PASS	88 PASS	
7.2.4	Stuff error for FD frame payload Bytes			168 PASS	
7.2.5	CRC error	3 PASS	3 PASS	6 PASS	
7.2.6	Combination of CRC error and form error	2 PASS	2 PASS	4 PASS	
7.2.7	Form error in data frame at "CRC Delimiter" bit position	1 PASS	1 PASS	1 PASS	
7.2.8	Form error at fixed stuff bit in FD frames			26 PASS	
7.2.9	Form error in data frame at "ACK Delimiter" bit position	1 PASS	1 PASS	1 PASS	
7.2.10	Form error in data frame at "EOF"	5 PASS	5 PASS	5 PASS	
7.2.11	Message non-validation	1 PASS	1 PASS	1 PASS	
7.3	**Test class 3, error frame management**				
7.3.1	Error flag longer than 6 bits	3 PASS	3 PASS	3 PASS	
7.3.2	Data frame starting on the third bit of intermission field	1 PASS	1 PASS	1 PASS	
7.3.3	Bit error in error flag	3 PASS	3 PASS	3 PASS	
7.3.4	Form error in error delimiter	3 PASS	3 PASS	3 PASS	

Ref.	Description	Result CC_CC	Result FD_CC	Result FD_FD	Comment
7.4	**Test class 4, overload frame management**				
7.4.1	MAC overload generation during intermission field	2 PASS	2 PASS	2 PASS	
7.4.2	Last bit of EOF	1 PASS	1 PASS	1 PASS	
7.4.3	Eighth bit of an error and overload delimiter	2 PASS	2 PASS	2 PASS	
7.4.4	Bit error in overload flag	3 PASS	3 PASS	3 PASS	
7.4.5	Form error in overload delimiter	3 PASS	3 PASS	3 PASS	
7.4.6	MAC overload generation during intermission field following an error frame	2 PASS	2 PASS	2 PASS	
7.4.7	MAC overload generation during intermission field following an overload frame	2 PASS	2 PASS	2 PASS	
7.5	**Test class 5, passive error state class**				
7.5.1	passive error flag completion test 1	3 PASS	3 PASS	3 PASS	
7.5.2	Data frame acceptance after passive error frame transmission	1 PASS	1 PASS	1 PASS	
7.5.3	Acceptance of 7 consecutive dominant bits after passive error flag	3 PASS	3 PASS	3 PASS	
7.5.4	passive state unchanged on further errors	1 PASS	1 PASS	1 PASS	
7.5.5	passive error flag completion – test case 2	3 PASS	3 PASS	3 PASS	
7.5.6	Form error in passive error delimiter	3 PASS	3 PASS	3 PASS	
7.5.7	Transition from active to passive ERROR FLAG	1 PASS	1 PASS	1 PASS	
7.6	**Test class 6, error counter management**				
7.6.1	REC increment on bit error in active error flag	3 PASS	3 PASS	3 PASS	
7.6.2	REC increment on bit error in overload flag	3 PASS	3 PASS	3 PASS	
7.6.3	REC increment when active error flag is longer than 13 bits	1 PASS	1 PASS	1 PASS	
7.6.4	REC increment when overload flag is longer than 13 bits	1 PASS	1 PASS	1 PASS	
7.6.5	REC increment on bit error in the ACK field	1 PASS	1 PASS	1 PASS	

Ref.	Description	Result CC_CC	Result FD_CC	Result FD_FD	Comment
7.6.6	REC increment on form error in CRC delimiter	1 PASS	1 PASS	1 PASS	
7.6.7	REC increment on form error in ACK delimiter	1 PASS	1 PASS	1 PASS	
7.6.8	REC increment on form error in EOF field	3 PASS	3 PASS	3 PASS	
7.6.9	REC increment on stuff error	8 PASS	8 PASS	6 PASS	
7.6.10	REC increment on CRC error	3 PASS	3 PASS	8 PASS	
7.6.11	REC increment on dominant bit after end of error flag	1 PASS	1 PASS	1 PASS	
7.6.12	REC increment on form error in error delimiter	2 PASS	2 PASS	2 PASS	
7.6.13	REC increment on form error in overload delimiter	2 PASS	2 PASS	2 PASS	
7.6.14	REC decrement on valid frame reception	1 PASS	1 PASS	1 PASS	
7.6.15	REC decrement on valid frame reception during passive state	1 PASS	1 PASS	1 PASS	
7.6.16	REC non-increment on last bit of EOF field	1 PASS	1 PASS	1 PASS	
7.6.17	REC non-increment on 13-bit length overload flag	1 PASS	1 PASS	1 PASS	
7.6.18	REC non-increment on 13-bit length error flag	1 PASS	1 PASS	1 PASS	
7.6.19	REC non-increment on last bit of error delimiter	1 PASS	1 PASS	1 PASS	
7.6.20	REC non-increment on last bit of overload delimiter	1 PASS	1 PASS	1 PASS	
7.6.21	REC non-decrement on transmission	1 PASS	1 PASS	1 PASS	
7.6.22	REC increment on form error at fixed stuff bit in FD frames			4 PASS	
7.6.23	REC non increment on protocol exception in FD frames			2 PASS	
8	**Test Type 2, transmitted frame**				
8.1	**Test class 1, valid frame format**				
8.1.1	Identifier and number of data bytes test in base format	45 PASS	45 PASS	80 PASS	
8.1.2	Identifier and number of data bytes test in extended format	45 PASS	45 PASS	80 PASS	

Ref.	Description	Result CC_CC	Result FD_CC	Result FD_FD	Comment
8.1.3	Arbitration in base format frame	12 PASS	12 PASS	11 PASS	
8.1.4	Arbitration in extended format frame test	32 PASS	32 PASS	31 PASS	
8.1.5	Message validation	1 PASS	1 PASS	1 PASS	
8.1.6	Stuff bit generation capability in base format frame	6 PASS	6 PASS	10 PASS	
8.1.7	Stuff bit generation capability in extended frame	3 PASS	3 PASS	10 PASS	
8.1.8	Transmission on the third bit of intermission field after arbitration lost	2 PASS	2 PASS	4 PASS	
8.1.9	TRANSMISSION AFTER MINIMUM TIME FOR BUS IDLE AFTER PROTOCOL		3 PASS	3 PASS	
8.2	**Test class 2, error detection**				
8.2.1	Bit error test in base format frame	13 PASS	13 PASS	24 PASS	
8.2.2	Bit error in extended format frame	14 PASS	14 PASS	24 PASS	
8.2.3	Stuff error test in base format frame	35 PASS	35 PASS	39 PASS	
8.2.4	Stuff error test in extended frame format	35 PASS	35 PASS	79 PASS	
8.2.5	Form error test	5 PASS	5 PASS	18 PASS	
8.2.6	Acknowledgement error	1 PASS	1 PASS	1 PASS	
8.2.7	Form field tolerance test for FD frame format			2 PASS	
8.2.8	Bit error at stuff bit position for FD frame payload Bytes			168 PASS	

Ref.	Description	Result CC_CC	Result FD_CC	Result FD_FD	Comment
8.3	**Test class 3, error frame management**				
8.3.1	Error flag longer than 6 bits	3 PASS	3 PASS	3 PASS	
8.3.2	Transmission on the third bit of intermission field after error frame	2 PASS	2 PASS	2 PASS	
8.3.3	Bit error in error flag	3 PASS	3 PASS	3 PASS	
8.3.4	Form error in error delimiter	3 PASS	3 PASS	3 PASS	
8.4	**Test class 4, overload frame management**				
8.4.1	MAC overload generation in intermission field	2 PASS	2 PASS	2 PASS	
8.4.2	Eighth bit of an error and overload delimiter	2 PASS	2 PASS	2 PASS	
8.4.3	Transmission on the third bit of intermission after overload frame	2 PASS	2 PASS	2 PASS	
8.4.4	Bit error in overload flag	3 PASS	3 PASS	3 PASS	
8.4.5	Form error in overload delimiter	3 PASS	3 PASS	3 PASS	
8.5	**Test class 5, passive error state and bus-off**				
8.5.1	Acceptance of active error flag overwriting passive error flag	3 PASS	3 PASS	3 PASS	
8.5.2	Frame acceptance after passive error frame transmission	1 PASS	1 PASS	1 PASS	
8.5.3	Acceptance of 7 consecutive dominant bits after passive error flag	3 PASS	3 PASS	3 PASS	
8.5.4	Reception of a frame during Suspend transmission	3 PASS	3 PASS	3 PASS	
8.5.5	Transmission of a frame after Suspend transmission Test case 1	1 PASS	1 PASS	1 PASS	
8.5.6	Transmission of a frame after Suspend transmission - Test case 2	1 PASS	1 PASS	1 PASS	
8.5.7	Transmission of a frame after Suspend transmission - Test case 3	1 PASS	1 PASS	1 PASS	
8.5.8	Transmission of a frame without Suspend transmission	5 PASS	5 PASS	5 PASS	
8.5.9	No transmission of a frame between the third bit of intermission field and 8th bit of suspend transmission	4 PASS	4 PASS	3 PASS	
8.5.10	Bus-off state	1 PASS	1 PASS	1 PASS	

Ref.	Description	Result CC_CC	Result FD_CC	Result FD_FD	Comment
8.5.11	Bus-off recovery	2 PASS	2 PASS	2 PASS	
8.5.12	Completion condition for a passive error flag	1 PASS	1 PASS	1 PASS	
8.5.13	Form Error in passive error delimiter	3 PASS	3 PASS	3 PASS	
8.5.14	Maximum recovery time after a corrupted frame	1 PASS	1 PASS	1 PASS	
8.5.15	Transition from active to passive ERROR FLAG	1 PASS	1 PASS	1 PASS	
8.6	**Test class 6, Error counter management**				
8.6.1	TEC increment on bit error during active error flag	3 PASS	3 PASS	3 PASS	
8.6.2	TEC increment on bit error during overload flag	3 PASS	3 PASS	3 PASS	
8.6.3	TEC increment when active error flag is followed by dominant bits	1 PASS	1 PASS	1 PASS	
8.6.4	TEC increment when passive error flag is followed by dominant bits	5 PASS	5 PASS	5 PASS	
8.6.5	TEC increment when overload flag is followed by dominant bits	1 PASS	1 PASS	1 PASS	
8.6.6	TEC increment on bit error in data frame	8 PASS	8 PASS	13 PASS	
8.6.7	TEC increment on form error in a frame	5 PASS	5 PASS	7 PASS	
8.6.8	TEC increment on acknowledgement error	1 PASS	1 PASS	1 PASS	
8.6.9	TEC increment on form error in error delimiter	8 PASS	8 PASS	8 PASS	
8.6.10	TEC increment on form error in overload delimiter	2 PASS	2 PASS	2 PASS	
8.6.11	TEC decrement on successful frame transmission for TEC < 128	1 PASS	1 PASS	1 PASS	
8.6.12	TEC decrement on successful frame transmission for TEC > 127	1 PASS	1 PASS	1 PASS	
8.6.13	TEC non-increment on 13-bit long overload flag	1 PASS	1 PASS	1 PASS	
8.6.14	TEC non-increment on 13-bit long error flag	1 PASS	1 PASS	1 PASS	
8.6.15	TEC non-increment on form error at last bit of overload delimiter	1 PASS	1 PASS	1 PASS	
8.6.16	TEC non-increment on form error at last bit of error delimiter	1 PASS	1 PASS	1 PASS	

Ref.	Description	Result CC_CC	Result FD_CC	Result FD_FD	Comment
8.6.17	TEC non-increment on acknowledgement error in passive state	1 PASS	1 PASS	1 PASS	
8.6.18	TEC increment after acknowledgement error in passive state	1 PASS	1 PASS	1 PASS	
8.6.19	TEC non-increment on stuff error during arbitration	1 PASS	1 PASS	1 PASS	
8.6.20	TEC non-decrement on transmission while arbitration lost	1 PASS	1 PASS	1 PASS	
8.6.21	TEC non increment after arbitration lost and error	1 PASS	1 PASS	1 PASS	
9	**Test type 3, bi-directional frame**				
9.1	**Bi-directional frame type (RTR – C&S add-on)**				
9.1.1	Receive base frame format remote frame and number of data (C&S Add-on)	9 PASS	9 PASS		
9.1.2	Receive extended remote frame and number of data (C&S Add-on)	9 PASS	9 PASS		
9.1.3	Receive base frame format remote frame and number of data DLC greater than 8 (C&S Add-on)	7 PASS	7 PASS		
9.1.4	Transmit base frame format remote frame and number of data (C&S Add-on)	9 PASS	9 PASS		
9.1.5	Transmit extended remote frame and number of data (C&S Add-on)	9 PASS	9 PASS		
9.1.6	Transmit base frame format remote frame DLC greater than 8 (C&S Add-on)	7 PASS	7 PASS		
9.1.7	Arbitration in standard remote frame (C&S Add-on)	2 PASS	2 PASS		
9.1.8	Arbitration in extended remote frame (C&S Add-on)	2 PASS	2 PASS		
9.6	**Error counter management class**				
9.6.1	REC unaffected when increasing TEC	1 PASS	1 PASS	1 PASS	
9.6.2	TEC unaffected when increasing REC	1 PASS	1 PASS	1 PASS	

6 Test List: ISO16845-1 Test classes 7 and 8 (Bit Timing Tests)

6.1 Bit Timing Test Setup

Generation of Bit Timing Test Atoms

To reduce the execution time of the bit timing test suite, a limited number of configurations are tested instead of the whole possible spectrum. These configurations represent the most critical timing settings where errors can occur.

Test cases which define a variable error position as like synchronisation tests, using different phase errors are performed with error "e" at the min, max and a middle value in ranges as defined in test case. If an error comes across with these settings, the configuration is expanded to isolate the error. If the chip passes these tests, the other possible timing settings shall be “pass” too.

Test cases which define a variable resynchronisation jump width as like synchronisation tests are performed with resynchronisation jump width "RSJW" at the min, max and a middle value in ranges as defined in test case. If an error comes across with these settings, the configuration is expanded to isolate the error. If the chip passes these tests, the other possible timing settings shall be “pass” too.

Bit Timing Configurations:

With reference to chapter 6.2.3 of ISO16845-1 "Bit rate configuration parameter variation for bit timing tests" the tests are performed with:

For Classical CAN configurations:

— at least one configuration for minimum programmable number of TQ(N)s;

— at least one configuration for maximum programmable number of TQ(N)s;

— at least one configuration for a programmable number of TQ(N)s in the middle between MIN and MAX number of TQ(N)s.

For FD enabled configuration:

— at least one configuration for minimum possible number of TQ(D)s;

— at least one configuration for maximum possible number of TQ(D)s;

— at least one configuration for a possible number of TQ(D)s in the middle of MIN and MAX.

Test with shared prescaler (different number of TQs for nominal and data bit rate) only.

Tested Configurations CC_CC:

Configuration Table for Bit Timing Tests with 80 MHz CAN Clock, Classical CAN.			
Test configuration	BRP	NTQ	Bitrate
Setting #1	10	8	1000.000 kbit/s
Setting #2	10	16	500.000 kbit/s
Setting #3	10	25	320.000 kbit/s
Setting #4	12	10	666.667 kbit/s
Setting #5	12	20	333.333 kbit/s
Setting #6	12	25	266.667 kbit/s

Table 1 CC_CC

Tested Configurations FD_CC & FD_FD:

Configuration Table for Bit Timing Tests with 80 MHz CAN Clock, CAN FD enabled.						
Test configuration	BRP nominal	NTQ nominal	Bitrate nominal	BRP data	NTQ data	Bitrate data
Setting #1	3	30	888.889 kbit/s	3	10	2666.667 kbit/s
Setting #2	3	160	166.667 kbit/s	3	25	1066.667 kbit/s
Setting #3	3	380	70.175 kbit/s	3	40	666.667 kbit/s
Setting #4	2	40	1000.000 kbit/s	2	5	8000.000 kbit/s
Setting #5	2	200	200.000 kbit/s	2	30	1333.333 kbit/s
Setting #6	2	360	111.111 kbit/s	2	48	833.333 kbit/s

Table 2 FD_CC & FD_FD

6.2 TEST CLASS 7&8, BIT TIMING Classical CAN (CC_CC & FD_CC)

The ISO16845-1 pointed out a CAN Version for which a test case is applicable. CAN Implementations supporting CAN FD are often also support classical CAN. So the tests are performed in different IUT modes, for classical CAN and for CAN FD enabled. The resulting test combinations are:

- IUT in classical CAN mode and tests applied for classical CAN, in short "CC_CC".
- IUT in CAN FD mode and tests applied for classical CAN, in short "FD_CC".

The meaning of greyed fields in result Colum is that for the given IUT mode and Frame format combination is no test defined.

Following "Ref." numeration relates on the corresponding test specification ISO16845-1.

Ref.	Description	Result CC_CC	Result FD_CC	Result FD_FD	Comment
7	**Bit Timing "CAN FD enabled"**				
7.7	**Test type 1, received frame**				
7.7.1	Sample point test	19 PASS	18 PASS		
7.7.2	**Hard synchronisation**				
7.7.2.1	Hard synchronisation on SOF reception	57 PASS	54 PASS		
7.7.2.2_CS	Hard synchronisation after glitch test - C&S add-on	19 PASS	18 PASS		
7.7.3	Synchronisation when e > 0 and e <= SJW	93 PASS	101 PASS		
7.7.4	Synchronisation when e > 0 and e > SJW	134 PASS	130 PASS		
7.7.5	Synchronisation when e < 0 and |e| <= SJW	93 PASS	101 PASS		
7.7.6	Synchronisation when e < 0 and |e| > SJW	96 PASS	101 PASS		
7.7.7	Glitch filtering test on positive phase error	56 PASS	18 PASS		

Ref.	Description	Result CC_CC	Result FD_CC	Result FD_FD	Comment
7.7.8	Glitch filtering test on negative phase error	56 PASS	18 PASS		
7.7.9	**Glitch filtering test in Idle State**				
7.7.9.1	Glitch filtering test in Idle State - single pulse	19 PASS	18 PASS		
7.7.9.2	Glitch filtering test in Idle State - mutiple pulses	19 PASS	18 PASS		
7.7.10	Non-Re-synchronisation after a Dominant sampled bit	19 PASS	18 PASS		
7.7.11	Synchronization when e < 0 and |e| <= SJW(N) at "ACK" bit position (IPT)	93 PASS	101 PASS		
7.7.12CS	Synchronisation when e > SJW & e < SP => e=1/2tBit (first Bit of Intermission)	19 PASS	46 PASS		
7.7.13CS	**Glitch detection while bus integration after protocol except. (C&S)**				
7.7.13CS.1	Glitch detection while bus integration - IUT as transmitter		6 PASS		
7.7.13CS.2	Glitch detection while bus integration - IUT as receiver		6 PASS		
7.7.14cs	Glitch filtering test in non-Idle State		18 PASS		
8	**Bit Timing "CAN FD enabled"**				
8.7	**Test type 2, transmitted frame**				
8.7.1	Sample Point Test	19 PASS	18 PASS		
8.7.2	Hard synchronisation on SOF reception before sample point	19 PASS	18 PASS		
8.7.3	Hard Synchronisation on SOF Reception after sample point (IPT)	71 PASS	18 PASS		

Ref.	Description	Result CC_CC	Result FD_CC	Result FD_FD	Comment
8.7.4	Synchronisation when e < 0 and |e| <= SJW (IPT)	84 PASS	88 PASS		
8.7.5	Synchronisation for e < 0 and |e| > SJW (IPT)	70 PASS	68 PASS		
8.7.6	Glitch filtering test on negative phase error	56 PASS	18 PASS		
8.7.7	Non-synchronisation on Dominant bit transmission	19 PASS	18 PASS		
8.7.8	Synchronisation before information processing time (IPT)	56 PASS	46 PASS		
8.7.9	Sync after sample point on dominant bit (IPT)	56 PASS	46 PASS		
8.7.10CS	Synchronisation when e > SJW & e < SP (first Bit of Intermission)	19 PASS	18 PASS		
8.7.11CS	**detection while in integration mode after bus-off (C&S)**				
8.7.11CS.1	Glitch detection while in integration mode - IUT transmit into idle		6 PASS		
8.7.11CS.2	Glitch detection while in integration mode - IUT transmit into arbitration		6 PASS		
8.7.12CS	**filtering test in non-idle state (C&S)**				
8.7.12CS.1	Glitch filtering test in non-idle state - arb. lost		18 PASS		
8.7.12CS.2	Glitch filtering test in non-idle state - after error		18 PASS		

6.3 TEST CLASS 7&8, BIT TIMING FD CAN (FD_FD)

Ref.	Description	Result CC_CC	Result FD_CC	Result FD_FD	Comment
7	**Bit Timing "CAN FD enabled"**				
7.8	**Test type 1, received frame**				
7.8.1	**Sample point test**				
7.8.1.1a	at “BRS” bit position #1			18 PASS	
7.8.1.1b	at “BRS” bit position #2			18 PASS	
7.8.1.2	at “DATA” bit position			15 PASS	
7.8.1.3	at “CRC Delimiter” bit position (IPT)			15 PASS	
7.8.2	**Hard synchronization**				
7.8.2.1	on "res" bit (delayed end of FDF)			54 PASS	
7.8.2.2	on "res" bit (early end of FDF)			46 PASS	
7.8.3	**Synchronization when e > 0 and e <= SJW(D)**				
7.8.3.1	at ESI bit position			68 PASS	
7.8.3.2	at DATA field position (IPT)			68 PASS	
7.8.3.3	at CRC Delimiter bit position			68 PASS	
7.8.4	**Synchronization when e > 0 and e > SJW(D)**				
7.8.4.1	at ESI bit position			91 PASS	

Ref.	Description	Result CC_CC	Result FD_CC	Result FD_FD	Comment
7.8.4.2	at DATA field position (IPT)			91 PASS	
7.8.4.3	at CRC Delimiter bit position			91 PASS	
7.8.5	**Synchronization when e < 0 and |e| <= SJW(D)**				
7.8.5.1	at ESI bit position			PASS 85	
7.8.5.2	at DATA field position			68 PASS	
7.8.5.3	at "ACK" bit position (IPT)			101 PASS	
7.8.6	**Synchronization when e < 0 and |e| > SJW(D)**				
7.8.6.1	at ESI bit position			73 PASS	
7.8.6.2	at DATA field position			73 PASS	
7.8.6.3	at "ACK" bit position			101 PASS	
7.8.7	**Glitch filtering test on positive phase error**				
7.8.7.1	at "res" bit position			18 PASS	
7.8.7.2	at "DATA" field position			15 PASS	
7.8.7.3	at "ACK" bit position			18 PASS	
7.8.8	**Glitch filtering test on negative phase error**				

Ref.	Description	Result CC_CC	Result FD_CC	Result FD_FD	Comment
7.8.8.1	at "ESI" bit position			15 PASS	
7.8.8.2	at "DATA" field position			15 PASS	
7.8.8.3	at "ACK" bit position			15 PASS	
7.8.9	**Non-Re-synchronization after a dominant sampled**				
7.8.9.1	at "BRS" bit position			18 PASS	
7.8.9.2	at "DATA" field position (IPT)			15 PASS	
7.8.9.3	at "CRC Delimiter" bit position (IPT)			15 PASS	
8	**Bit Timing "CAN FD enabled"**				
8.8	**Test type 2, transmitted frame**				
8.8.1	**Sample point test**				
8.8.1.1	at "res" bit			18 PASS	
8.8.1.2	at BRS bit			18 PASS	
8.8.1.3	at DATA field position			15 PASS	
8.8.1.4	at CRC Delimiter bit			15 PASS	
8.8.2	**Secondary Sample point test**				
8.8.2.1	at "res" bit -NEW delay calculation-			33 PASS	

Ref.	Description	Result CC_CC	Result FD_CC	Result FD_FD	Comment
8.8.2.2	at BRS bit (IPT)			33 PASS	
8.8.2.3	at DATA field position			33 PASS	
8.8.2.4	at end of data phase			33 PASS	
8.8.3	**No Synchronization when e < 0 and |e| <= SJW(D)**				
8.8.3.1	at BRS bit position			15 PASS	
8.8.3.2	at DATA field position			15 PASS	
8.8.4	**Glitch filtering test on negative phase error within FD frame**				
8.8.4.1	at "ESI" bit position			15 PASS	
8.8.4.2	at “DATA” field position			15 PASS	
8.8.5	**Non-synchronization on dominant bit transmission in FD frame**				
8.8.5.1	at "ESI" bit position			15 PASS	
8.8.5.2	at “DATA” field position			15 PASS	

7 Test List: C&S Robustness Test

7.1.1 Test Setup

Configuration Table for Robustness Tests with 80 MHz CAN Clock.			
Test configuration	BRP	NTQ	Bitrate
Setting #1	10	8	1000.000 kbit/s
Setting #2	10	16	500.000 kbit/s
Setting #3	10	25	320.000 kbit/s

Table 3 Robustness CC Mode

Configuration Table for Robustness Tests with 80 MHz CAN Clock, CAN FD enabled.						
Test configuration	BRP nominal	NTQ nominal	Bitrate nominal	BRP data	NTQ data	Bitrate data
Setting #1	2	40	1000.000 kbit/s	2	5	8000.000 kbit/s
Setting #2	2	200	200.000 kbit/s	2	30	1333.333 kbit/s
Setting #3	2	360	111.111 kbit/s	2	48	833.333 kbit/s

Table 4 Robustness FD Mode

7.1.2 Test List

Following test case numeration relates on the corresponding test specification.

ref	Description	Test script	Result	Comment
6	**Robustness**			
6.1	**Classic CAN format - LT: Odd Identifiers**			
6.1.1	**CC IDE MIX Random Test - LT: Odd Identifiers**	ROB_61_CC_1000k.tst	PASS	
6.1.2	**CC IDE MIX Random Test - LT: Odd Identifiers**	ROB_61_CC_500k.tst	PASS	
6.1.3	**CC IDE MIX Random Test - LT: Odd Identifiers**	ROB_61_CC_320k.tst	PASS	
6.2	**Classic CAN format - LT: Even Identifiers**			
6.2.1	**CC IDE MIX Random Test - LT: Even Identifiers**	ROB_62_CC_1000k.tst	PASS	
6.2.2	**CC IDE MIX Random Test - LT: Even Identifiers**	ROB_62_CC_500k.tst	PASS	
6.2.3	**CC IDE MIX Random Test - LT: Even Identifiers**	ROB_62_CC_320k.tst	PASS	
6.3	**Classic CAN format - LT: Odd Identifiers; with Errors**			
6.3.1	**CC IDE MIX Random Test - LT: Odd Identifiers; with Errors**	ROB_63_CC_1000k.tst	PASS	
6.3.2	**CC IDE MIX Random Test - LT: Odd Identifiers; with Errors**	ROB_63_CC_500k.tst	PASS	
6.3.3	**CC IDE MIX Random Test - LT: Odd Identifiers; with Errors**	ROB_63_CC_320k.tst	PASS	
6.4	**Classic CAN format - LT: Even Identifiers; with Errors**			
6.4.1	**CC IDE MIX Random Test - LT: Even Identifiers; with Errors**	ROB_64_CC_1000k.tst	PASS	
6.4.2	**CC IDE MIX Random Test - LT: Even Identifiers; with Errors**	ROB_64_CC_500k.tst	PASS	
6.4.3	**CC IDE MIX Random Test - LT: Even Identifiers; with Errors**	ROB_64_CC_320k.tst	PASS	
7	**Robustness FD**			
7.1	**FD CAN format - LT: Odd Identifiers**			
7.1.1	**FD MIX ALL Random Test - LT: Odd Identifiers**	ROB_71_FD_1000k_8000k.tst	PASS	
7.1.2	**FD MIX ALL Random Test - LT: Odd Identifiers**	ROB_71_FD_200k_1333k.tst	PASS	
7.1.3	**FD MIX ALL Random Test - LT: Odd Identifiers**	ROB_71_FD_111k_833k.tst	PASS	

ref	Description	Test script	Result	Comment
7.2	**FD CAN format - LT: Even Identifiers**			
7.2.1	**FD MIX ALL Random Test - LT: Even Identifiers**	ROB_72_FD_1000k_8000k.tst	PASS	
7.2.2	**FD MIX ALL Random Test - LT: Even Identifiers**	ROB_72_FD_200k_1333k.tst	PASS	
7.2.3	**FD MIX ALL Random Test - LT: Even Identifiers**	ROB_72_FD_111k_833k.tst	PASS	
7.3	**FD CAN format - LT: Odd Identifiers; with Error**			
7.3.1	**FD MIX ALL Random Test - LT: Odd Identifiers; with Error**	ROB_73_FD_1000k_8000k.tst	PASS	
7.3.2	**FD MIX ALL Random Test - LT: Odd Identifiers; with Error**	ROB_73_FD_200k_1333k.tst	PASS	
7.3.3	**FD MIX ALL Random Test - LT: Odd Identifiers; with Error**	ROB_73_FD_111k_833k.tst	PASS	
7.4	**FD CAN format - LT: Even Identifiers; with Error**			
7.4.1	**FD MIX ALL Random Test - LT: Even Identifiers; with Error**	ROB_74_FD_1000k_8000k.tst	PASS	
7.4.2	**FD MIX ALL Random Test - LT: Even Identifiers; with Error**	ROB_74_FD_200k_1333k.tst	PASS	
7.4.3	**FD MIX ALL Random Test - LT: Even Identifiers; with Error**	ROB_74_FD_111k_833k.tst	PASS	