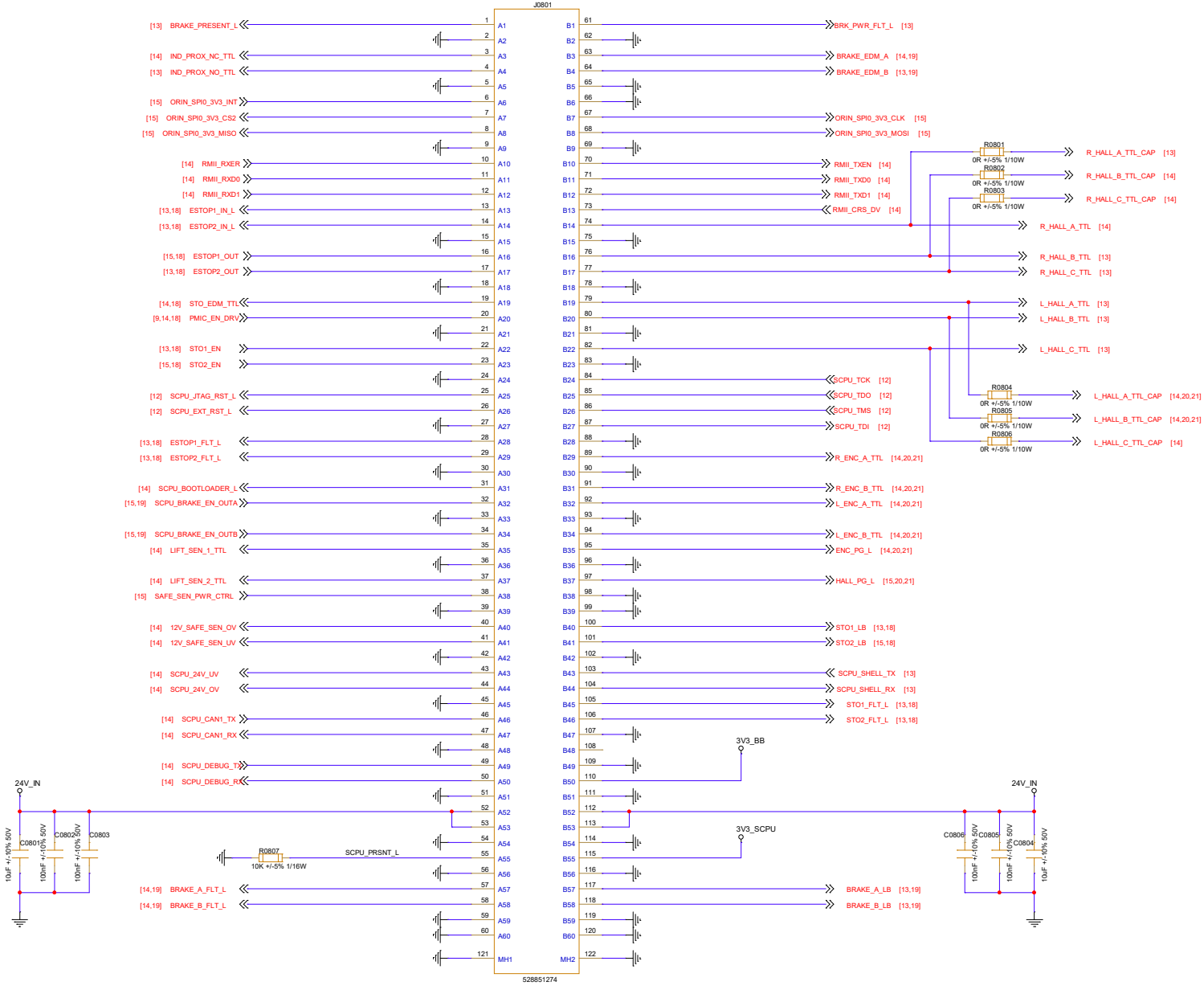
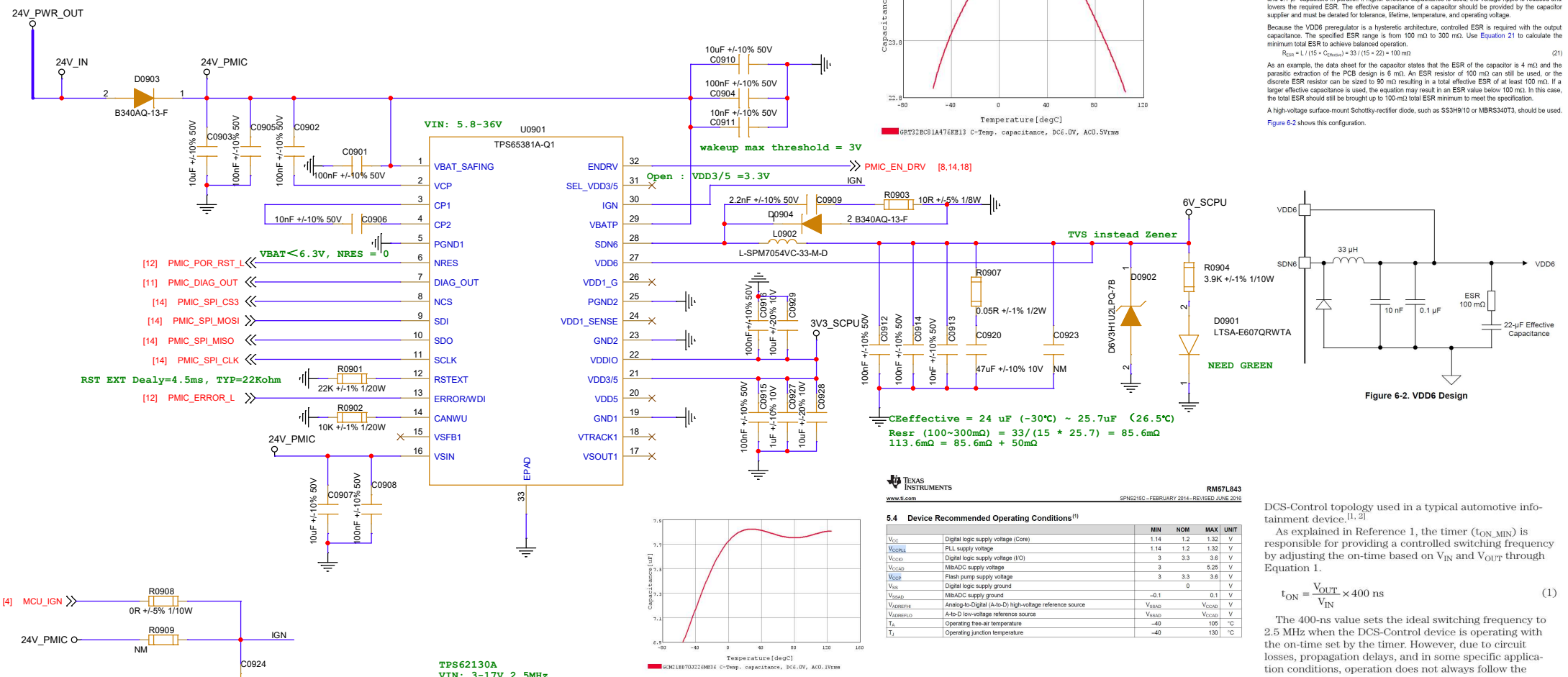
INTERFACE, DO NOT PLACE ON BOARD



Organization	Quectel Wireless Solutions		
Project	SRAM701A	Ver	1.1
Drawn By	SONI	Checked By	SONI
Size	A2		
Date:	Wednesday, June 10, 2026	Sheet	8 of 21

SCPU POWER



1V2_SCPU PARAMS	
V_IN	5.4-6.6V
V_OUT	1.2V
I_out (AVG)	970mA
I_OUT (PEAK)	1.35A
F_SW	2.5MHz

Figure 6-2. VDD6 Design

6.2.2.1 VDD6 Preregulator

The inductor, output capacitor, and total effective series resistance (ESR) of the output capacitance must be considered to achieve balanced operation of the VDD6 preregulator.

The output inductor must be greater than or equal to the minimum 22-µH inductance. The typical specified inductance is 33 µH, which was selected for this design.

The effective output capacitance for the VDD6 preregulator is specified from 22 µF to 47 µF. An effective capacitance of 22 µF at the 6-V DC operating point was selected for this design. This value allows for additional downstream input capacitance on voltage regulator inputs. To filter high frequencies, use 10-nF and 0.1-µF capacitors in parallel. If higher effective capacitance is used, the voltage ripple is reduced and lowers the required ESR. The effective capacitance of a capacitor should be provided by the capacitor supplier and must be derated for tolerance, lifetime, temperature, and operating voltage.

Because the VDD6 preregulator is a hysteretic architecture, controlled ESR is required with the output capacitance. The specified ESR range is from 100 mΩ to 300 mΩ. Use Equation 21 to calculate the minimum total ESR to achieve balanced operation.

$$R_{ESR} = L / (15 \times C_{Effective}) = 33 / (15 \times 22) = 100\ m\Omega \quad (21)$$

As an example, the data sheet for the capacitor states that the ESR of the capacitor is 4 mΩ and the parasitic extraction of the PCB design is 6 mΩ. An ESR resistor of 100 mΩ can still be used, or the discrete ESR resistor can be sized to 90 mΩ resulting in a total effective ESR of at least 100 mΩ. If a larger effective capacitance is used, the equation may result in an ESR value below 100 mΩ. In this case, the total ESR should still be brought up to 100-mΩ total ESR minimum to meet the specification.

A high-voltage surface-mount Schottky-rectifier diode, such as SS3H9/10 or MBRS340T3, should be used.

Figure 6-2 shows this configuration.

TEXAS INSTRUMENTS
www.ti.com
RM57L843
SPNS215C – FEBRUARY 2014 – REVISED JUNE 2016

5.4 Device Recommended Operating Conditions(1)

		MIN	NOM	MAX	UNIT
V_{CC}	Digital logic supply voltage (Core)	1.14	1.2	1.32	V
V_{CCPLL}	PLL supply voltage	1.14	1.2	1.32	V
V_{CCIO}	Digital logic supply voltage (I/O)	3	3.3	3.6	V
V_{CCAD}	MibADC supply voltage	3		5.25	V
V_{CCP}	Flash pump supply voltage	3	3.3	3.6	V
V_{SS}	Digital logic supply ground		0		V
V_{SSAD}	MibADC supply ground	–0.1		0.1	V
$V_{ADREFHI}$	Analog-to-Digital (A-to-D) high-voltage reference source	V_{SSAD}		V_{CCAD}	V
$V_{ADREFLO}$	A-to-D low-voltage reference source	V_{SSAD}		V_{CCAD}	V
T_A	Operating free-air temperature	–40		105	°C
T_J	Operating junction temperature	–40		130	°C

DCS-Control topology used in a typical automotive infotainment device.[1, 2]

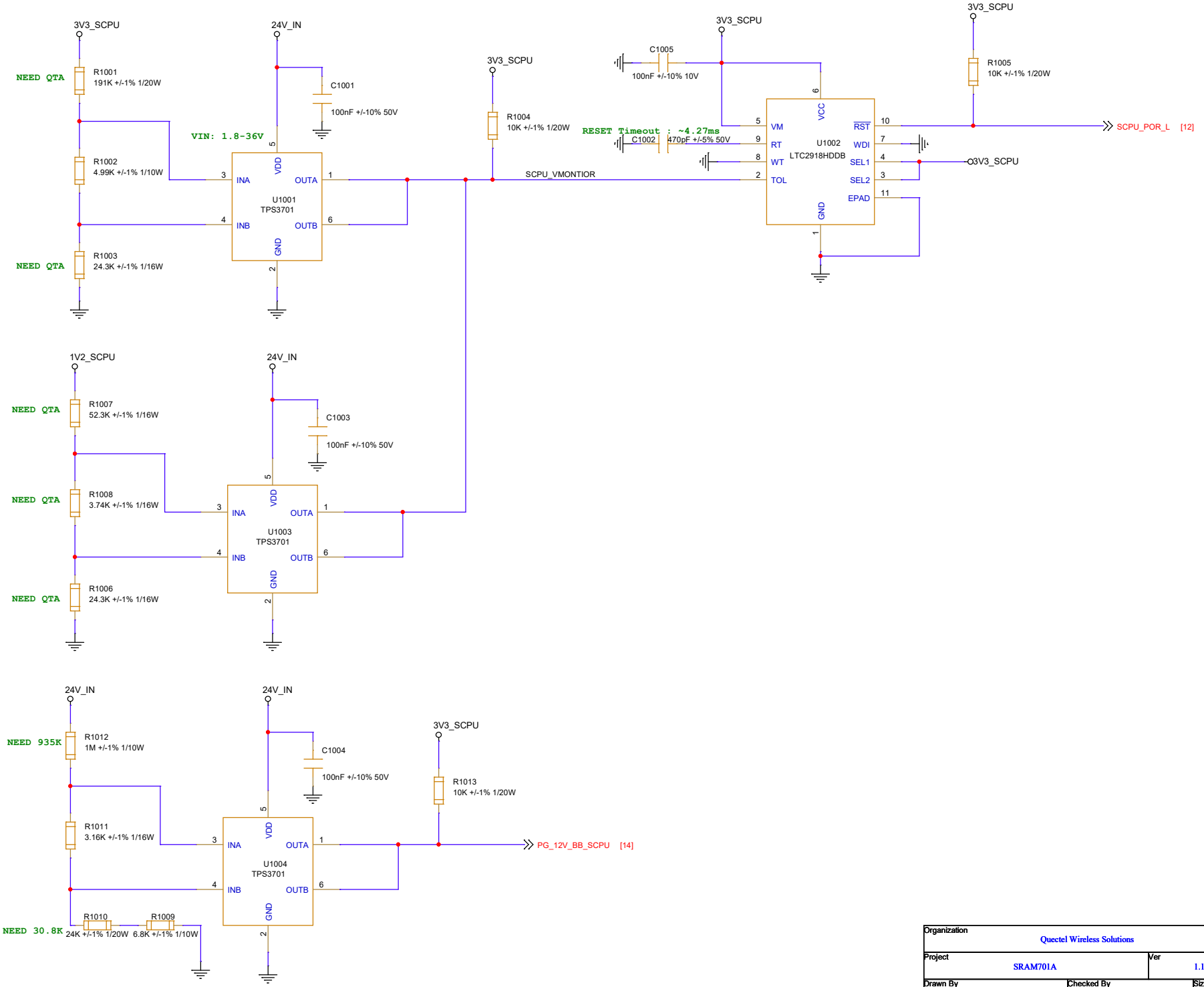
As explained in Reference 1, the timer (t_{ON_MIN}) is responsible for providing a controlled switching frequency by adjusting the on-time based on V_{IN} and V_{OUT} through Equation 1.

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \times 400\ ns \quad (1)$$

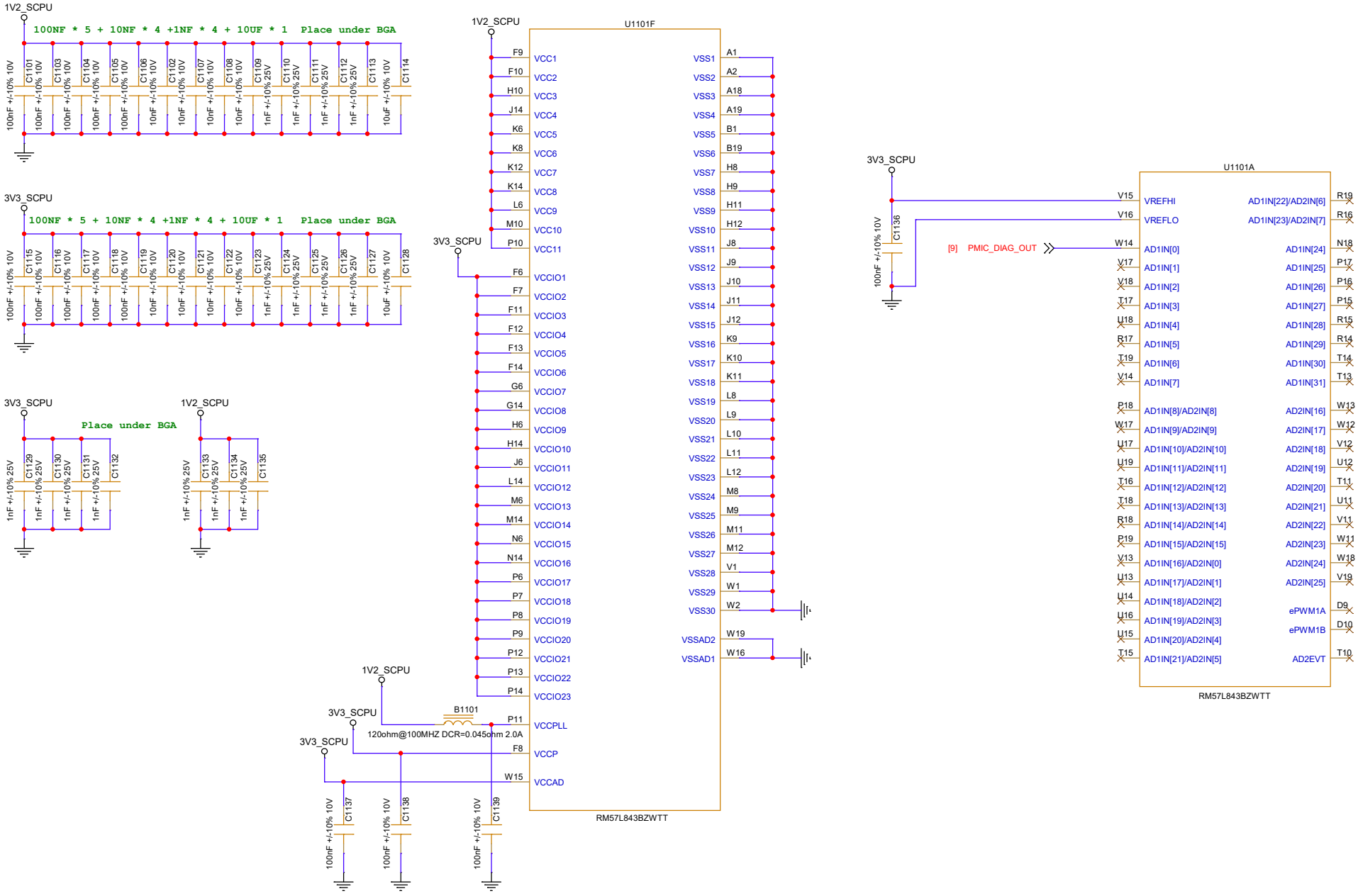
The 400-ns value sets the ideal switching frequency to 2.5 MHz when the DCS-Control device is operating with the on-time set by the timer. However, due to circuit losses, propagation delays, and in some specific application conditions, operation does not always follow the on-time set by the timer. As a result, the frequency varies. The reasons for this variation are grouped together based on the duty cycle, ideally V_{OUT}/V_{IN}, at which the device operates.

Measured data explains the principles behind the DCS-Control topology's frequency variation. To better explain the concepts, the TPS62130 (catalog version) was chosen and it offers two switching frequencies: 2.5 MHz and 1.25 MHz. The 2.5-MHz data exactly matches the TPS62130A-Q1 data because both converters offer the 2.5-MHz setting. All data was taken on the evaluation module with a 2.2-µH inductor and two 22-µF output capacitors (to overcome the DC bias effect).[3]

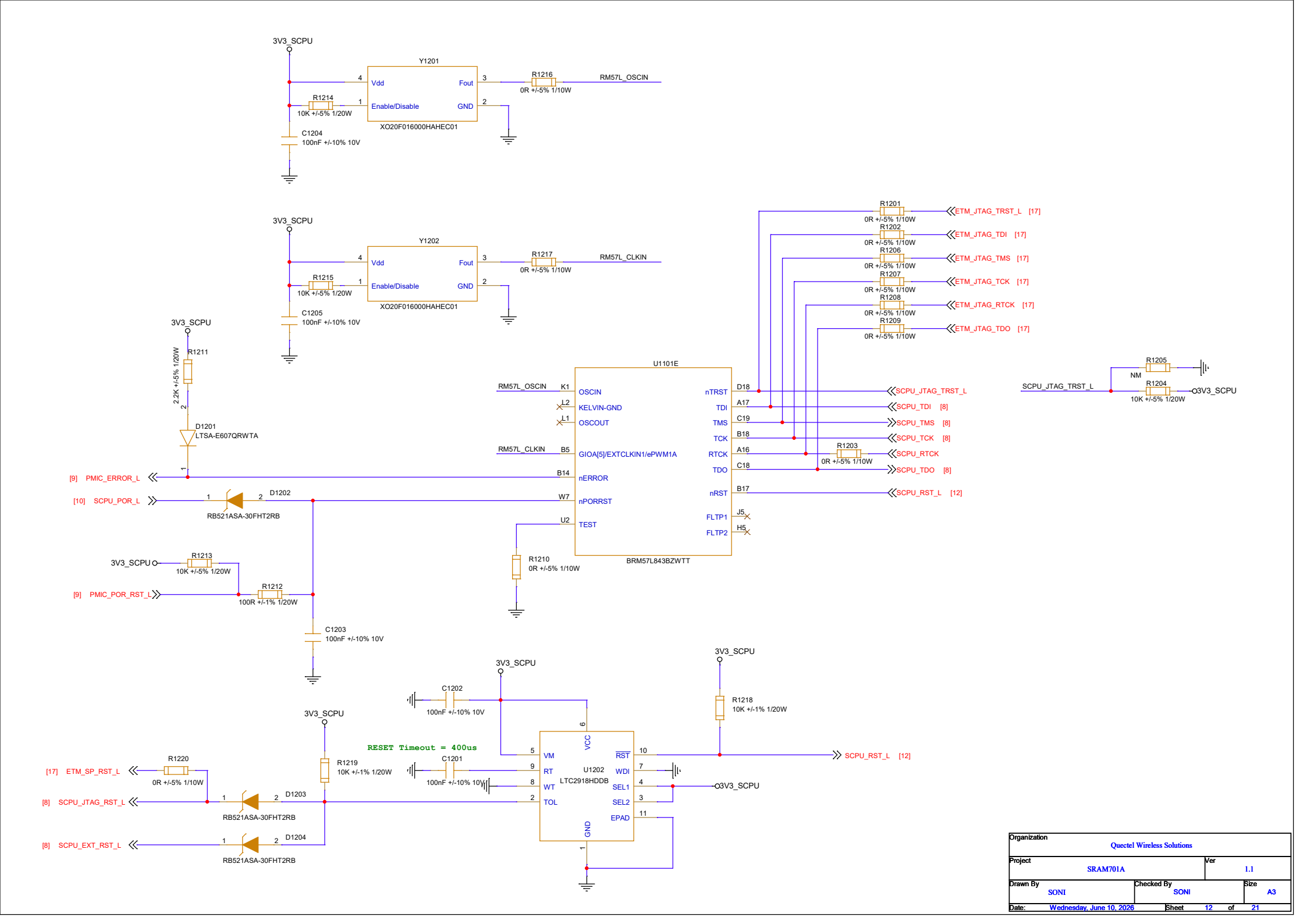
Organization	Quectel Wireless Solutions
Project	SRAM701A
Ver	1.1
Drawn By	SONI
Checked By	SONI
Size	A3
Date:	Wednesday, June 10, 2026
Sheet	9 of 21



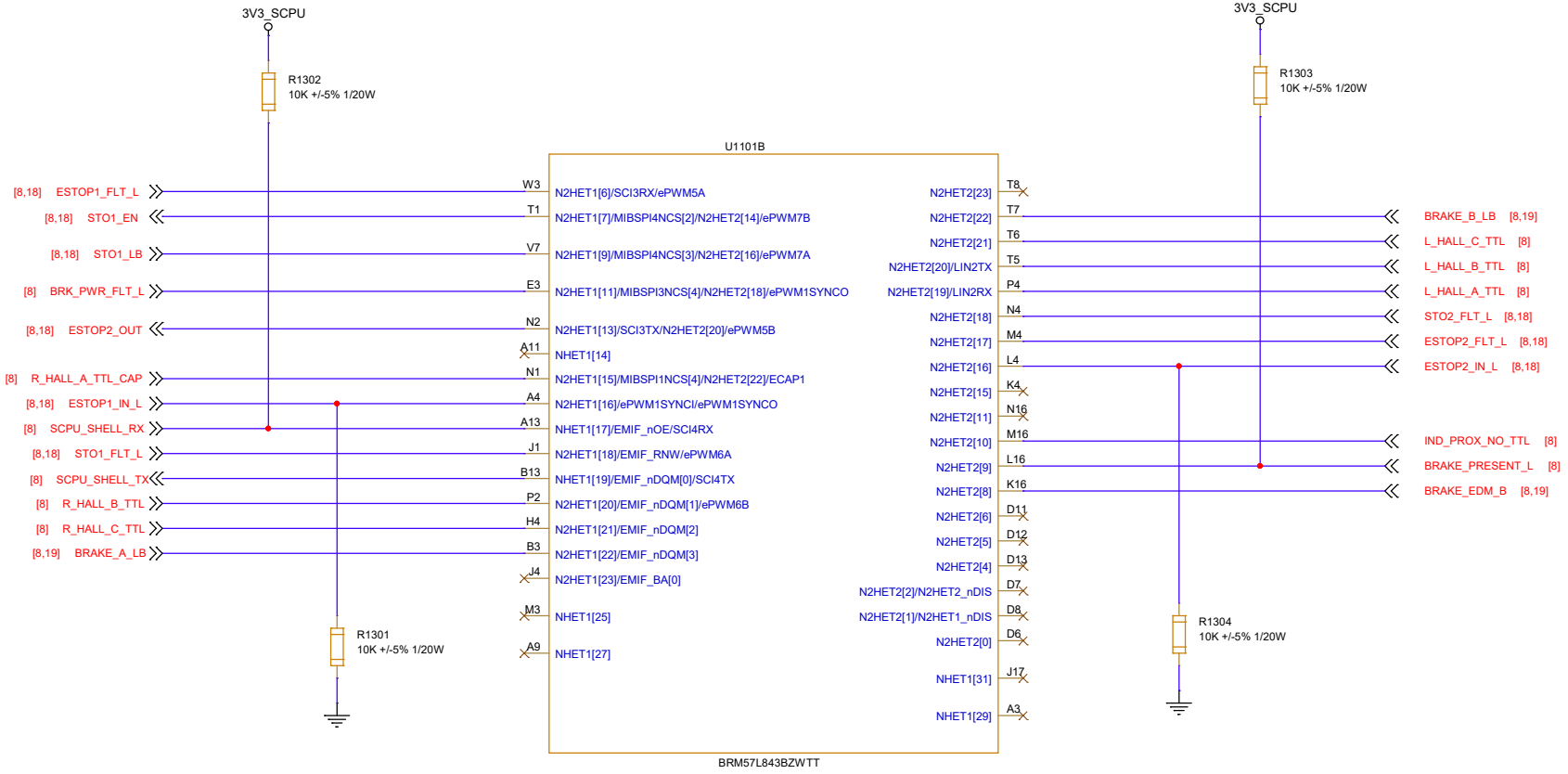
Organization	Quectel Wireless Solutions		
Project	SRAM701A	Ver	1.1
Drawn By	SONI	Checked By	SONI
Size	A3		
Date:	Wednesday, June 10, 2026	Sheet	10 of 21



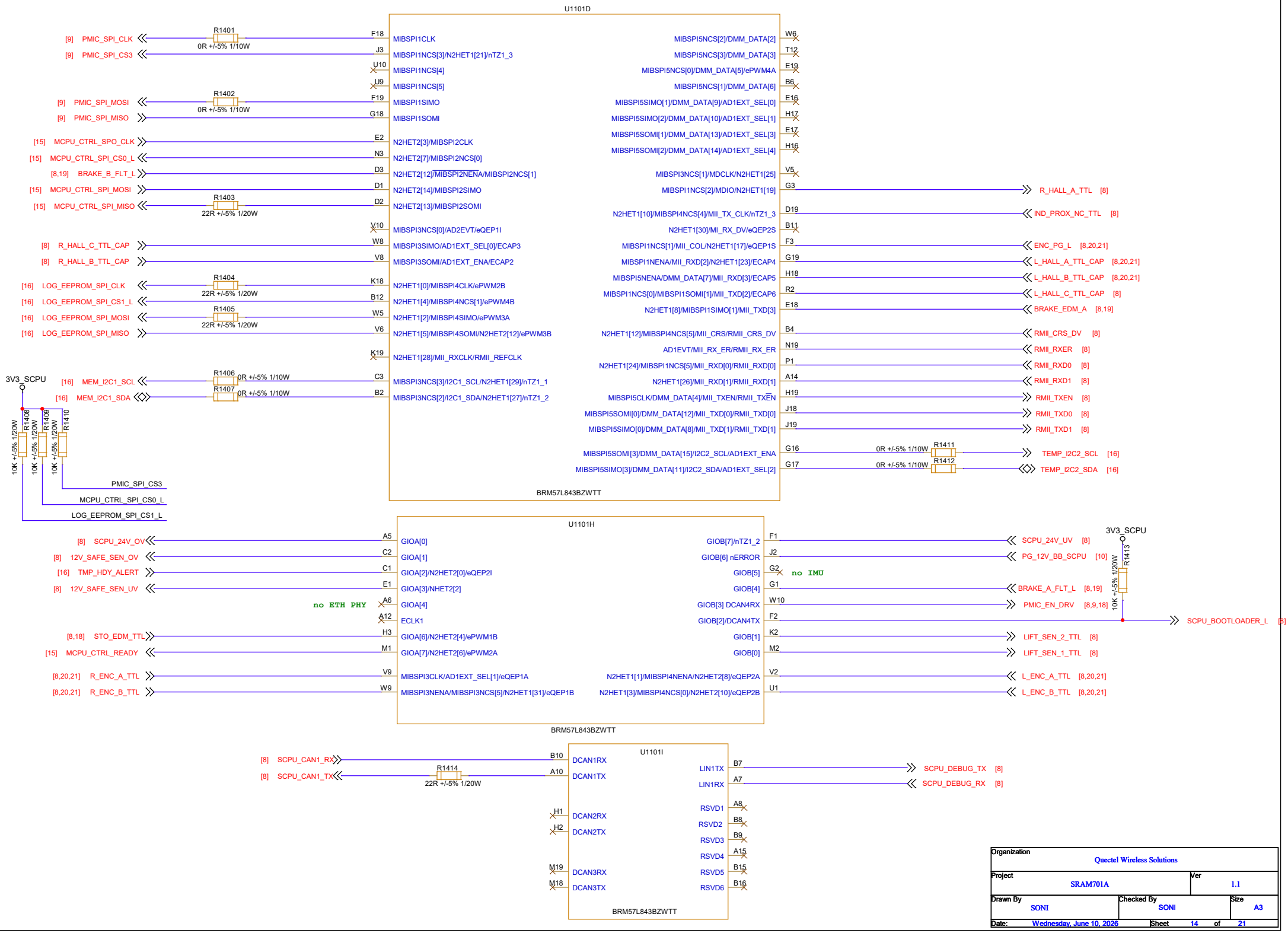
Organization	Quectel Wireless Solutions		
Project	SRAM701A	Ver	1.1
Drawn By	SONI	Checked By	SONI
Size	A3		
Date:	Wednesday, June 10, 2026	Sheet	11 of 21



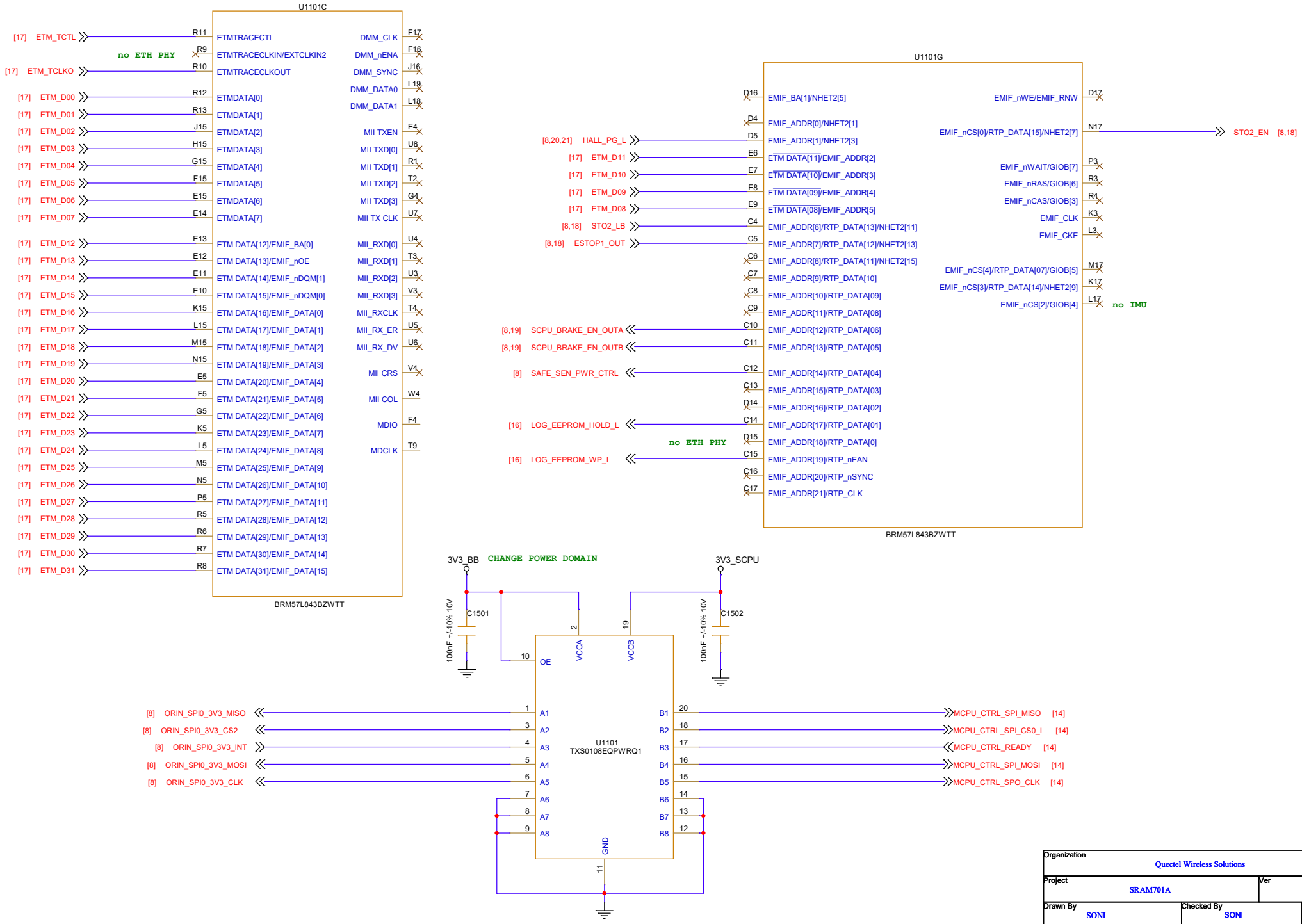
Organization	Quectel Wireless Solutions		
Project	SRAM701A	Ver	1.1
Drawn By	SONI	Checked By	SONI
Size	A3		
Date:	Wednesday, June 10, 2026	Sheet	12 of 21



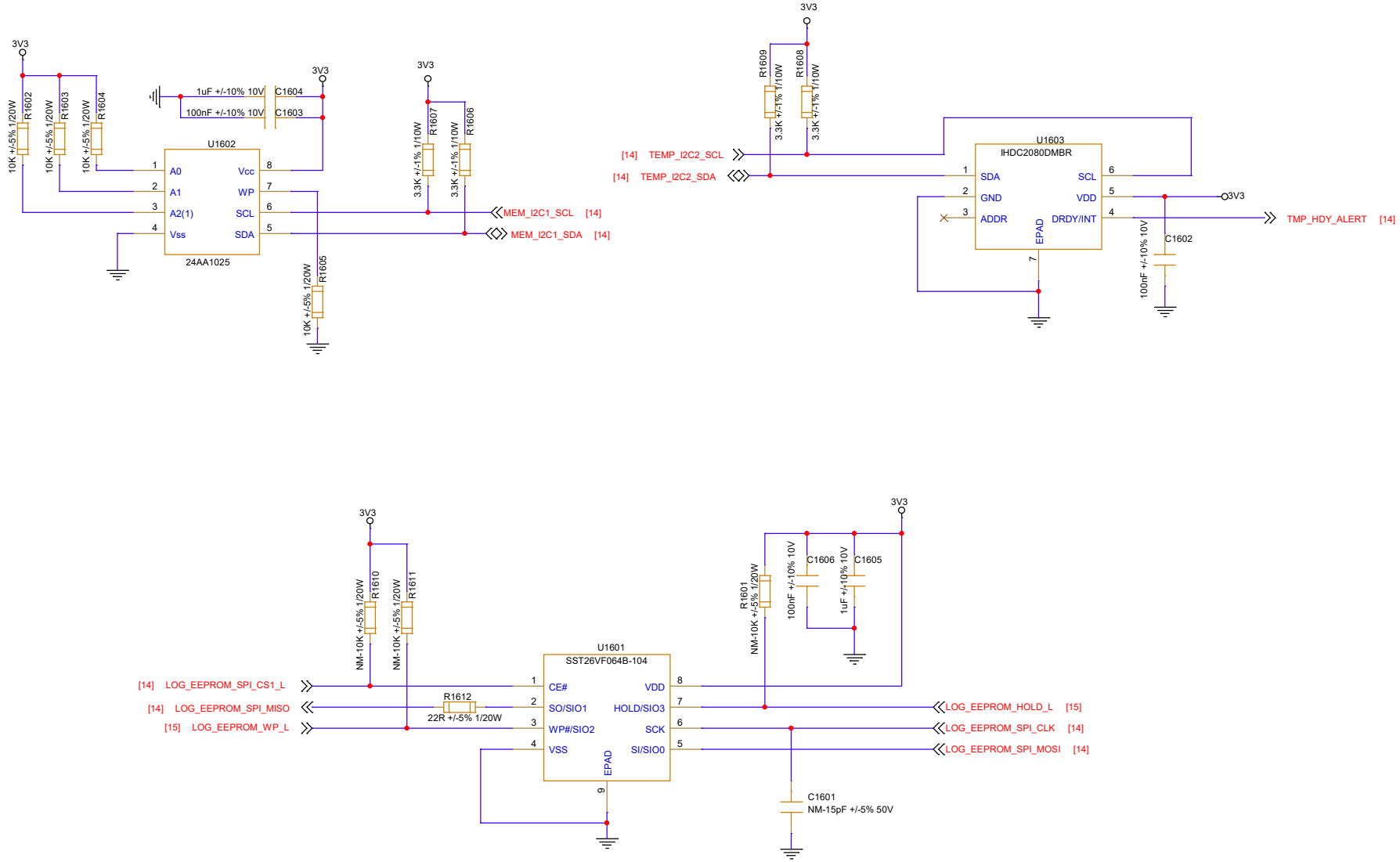
Organization	Quectel Wireless Solutions		
Project	SRAM701A	Ver	1.1
Drawn By	SONI	Checked By	SONI
Size	A3		
Date:	Wednesday, June 10, 2026	Sheet	13 of 21



Organization	Quectel Wireless Solutions		
Project	SRAM701A	Ver	1.1
Drawn By	SONI	Checked By	SONI
Size	A3		
Date:	Wednesday, June 10, 2026	Sheet	14 of 21

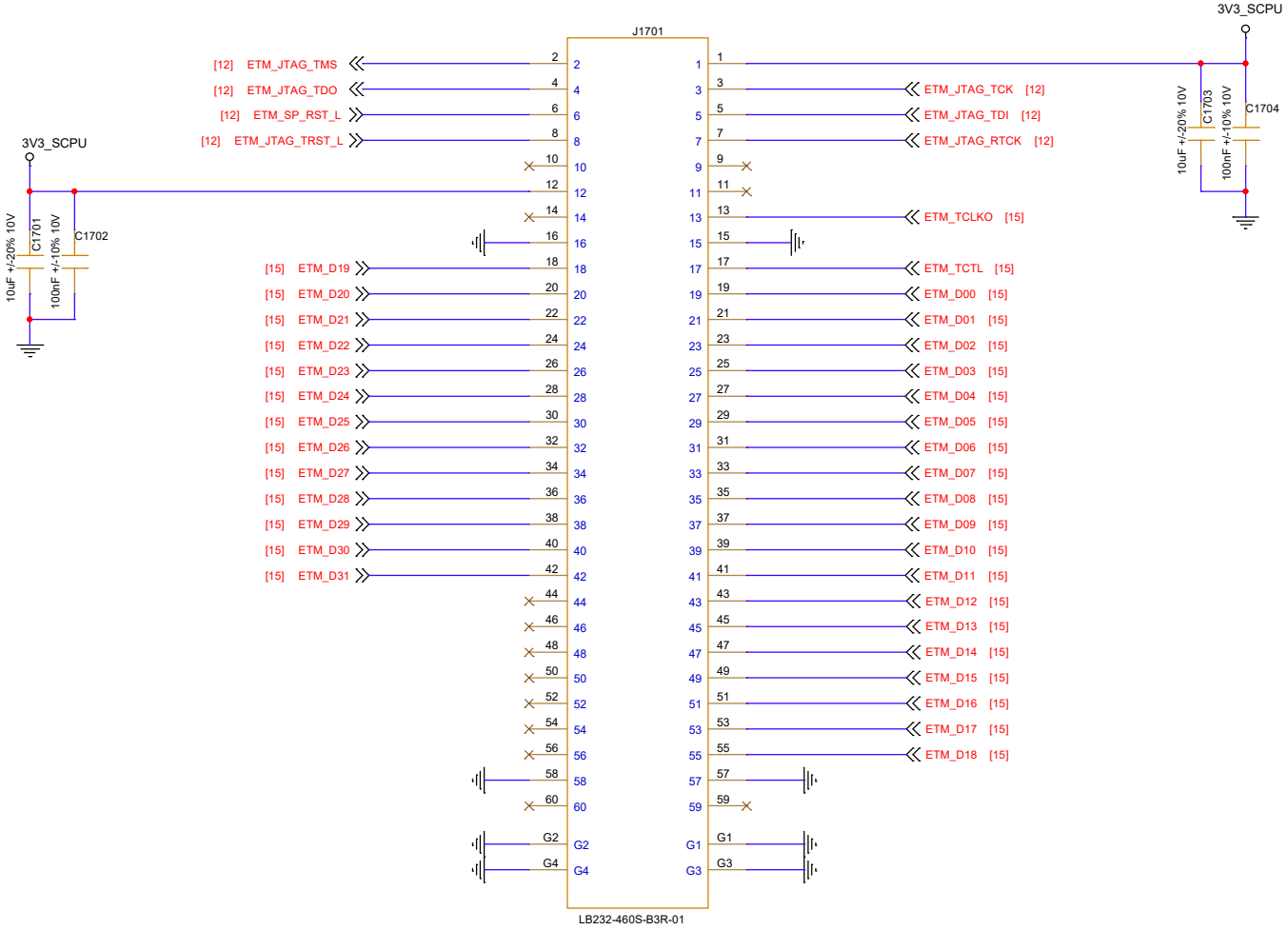


Organization	Quectel Wireless Solutions		
Project	SRAM701A	Ver	1.1
Drawn By	SONI	Checked By	SONI
Size	A3		
Date:	Wednesday, June 10, 2026	Sheet	15 of 21



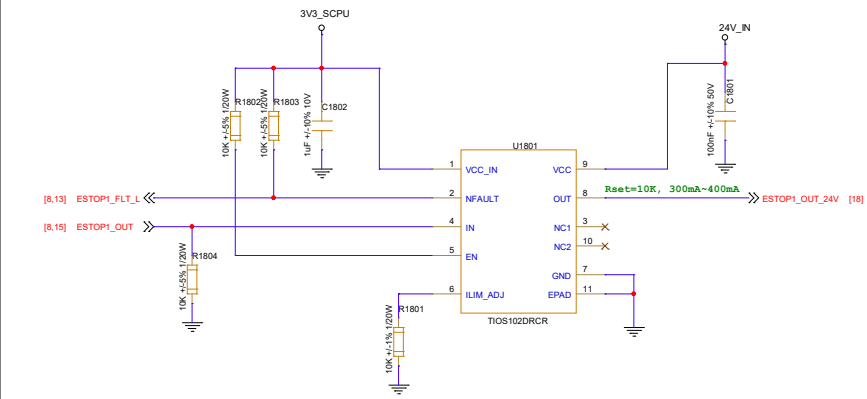
Organization	Quectel Wireless Solutions		
Project	SRAM701A	Ver	1.1
Drawn By	SONI	Checked By	SONI
Size	A3		
Date:	Wednesday, June 10, 2026	Sheet	16 of 21

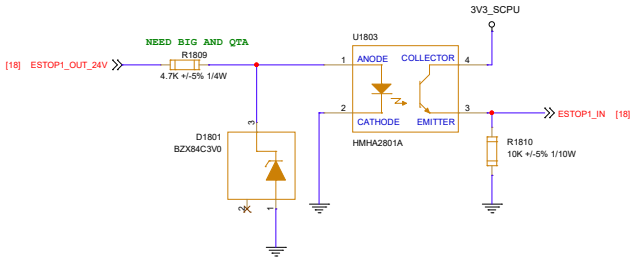
TRACE Probe Connector

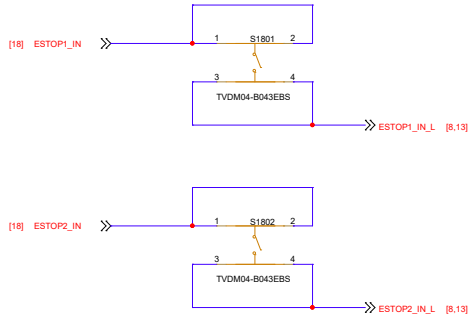


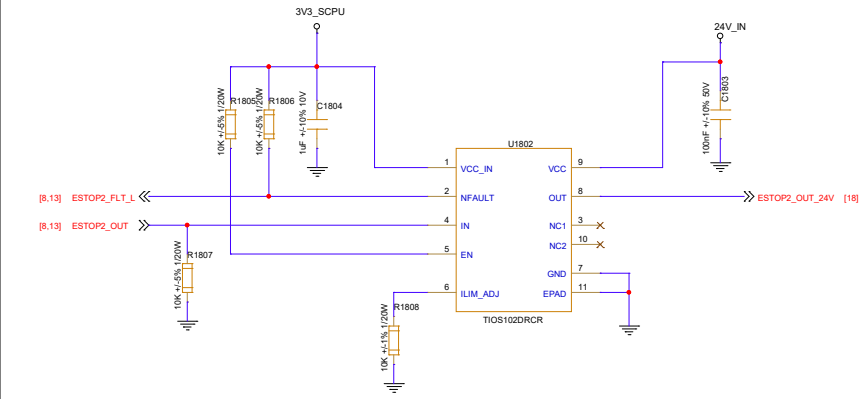
Organization	Quectel Wireless Solutions		
Project	SRAM701A	Ver	1.1
Drawn By	SONI	Checked By	SONI
Size	A3		
Date:	Wednesday, June 10, 2026	Sheet	17 of 21

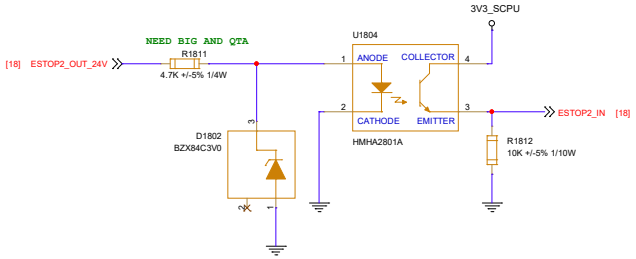
DRIVER1

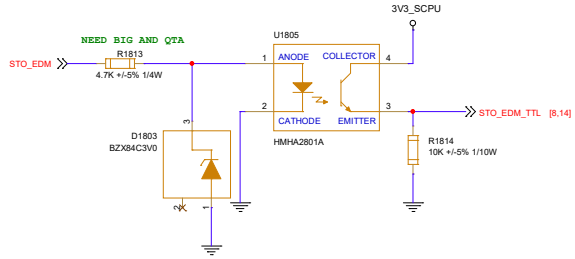


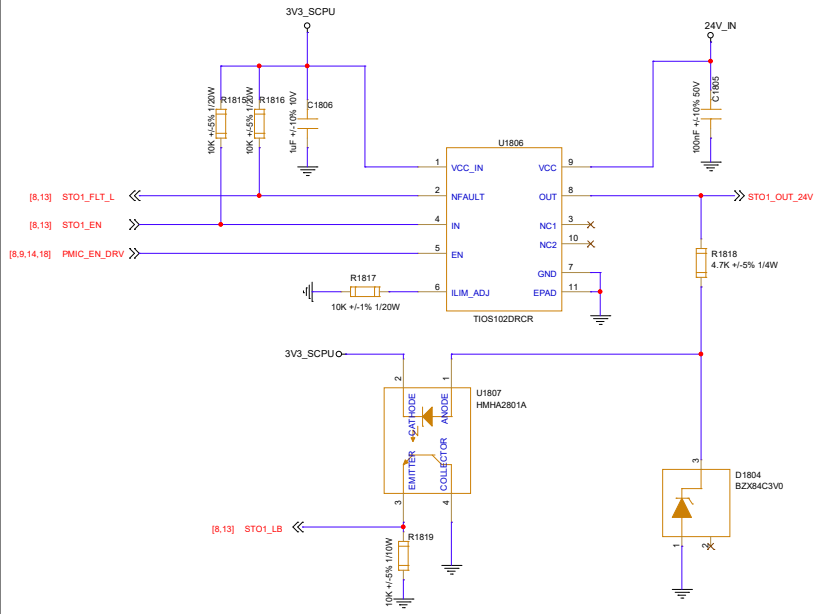


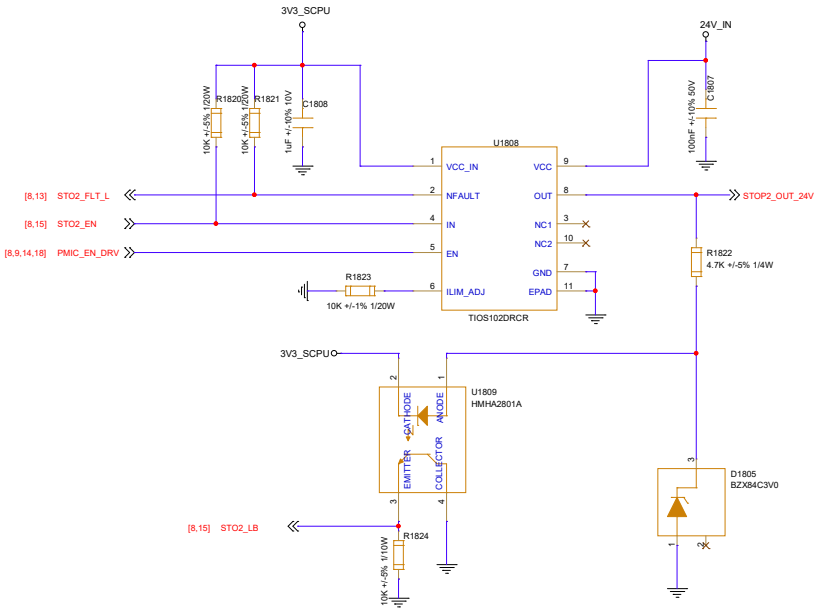






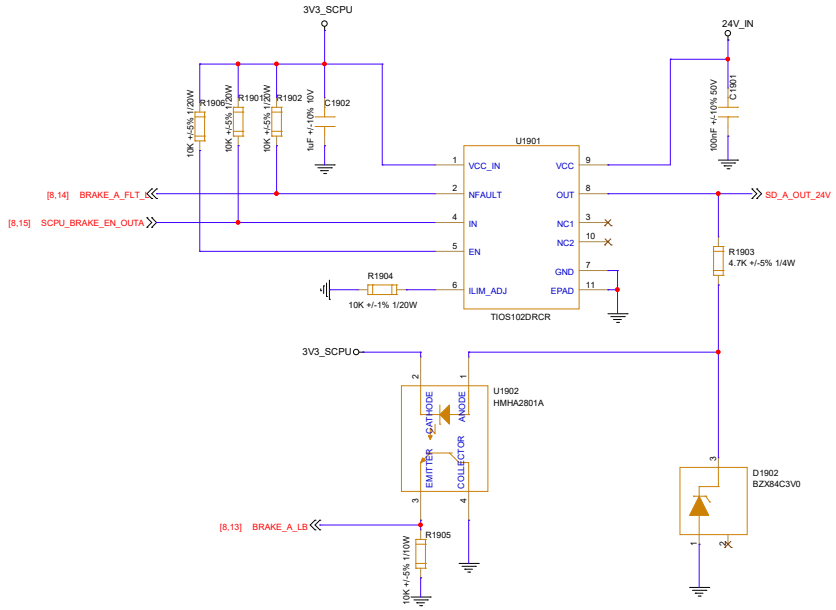


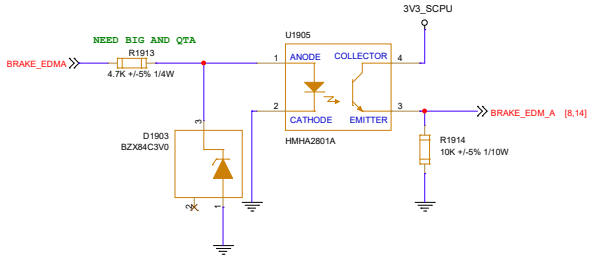


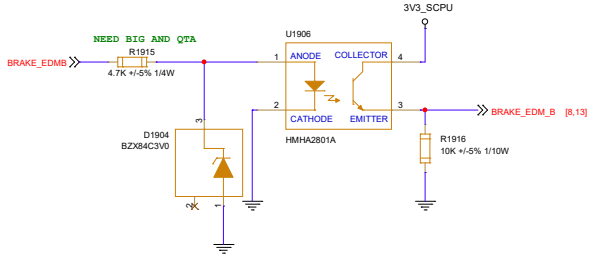


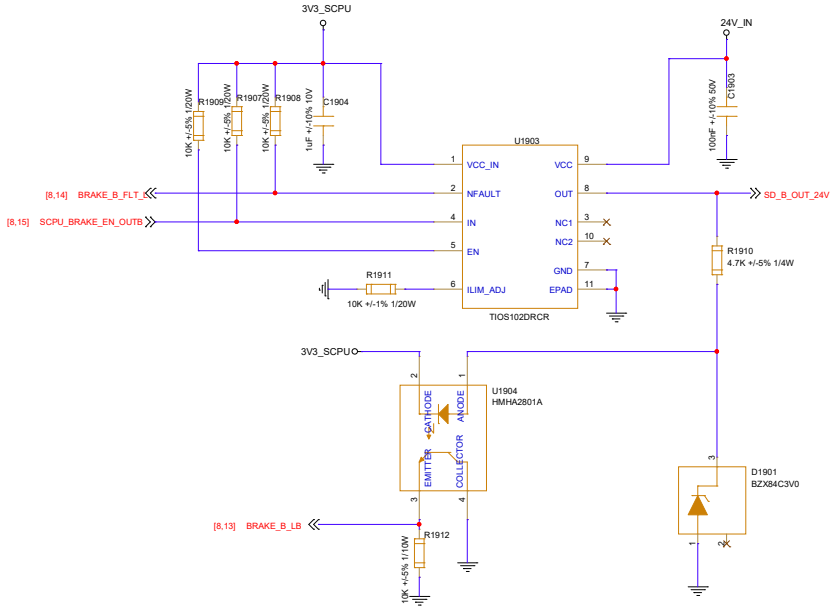
Organization	Quectel Wireless Solutions		
Project	SRAM701A	Ver	1.1
Drawn By	SONI	Checked By	SONI
Size	A2		
Date:	Wednesday, June 10, 2026	Sheet	18 of 21

DRIVER2



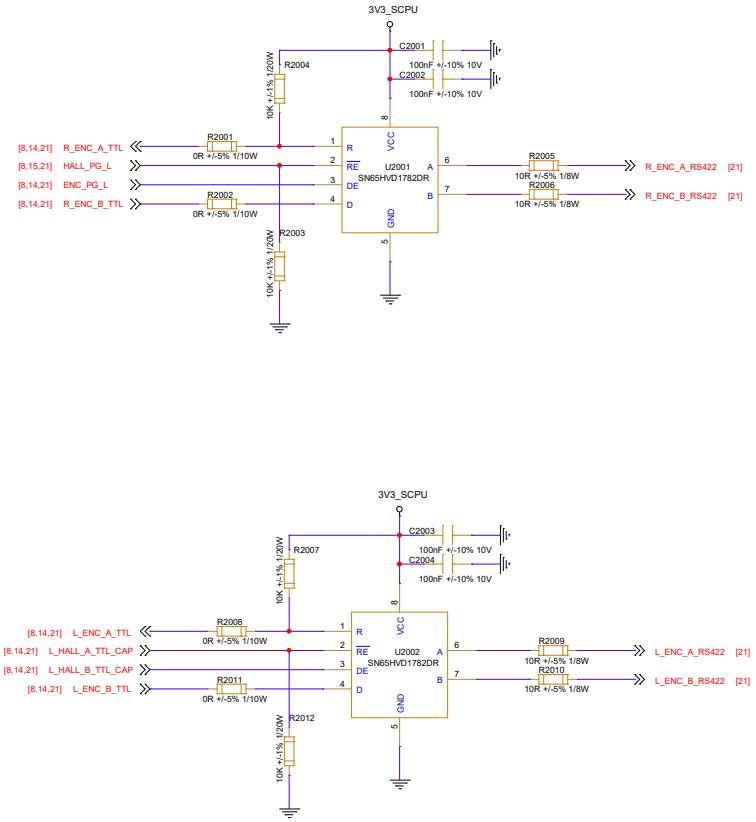






Organization	Quectel Wireless Solutions		
Project	SRAM701A	Ver	1.1
Drawn By	SONI	Checked By	SONI
Size	A2		
Date:	Wednesday, June 10, 2026	Sheet	19 of 21

DRIVER3



Organization: Quectel Wireless Solutions			
Project: SRAM701A		Ver: 1.1	
Drawn By: SONI	Checked By: SONI		Size: A2
Date: Wednesday, June 10, 2026	Sheet 20 of 21		