The Finer Points of a UWIRE Data Transfer for LMK0480x

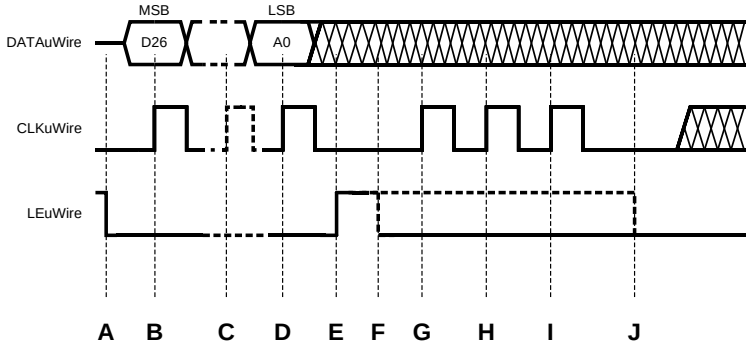

Figure 1 - Timing Diagram of UWIRE transfer

A. Falling edge of previous transfer's Latch Enable (LEuWire)
   - This does not suggest that LEuWire is normally high. All characterization of LMK devices is performed with a normally low LEuWire.

B. Rising edge of clock
   - On the rising edge of the clock, a DATAuWire bit is shifted into a temporary register.
   - A total of 32 rising clock edges must occur to completely load a new register value. The first 27 of bits are the "data" MSB first, then the address.
     - D26 – D25 – D24 … D2 – D1 – D0 – A4 – A3 – A2 – A1 – A0

C. See B

D. See B

E. Latch Enable (LEuWire) rising edge
   - Upon the rising edge, the contents of the temporary register is copied to the addressed register.
   - When programming R30 the VCO calibration routine begins if the internal VCO is used.
   - When programming R0 to R5:
     - If the CLKoutX_Y divide value is <= 25, then the new divide value is instantly loaded.
     - If the CLKoutX_Y divide value is > 25, then the previous divide value > 25 is loaded. Before any divide value > 25 is set, the previous divide value default is 1.
       - This can result in a brief high frequency output when programming a divider > 25 for the first time.
     - If the CKLoutX_Y delay value is <= 12, then the new delay value is instantly loaded.
     - If the CLKoutX_Y delay value is > 12, then the previous delay value > 12 is loaded. Before a delay value > 12 is set, the previous delay value default is 5.
       - Since the delay value is not set until the 3rd rising CLKuWire edge, SYNC_EN_AUTO cannot be used if the LEuWire falling edge occurs before the 3rd rising CLKuWire edge.
   - While LE is high CLKuWire and DATAuWire are disconnected from the internal temporary shift register.
   - On LMK01800 – RESET occurs HERE. (not on falling edge)

F. Latch Enable (LEuWire) falling edge
   - Under normal programming, after LEuWire is raised, LEuWire is lowered once again.
   - When programming R0 with the reset bit set… default state is now set on all registers.
   - Under certain conditions, there are reasons to keep LE high and continue to clock the CLKuWire as described in (G).
   - The falling edge of LEuWire causes a SYNC to be automatically generated when SYNC_EN_AUTO = 1.

G. Optional – CLKuWire while LE is still high.
   - When programming R0 to R5
     - The 3rd rising CLKuWire after LEuWire went high will update the CLKoutX_Y_DIV value (if > 25) and CLKoutX_Y_DDLY value (if > 12).
     - By providing these three (3) clocks before LEuWire is returned low, SYNC_EN_AUTO may be set for any digital delay value.

H. See G, 2nd clock.

I. See G, 3rd clock.
   - At the third clock, the RESET bit in R0 is cleared if it was set during a reset operation.

If LE is brought high again without clocking any new data into the temporary shift register, then the same programming is re-entered. This can result in a SYNC or other such things associated with LE pin toggle.