TMS320C6678 EVM Board for TI

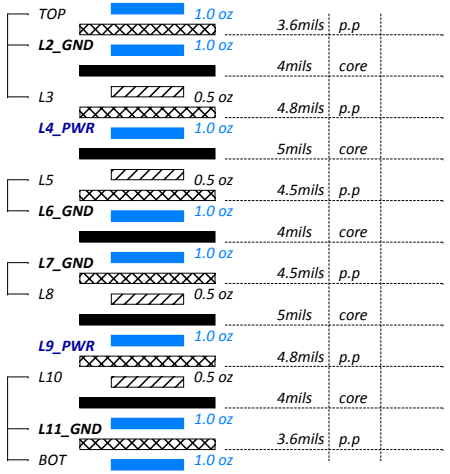
Product name : DSPM-8301E

Rev. A102-1

PCB PN : 19C2830101

Project Code :

PCB Thickness : 62 mils(1.6mm)
12 Layers



Texas Instruments
20450 Century Blvd
Germantown, MD 20874
USA

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TEXAS INSTRUMENTS ADVANTECH

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COVER PAGE		
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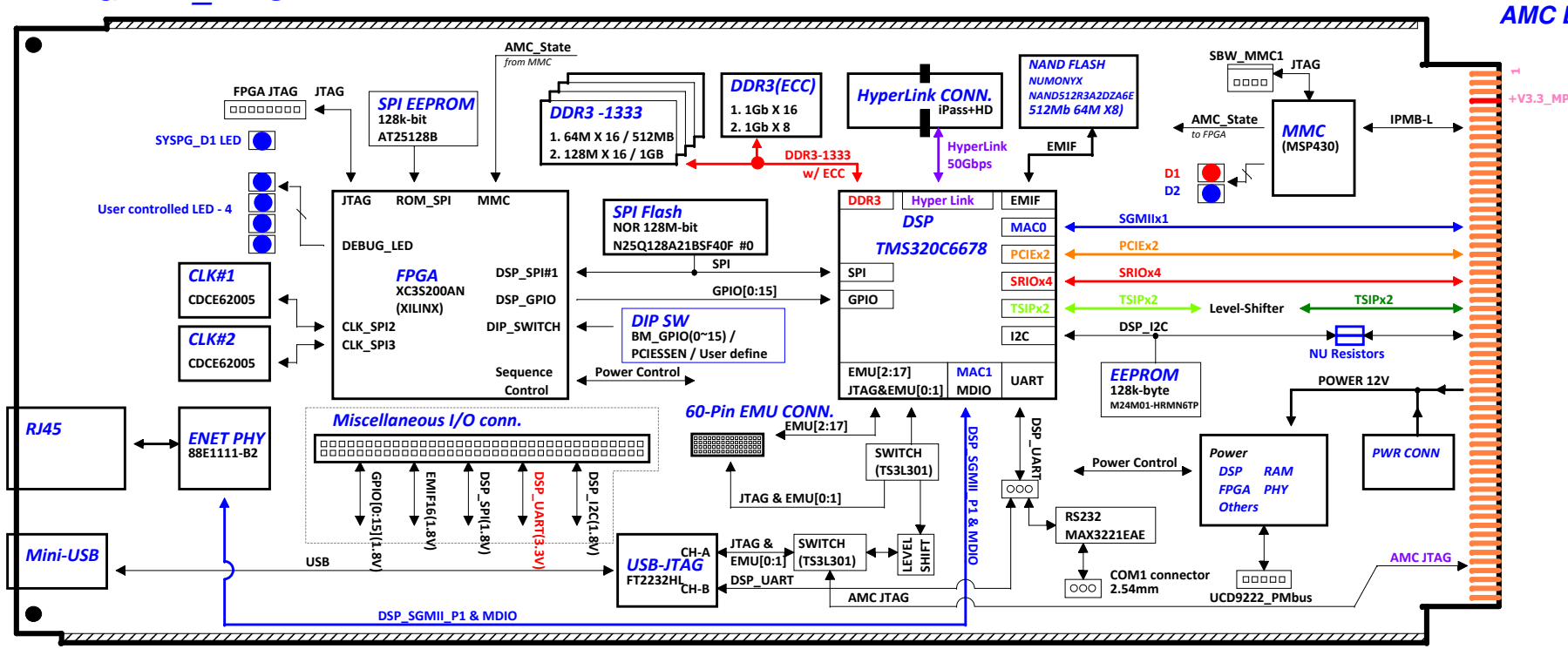
BLOCK DIAGRAM_AMC



Miscellaneous I/O 80 Pin conn. Signal

PIN	Port mapping
02	EMIFA00
04	EMIFA01
06	EMIFA02
08	EMIFA03
10	EMIFA04
12	EMIFA05
14	EMIFA06
16	EMIFA07
18	EMIFA08
20	EMIFA09
22	EMIFA10
24	EMIFA11
26	EMIFA12
28	EMIFA13
30	EMIFA14
32	EMIFA15
34	EMIFA16
36	EMIFA17
38	EMIFA18
40	EMIFA19

PIN	Port mapping
42	EMIFA20
44	EMIFA21
46	EMIFA22
48	EMIFA23
50	GPIO00
52	GPIO01
54	GPIO02
56	GPIO03
58	GPIO04
60	GPIO05
62	GPIO06
64	GPIO07
66	GPIO08
68	GPIO09
70	GPIO10
72	GPIO11
74	GPIO12
76	GPIO13
78	GPIO14
80	GPIO15

PIN	Port mapping
01	GND
03	SDA
05	SCL
07	EMIFD0
09	EMIFD1
11	EMIFD2
13	EMIFD3
15	EMIFD4
17	EMIFD5
19	EMIFD6
21	EMIFD7
23	EMIFD8
25	EMIFD9
27	EMIFD10
29	EMIFD11
31	EMIFD12
33	EMIFD13
35	EMIFD14
37	EMIFD15
39	EMIFCE1Z

PIN	Port mapping
41	EMIFCE2Z
43	EMIFBE0z
45	EMIFBE1z
47	EMIFOEz
49	EMIFWEz
51	EMIFRnW
53	EMIFWAIT1
55	TIMI0
57	TIMO0
59	TIMI1
61	TIMO1
63	SSPMISO
65	SSPMOSI
67	SSPCS1
69	SSPCK
71	UARTTXD
73	UARTRXD
75	UARTRTS
77	UARTCTS
79	GND

AMC Port mapping

PIN	Port mapping
TCLKA	TSIP_CLK0
TCLKB	TSIP_CLK1
FCLKA	100MHz
00	SGMII
01	
02	
03	
04	PCI-E_1
05	PCI-E_2
06	
07	
08	SRIO_1
09	SRIO_2
10	SRIO_3

PIN	Port mapping
11	SRIO_4
12	TSIP0 [0..3]
13	TSIP1 [0..3]
14	
15	Alternate I2C link
16	
TCLKC	TSIP_FS0
TCLKD	TSIP_FS1
17	
18	
19	
20	
	AMC_JTAG

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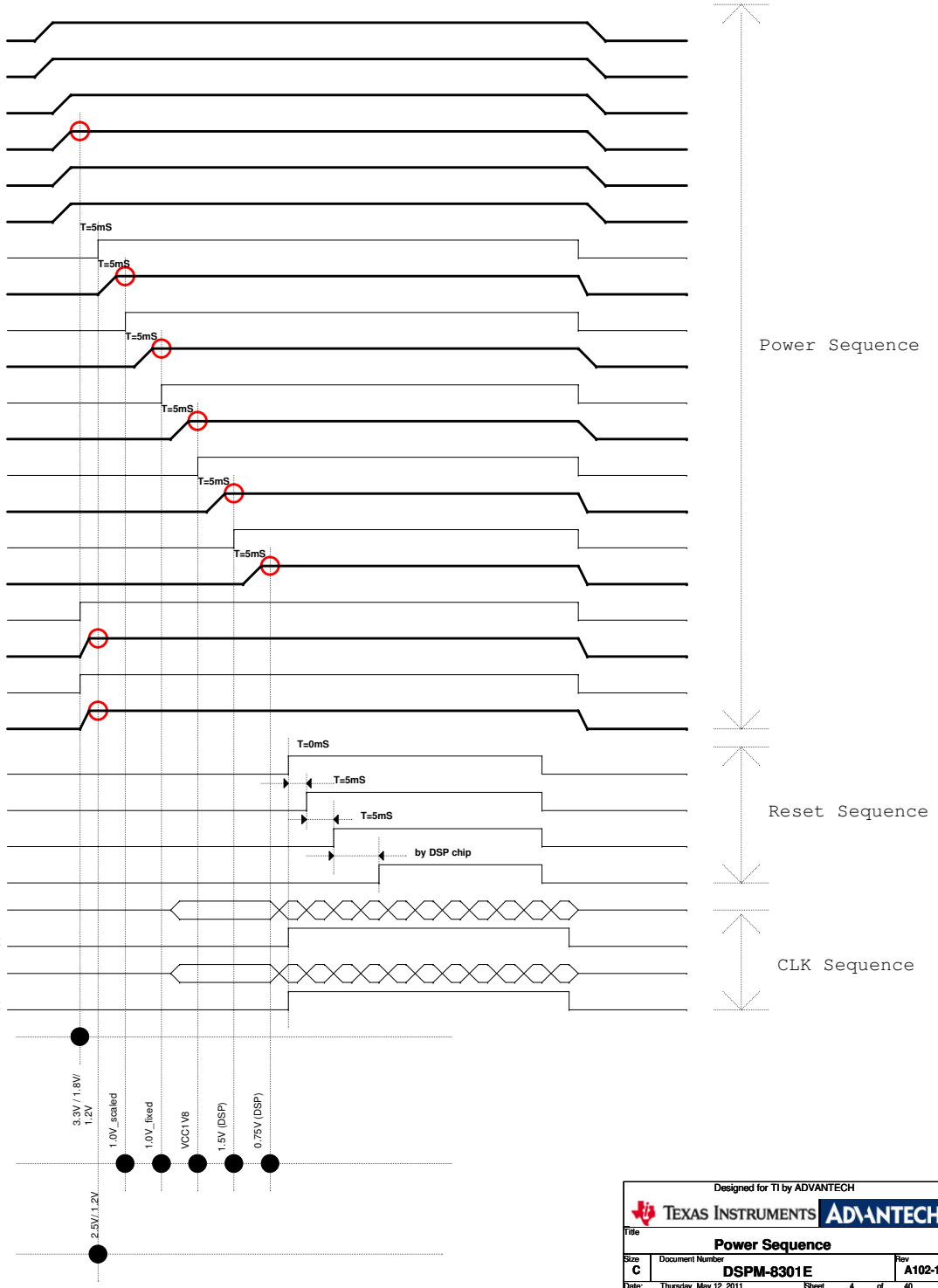
Power Sequence

Label	Time	Description
T0	1ms	S2 plane power stable to S3 enable signal assertion

				VCC3V3_MP_AMC
S0		MMC		VCC3V3_MP
S1				VCC12
S2	Other	FT2232H	XC3S200AN	VCC3V3_AUX
S3			XC3S200AN	VCC1V8_AUX
S4		88E1111	XC3S200AN	VCC1V2
S5				PMBUS & UCD9222_ENA1
S6		DSP TMS320C6678		CVDD
S7				UCD9222_VID2 & UCD9222_ENA2
S8		DSP TMS320C6678		VCC1V0
S9				VCC1V8_EN
S10		DSP TMS320C6678		VCC1V8
S11				VCC1V5_EN
S12	DDR3	DSP TMS320C6678		DDR3 SDRAM VCC1V5
S13				VCC0V75_EN
S14	DDR3	DSP TMS320C6678		DDR3 Vref VCC0V75
S15				VCC2V5_EN
S16		88E1111		VCC2V5
S17				VCC5_EN
S18		XDS560V2 Mazzenine Board		VCC5



Ther is no specific power-up nor power-down sequence.

XILINX_XC3S200AN

1.2V_AUX (VCCINT)
1.8V_AUX (VCC1V8_AUX)
3.3V_AUX (VCCAUX)

XILINX_XC3S200AN

When power on: VDD → VCC_1V0 scaled (0ms<t<100us) → VCC_1V0 Fixed (0ms<t<100us) → VCC1V8 (0ms<t<100us) → 1.5V/(DDR3_IO) 0.75V/(DDR3_Vref)

When power down: 1.5V/(DDR3_IO) 0.75V/(DDR3_Vref) (0ms<t<100us) → VCC1V8 (0ms<t<100us) → VCC_1V0 Fixed (0ms<t<100ms) → VCC_1V0 scaled → VDD

DSP TMS320C6678

VCC1V0 Scaled/(CVDD)
VCC1V0 Fixed/(CVDD1)
VCC1V8/ (DVDD18)
1.5V/(DDR3_IO)
0.75V/(DDR3_Vref)

DSP TMS320C6678

Ther is no specific power-up nor power-down sequence.

88E1111 (PHY)

2.5V
1.2V

88E1111

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POWER CONSUMPTION

							Max. Power Design			Operating (for Thermal)		
		V	I	Qty	Isub.	Efficiency	Pd (W)	I12V	I3vsb	Utilization	Pd (W)	Note
CVDD (12V-->1.0V)					**8.000**			**0.741**				UCD9222 + UCD7242
	TMS320C6678	1.00	8.000	1	8.000	90%	8.889	0.741	x	70%	6.222	
VCC1V0 (12V-->1.0V)					**5.000**			**0.463**				
	TMS320C6678	1.00	5.000	1	5.000	90%	5.556	0.463	x	70%	3.889	
VCC1V5 (12V-->1.5V)					**2.300**			**0.319**				TPS54620
	TMS320C6678	1.50	0.850	1	0.850	90%	1.417	0.118	x	70%	0.992	
	DDR3	1.50	0.240	5	1.200	90%	2.000	0.167	x	100%	2.000	
	VCC0V75 (VTT for DDR3) 1.5V-->0.75V							x				TPS51200
	DDR3	0.75	0.050	5	0.250	45%	0.417	0.035	x	70%	0.292	
VCC3V3_AUX (12V-->3.3V_AUX)					**2.484**			**0.748**				TPS54620
	FPGA	3.30	0.024	1	0.024	85%	0.093	0.008	x	70%	0.065	
	XDS560V2 Mazzenine Board	3.30	0.300	1	0.300	85%	1.165	0.097	x	70%	0.815	
	FT2232H	3.30	0.210	1	0.210	85%	0.815	0.068	x	70%	0.571	
	Others	3.30	0.660	1	0.660	85%	2.562	0.214	x	70%	1.794	
	VCC1V8_AUX (3.3V_AUX-->1.8V_AUX)							x				TPS73701DCQ
	FPGA	1.80	0.200	1	0.200	46%	0.783	0.065	x	70%	0.548	
	Others	1.80	0.100	1	0.100	46%	0.391	0.033	x	70%	0.274	
	VCC1V8 (3.3V_AUX-->1.8V)							x				TPS73701DCQ
	TMS320C6678	1.80	0.330	1	0.330	46%	1.291	0.108	x	70%	0.904	
	FT2232H	1.80	0.075	1	0.075	46%	0.293	0.024	x	70%	0.205	
	VCC1V2_AUX (3.3V_AUX-->1.2V_AUX)							x				TPS73701DCQ
	FPGA	1.20	0.125	1	0.125	30%	0.500	0.042	x	70%	0.350	
	88E1111	1.00	0.250	1	0.250	90%	0.278	0.023	x	70%	0.194	
	VCC2V5 (3.3V_AUX-->2.5V)							x				TPS73701DCQ
	88E1111	2.50	0.210	1	0.210	65%	0.808	0.067	x	70%	0.565	
VCC5 (12V-->5V)					**1.000**			**0.490**				TPS54231
	XDS560V2 Mazzenine Board	5.00	1.000	1	1.000	85%	5.882	0.490	x	70%	4.118	
VCC3V3_MP_AMC (150mA)					**0.048**			x	**0.048**			
	MMC_MSP430	3.30	0.048	1	0.048	100%	0.158	x	0.048	70%	0.111	
Total power consumption							**Pmax.**	**I12V**	**I3VSB**		**Pop.**	
							33.298	**2.762**	**0.096**		**23.909**	

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Title: POWER CONSUMPTION

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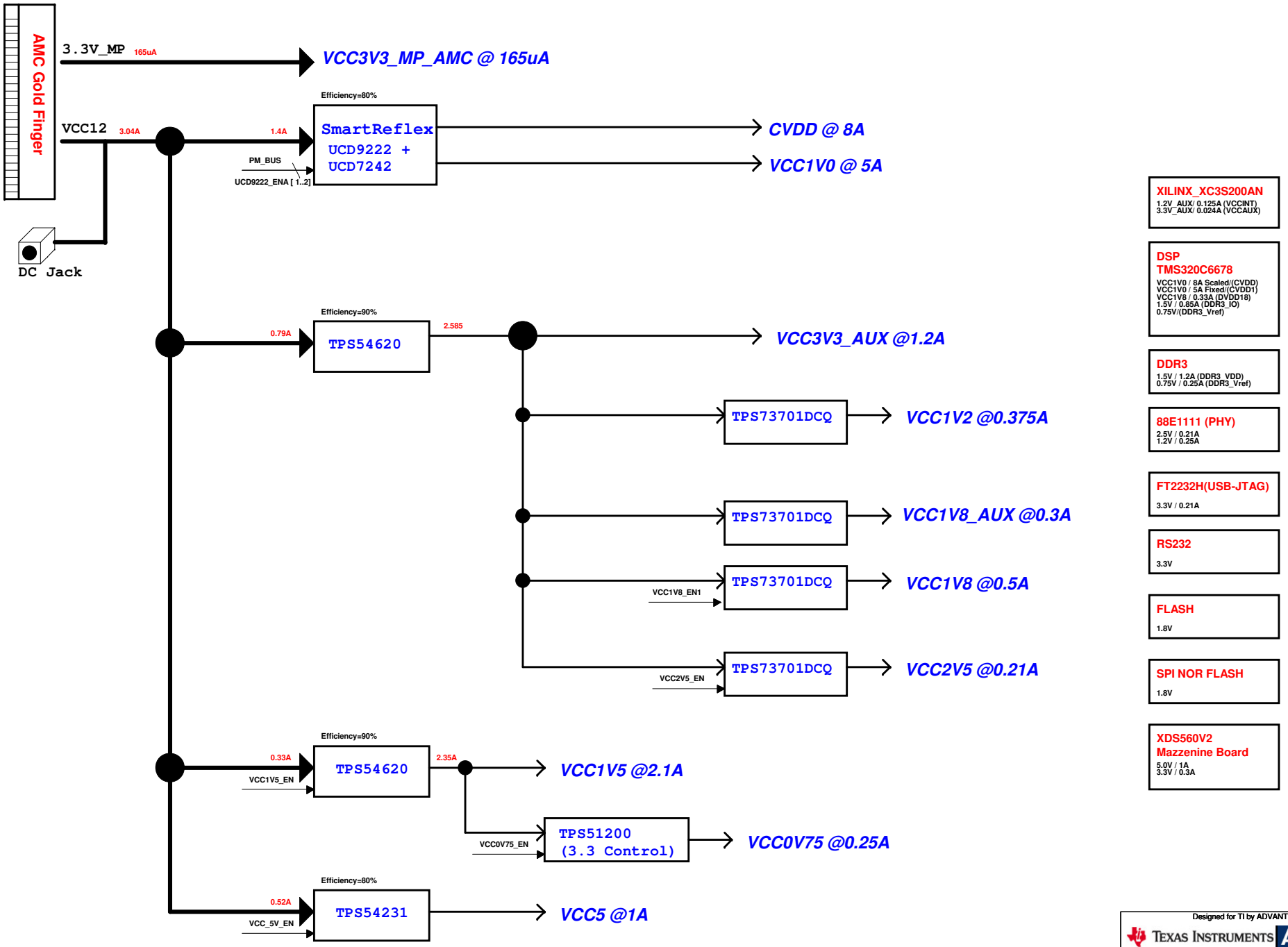
POWER DISTRIBUTION



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Title	POWER DISTRIBUTION	
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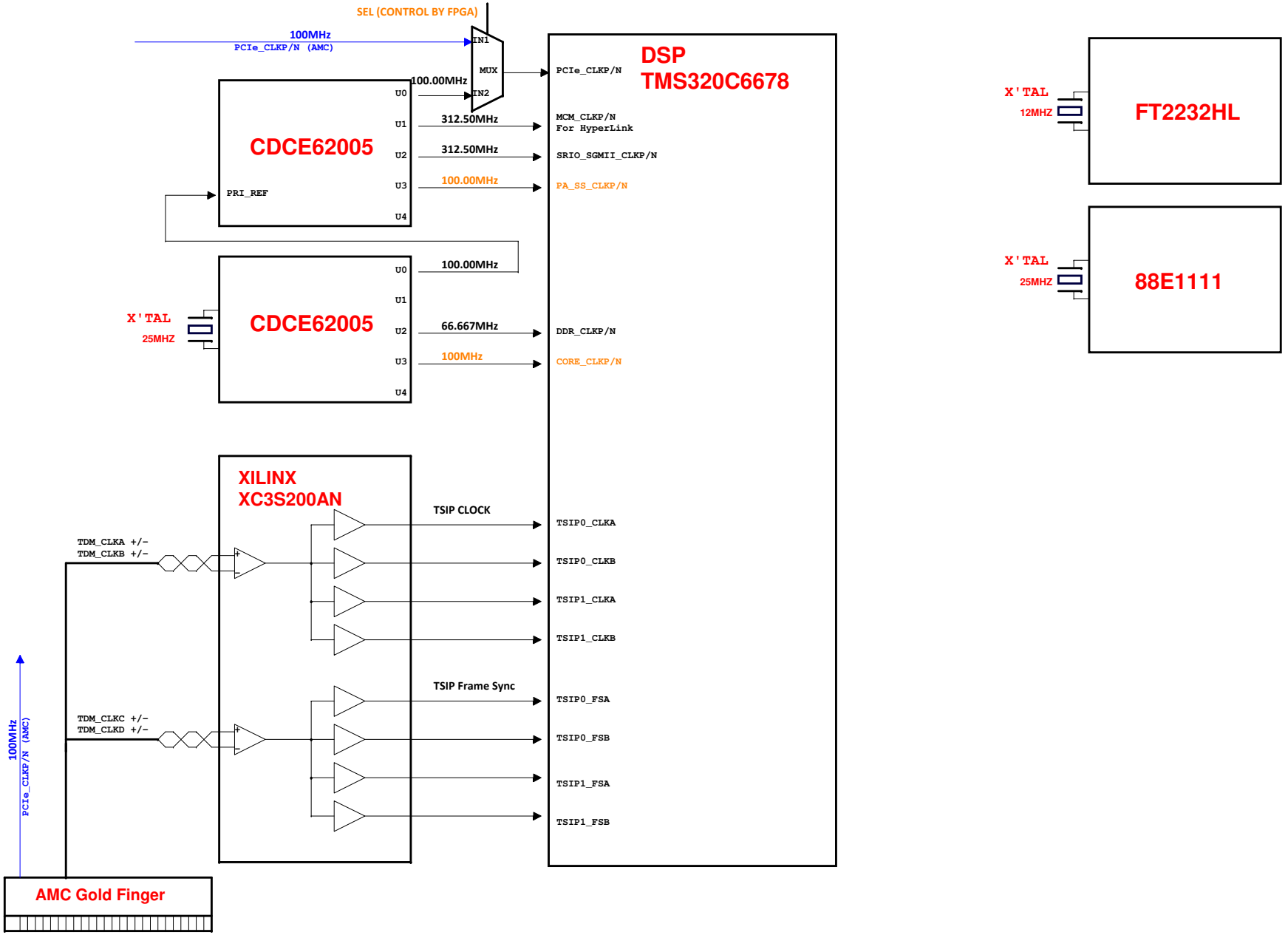
CLOCK DIAGRAM



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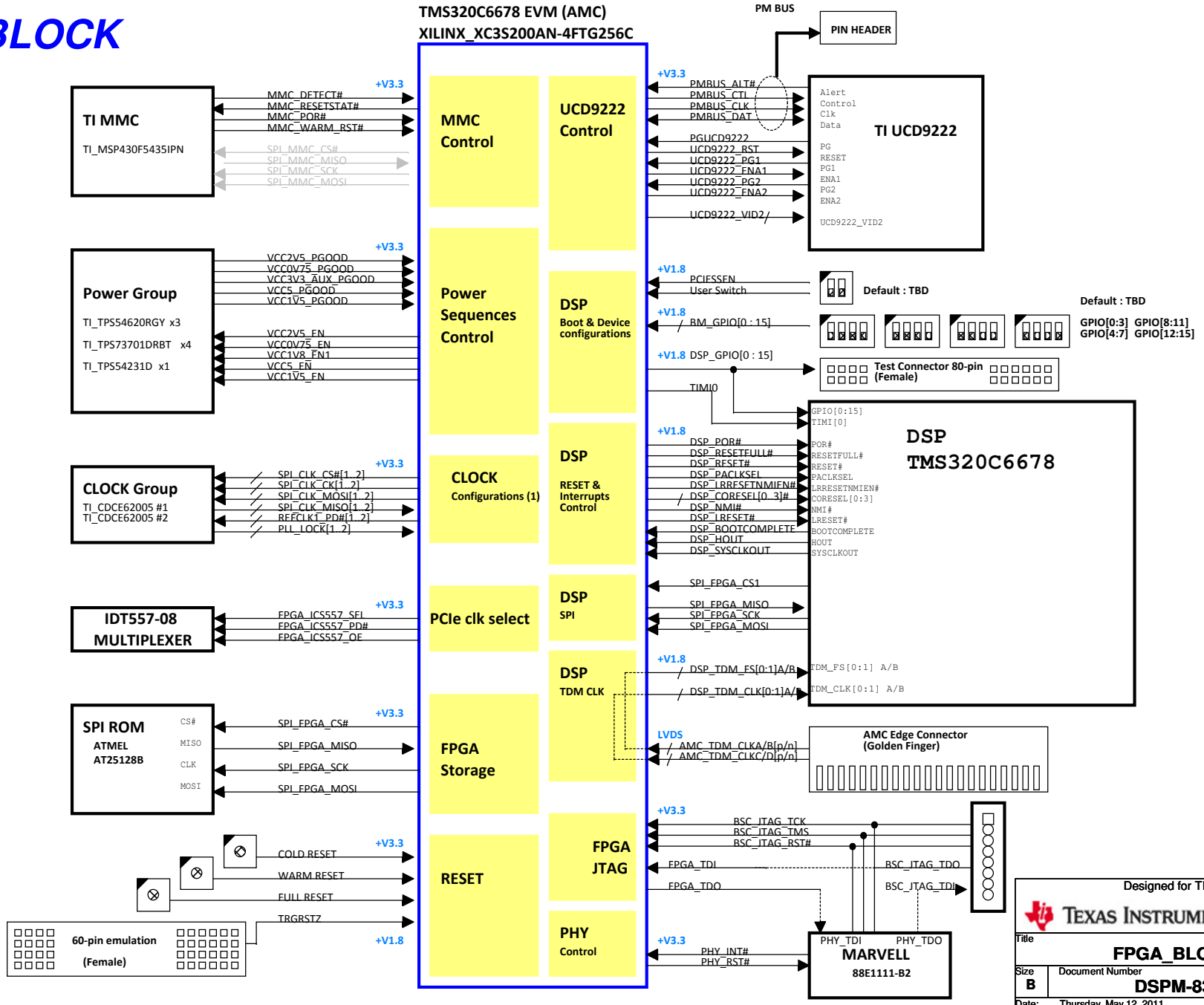
FPGA_BLOCK


TMS320C6678 EVM (AMC)
XILINX_XC3S200AN-4FTG256C
PM BUS
PIN HEADER
TI MMC
TI_MSP430F5435IPN
MMC_DETECT#
MMC_RESETSTAT#
MMC_POR#
MMC_WARM_RST#
SPI_MMC_CS#
SPI_MMC_MISO
SPI_MMC_SCK
SPI_MMC_MOSI
+V3.3
MMC Control
UCD9222 Control
PMBUS_ALT#
PMBUS_CTL
PMBUS_CLK
PMBUS_DAT
PGUCD9222
UCD9222_RST
UCD9222_PG1
UCD9222_ENA1
UCD9222_PG2
UCD9222_ENA2
UCD9222_VID2
Alert
Control
Clk
Data
PG
RESET
PG1
ENA1
PG2
ENA2
UCD9222_VID2
TI UCD9222
Power Group
TI_TPS54620RGY x3
TI_TPS73701DRBT x4
TI_TPS54231D x1
VCC2V5_PGOOD
VCC0V75_PGOOD
VCC3V3_AUX_PGOOD
VCC5_PGOOD
VCC1V5_PGOOD
VCC2V5_EN
VCC0V75_EN
VCC1V8_EN1
VCC5_EN
VCC1V5_EN
Power Sequences Control
DSP Boot & Device configurations
+V1.8
PCIESSEN
User Switch
Default : TBD
BM_GPIO[0 : 15]
Default : TBD
GPIO[0:3] GPIO[8:11]
GPIO[4:7] GPIO[12:15]
DSP_GPIO[0 : 15]
Test Connector 80-pin (Female)
TIMI0
GPIO[0:15]
TIMI[0]
DSP TMS320C6678
CLOCK Group
TI_CDCE62005 #1
TI_CDCE62005 #2
SPI_CLK_CS#[1..2]
SPI_CLK_CK[1..2]
SPI_CLK_MOSI[1..2]
SPI_CLK_MISO[1..2]
REFCLK1_PD#[1..2]
PLL_LOCK[1..2]
CLOCK Configurations (1)
DSP RESET & Interrupts Control
DSP_POR#
DSP_RESETFULL#
DSP_RESET#
DSP_PACLKSEL
DSP_LRRESETNMIEN#
DSP_CORESEL[0..3]#
DSP_NMI#
DSP_LRESET#
DSP_BOOTCOMPLETE
DSP_HOUT
DSP_SYSCLKOUT
POR#
RESETFULL#
RESET#
PACLKSEL
LRRESETNMIEN#
CORESEL[0:3]
NMI#
LRESET#
BOOTCOMPLETE
HOUT
SYSCLKOUT
IDT557-08 MULTIPLEXER
FPGA_ICS557_SEL
FPGA_ICS557_PD#
FPGA_ICS557_OE
PCIe clk select
DSP SPI
SPI_FPGA_CS1
SPI_FPGA_MISO
SPI_FPGA_SCK
SPI_FPGA_MOSI
DSP TDM CLK
DSP_TDM_FS[0:1]A/B
DSP_TDM_CLK[0:1]A/B
TDM_FS[0:1] A/B
TDM_CLK[0:1] A/B
SPI ROM
ATMEL
AT25128B
CS#
MISO
CLK
MOSI
SPI_FPGA_CS#
SPI_FPGA_MISO
SPI_FPGA_SCK
SPI_FPGA_MOSI
FPGA Storage
LVDS
AMC_TDM_CLKA/B[p/n]
AMC_TDM_CLKC/D[p/n]
AMC Edge Connector (Golden Finger)
COLD RESET
WARM RESET
FULL RESET
TRGRSTZ
60-pin emulation
(Female)
RESET
FPGA JTAG
BSC_JTAG_TCK
BSC_JTAG_TMS
BSC_JTAG_RST#
FPGA_TDI
FPGA_TDO
BSC_JTAG_TDO
BSC_JTAG_TDI
PHY Control
PHY_INT#
PHY_RST#
PHY_TDI
PHY_TDO
MARVELL
88E1111-B2
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FPGA_BLOCK
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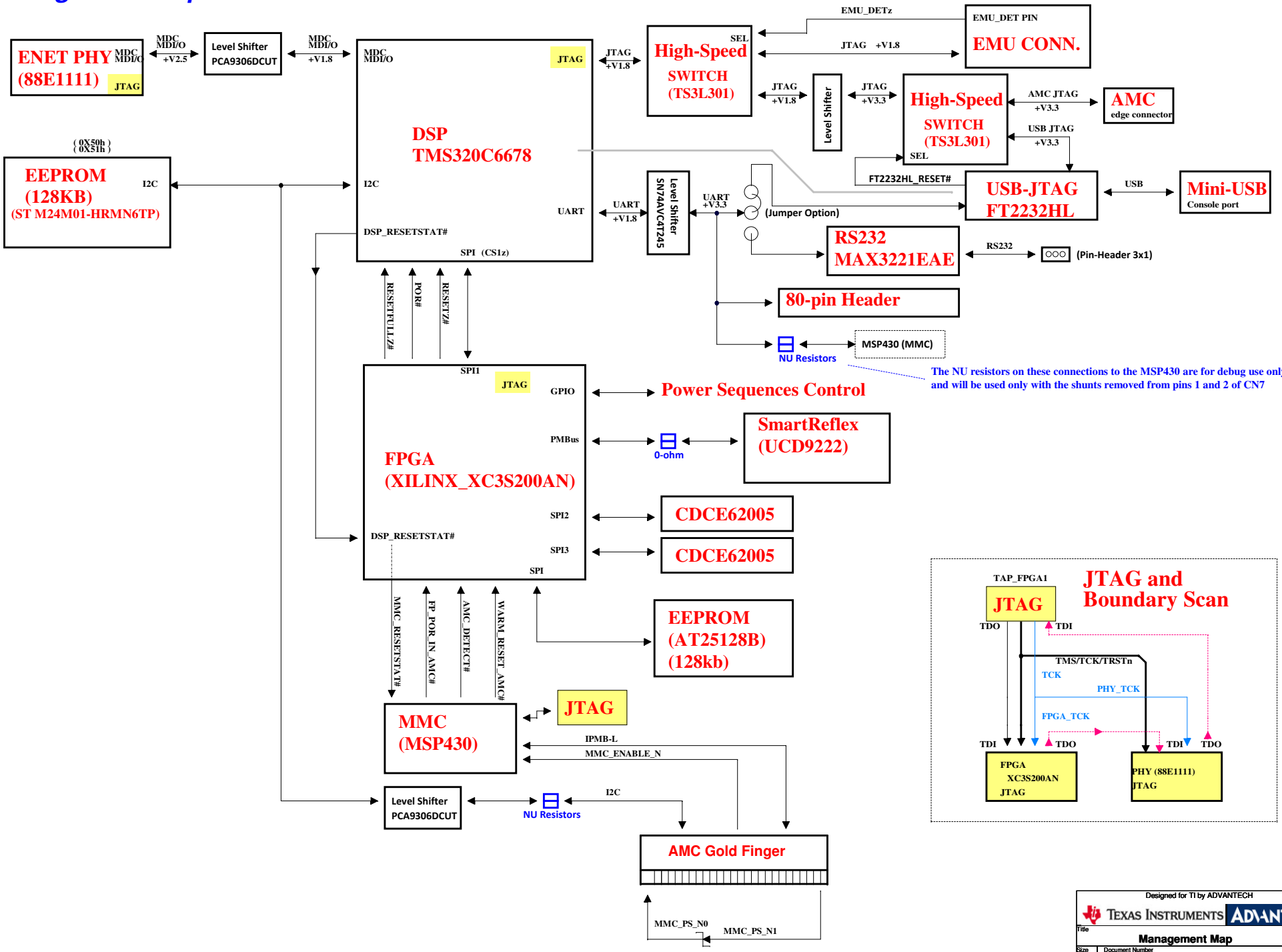
Management Map



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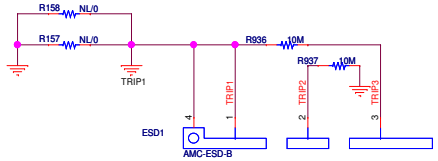
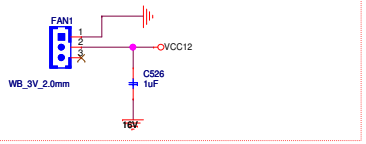
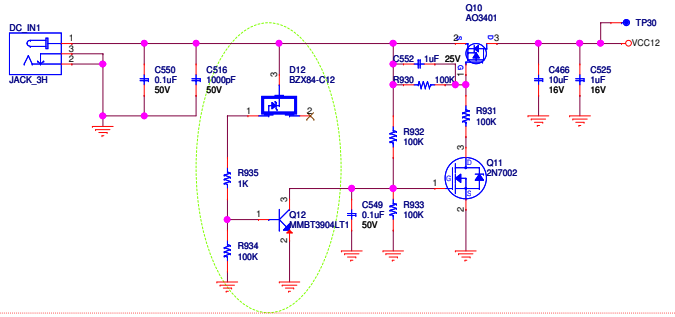
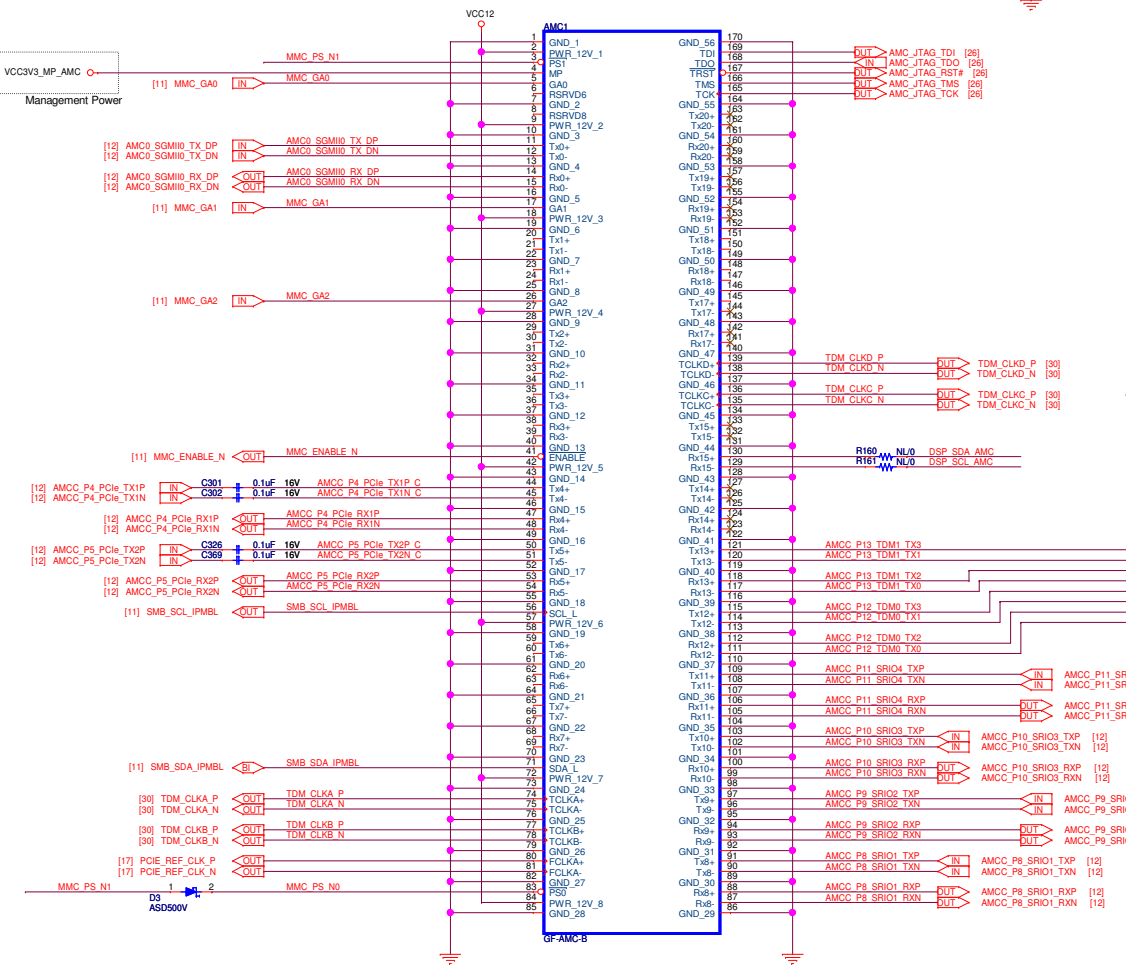
Front panel and ESD Strip

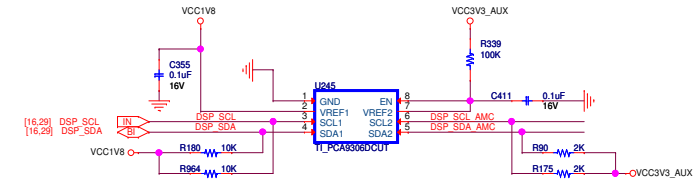


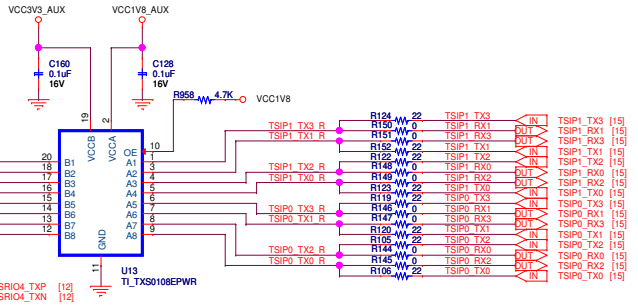


OVP: ~12.7V+0.6V = ~13.3V

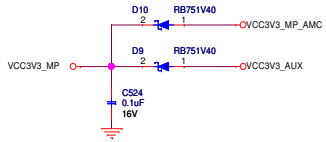


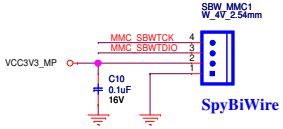


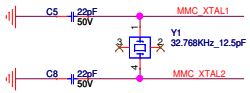


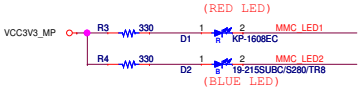


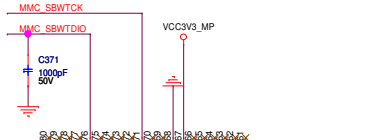
Power for MSP430

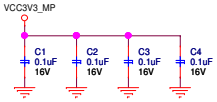


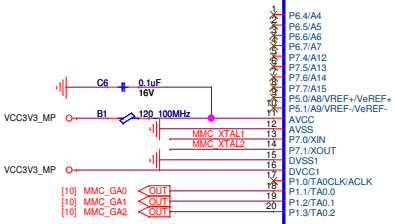


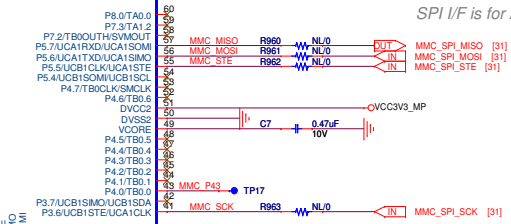




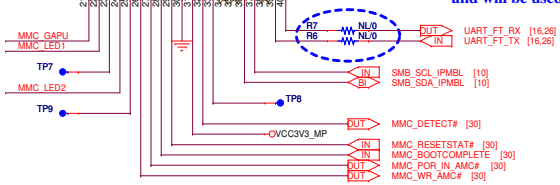




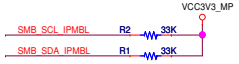


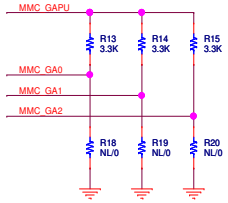


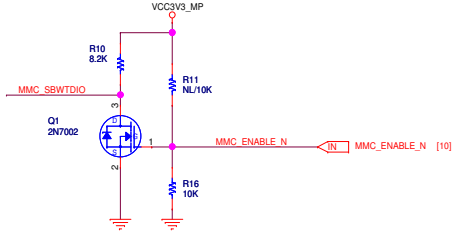
SPI I/F is for Advantech FPGA debugging.



The NU resistors on these connections to the MSP430 are for debug use only and will be used only with the shunts removed from pins 1 and 2 of CN7







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TEXAS INSTRUMENTS ADVANTECH

Title	MMC	
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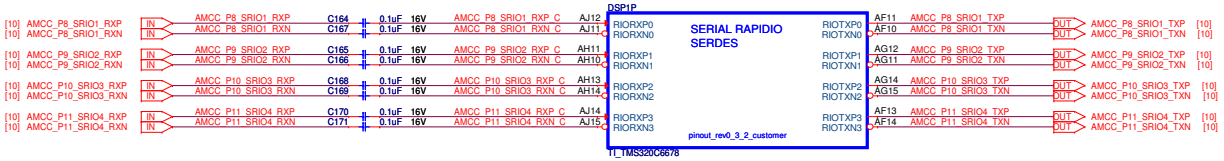
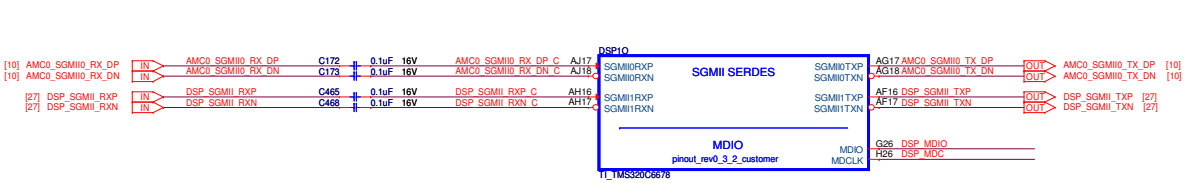
SRIO

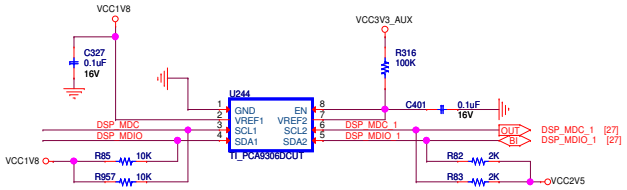


Caution!

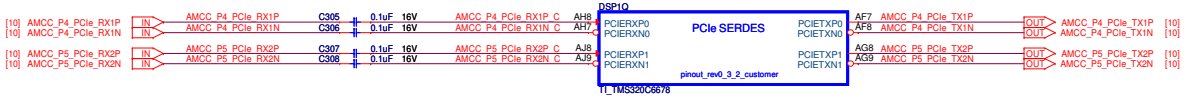
"Place ALL SERDES DC-blocking caps on top layer adjacent to the DSP's RX pins so that there are no additional vias"

SGMII

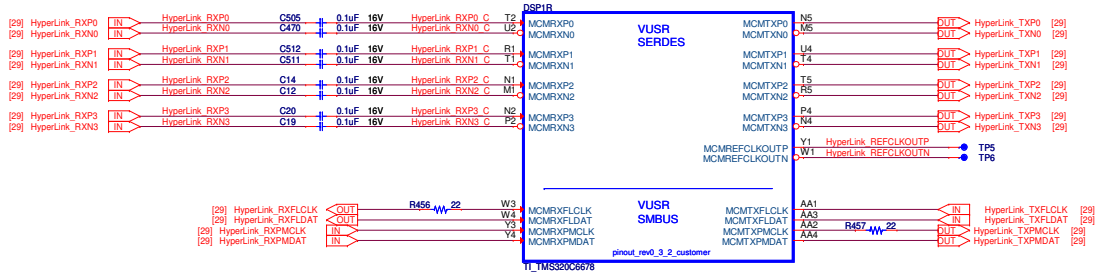




PCIE



HyperLink



"The HyperLink routes must have a maximum of 2 vias and no via stubs – top layer routing recommended"

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TEXAS INSTRUMENTS ADVANTECH

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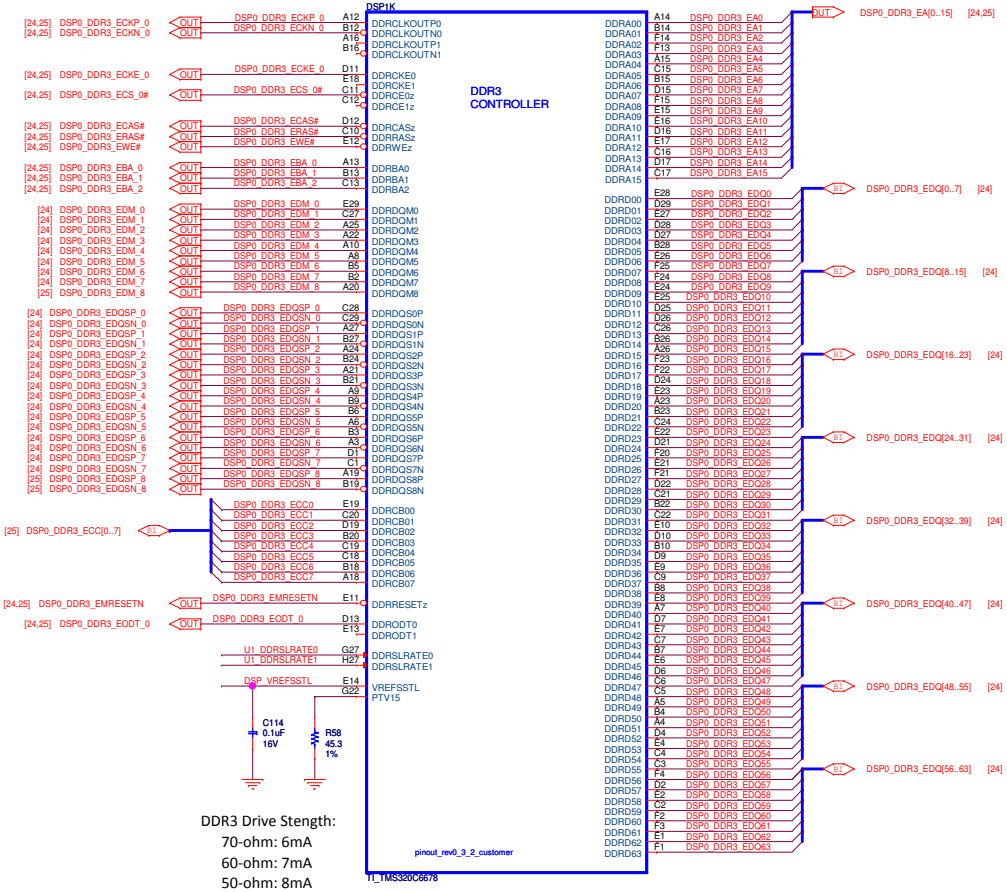


DDR3 Drive Stength:

70-ohm: 6mA

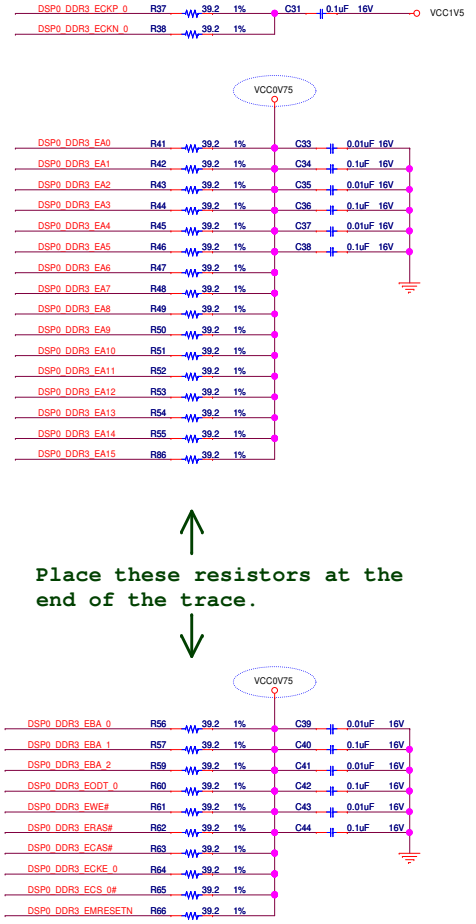
60-ohm: 7mA

50-ohm: 8mA

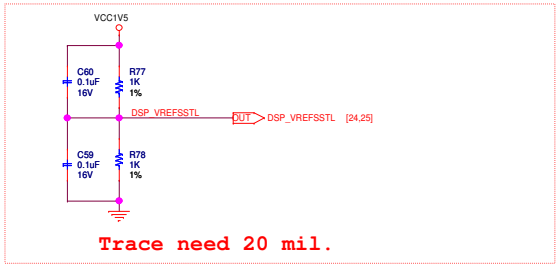
45-ohm: 9mA

40-ohm: 10mA

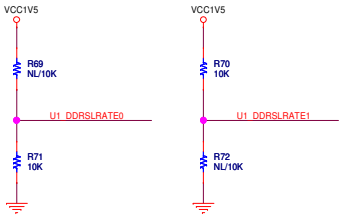
36-ohm: 11mA



Place these resistors at the end of the trace.



Trace need 20 mil.



DDR3 Slew-Rate Setting (DDRSLRATE[1:0]):

0 0 Fastest

1 0 Fast

0 1 Slow

1 1 Slowest

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Title		
DSP_DDR3		
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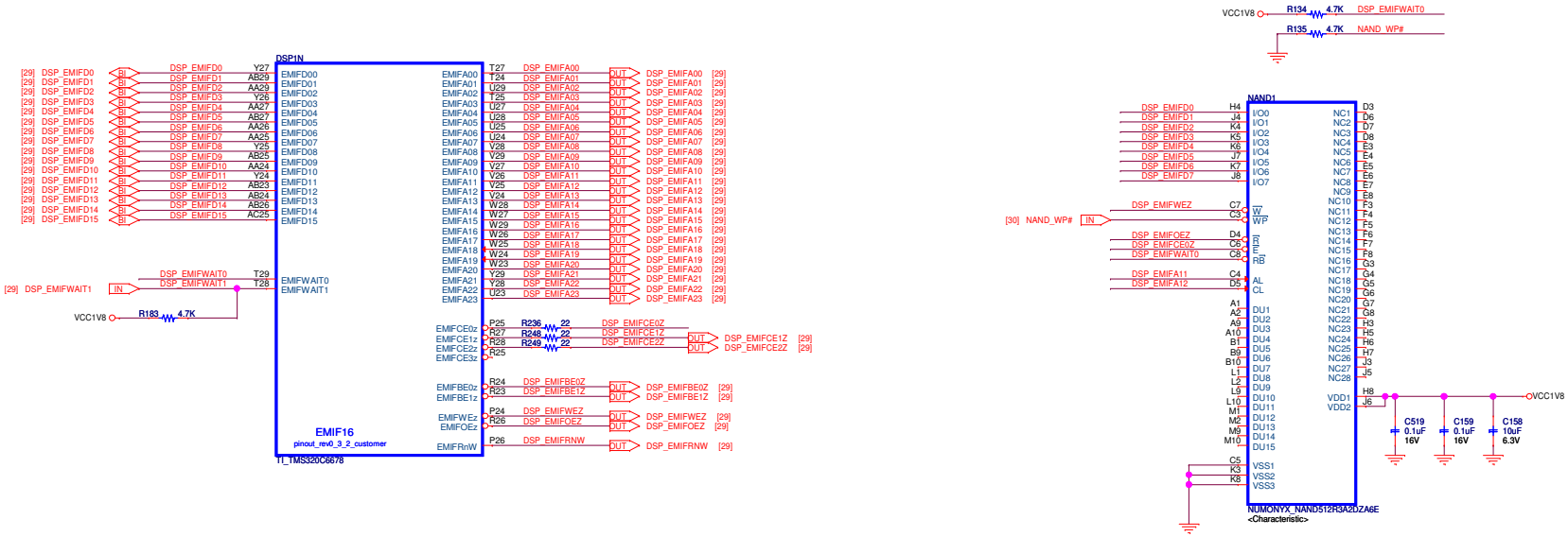

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Title	DSP_EMIF	
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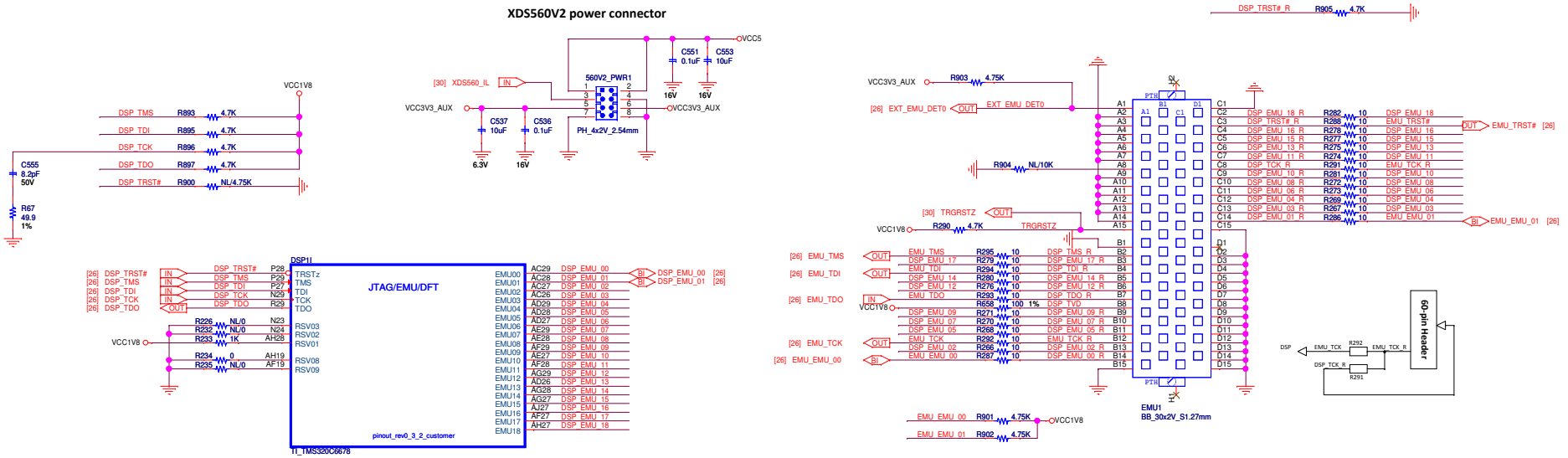
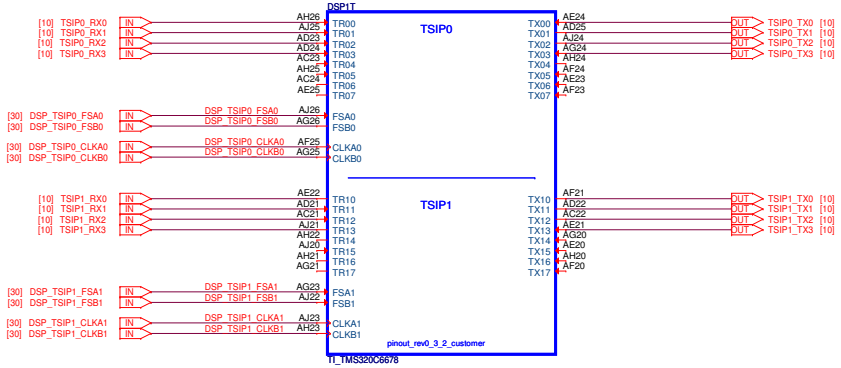
JTAG & EMU



TSIP0, 1



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TEXAS INSTRUMENTS ADVANTECH

Title	DSP_JTAG_EMU_TSIP		
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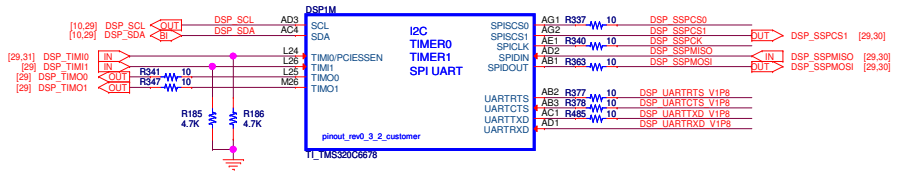
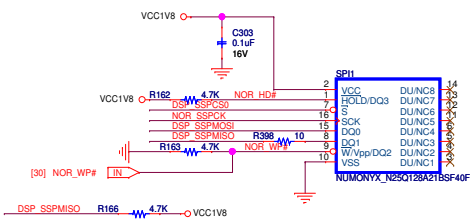
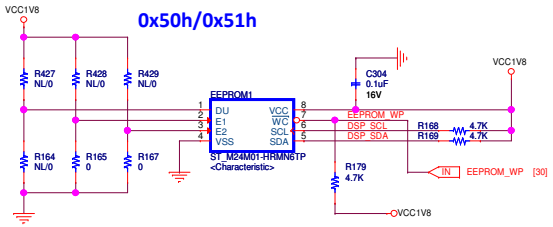
I2C, TIMER0,1, SPI, UART



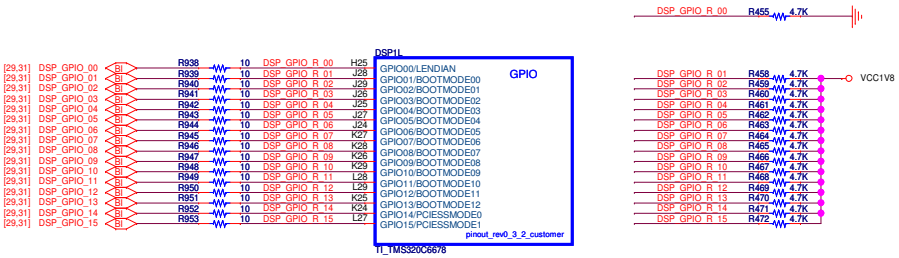
16M SPI NOR Flash

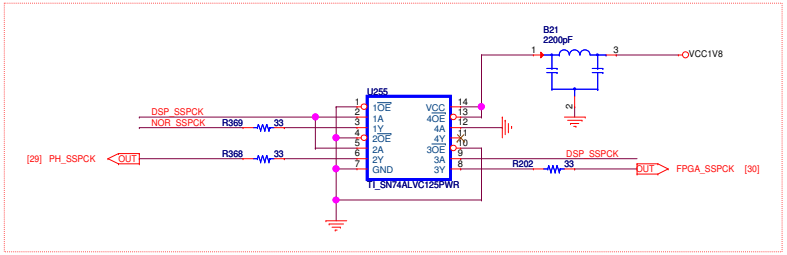


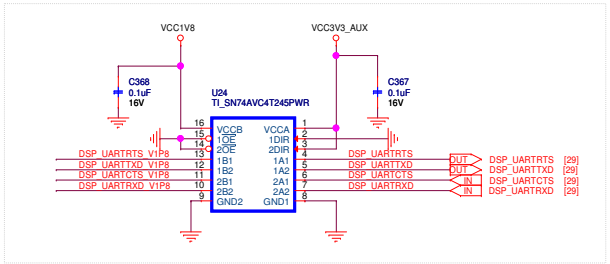
1M-bit I2C EEPROM
0x50h/0x51h



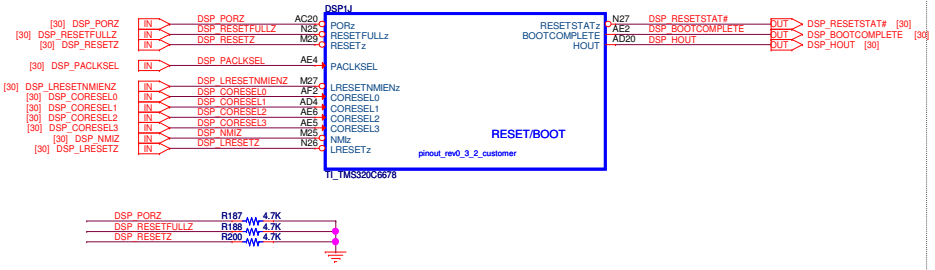
GPIO

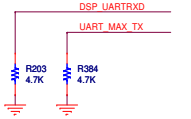


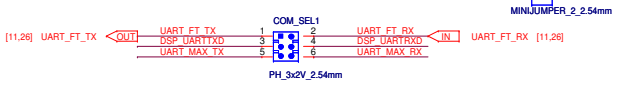




Reset Control



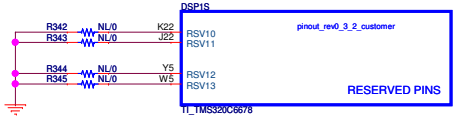


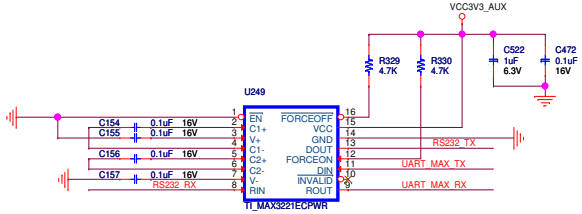


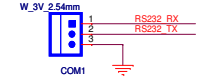
SMD to DIP for PCB space.

JP-UART(1-3) & (2-4) : UART over USB Connector (Default)
JP-UART(3-5) & (4-6) : UART over 3-Pin Header J5

Reserved







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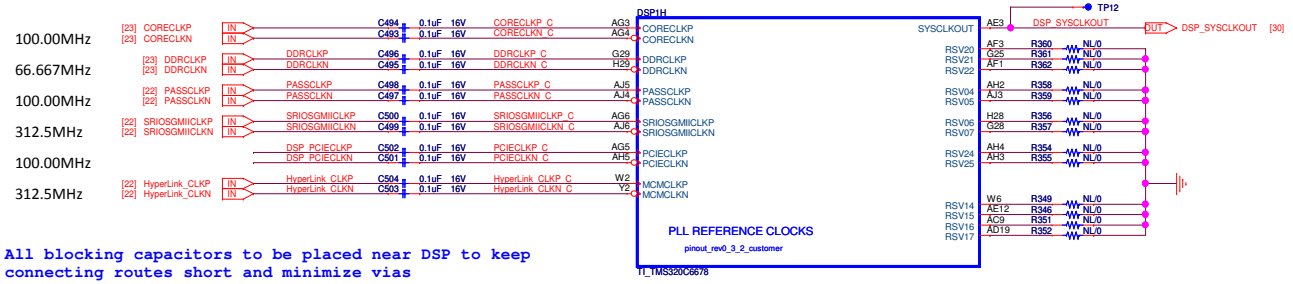
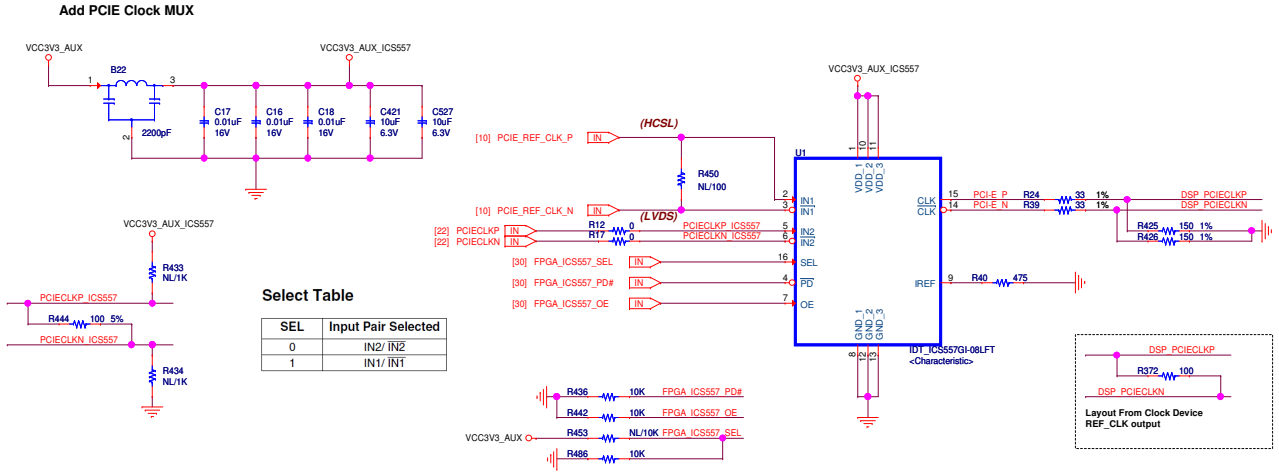
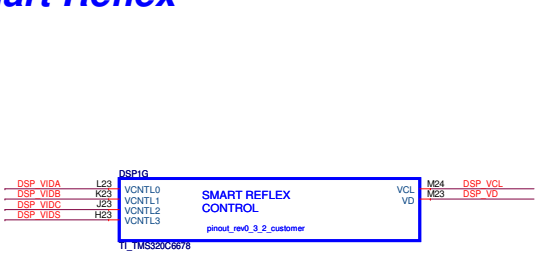
DSP CLOCK

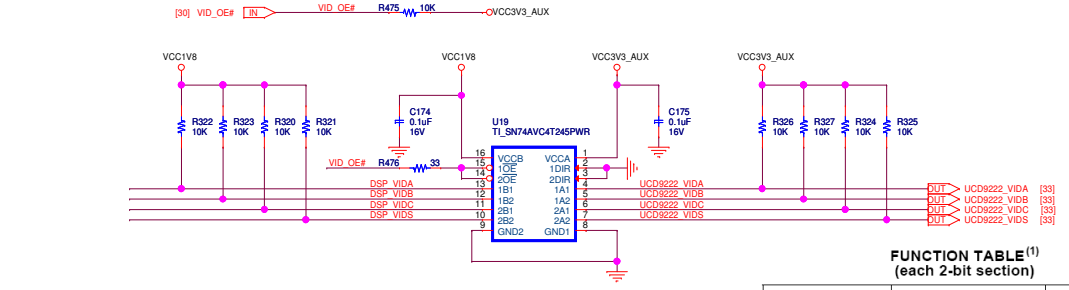


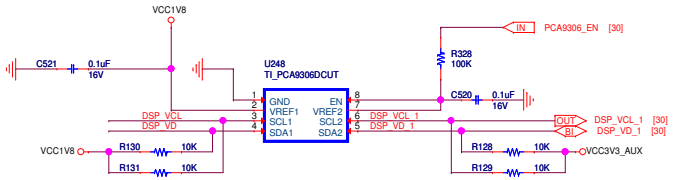
"All DC-blocking capacitors to be placed near DSP to keep connecting routes short and minimize vias"



Smart Reflex







FUNCTION TABLE(1)
(each 2-bit section)

CONTROL INPUTS		OUTPUT CIRCUITS		OPERATION
$\overline{OE}$	DIR	A PORT	B PORT	
L	L	Enabled	Hi-Z	B data to A bus
L	H	Hi-Z	Enabled	A data to B bus
H	X	Hi-Z	Hi-Z	Isolation

(1) Input circuits of the data I/Os are always active.

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Title: DSP_CLOCK_Smart Reflex

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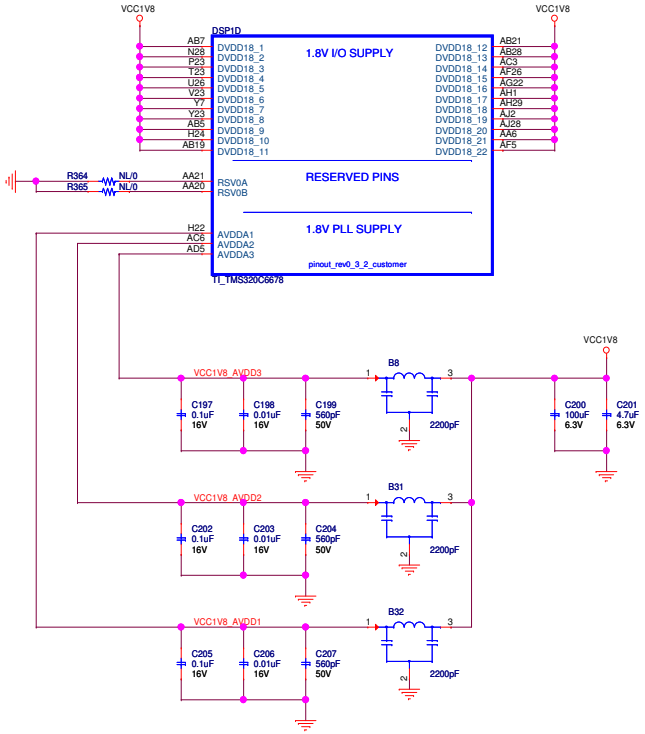
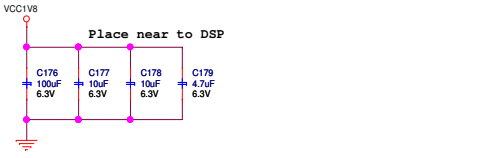
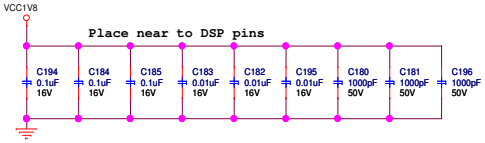
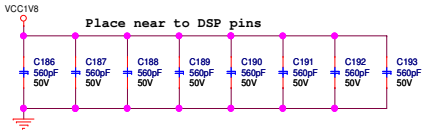
1.8V

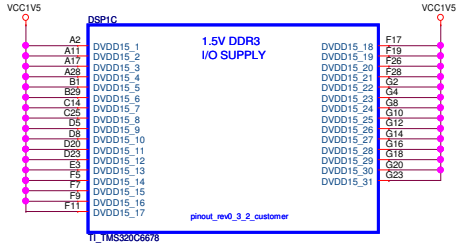


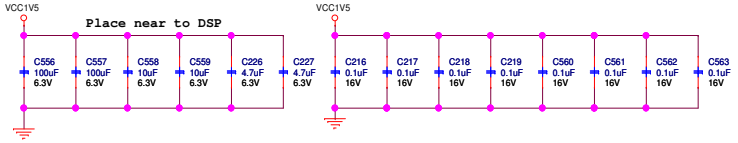


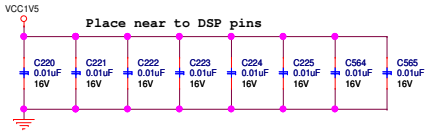


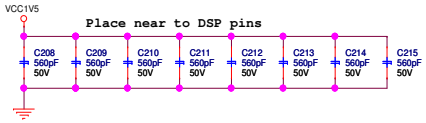


1.5V









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Title: DSP_POWERA

Size	Document Number	Rev
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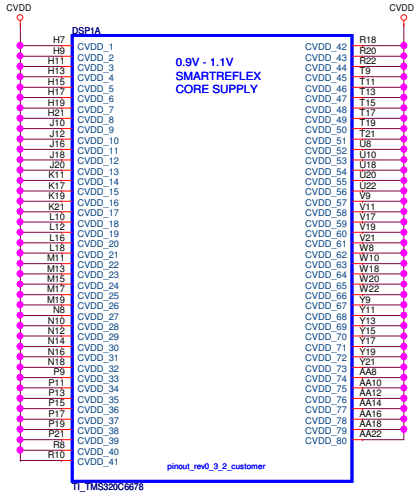
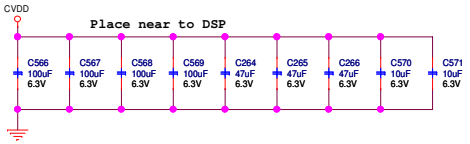
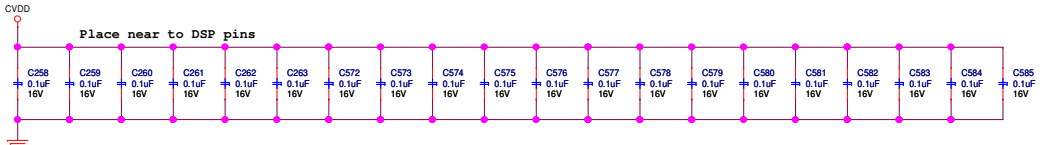
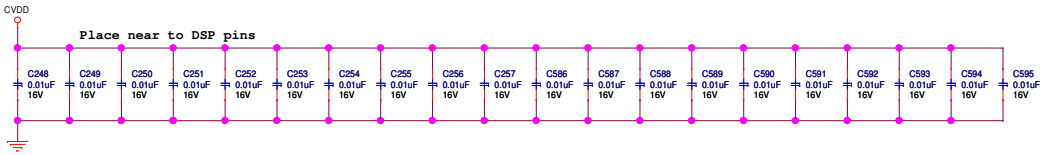
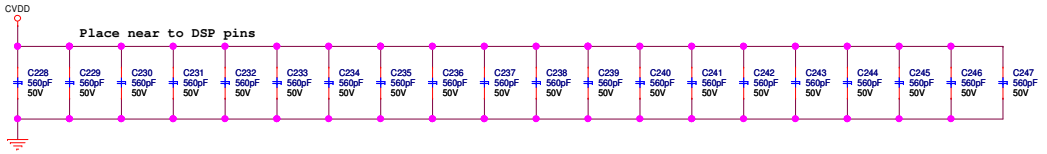
0.9V - 1.1V (Smart Reflex)



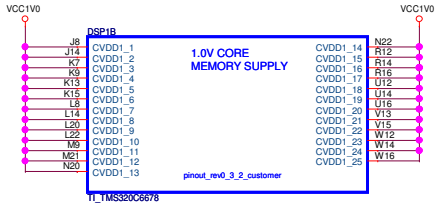


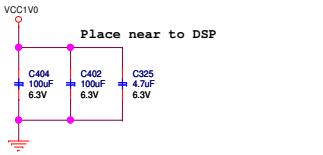


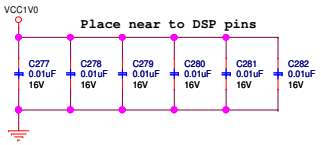


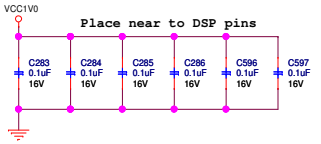


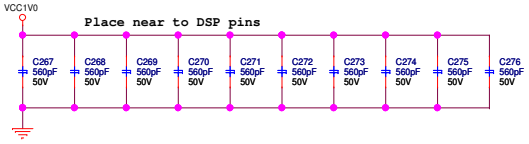
VCC1V0











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Title		
DSP_POWERB		
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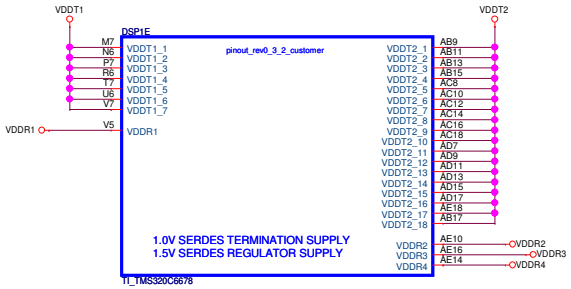
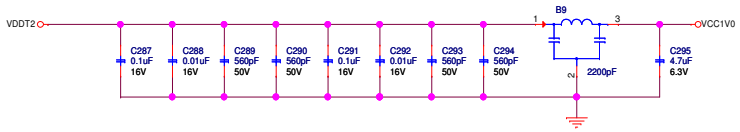
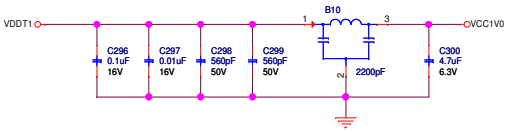
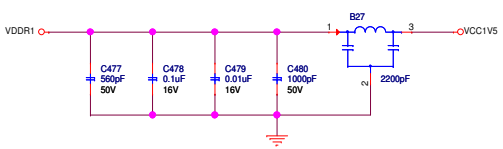
1.0V & 1.5V for Serdes

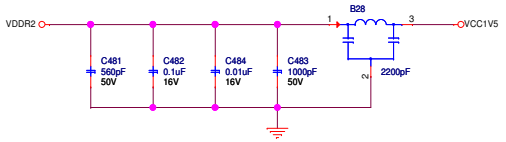


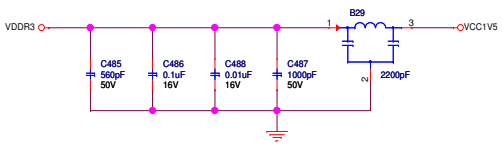
Place near to DSP pins

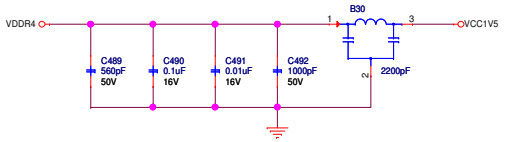












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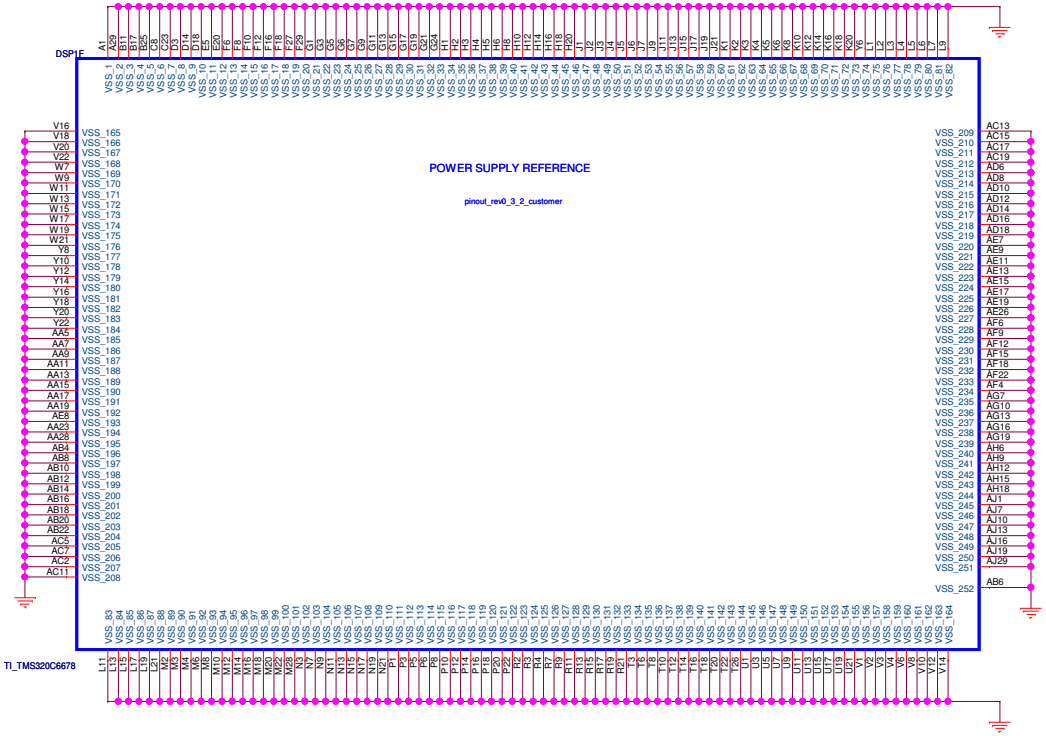
Title		
DSP_POWERC		
Size: C	Document Number: DSPM-8301E	Rev: A102-1
Date: Thursday, May 12, 2011	Sheet 20 of 40	



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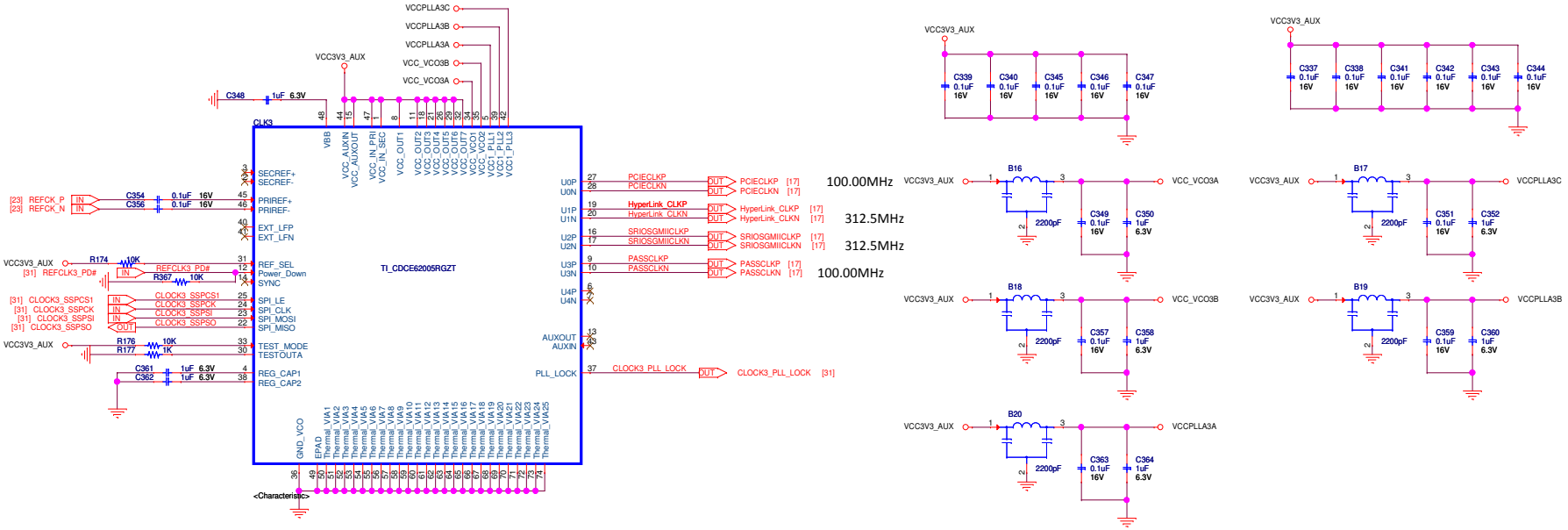
TEXAS INSTRUMENTS ADVANTECH

Title		
DSP_GND		
Size: C	Document Number: DSPM-8301E	Rev: A102-1
Date: Thursday, May 12, 2011	Sheet 21 of 40	

CLOCK GEN3



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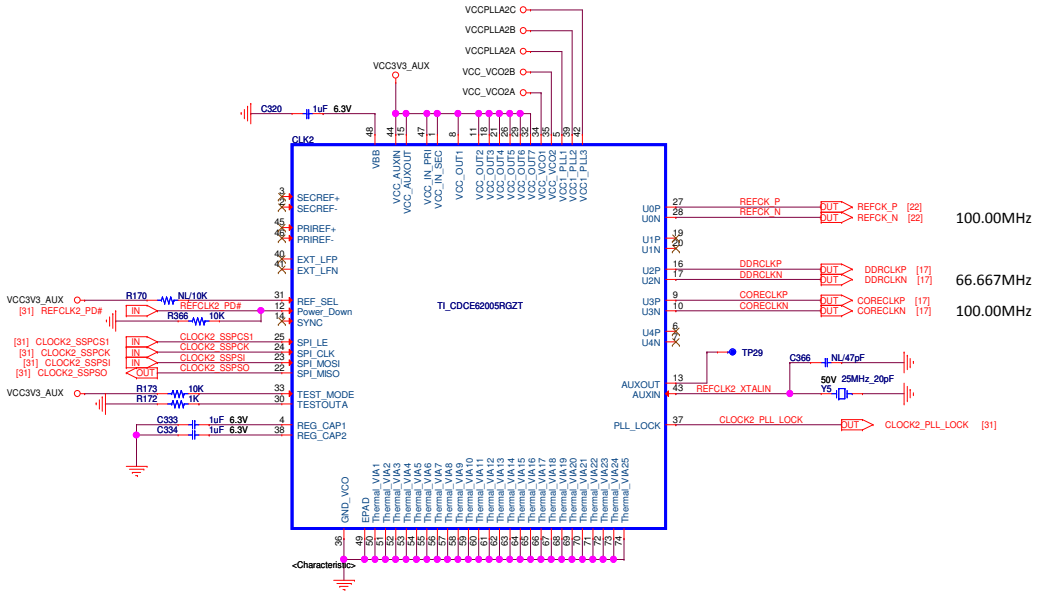
TEXAS INSTRUMENTS ADVANTECH

Title	DSP_CLOCK_GEN3	
Size: C	Document Number: DSPM-8301E	Rev: A102-1
Date: Thursday, May 12, 2011	Sheet 22 of 40	

CLOCK GEN2



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TEXAS INSTRUMENTS ADVANTECH

Title		
CLOCK GEN2		
Size: C	Document Number: DSPM-8301E	Rev: A102-1
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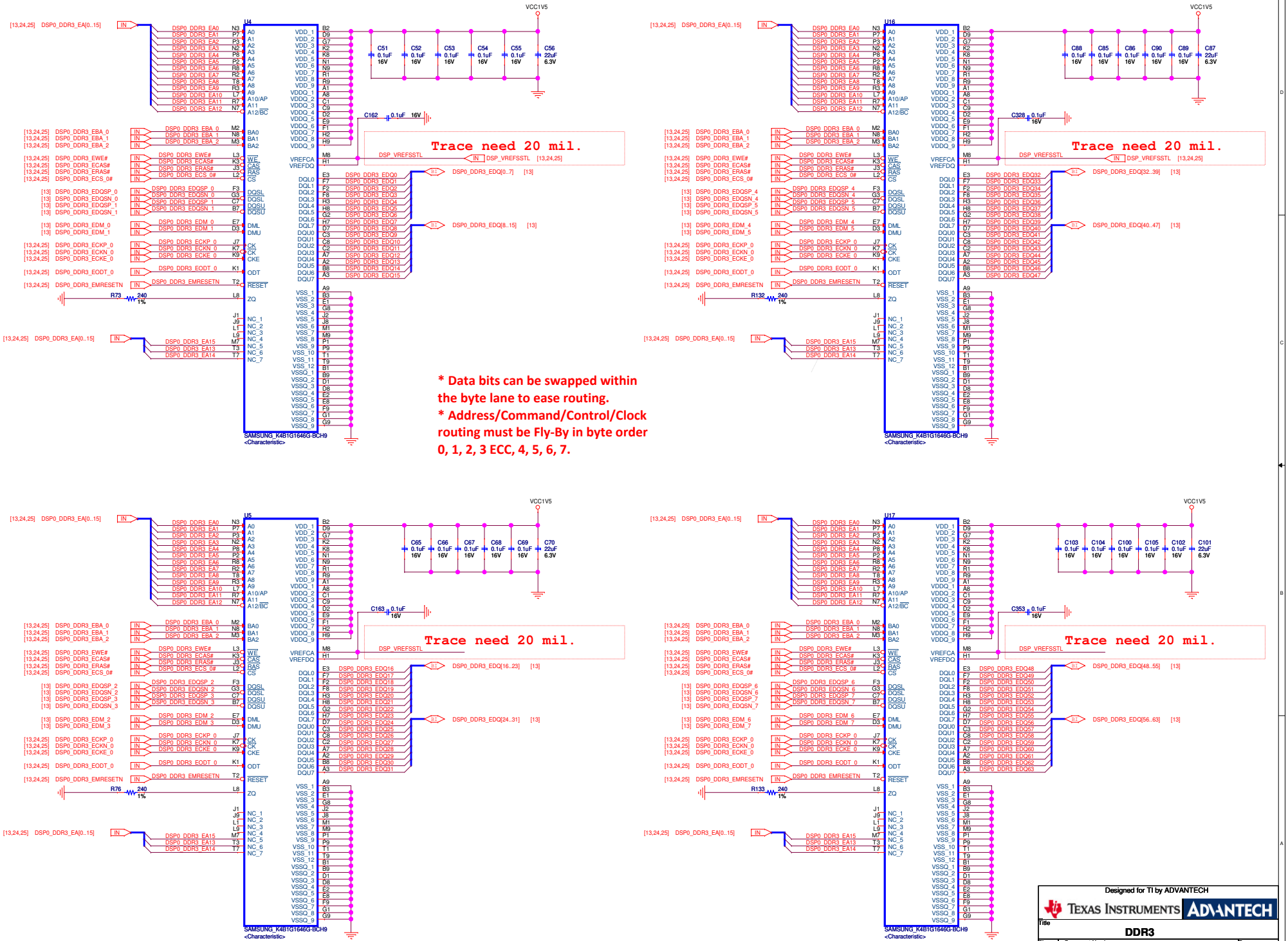
VCC1V5
U4
U16
U5
U17
SAMSUNG_K4B1G1646G-BCH9
<Characteristic>
Trace need 20 mil.
DSP_VREFSSTL
DSP0_DDR3_EA[0..15]
DSP0_DDR3_EDQ[0..7]
DSP0_DDR3_EDQ[8..15]
DSP0_DDR3_EDQ[32..39]
DSP0_DDR3_EDQ[40..47]
DSP0_DDR3_EDQ[16..23]
DSP0_DDR3_EDQ[24..31]
DSP0_DDR3_EDQ[48..55]
DSP0_DDR3_EDQ[56..63]
* Data bits can be swapped within the byte lane to ease routing.
* Address/Command/Control/Clock routing must be Fly-By in byte order 0, 1, 2, 3 ECC, 4, 5, 6, 7.
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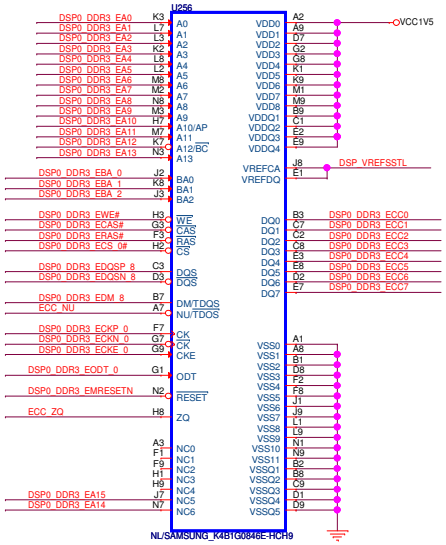
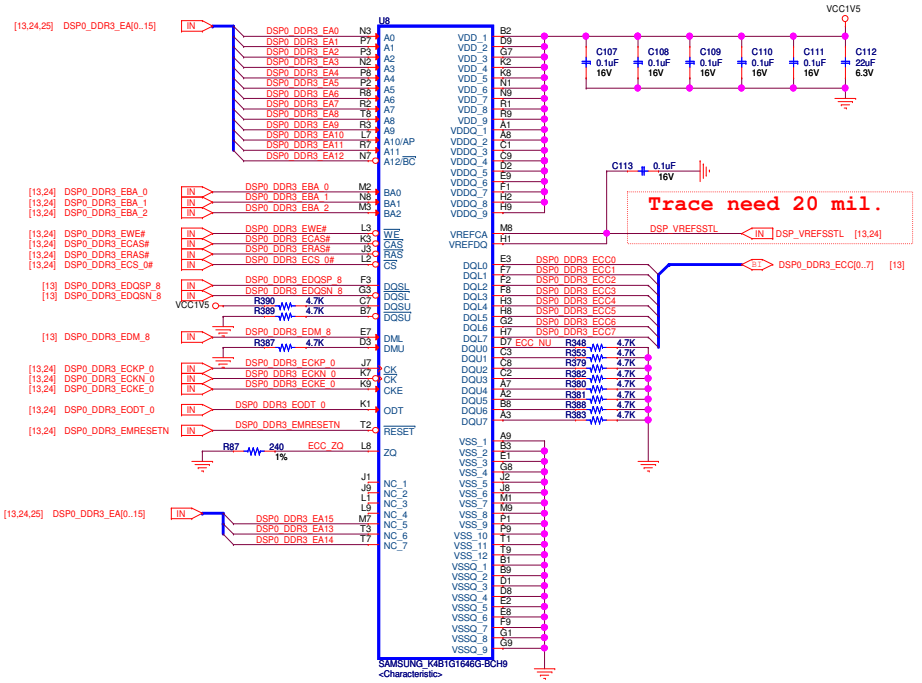
TEXAS INSTRUMENTS
ADVANTECH
Title
DDR3
Size C
Document Number DSPM-8301E
Rev A102-1
Date: Thursday, May 12, 2011
Sheet 24 of 40

CO-LAYOUT



U4, U5, U16, U17, U8 change SAMSUNG_K4B1G1646G



Sep.21.2010:

There are two combinations of DDR3 on ECC:

3.a. 512MB: (1Gb, X16) 5pcs

3.b. 1024MB: (2Gb, X16) 4pcs & (1Gb X8, ECC) 1pcs

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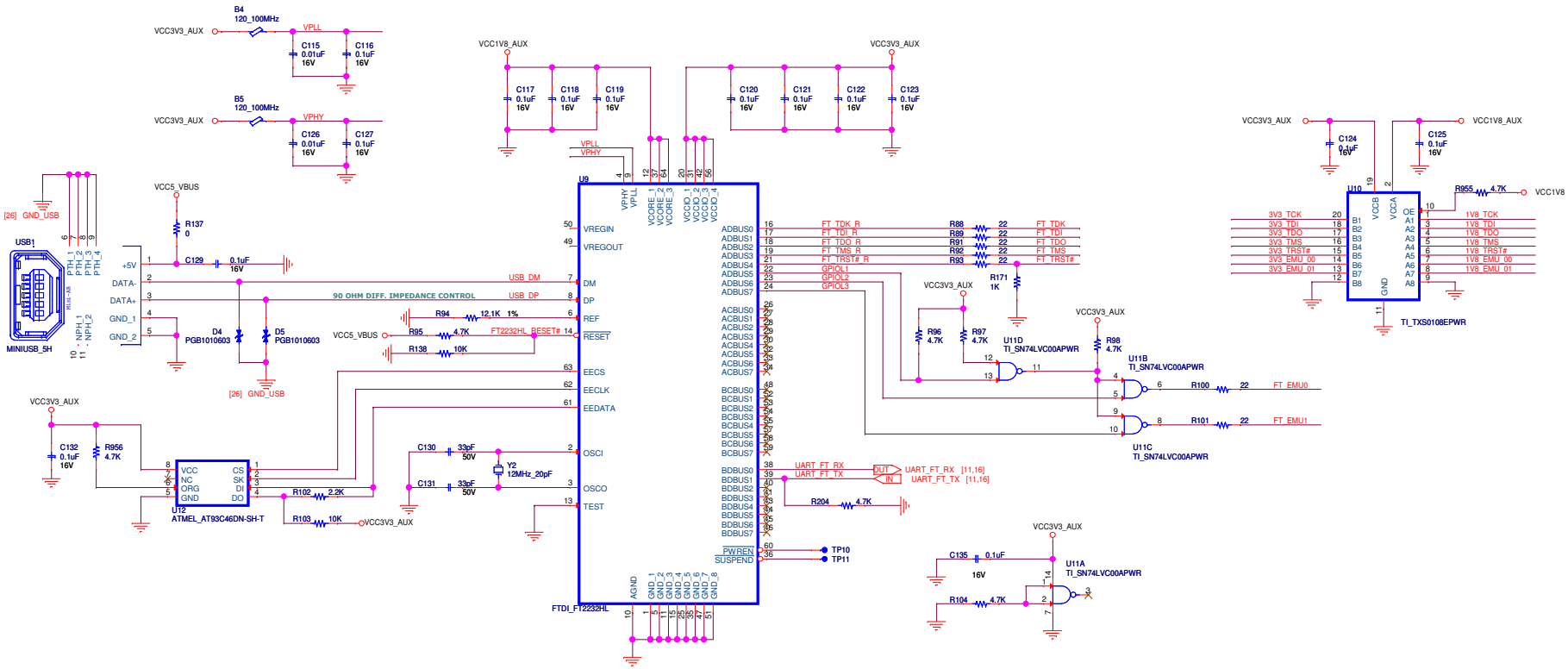
TEXAS INSTRUMENTS ADVANTECH

Title: DDR3_ECC		
Size: C	Document Number: DSPM-8301E	Rev: A102-1
Date: Thursday, May 12, 2011	Sheet 25 of 40	



FUNCTION TABLE

INPUT SEL	INPUT/OUTPUT An	FUNCTION
L	nB_1	$A_n = nB_1$
H	nB_2	$A_n = nB_2$

Switch for JTAG emulation
FT2232HL_RESET# = 0 --> AMC
FT2232HL_RESET# = 1 --> Mini USB

Switch for JTAG emulation
EXT_EMU_DET = 0 --> External / Mezzanine Emulator
EXT_EMU_DET = 1 --> On board emulation

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TEXAS INSTRUMENTS ADVANTECH

Title: **USB-JTAG**

Size	Document Number	Rev
C	DSPM-8301E	A102-1

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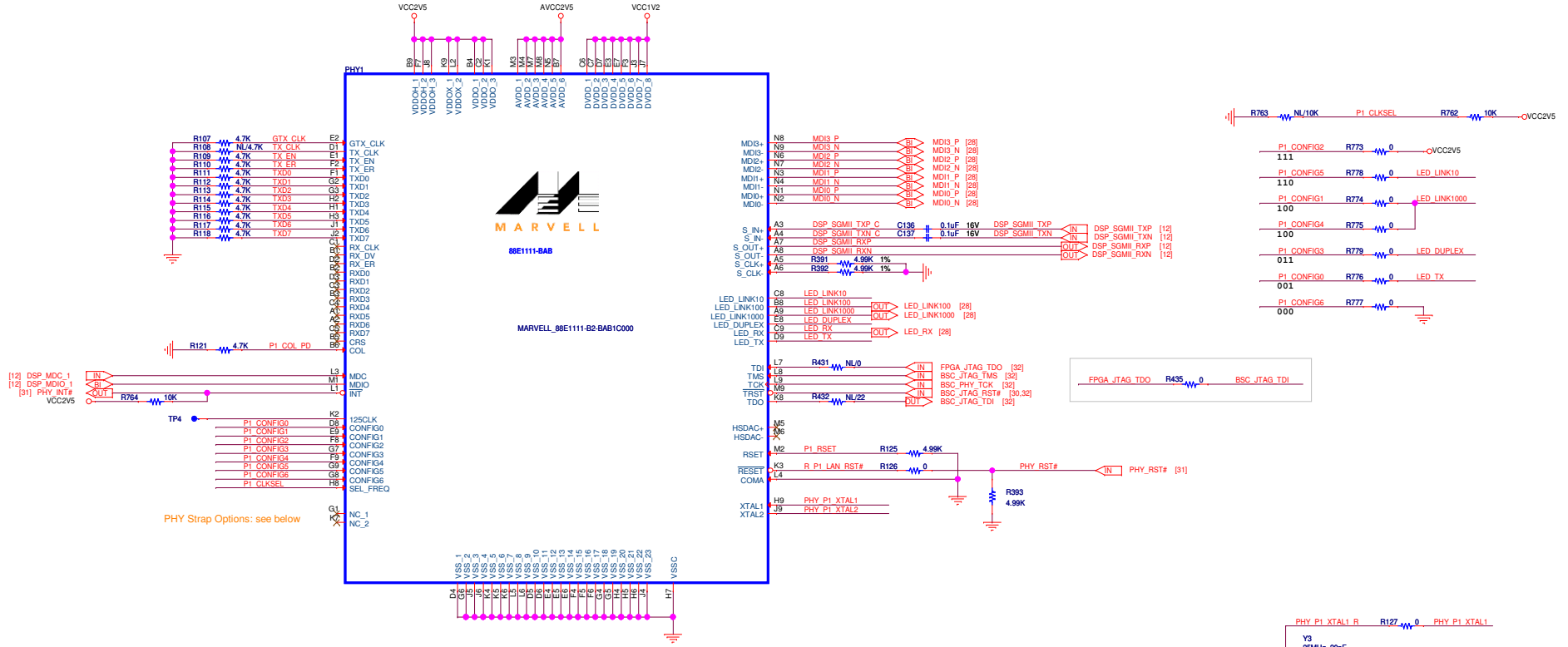

88E1111 Device Pin to Configuration Bit Mapping

Pin	Bit[2]	Bit[1]	Bit[0]
CONFIG0	PHYADR[2]	PHYADR[1]	PHYADR[0]
CONFIG1	ENA_PAUSE	PHYADR[4]	PHYADR[3]
CONFIG2	ANEG[3]	ANEG[2]	ANEG[1]
CONFIG3	ANEG[0]	ENA_XC	DIS_125
CONFIG4	HWCFG_MODE[2]	HWCFG_MODE[1]	HWCFG_MODE[0]
CONFIG5	DIS_FC	DIS_SLEEP	HWCFG_MODE[3]
CONFIG6	SEL_TWSI	INT_POL	75/50 OHM

Pin to Constant Mapping

Pin	Bit[2:0]
VDDO	111
LED_LINK10	110
LED_LINK100	101
LED_LINK1000	100
LED_DUPLEX	011
LED_RX	010
LED_TX	001
VSS	000

CONFIG Pin Connection

PHY Address = 0x01

Pin	LED Pin Connection	Hardware Configuration Bit Setting	PHY Configuration
CONFIG0	001	LED_TX	PHY Address bit[2:0] 001
CONFIG1	100	LED_LINK1000	Enable Pause ,PHY Address bit[4:3] = 00
CONFIG2	111	VDDO	Auto-Neg advertise all capabilities ,prefer Master
CONFIG3	011	LED_DUPLEX	Enable MDI crossover, disable 125CLK
CONFIG4	100	LED_LINK1000	SGMII without Clock with SGMII Auto-Neg to copper
CONFIG5	110	LED_LINK10	Disable fiber /copper Auto-detect, Disable sleep
CONFIG6	000	VSS	Select MDIO interface, INT signal active high, 50 ohm SERDES

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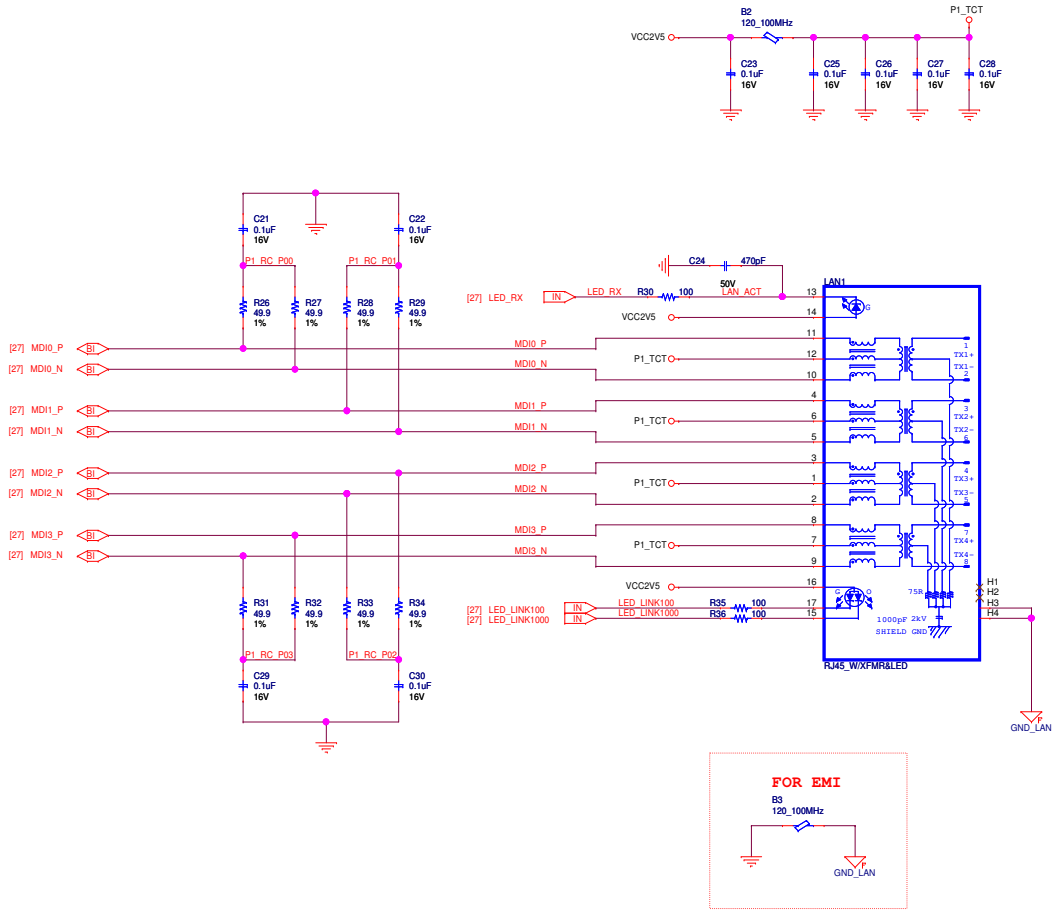
Texas Instruments ADVANTECH

Title: Gigabit Ethernet PHY

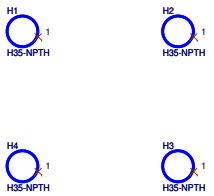
Size: C | Document Number: DSPM-8301E | Rev: A102-1

Date: Tuesday, May 31, 2011 | Sheet 27 of 40

RJ-45

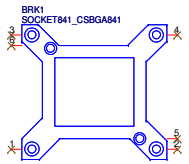


Heatsink Holes



AMC Hole

On board



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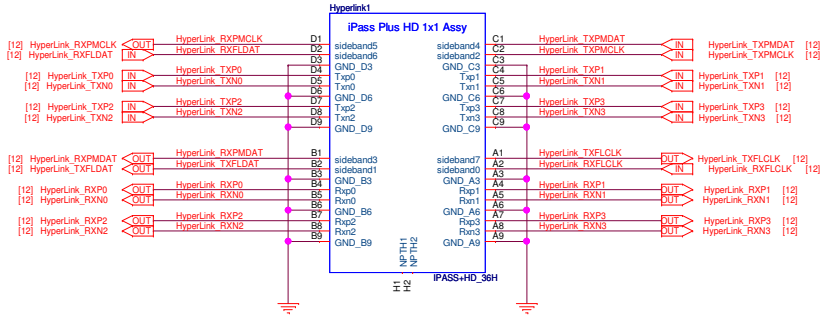
TEXAS INSTRUMENTS ADVANTECH

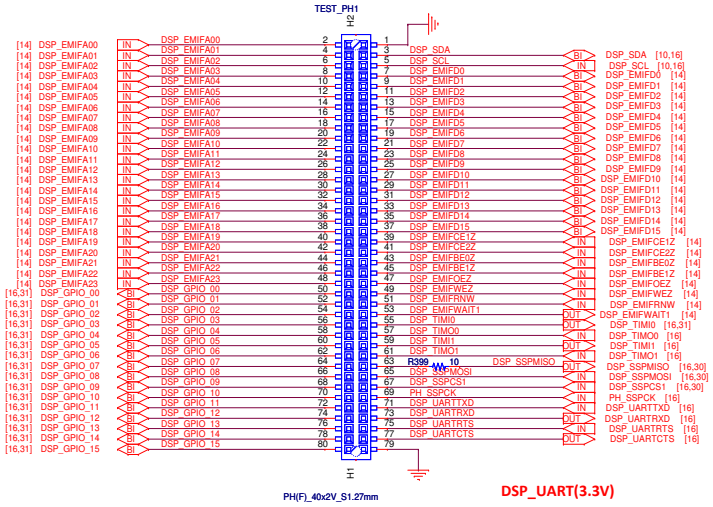
Title		
RJ45		
Size: C	Document Number: DSPM-8301E	Rev: A102-1
Date: Thursday, May 12, 2011	Sheet 28 of 40	

IPASS+HD for HyperLink Bus connection



Pin Header for debug

the interfaces on the 80-pin header are all 1.8V LVCMOS except for the UART which is 3.3V LVCMOS



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TEXAS INSTRUMENTS ADVANTECH

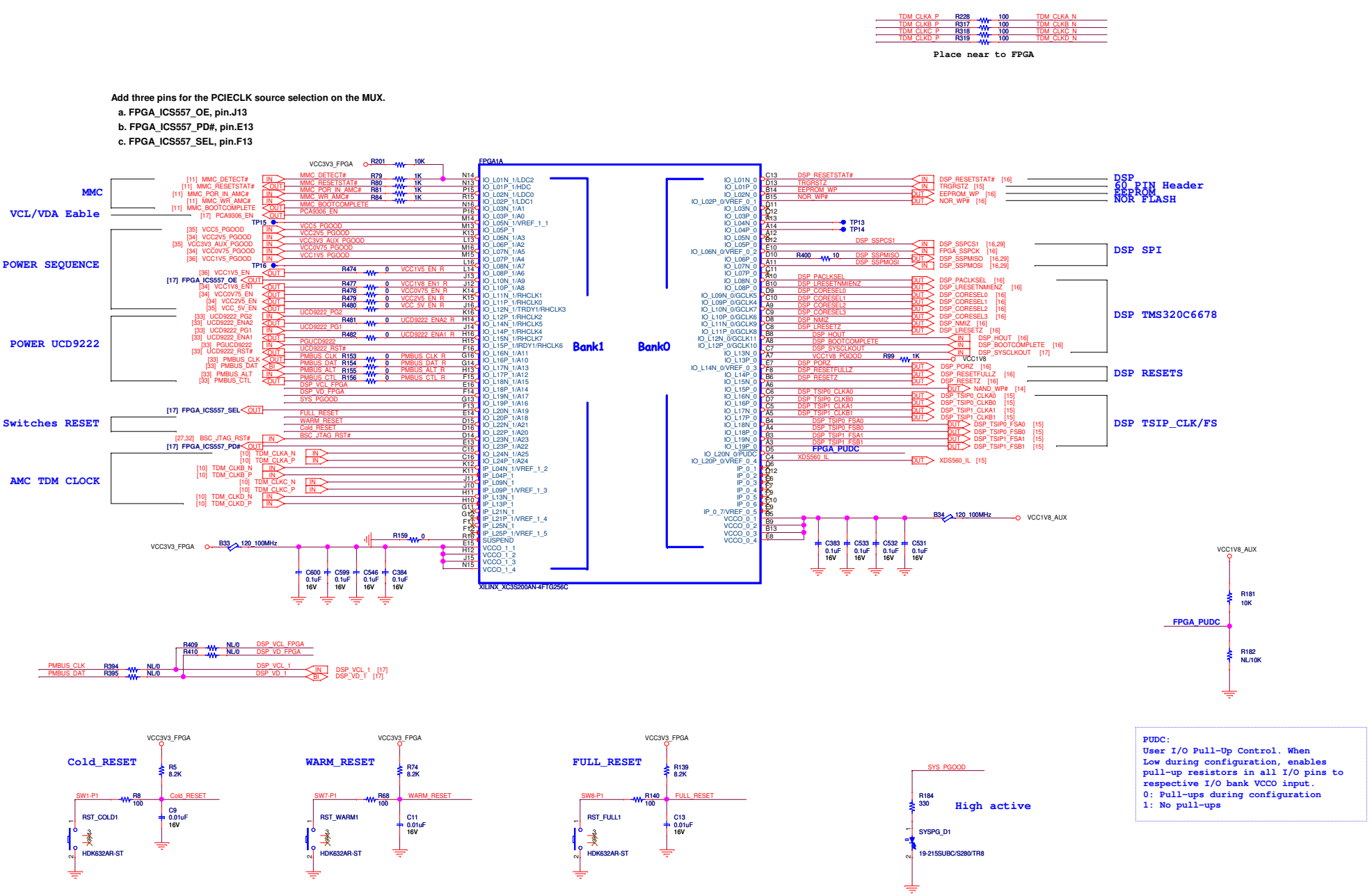
Title: Connectors for HyperLink & Debug		
Size: C	Document Number: DSPM-8301E	Rev: A102-1
Date: Thursday, May 12, 2011	Sheet 29 of 40	

Add three pins for the PCIECLK source selection on the MUX.

a. FPGA_ICS557_OE, pin.J13

b. FPGA_ICS557_PD#, pin.E13

c. FPGA_ICS557_SEL, pin.F13



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TEXAS INSTRUMENTS ADVANTECH

Title			
FPGA_XC3S200AN_A			
Size: C	Document Number: DSPM-8301E		Rev: A102-1
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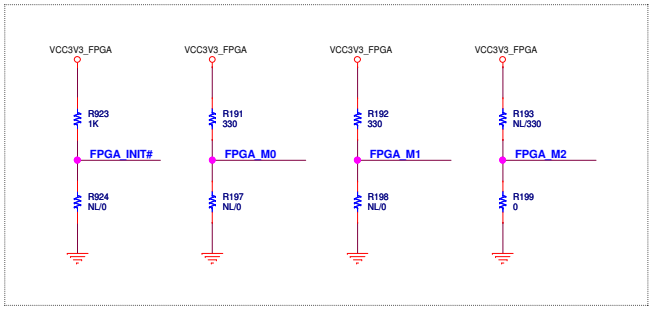
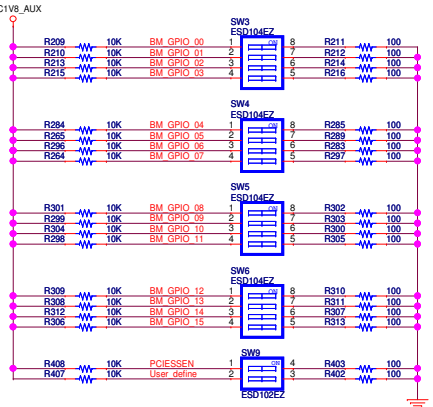
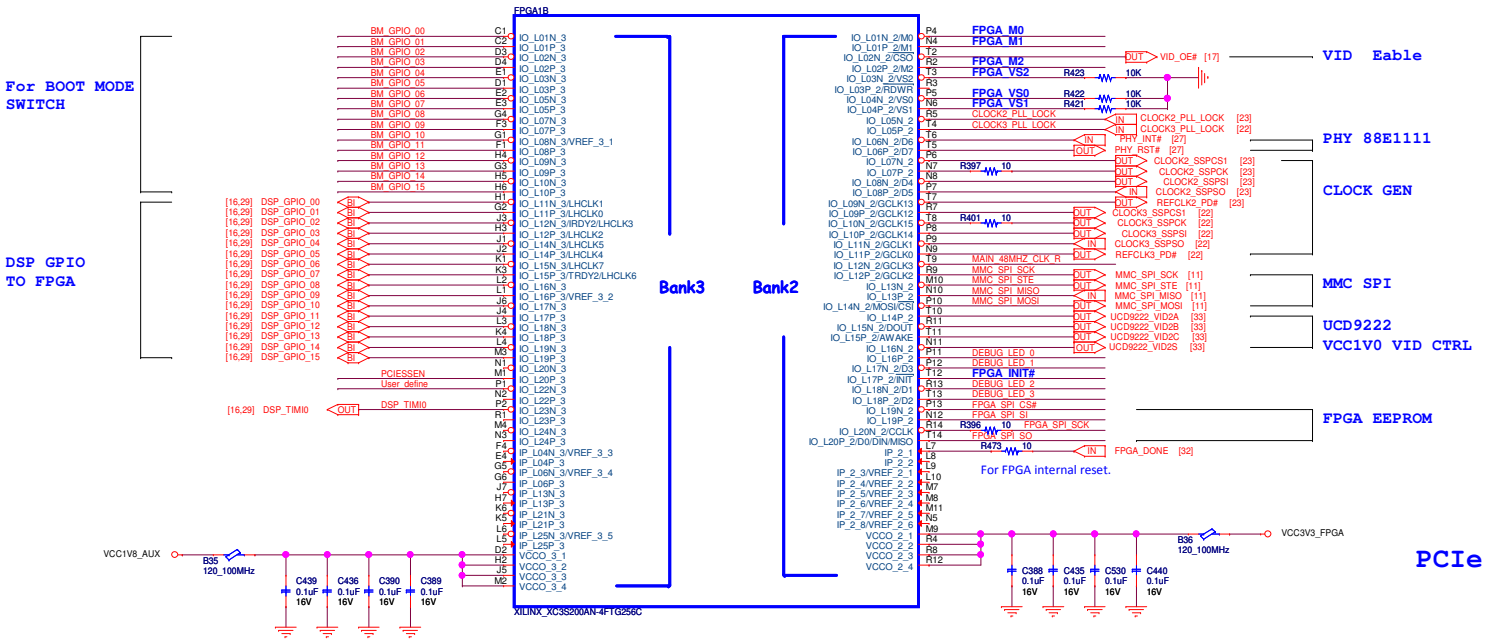
BOOT STRAP CONFIGURATION

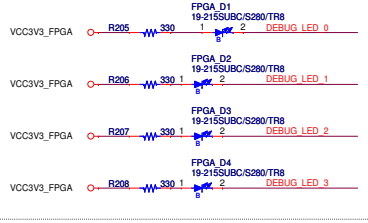
default value : TBD

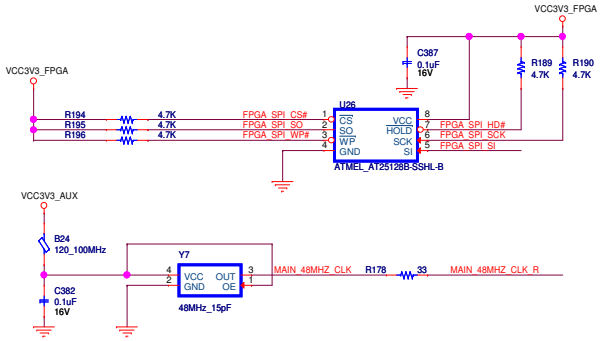






DEBUG_LED





Boot Configuration

DIP Switch	DSP	Boot Mode	Primary Function	
			Pull Up	Pull Down
BM_GPIO0	GPIO0	LENDIAN	Little Endian	Big Endian
BM_GPIO1	GPIO1	BOOTMODE00	Boot Device	
BM_GPIO2	GPIO2	BOOTMODE01	Boot Device	
BM_GPIO3	GPIO3	BOOTMODE02	Boot Device	
BM_GPIO4	GPIO4	BOOTMODE03	Device Cfg	
BM_GPIO5	GPIO5	BOOTMODE04	Device Cfg	
BM_GPIO6	GPIO6	BOOTMODE05	Device Cfg	
BM_GPIO7	GPIO7	BOOTMODE06	Device Cfg	
BM_GPIO8	GPIO8	BOOTMODE07	Device Cfg	
BM_GPIO9	GPIO9	BOOTMODE08	Device Cfg	
BM_GPIO10	GPIO10	BOOTMODE09	Device Cfg	
BM_GPIO11	GPIO11	BOOTMODE10	PLL Multiplier/I2C	
BM_GPIO12	GPIO12	BOOTMODE11	PLL Multiplier/I2C	
BM_GPIO13	GPIO13	BOOTMODE12	PLL Multiplier/I2C	
BM_GPIO14	GPIO14	PCIESSMODE0	Endpt/RootComplex	
BM_GPIO15	GPIO15	PCIESSMODE1	Endpt/RootComplex	

Boot Device

BM_GPIO 3 2 1	BOOT Device	NOTE
0 0 0	EMIF16	
0 0 1	sRIO	
0 1 0	SMGII	PA driven from core clk
0 1 1	SGMII	PA driver from PA clk
1 0 0	PCIe	
1 0 1	I2C	
1 1 0	SPI	
1 1 1	HyperLink	

Device Configuration

BM_GPIO [10:4]	Device Configuration Field	The device configuration fields GPIO[10:4] are used to configure the boot peripheral and, therefore, the bit definitions depend on the boot mode.

PLL Settings

BM_GPIO 13 12 11	INPUT CLK (MHz)	CorePac System PLL Configuration
0 0 0	50.00	
0 0 1	66.67	
0 1 0	80.00	PA driven from core clk
0 1 1	100.00	PA driver from PA clk
1 0 0	156.25	
1 0 1	250.00	
1 1 0	312.50	
1 1 1	122.88	

PCIe Mode selection(PCIESSMODE[1:0])

BM_GPIO[15:14] INPUT	Description
00b	PCIe in End-point mode
01b	PCIe in Legacy End-point mode(no support for MSI)
10b	PCIe in Legacy Root complex mode

PCIESSEN

Input	Description
0	Initial state of the power domain and the clock domain for PCIE subsystem is disabled
1	Initial state of the power domain and the clock domain for PCIE subsystem is enabled

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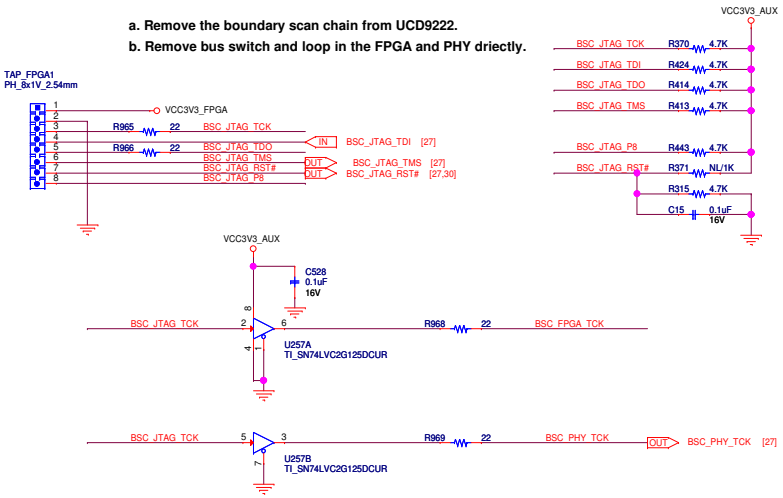
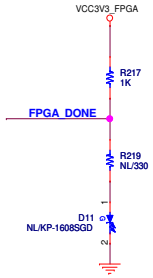
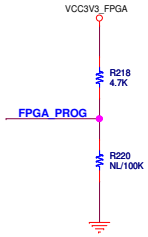
TEXAS INSTRUMENTS ADVANTECH

Title	FPGA_XC3S200AN_B	
Size C	Document Number DSPM-8301E	Rev A102-1
Date: Thursday, May 12, 2011	Sheet 31 of 40	

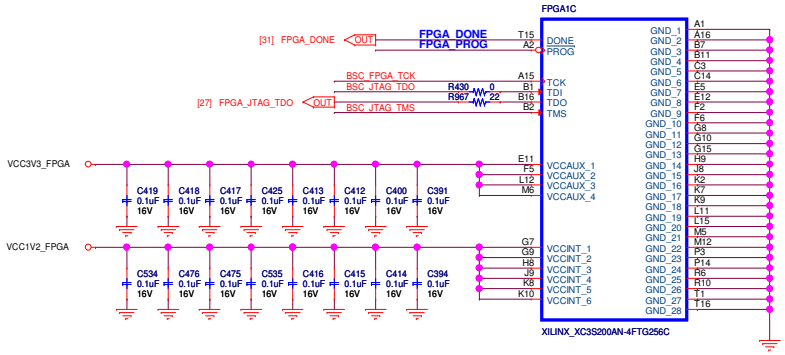
a. Remove the boundary scan chain from UCD9222.
b. Remove bus switch and loop in the FPGA and PHY driectly.

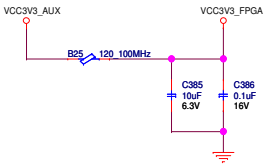


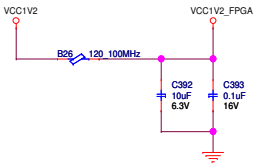




During Configuration :
Must be High to allow
configuration to start.







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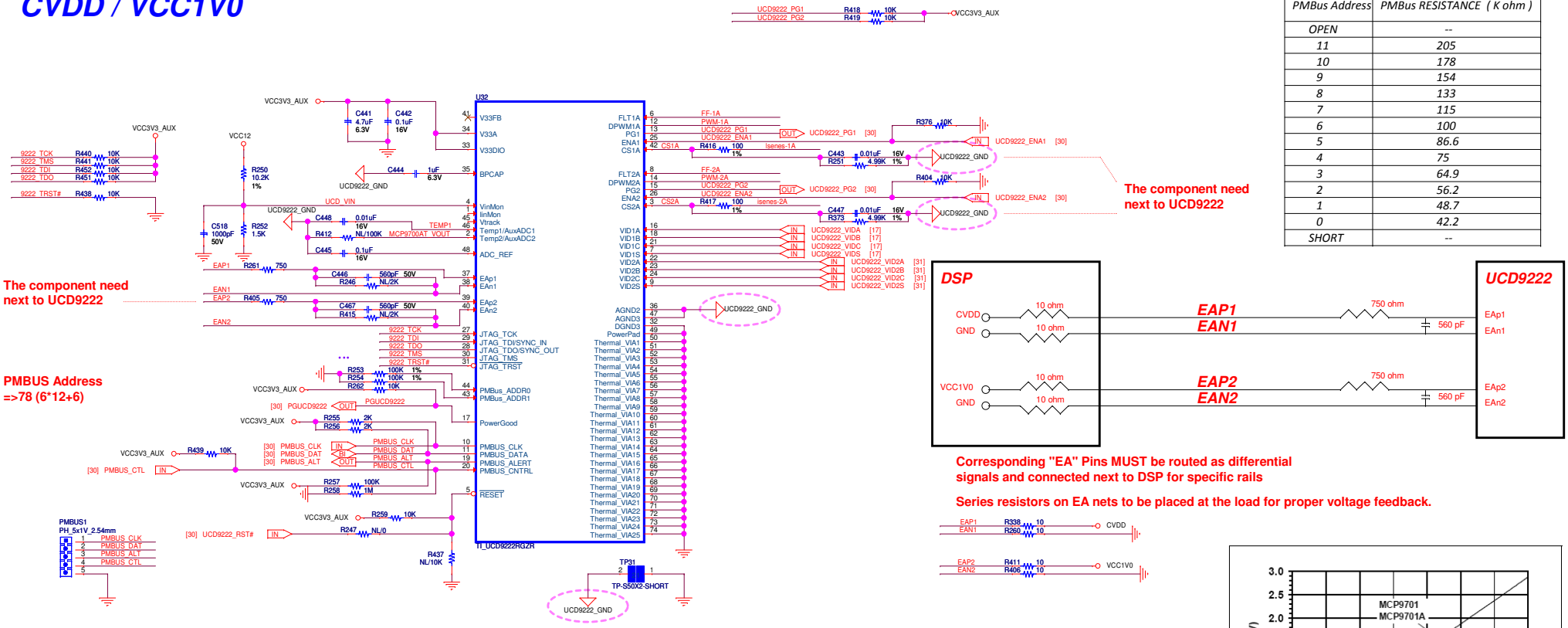
Title	FPGA_XC3S200AN_C	
Size C	Document Number DSPM-8301E	Rev A102-1
Date: Thursday, May 12, 2011	Sheet 32 of 40	

CVDD / VCC1V0

PMBus Address Bins

PMBus Address	PMBus RESISTANCE (K ohm)
OPEN	--
11	205
10	178
9	154
8	133
7	115
6	100
5	86.6
4	75
3	64.9
2	56.2
1	48.7
0	42.2
SHORT	--



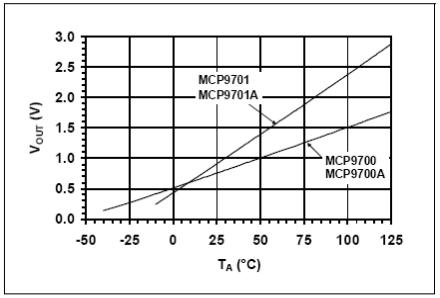


FIGURE 2-16: *Output Voltage vs. Ambient Temperature.*

+++output capacitor Calculation for VCC1V0+++

$$V_{PPQ} \approx \frac{\Delta I}{8 \times C \times f_s}$$

(VPPQ=10mV)

C= 5 / (10m * 8 * 750k)
C=83.3uF

Temperature Coefficient: 10 mV/℃
Output Voltage: TA = 0 ℃ => Vout= 500mV

1.0V@ 5A

DSP Vcore @8A

+++output capacitor Calculation for VCC1V0+++

$$V_{PPQ} \approx \frac{\Delta I}{8 \times C \times f_s}$$

(VPPQ=10mV)

C= 8 / (10m * 8 * 750k)
C= 133.3uF

+++Inductor Calculation for VCC1V0+++

$$L = \frac{V_{IN} - V_{OUT}}{\Delta I} \frac{D}{f_s}$$

L= (12 - 1) / 5 * (1/12) / 750K
L= (11 / 5) * (0.083 / 750K)
L= 0.243 uH

+++Inductor Calculation for CVDD+++

$$L = \frac{V_{IN} - V_{OUT}}{\Delta I} \frac{D}{f_s}$$

L= (12 - 1) / (8) * (1/12) / 750K
L= (11 / 8) * (0.083 / 750K)
L= 0.152 uH

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Title: Power ucd9222

Size	Document Number	Rev
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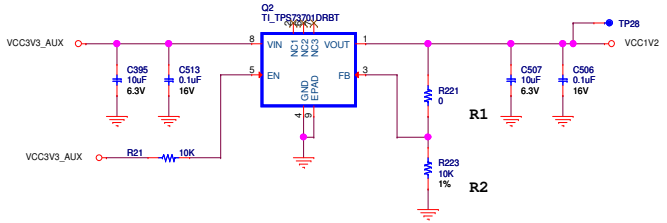
VCC1V2

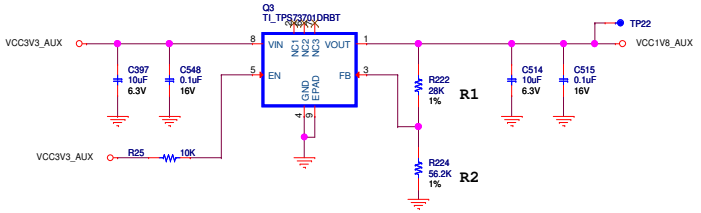
1.2V @0.38A



Vout=(R1+R2)/R2*1.204
1.204V = (0+10k)/10k*1.204

VCC1V8_AUX

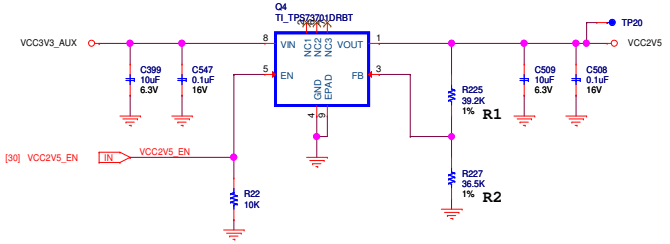
1.8V_AUX @0.3A



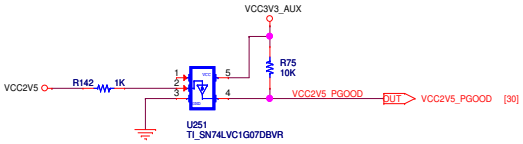
Vout=(R1+R2)/R2*1.204
1.805V =(28k+56.2k)/56.2k*1.205

VCC2V5

2.5V @0.21A

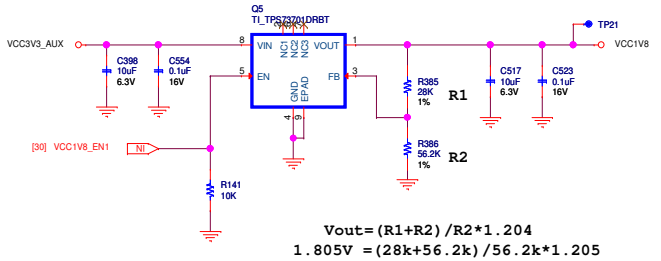


Vout=(R1+R2)/R2*1.204
2.50V =(39.2k+36.5k)/36.5k*1.204



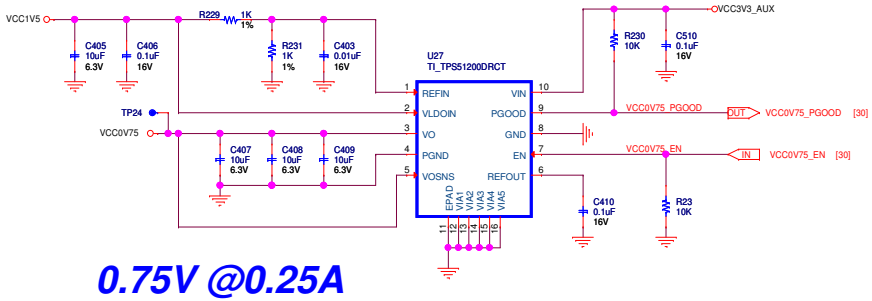
VCC1V8

1.8V@0.5A



Vout=(R1+R2)/R2*1.204
1.805V =(28k+56.2k)/56.2k*1.205

VCC0V75



0.75V @0.25A

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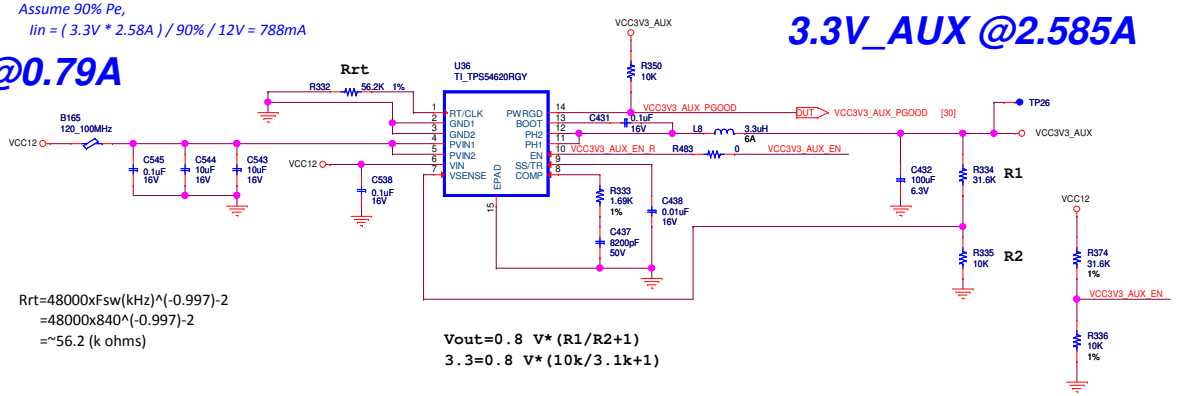
VCC3V3_AUX

Assume 90% Pe,
*Iin = (3.3V * 2.58A) / 90% / 12V = 788mA*

12V@0.79A

3.3V_AUX @2.585A



Rrt=48000xFsw(kHz)^(-0.997)-2
=48000x840^(-0.997)-2
=~56.2 (k ohms)

Vout=0.8 V*(R1/R2+1)
3.3=0.8 V*(10k/3.1k+1)

(Over all tolerance is 5% ,DC tolerance is 2.5%)
+++output capacitor Calculation+++
Cout>(2*delta(Iout))/(Fsw*delta(Vout))
Cout>(2*3/(840kHz*0.0825)
Cout>~87uF

Reference Capacitor=100uF

(KIND=0.3)
+++Inductor Calculation+++
L = (Vin - Vout)/(Iout * Kind) * (Vout/(Vin * Fsw)
L = ((12 - 3.3)/(3A * 0.3) * (3.3 / (12 * 840kHz))
L = 9.67 * 0.33u
L = ~3.2 uH

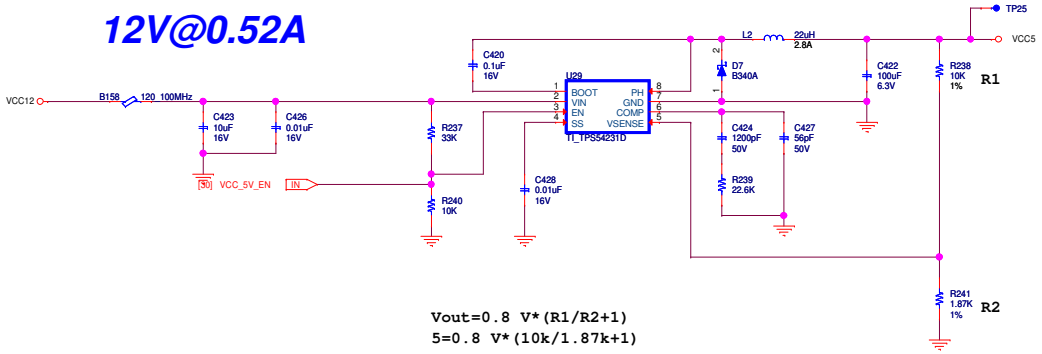
Reference Inductor 3.3uH

VCC5

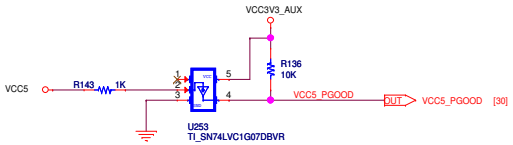
Assume 80% Pe,
*Iin = (5V * 1A) / 80% / 12V = 520mA*

12V@0.52A

5V @1A



Vout=0.8 V*(R1/R2+1)
5=0.8 V*(10k/1.87k+1)



+++output capacitor Calculation+++

$$C_{O\_min} = 1/(2 \times \pi \times R_O \times F_{CO\_max})$$

Cout=1/(2 * 3.14 * 5 * 25K)
Cout=1.3 uf

Reference Capacitor=100uF

+++Inductor Calculation+++ (KIND=0.3)
L = ((Vin(max) - Vout)/Iout * Kind)) * (Vout/(Vin(max) * Fsw))
L = ((12.6 - 5)/1 * Kind) * (5 / (12.7 * 570K))
L = ((7.6/ 0.3) * (5 / (7239K))
L = (25.3) * (0.69M)
L = 17.5uH

Reference Inductor 22uH

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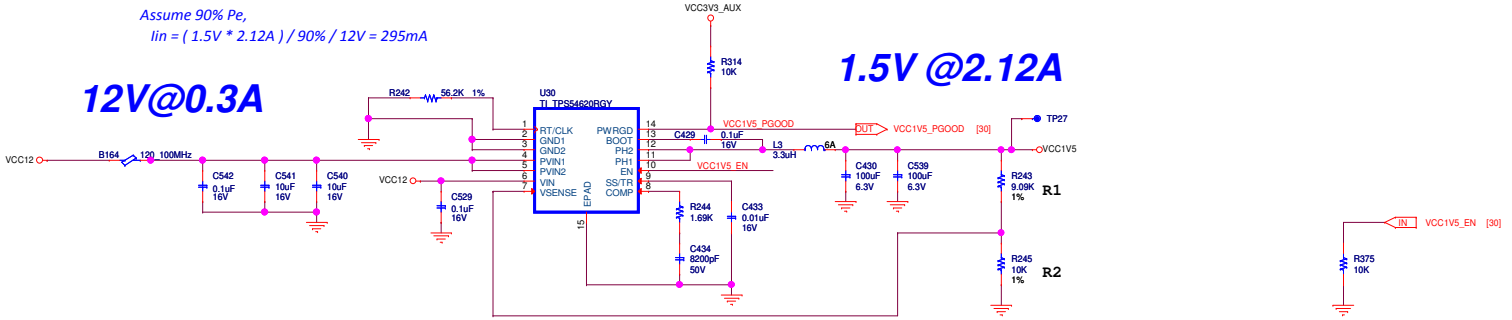
VCC1V5



Vout=0.8 V*(R1/R2+1)

1.52=0.8 V*(9.09k/10k+1)

(Over all tolerance is 5% ,DC tolerance is 2.5%) (KIND=0.3)

+++output capacitor Calculation+++
Cout=(2*delta(Iout))/(Fsw*delta(Vout))
Cout=(2*2.5A)/(840kHz*0.0375)
Cout=~159uF

Reference Capacitor=200uF

+++Inductor Calculation+++
L = (Vin - Vout)/(Iout * Kind) * Vout/(Vin * Fsw)
L = (12 - 1.5)/(2.5A * 0.3) * 1.5 / (12 * 840kHz)
L = ~2.08uH

Reference Inductor 3.3uH

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