

FAILURE ANALYSIS REPORT

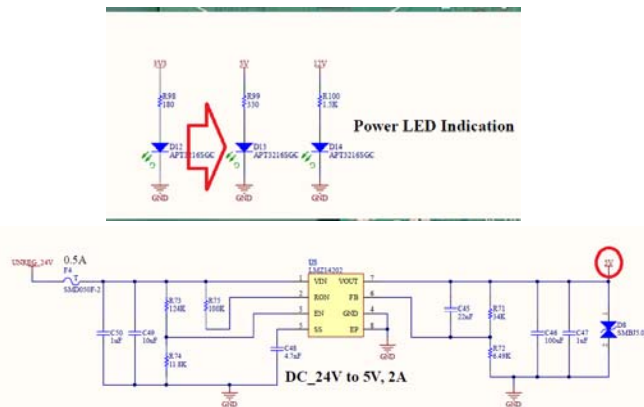
Part Number: LMZ14202TZ-ADJ/NOPB
WO#: 242261

Date: May 8, 2023
FA Engineer: Roderick Soriano

Work Order Details

WO Number	242261	PO/Reference Number	RFQ#52440
Customer	WAT INT'L(HK) CO.,LTD	Quantity Received	3
Part Number	LMZ14202TZ-ADJ/NOPB	Quantity Inspected	3
Manufacturer	Texas Instruments	Package Type	TO-PMOD-7
Product Description	DC DC CONVERTER 0.8-6V		
Datasheet Reference	https://www.ti.com/lit/ds/symlink/lmz14202.pdf?ts=1682347497337&ref_url=https%253A%252F%252Fwww.google.com%252F		

3 pieces of Texas Instruments LMZ14202TZ-ADJ/NOPB were received for Failure Analysis. Customer provided 1 piece good sample, 1 piece unused sample and 1 piece fail sample which reported to that the fail sample failed with 5Vdc Missing.



U5 Pin	New U5	Bad U5(1)	Bad U5(2)	Bad U5(3)	Bad U5(4)
1 VIN	7 MΩ	1.1 MΩ	1.1MΩ	0.9 MΩ	1.1 M
2 Ron	13 MΩ	13 MΩ	13 MΩ	13.1MΩ	13.3 M
3 EN	14 MΩ	2 MΩ	8.5 KΩ	2 Ω	13.65 M
4 GND					
5 SS	10 MΩ	2.8 KΩ	8.5 KΩ	7.2 Ω	2.8Ω
6 FB	16 MΩ	2.8 KΩ	15.4 MΩ	399 KΩ	390KΩ
7 VOT	6 MΩ	5.57 MΩ	5.64m	1.3Ω	∞

Address:
White Horse Laboratories Ltd

Phone Number
86-755-8374-1887

URL:
<http://whitehorcelabs.com>

4A Technology Building H Gang Zhi Long Science Park Heping East Road Longhua New District, Shenzhen

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FM3057.4

Summary

External visual inspection on good, unused and fail samples upon receipt showed no gross external damaged which can be correlated to customer failure mode. The good, unused and fail samples passed chemical solution and scrape tests for remarking and resurfacing, indicating that the samples are not remarked. The good, unused and fail samples dimensions D, E and A were measured and are within manufacturer specification. The devices have the same exterior configuration as shown on the Package Outline Drawing (POD).

Electrical verification on good sample and unused sample showed passed result while, the fail sample failed with high output voltage when there is no load and low output voltage when there is 2A current load.

Curve Trace verification on fail sample showed resistive current-voltage curve while, the good sample and unused samples showed normal current-voltage curve across all tested pins with respect to ground.

Scanning Acoustic Microscopy (SAM) analysis on good, unused and fail sample showed no package delamination or voids.

X-ray analysis on good, unused and fail samples revealed consistent internal structure with normal bump connection with no visible internal anomalies.

Decapsulation on good, unused and fail samples reveals consistent die topography with the same National Semiconductor logo, LM3102A2 and other die markings, verifying that parts were manufactured by Texas Instruments but not traceable to requested part number. National Semiconductor was acquired by Texas Instruments. Further inspection on the top surface of fail sample showed scratches on die surface.

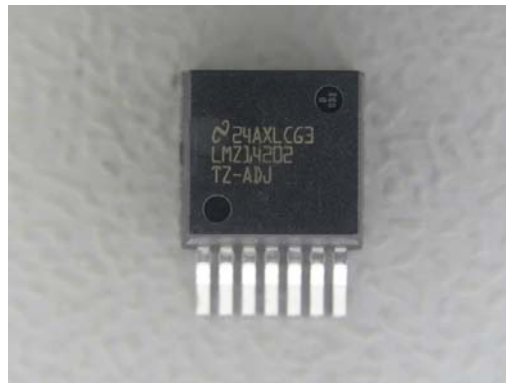
Summary

Based on the analysis result, the fail sample failed resistive at pin 5 and pin 6 with respect to ground due to scratches on die surface which probably creates a metal compression and crack propagation inside the die circuitry. The metal compression on die metal lines and propagation of crack inside the die will create a marginal connection between metal lines and gate oxide layer which may result leakage/resistive electrical failure. The scratches in the die surface is a physical damaged which probably induced when that die was still exposed at manufacturer processes from die preparation to die attach process.

External Visual Inspection (EVI)

External visual inspection on good, unused and fail samples upon receipt showed no gross external damaged which can be correlated to customer failure mode.

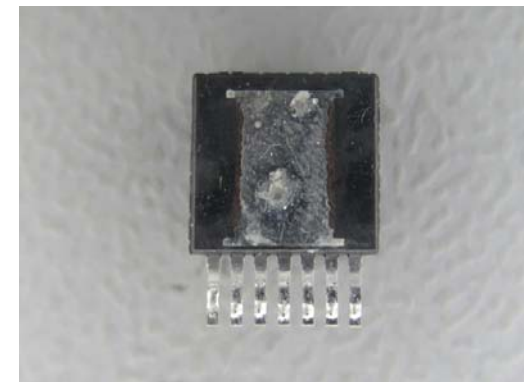
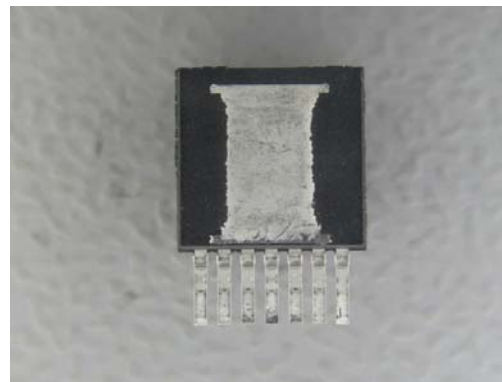
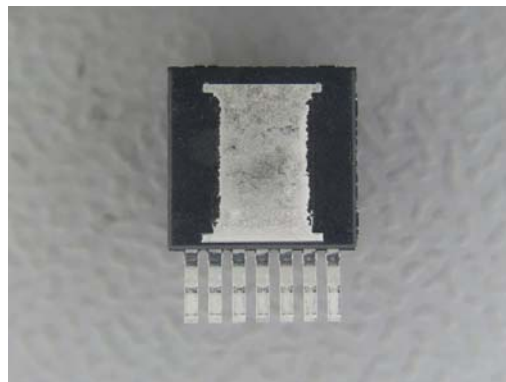
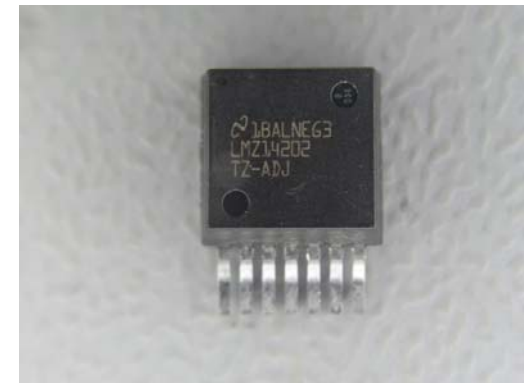
Good Sample



Unused Sample



Fail Sample



External Visual Inspection (EVI)

The good, unused and fail samples passed chemical solution and scrape tests for remarking and resurfacing, indicating that the samples are not remarked.

Good Sample

Unused Sample

Fail Sample

Chemical Resurfacing Test



After: PASS



After: PASS



After: PASS

Mechanical Resurfacing Test



After: PASS



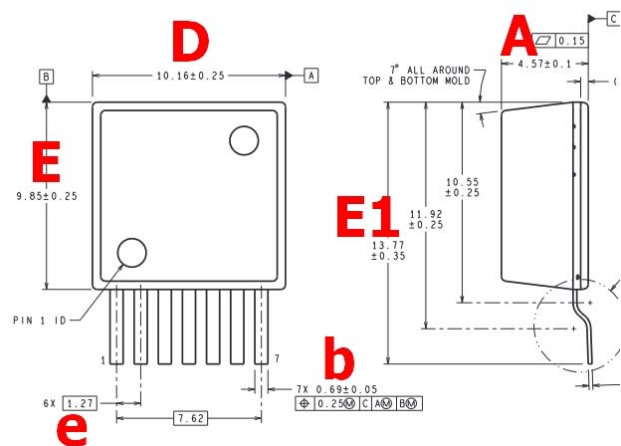
After: PASS



After: PASS

External Visual Inspection (EVI)

The good, unused and fail samples dimensions D, E and A were measured and are within manufacturer specification. The devices have the same exterior configuration as shown on the Package Outline Drawing (POD).



Good Sample



D = 10.39mm (PASS)

Unused Sample



D = 10.37mm (PASS)

Fail Sample



D = 10.36mm (PASS)



E = 9.82mm (PASS)



E = 9.95mm (PASS)



E = 9.79mm (PASS)



A = 4.59mm (PASS)



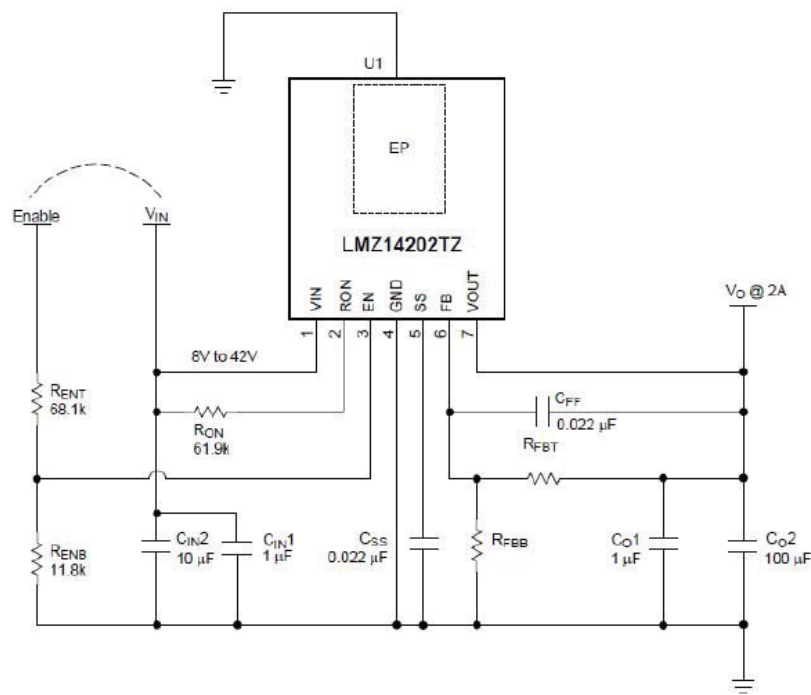
A = 4.58mm (PASS)



A = 4.57mm (PASS)

Electrical verification was performed on good, unused and fail samples to test the output voltage.

Electrical verification on good sample and unused sample showed passed result while, the fail sample failed with high output voltage when there is no load and low output voltage when there is 2A current load.



Description of Testing Procedure:

Set $V_{in}=8V$, $R_{FBT}=5.62K$, $R_{FBB}=1.07K$, connect to 2A current load to measure the output voltage.

The V_{out} should be within 4.845V to 5.095V.

Test Result Summary

Test Sample	TEST RESULT
Good Sample	Normal output voltage
Unused Sample	Normal output voltage
Fail Sample	Abnormal output voltage

Test Results

Good Sample



No load

Test result: Normal output voltage

Unused Sample



No load

Test result: Normal output voltage

Fail Sample



No load

Test result: High output voltage



2A current load

Test result: Normal output voltage



2A current load

Test result: Normal output voltage



2A current load

Test result: Low output voltage

Curve Trace Verification

Curve Trace verification was performed on good, unused and fail samples to determine the current-voltage characteristics of the samples.

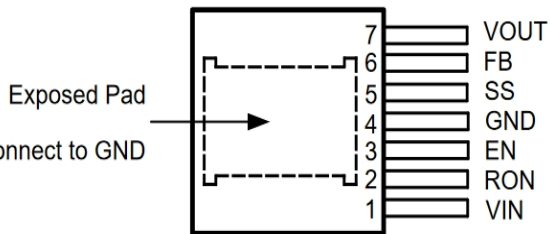
Verification on fail sample showed resistive current-voltage curve while, the good sample and unused samples showed normal current-voltage curve across all tested pins with respect to ground.

Curve Trace Verification Test Result Summary

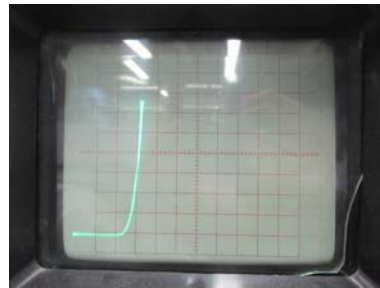
Tested Pins	Good Sample	Unused Sample	Fail Sample
Pin 1 (VIN)	CAPACITIVE	CAPACITIVE	CAPACITIVE
Pin 2 (RON)	DIODE	DIODE	DIODE
Pin 3 (EN)	DIODE	DIODE	DIODE
Pin 5 (SS)	DIODE	DIODE	RESISTIVE
Pin 6 (FB)	DIODE	DIODE	RESISTIVE
Pin 7 (VOUT)	DIODE	DIODE	DIODE

Pin map

NDW Package
7-Pin TO-PMOD
Top View

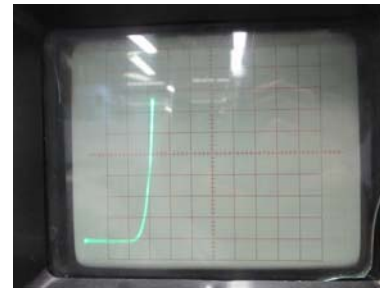


Good Sample



Pin 6 (FB)
vs.
Pin 4 (GND)

Unused Sample



Pin 6 (FB)
vs.
Pin 4 (GND)

Fail Sample



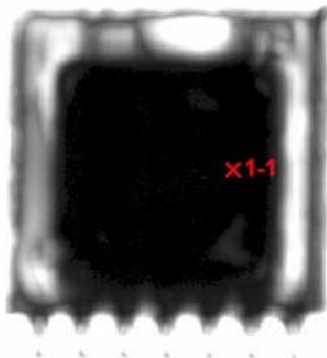
Pin 6 (FB)
vs.
Pin 4 (GND)

Scanning Acoustic Microscopy (SAM)

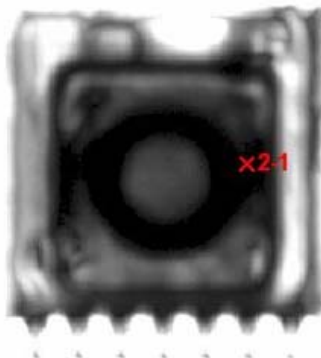
Scanning Acoustic Microscopy (SAM) was performed on good, unused and fail sample to verify delamination, voids and crack inside the package.

TSAM Analysis on good, unused and fail samples showed no anomaly on die area. The dark area in the samples are the copper coil which is located above the die surface.

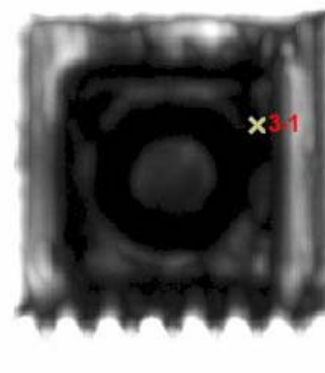
Good Sample



Unused Sample



Fail Sample



Scanning Acoustic Microscopy (SAM)

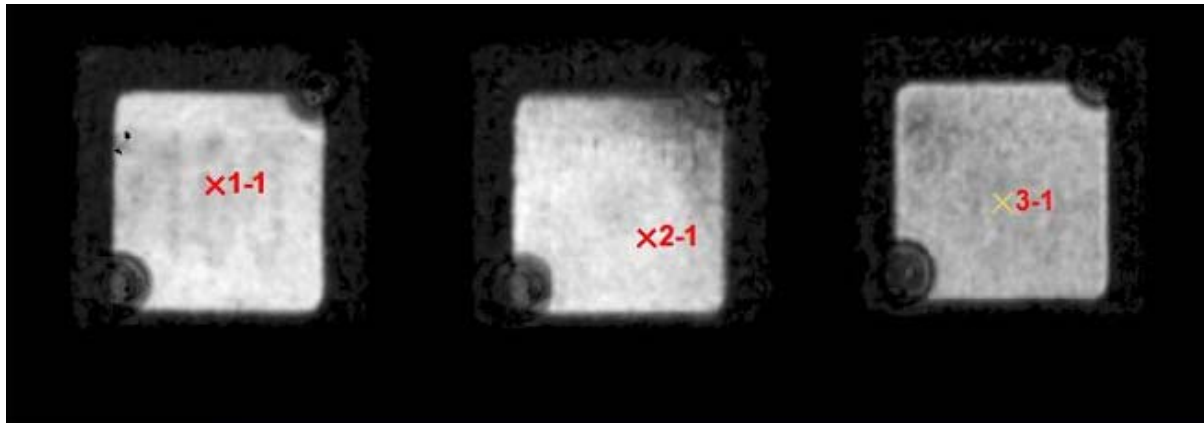
Scanning Acoustic Microscopy (SAM) was performed on good, unused and fail sample to verify delamination, voids and crack inside the package.

CSAM Analysis on good, unused and fail samples showed no visible delamination on die surface.

Good Sample

Unused Sample

Fail Sample



Scanning Acoustic Microscopy (SAM)

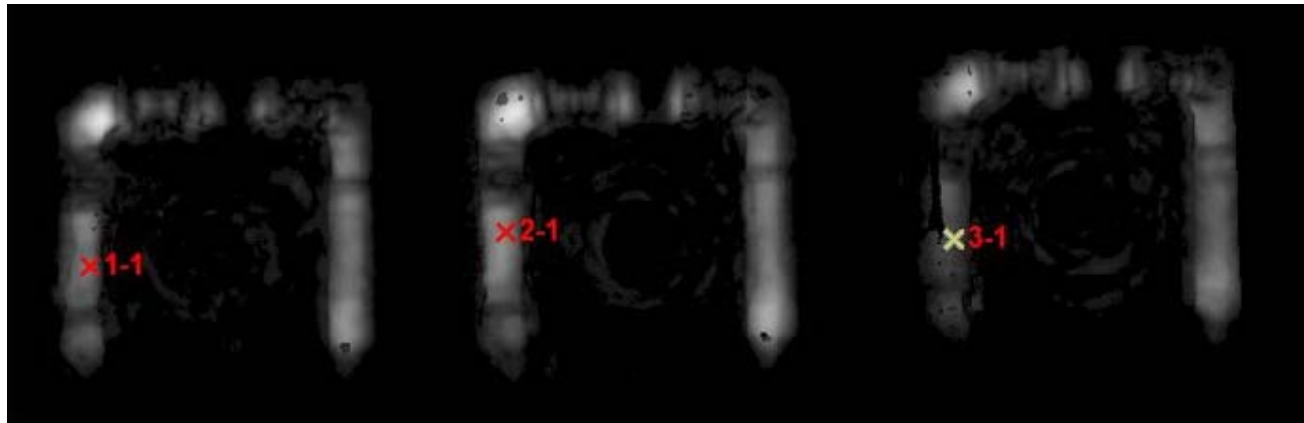
Scanning Acoustic Microscopy (SAM) was performed on good, unused and fail sample to verify delamination, voids and crack inside the package.

CSAM Analysis on good, unused and fail samples showed no delamination on leadframe surface.

Good Sample

Unused Sample

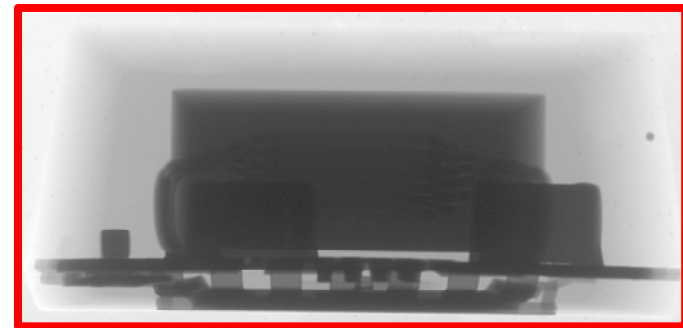
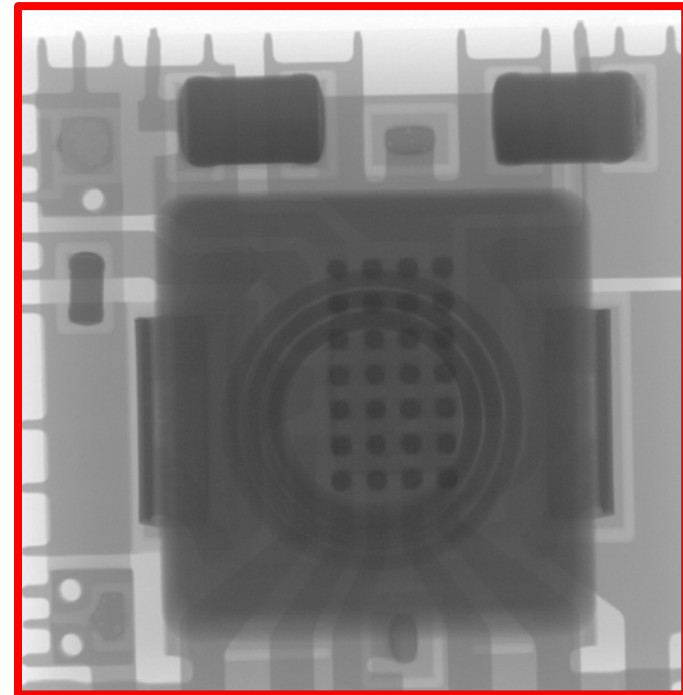
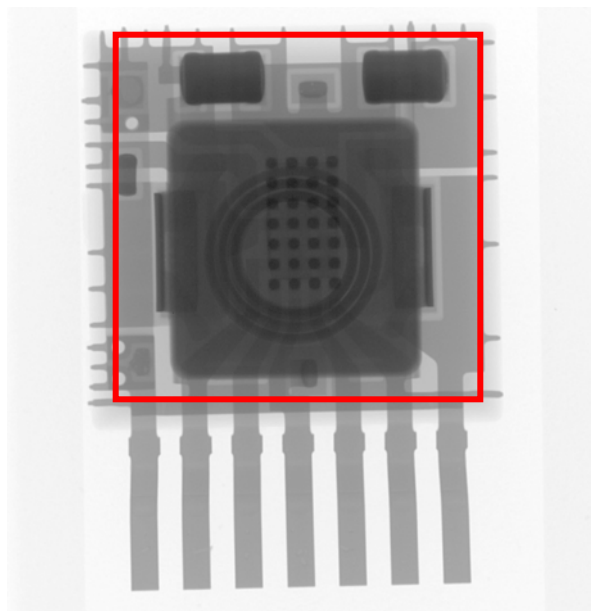
Fail Sample



X-ray Analysis

X-ray analysis was performed on good, unused and fail samples to check for internal connection anomalies, metallic contamination and other anomalies that can be observed through X-ray.

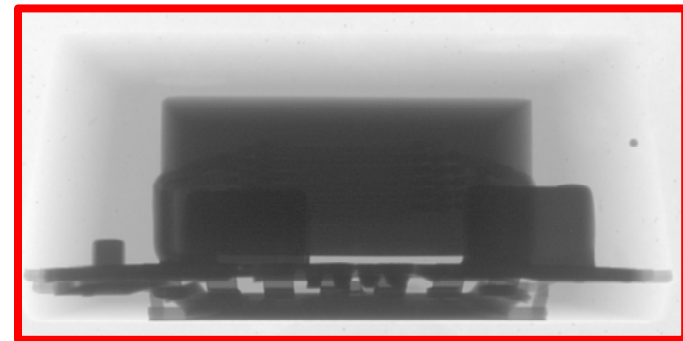
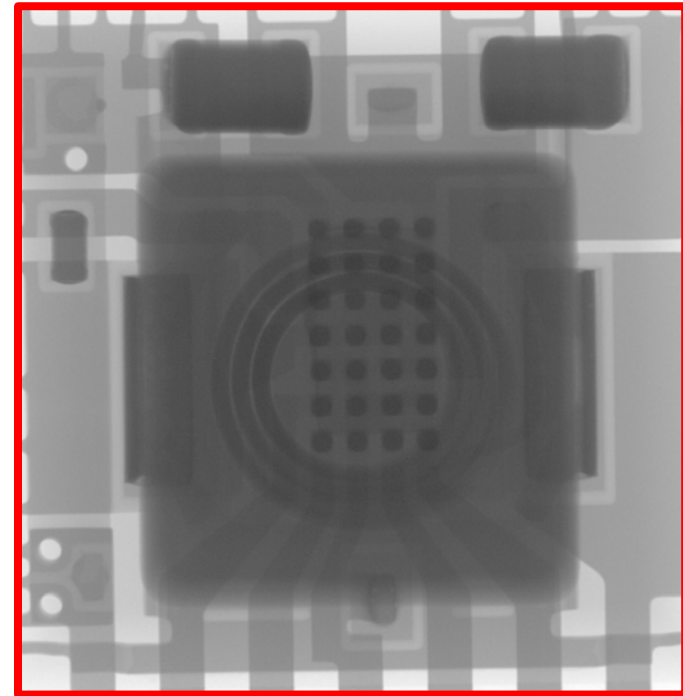
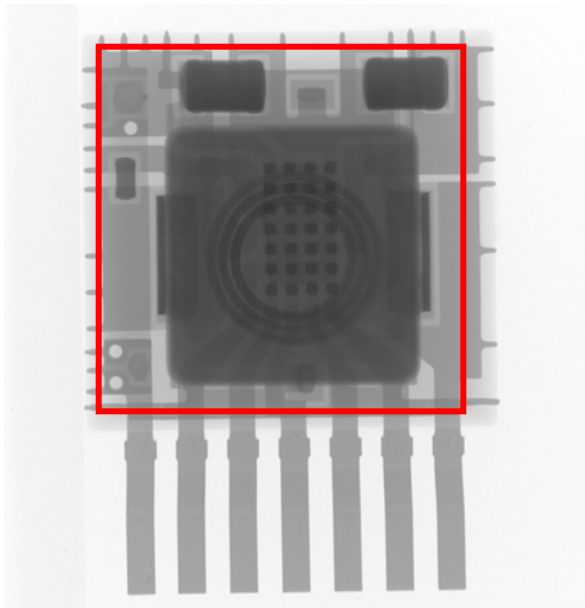
Analysis on good sample showed normal bump connection with no visible internal anomalies.



X-ray Analysis

X-ray analysis was performed on good, unused and fail samples to check for internal connection anomalies, metallic contamination and other anomalies that can be observed through X-ray.

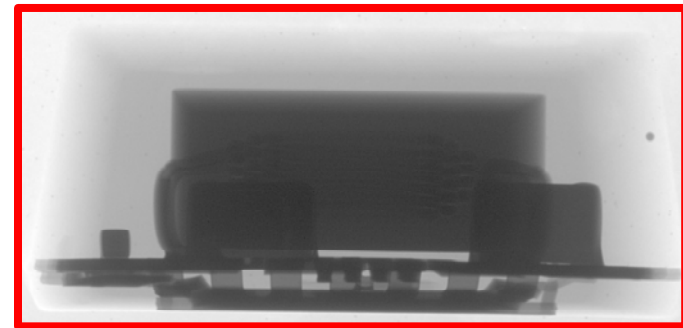
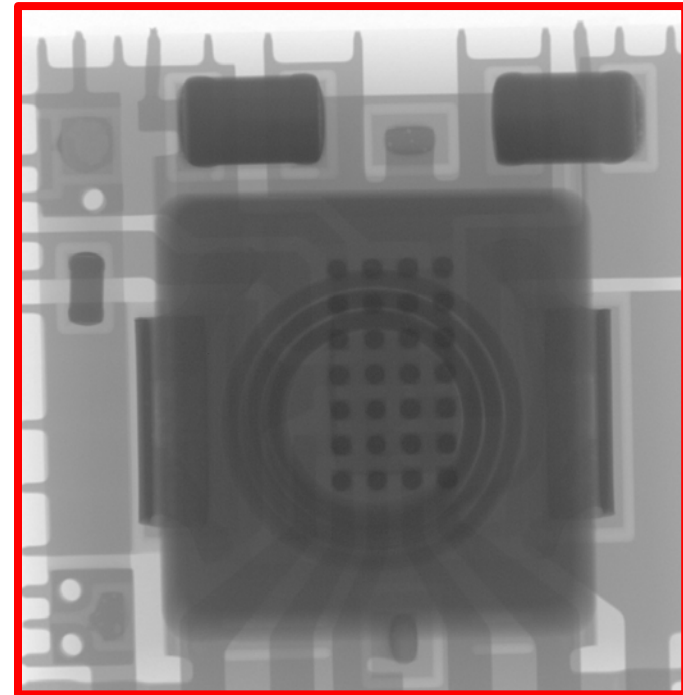
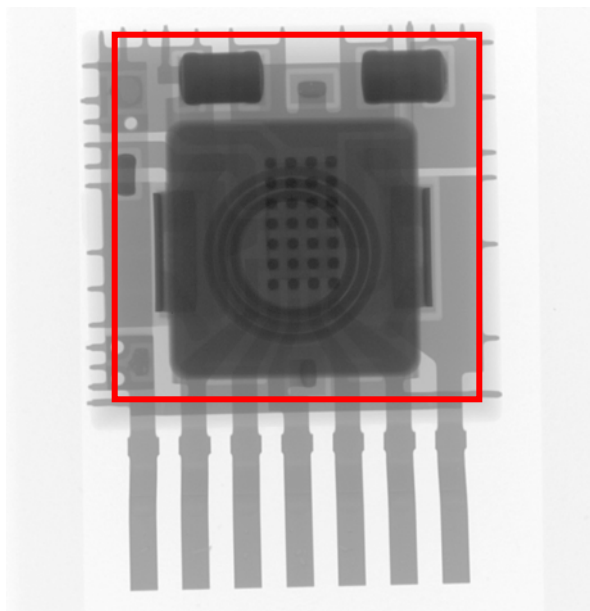
Analysis on unused sample showed normal bump connection with no visible internal anomalies.



X-ray Analysis

X-ray analysis was performed on good, unused and fail samples to check for internal connection anomalies, metallic contamination and other anomalies that can be observed through X-ray.

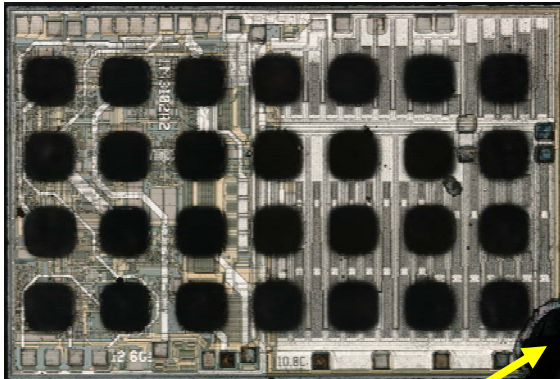
Analysis on fail sample showed normal bump connection with no visible internal anomalies.



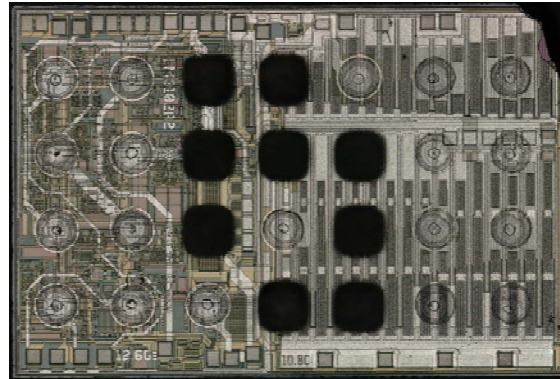
Decapsulation Analysis

Decapsulation was performed on good, unused and fail samples to expose the die surface for analysis. Decapsulation on good, unused and fail samples reveals consistent die topography with the same National Semiconductor logo, LM3102A2 and other die markings, verifying that parts were manufactured by Texas Instruments but not traceable to requested part number. National Semiconductor was acquired by Texas Instruments. The good sample and unused sample have die chipping which is due to decapsulation process artifacts.

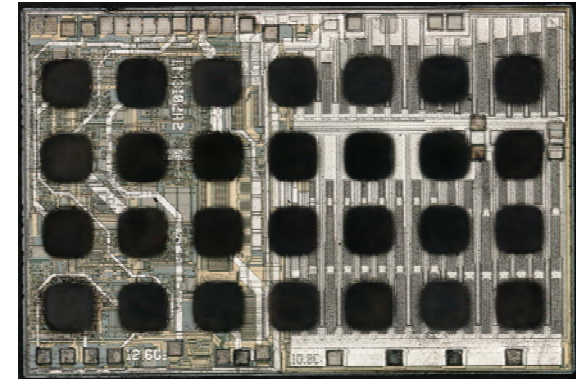
Good Sample



Unused Sample

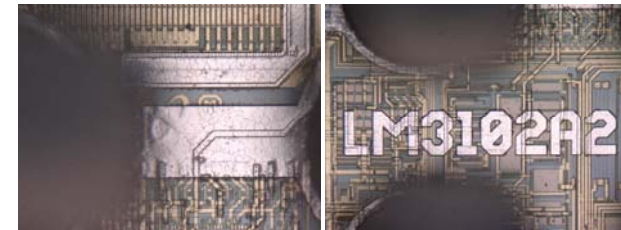
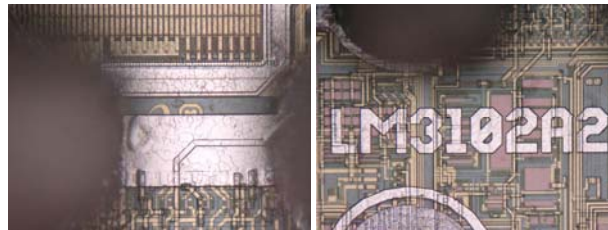
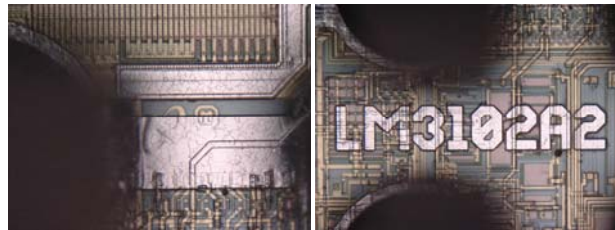


Fail Sample



Decapsulation Process Artifacts

Decapsulation Process Artifacts



Decapsulation Analysis

Further inspection on the top surface of fail sample showed scratches on die surface.

