TDA4VM Edge AI Kit - DUAL TPS65941x PMICs

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Project :

TDA4VM Edge AI Kit

Texas Instruments

Title

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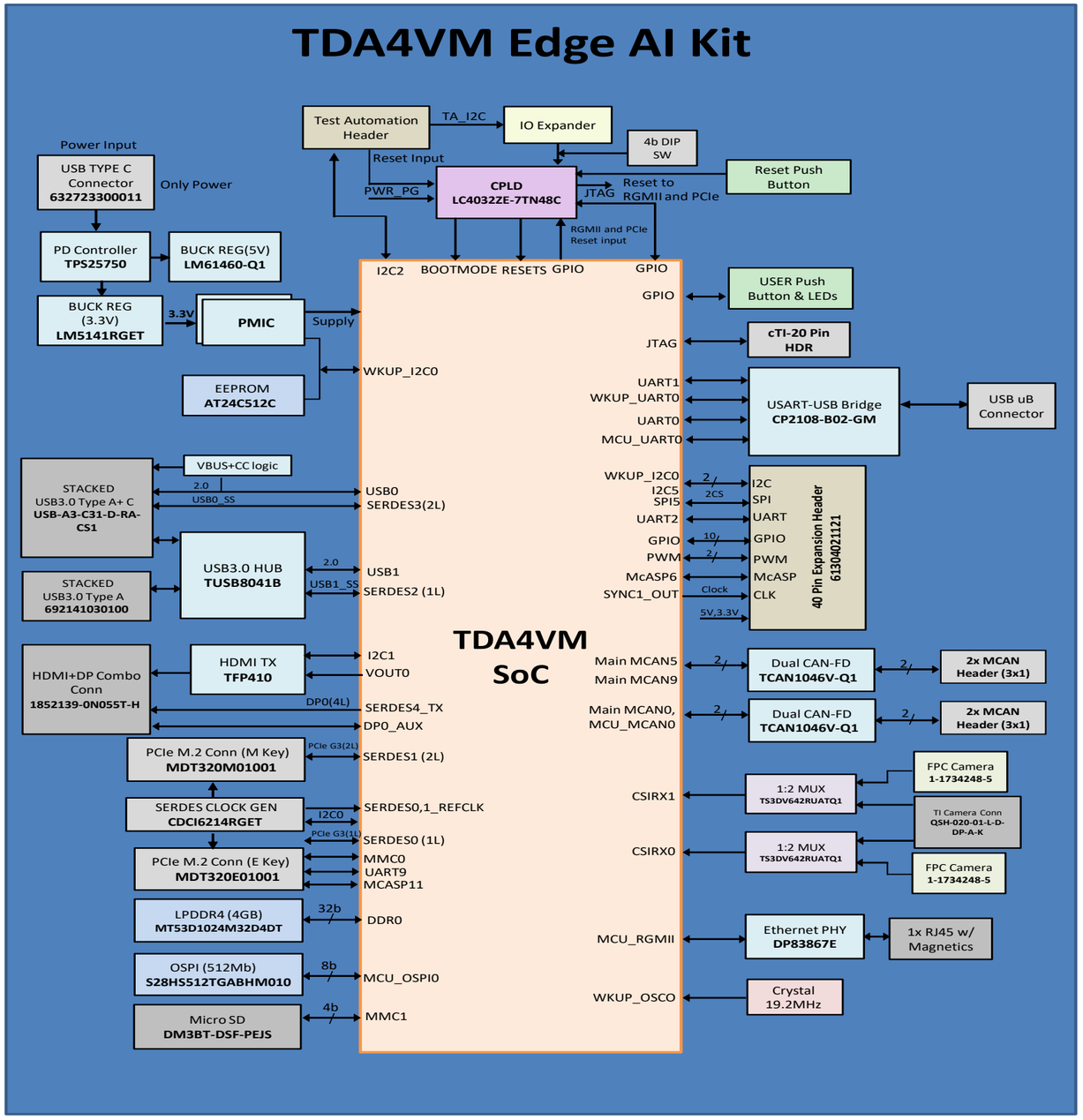
REVISION HISTORY

REV #	DATE	DESCRIPTION OF CHANGES	AUTHOR	REVIEWED BY	APPROVED BY
E2	08 APR 2021	Drafted from E1 version	Mistral Design Team		
	08 APR 2021	Pin swapping done for D17 and D18	Mistral Design Team		
	30 APR 2021	Part# updated for Capacitor C356 from GCM155R71C104JA55D to GCM155R71C104KA55D DNI'd the Test points TP2 and TP6	Mistral Design Team		
	25 MAY 2021	Added Buffer U61 for OSPI reset signal Added Buffer U62 for PCIe M.2 E key Reset and wake signals Updated the PMIC-B, Buck-5 FB to "VDD_RAM_0V85_REG" before FL6/FL18 Changed the supply of CPLD device U38 and CPLD Programming header J7 to VSYS_MCUIO_1V8 Updated MCU Ethernet RJ45 connector J8 Mfr.Part # to LPJG16314A4NL and Added Indication LED circuit for 100Mbps speed	Mistral Design Team		
	27 MAY 2021	Connected MCU_PORz_OUT signal to CPLD Updated 25Mhz Crystal Y1 connected to Ethernet PHY to Mfr.Part# ECS-250-18-23A-JGN-TR Added Test points TP66,TP67,TP68 and TP69 for reset signals to RGMII, PCIe M.2 E and M key signals	Mistral Design Team		
	31 MAY 2021	Updated USB Stacked TYPE 3.0 Conn to Mfr.Part# 484060003 Updated for Internal Review Comments	Mistral Design Team		
	01 JUN 2021	Updated USB 3.0 Hub Upstream port super speed lines	Mistral Design Team		
	02 JUN 2021	Updated for TI review comments(Partiallly)	Mistral Design Team		
	03 JUN 2021	Updated for internal review comments	Mistral Design Team		
	04 JUN 2021	Added Serdes reference clock generator for PCIe	Mistral Design Team		
	07 JUN 2021	Updated for internal review comments	Mistral Design Team		
	10 JUN 2021	Component package optimized for CDCI SEDES Clock section for PCB routing ease	Mistral Design Team		
	11 JUN 2021	Updated the Part# for FL26, FL27, FL28 FL29 to NFM15PC474R0J3D	Mistral Design Team		
	17 JUN 2021	Replaced 2-T, 0.1uF 0201 cap C409 to 3-T, 1uF 0402 Removed 2-T, 0.1uF 0201 cap C414	Mistral Design Team		
	22 JUN 2021	Updated notes for Silkscreen Connected VDDA_1P8_DSITX filtered supply to VDDA_1P8_MLB power group Connected VDDA_0P8_USB filtered supply to VDDA_0P8_UFS power group	Mistral Design Team		
	23 JUN 2021	Pin Swapping done for HDMI common mode choke and ESD diode U28 for routing ease	Mistral Design Team		
	25 JUN 2021	Updated part GCM31CD70G476ME to complete part number GCM31CD70G476ME02 Updated part GCM033C70J104K to complete part number GCM033C70J104KE02D Changed part RCA04060000Z0EALS alternate part RCL04060000Z0EA Changed part PNM0402E5000BST1 (500E) to RC0402FR-07499RL Pin Swapping done for HDMI common mode choke and ESD diode U28 for routing ease	Mistral Design Team		
	06 JUL 2021	Changed I2C Bootmode buffer address to 0x20h (R152 connected to GND) DNI'd decaps C655 and C656	Mistral Design Team		
	13 JUL 2021	Updated power flow block diagram	Mistral Design Team		
	21 JUL 2021	Baselined	Mistral Design Team		

Project : TDA4VM Edge AI Kit	Texas Instruments	Title: REVISION HISTORY Size: C | PROC112 001 J721EXSKG01EVM | Rev: E2 Date: Wednesday, July 21, 2021 | Sheet 2 of 48

SYSTEM BLOCK DIAGRAM



Project : TDA4VM Edge AI Kit	TEXAS INSTRUMENTS	Title: BLOCK DIAGRAM
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3-Phase DUAL PMIC PDN Recommended for New Designs
(3-Phase Buck supplying VDD_CPU)

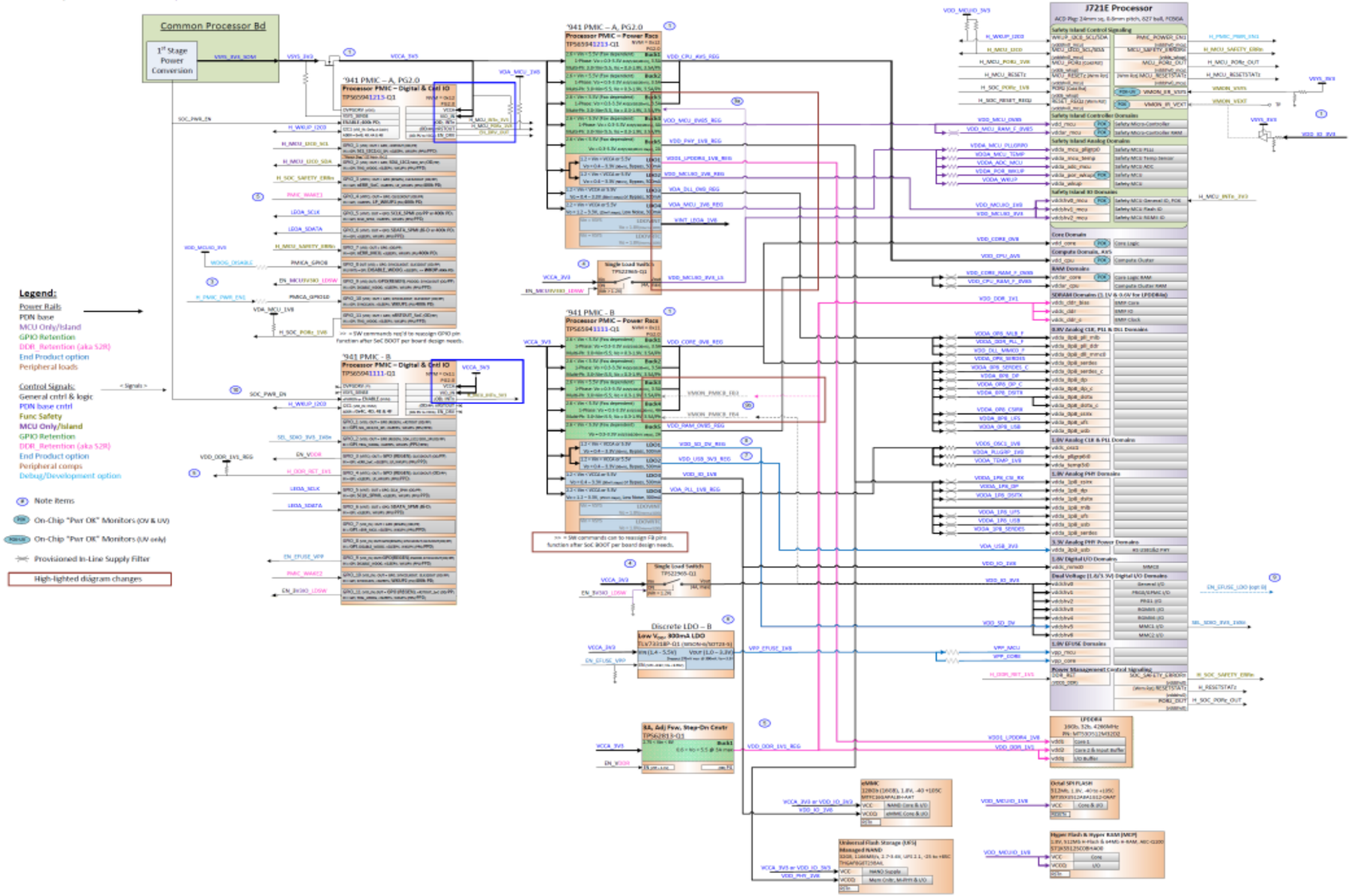
DRA829/TDA4VM 3-Phase Dual Leo2.0 PDN-0C
(Power Rail & GPIO Mapping Overview)

Leo PMIC-A, PN TPS6594**1213**RWERQ1 (TI PN ID = 1, MP Buck Rails = 2, NVM ID = **13**, PG2.0)
Leo PMIC-B, PN TPS6594**1111**RWERQ1 (TI PN ID = 1, MP Buck Rails = 2, NVM ID = **12**, PG2.0)

Features Supported (EVM Max Features):

1. SoC performance: Max 2.0GHz clock with SERDES interfaces operational
2. Functional Safety: ASIL-D capable system with independent MCU & Main power for FFI
3. SDRAM: 32Gb, 4-Die, 32b, 4266MTs, LPDDR4 mode
4. Boot & Mass Flash: Octal SPI or Hyperflash (SR1.1 only) & eMMC, UFS
5. Low power modes: MCU Only & DDR Retention
6. Signaling Levels: MCU & Main Dual VIO
7. End Product Options:
   a. Compliant high-speed SD Card
   b. Compliant USB 2.0 data eye
   c. HS SoC Efuse programming on-board

V0.14	1/27/2021	1. Added example of VDD_IO_3V3 OV/UV monitoring by SoC's VMON_IR_VEXT input connection option to voltage buffer & voltage R-div needed to interface with SoC's internal R-div network optimized for monitoring 1.8V power rails. 2. Added 2x ext voltage monitoring inputs options for OV/UV monitoring by Hera PMIC of any safety critical system power rails. Hera's quad buck config can reassign remote sense feedback inputs (FB3 & FB4) for power rail monitoring. 3. Updated notes 1 & 9 accordingly.
V0.15	2/13/2021	Following final PMIC NVM review for defining new common PN ("1213") for Leo PG2.0 used in PDN-0C & -1A: 1. Update notes 2. Changed PMIC-A FB3 VMON input to be connected to VCCA_3V3 since VDD_MCU/IO_3V3 rail is not supported, see note 9a. 3. Added PMIC-B FB3 & FB4 assignment for VMON by SW after SoC boot for ext power rail monitoring options, see note 9b.
V0.16	3/2/2021	1. Removing discrete load switch from supplying PMIC's VIO_IN since PG2.0 PMICs validation testing confirms no excessive glitches on GPIO or reset signals during of NVM initialization. Related "Note #2" has been removed.



Project : TDA4VM Edge AI Kit		Title: 3-Phase DUAL PMIC PDN-0B DIAGRAM	
		Size: C	PROC112 001 J721EXSKG01EVM — Rev: E2
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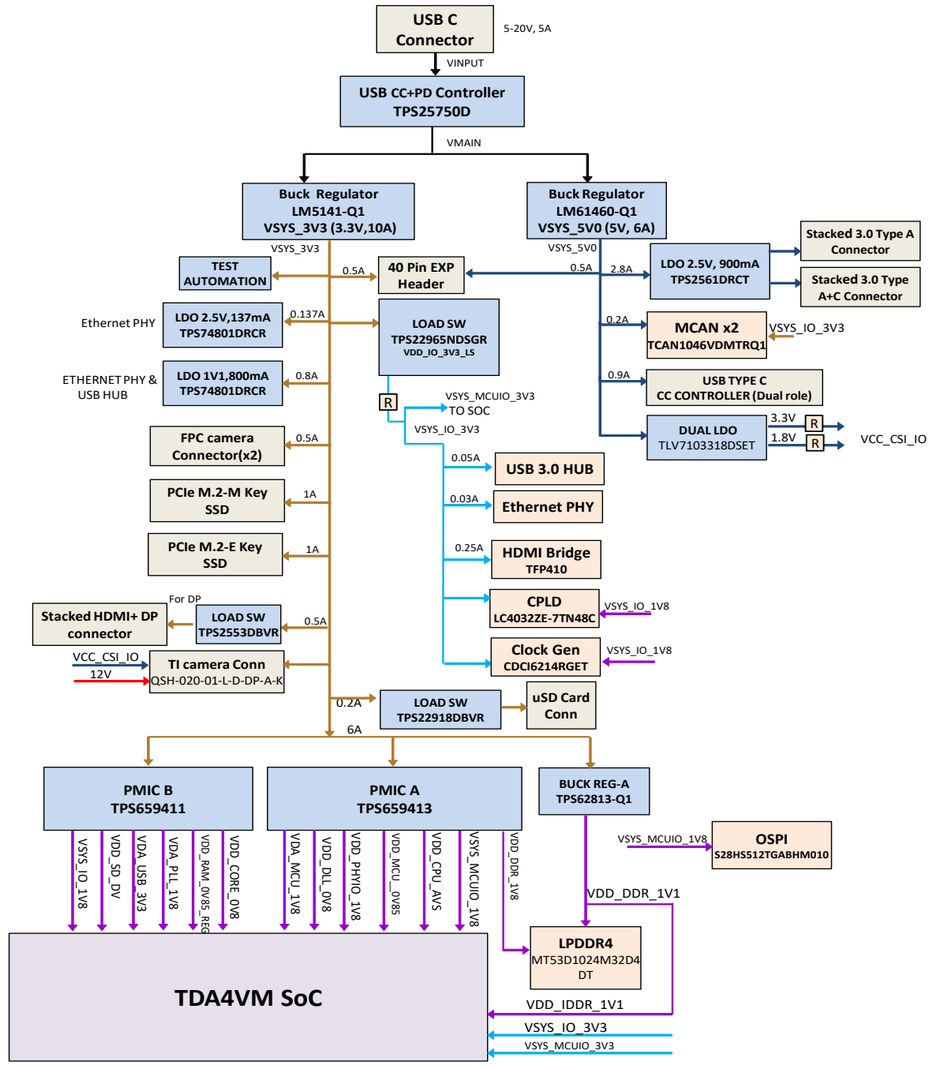
POWER FLOW DIAGRAM



Project : TDA4VM Edge AI Kit	TEXAS INSTRUMENTS	Title: POWER FLOW DIAGRAM
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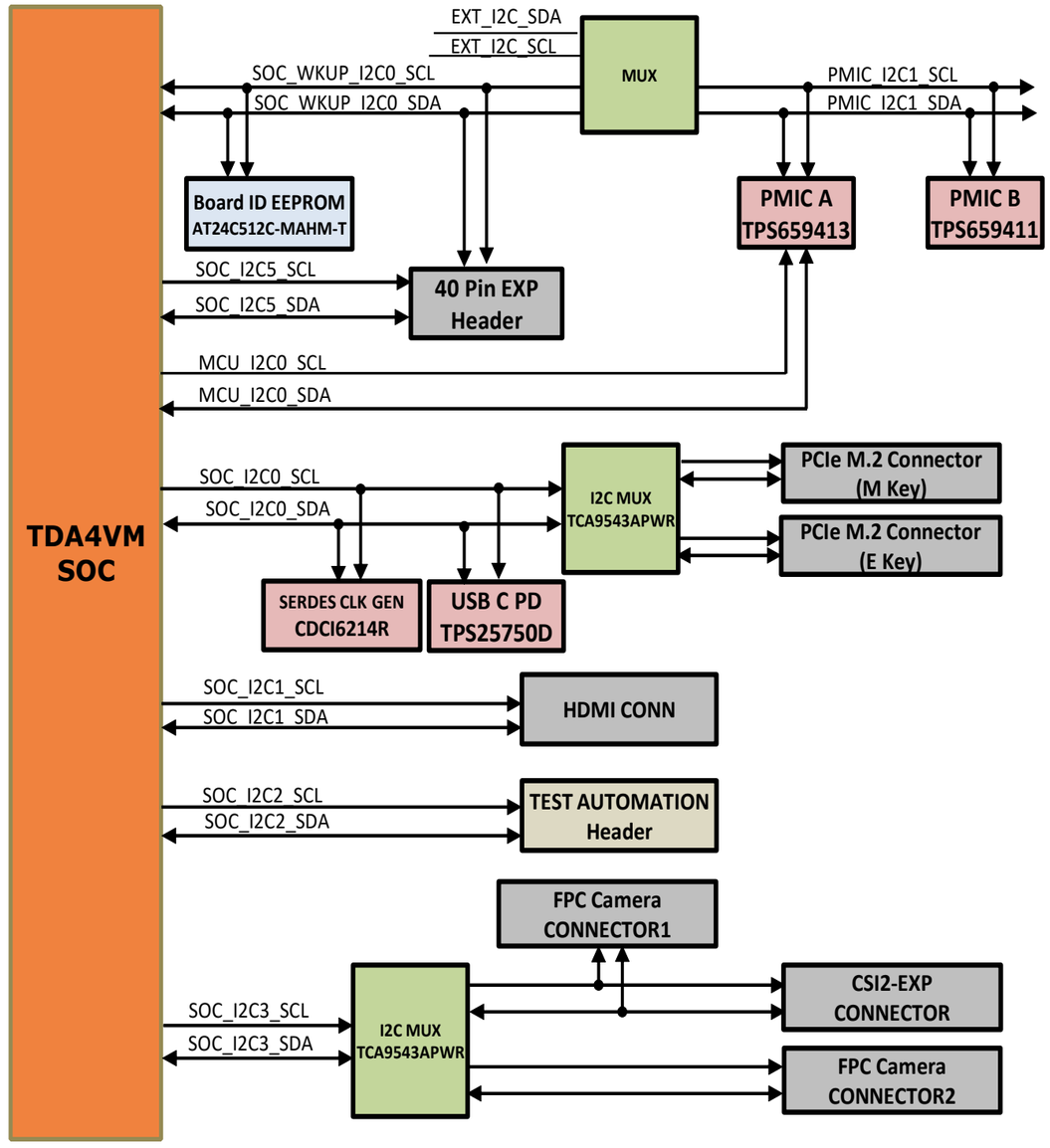
I2C TREE



Project : TDA4VM Edge AI Kit	Texas Instruments	Title: I2C TREE DIAGRAM
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GPIO MAPPING TABLE

GPIO Mapping							
Package Signal Name	**GPIO**	**Net name**	**Input/Output**	**IO Level**	**Default**	**State**	**Remarks**
WKUP Domain							
WKUP_GPIO0_3	WKUP_GPIO0_3	MCU_MCAN0_STB	Output	3.3V	NA	Active High	MCU CAN0 Standby
WKUP_GPIO0_4	WKUP_GPIO0_4	SOC_WAKE	Input	3.3V	PU	NA	SoC wake signal
WKUP_GPIO0_5	WKUP_GPIO0_5	BOARDID_EEPROM_WP	Output	3.3V	PD	Active High	Boot EEPROM Write protect
WKUP_GPIO0_6	WKUP_GPIO0_6	SOC_INT2z	Input	3.3V	PU	Active low	SOC Interrupt
WKUP_GPIO0_7	WKUP_GPIO0_7	H_MCU_INT#	Input	3.3V	PU	NA	MCU domain Interrupt
WKUP_GPIO0_8	WKUP_GPIO0_8	GPIO_uSD_PWR_EN	Output	3.3V	PU	Active High	GPIO for micro SD card power load switch power enable
WKUP_GPIO0_9	WKUP_GPIO0_9	SEL_SDIO_3V3_1V8n	Output	3.3V	PU	Active low	VDD_SD_DV 1.8V or 3.3V selection control
MCU_OSPI1_DQS	WKUP_GPIO0_31	MCU_OSPI0_INT#	Output	1.8V	PU	Active low	OSPI Interrupt Pin
WKUP_GPIO0_10	WKUP_GPIO0_10	GPIO_RGMII3_RST#	Output	3.3V	NA	Active low	Used as a reset signal for PRG0 Ethernet PHY Chip
WKUP_GPIO0_11	WKUP_GPIO0_11	SOC_PCIe1_M.2_RTSz	Output	3.3V	NA	NA	PCIe M.2 M key reset signal
MCU_OSPI1_D0	WKUP_GPIO0_32	CPLD_TCK	I/O	1.8V	PD	NA	JTAG Signals for CPLD
MCU_OSPI1_D1	WKUP_GPIO0_33	CPLD_TDI	I/O	1.8V	NA	NA	JTAG Signals for CPLD
MCU_OSPI1_D2	WKUP_GPIO0_34	CPLD_TDO	I/O	1.8V	NA	NA	JTAG Signals for CPLD
MCU_OSPI1_D3	WKUP_GPIO0_35	CPLD_TMS	I/O	1.8V	PU	NA	JTAG Signals for CPLD
MCU_OSPI1_CSN0	WKUP_GPIO0_36	M2_SDIO_RESET#	Output	1.8V	PU	Active low	Reset to SDIO(WiFi) Interface for PCIe M.2 E key
MCU_OSPI1_CSN1	WKUP_GPIO0_37	M2_SDIO_WAKE#	Output	1.8V	PU	Active low	Wake to SDIO(WiFi) Interface for PCIe M.2 E key
MCU_SPI0_CS0	WKUP_GPIO0_55	SYS_MCU_PWRDN	Output	3.3V	PD	Active High	System Power Down ('0' - normal operation, '1' - system power down)
PMIC_POWER_EN0	WKUP_GPIO0_66	RGMII_INT#	Input	3.3V	PU	NA	Ethernet Interrupt ('0' - interrupt pending, '1' - no interrupt)
Main Domain							
PRG1_PRU0_GPO4	GPIO0_5	40 Pin EXP Hdr - GPIO1	I/O	3.3V	NA	NA	GPIO for 40 Pin Expansion Header
PRG1_PRU0_GPO6	GPIO0_7	40 Pin EXP Hdr - GPIO2	I/O	3.3V	NA	NA	GPIO for 40 Pin Expansion Header
PRG1_PRU0_GPO7	GPIO0_8	40 Pin EXP Hdr - GPIO3	I/O	3.3V	NA	NA	GPIO for 40 Pin Expansion Header
PRG1_PRU0_GPO10	GPIO0_11	40 Pin EXP Hdr - GPIO4	I/O	3.3V	NA	NA	GPIO for 40 Pin Expansion Header
PRG0_PRU1_GPO8	GPIO0_71	40 Pin EXP Hdr - GPIO5	I/O	3.3V	NA	NA	GPIO for 40 Pin Expansion Header
PRG0_PRU1_GPO19	GPIO0_82	40 Pin EXP Hdr - GPIO6	I/O	3.3V	NA	NA	GPIO for 40 Pin Expansion Header
RGMII6_TX_CTL	GPIO0_97	40 Pin EXP Hdr - GPIO7	I/O	3.3V	NA	NA	GPIO for 40 Pin Expansion Header
SPI0_D1	GPIO0_115	40 Pin EXP Hdr- GPIO8	I/O	3.3V	NA	NA	GPIO for 40 Pin Expansion Header
PRG0_PRU0_GPO18	GPIO0_61	M.2_W_DISABLE1#	Output	3.3V	PU	Active low	WiFi disable1 signal for PCIe M.2 E key
PRG0_PRU0_GPO19	GPIO0_62	M.2_W_DISABLE2#	Output	3.3V	PU	Active low	WiFi disable2 signal for PCIe M.2 E key
PRG0_PRU1_GPO1	GPIO0_64	USER_LED1	Output	3.3V	PD	Active High	USER LED enable signal
PRG0_PRU1_GPO2	GPIO0_65	MCAN0_STB	Output	3.3V	NA	Active High	MCAN0 Standby
PRG0_PRU1_GPO3	GPIO0_66	MCAN5_STB	Output	3.3V	NA	Active High	MCAN5 Standby
PRG0_PRU1_GPO4	GPIO0_67	MCAN9_STB	Output	3.3V	NA	Active High	MCAN9 Standby
PRG0_PRU1_GPO9	GPIO0_72	SOC_PCIe0_M.2_RTSz	Output	3.3V	NA	NA	PCIe M.2 E key reset signal
PRG0_PRU1_GPO11	GPIO0_74	GPIO0_74	Output	3.3V	NA	NA	CSI2 Expansion Board Specific.
PRG0_PRU1_GPO12	GPIO0_75	GPIO0_75	Output	3.3V	NA	NA	CSI2 Expansion Board Specific.
PRG0_PRU1_GPO13	GPIO0_76	GPIO0_76	Output	3.3V	NA	NA	CSI2 Expansion Board Specific.
PRG0_PRU1_GPO14	GPIO0_77	GPIO0_77	Output	3.3V	NA	NA	CSI2 Expansion Board Specific.
PRG0_PRU1_GPO15	GPIO0_78	GPIO0_78	Output	3.3V	NA	NA	CSI2 Expansion Board Specific.
PRG0_PRU1_GPO16	GPIO0_79	GPIO0_79	Output	3.3V	NA	NA	CSI2 Expansion Board Specific.
SPI0_CS0	GPIO0_111	DP0_3V3 _EN	Output	3.3V	PD	Active High	Display Port Load Switch enable
SPI1_CS0	GPIO0_116	SOC_CAM0_GPIO1	I/O	3.3V	NA	NA	FPC Camera0 GPIO
SPI1_CS1	GPIO0_117	SOC_CAM0_GPIO2	I/O	3.3V	NA	NA	FPC Camera0 GPIO
SPI1_CLK	GPIO0_118	CSI_VIO_SEL	Output	3.3V	PD	Active High	CSI Dual IO selection
SPI1_D0	GPIO0_119	SOC_CAM1_GPIO1	I/O	3.3V	NA	NA	FPC Camera1 GPIO
SPI1_D1	GPIO0_120	SOC_CAM1_GPIO2	I/O	3.3V	NA	NA	FPC Camera1 GPIO
UART1_CTSN	GPIO0_127	HDMI_PDn	Output	3.3V	PD	Active low	HDMI power down signal
UART1_RTSN	GPIO1_0	HDMI_HPD	Input	3.3V	NA	NA	HDMI hot plug detect
RGMII5_TD2	GPIO0_88	CSI_MUX_SEL_2	Output	3.3V	PD	NA	CSI I2C MUX select(default 1.8V)
RGMII5_TD3	GPIO0_87	HDMI_LS_OE	Output	3.3V	PU	Active low	Enable signal for supply load switch for HDMI Connector
RGMII5_RD1	GPIO0_95	BT_UART_WAKE#	Output	3.3V	PU	Active low	Wake signal for Bluetooth(PCIe M.2 E key)
MCAN1_RX	GPIO1_3	USBC_DIR	Input	3.3V	PU	NA	USB C direction indication(Low-Position 1,High-Position 2)

Project : TDA4VM Edge AI Kit

Texas Instruments

Title: GPIO MAPPING TABLE

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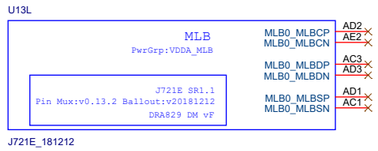
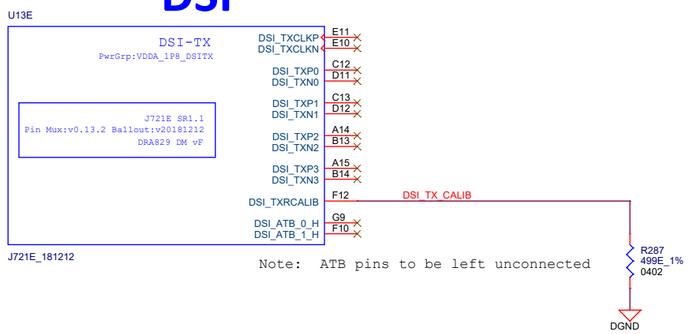
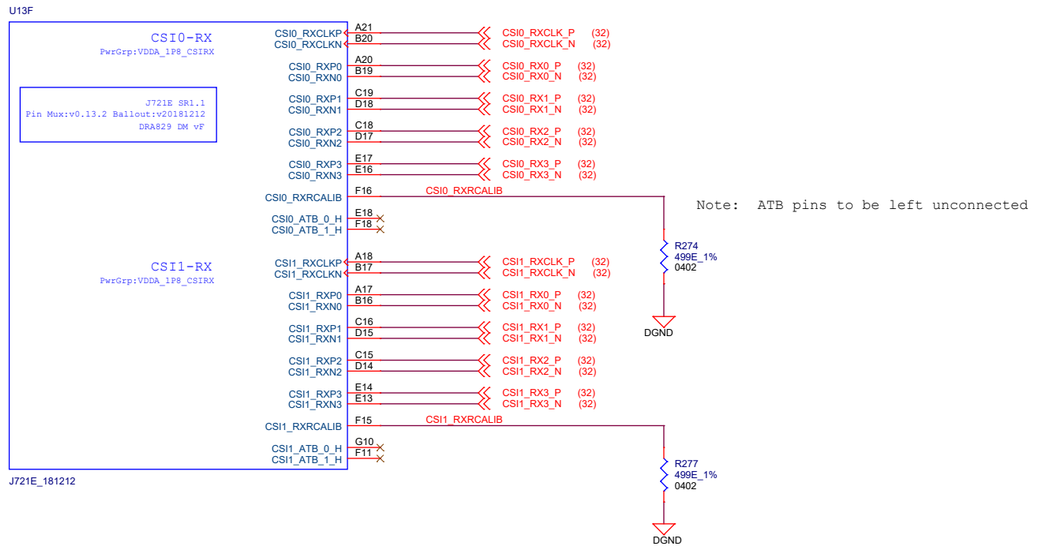
MLB



DSI



CSI Interface



Project : TDA4VM Edge AI Kit	TEXAS INSTRUMENTS	Title: MLB,CSI&DSI_INTERFACE
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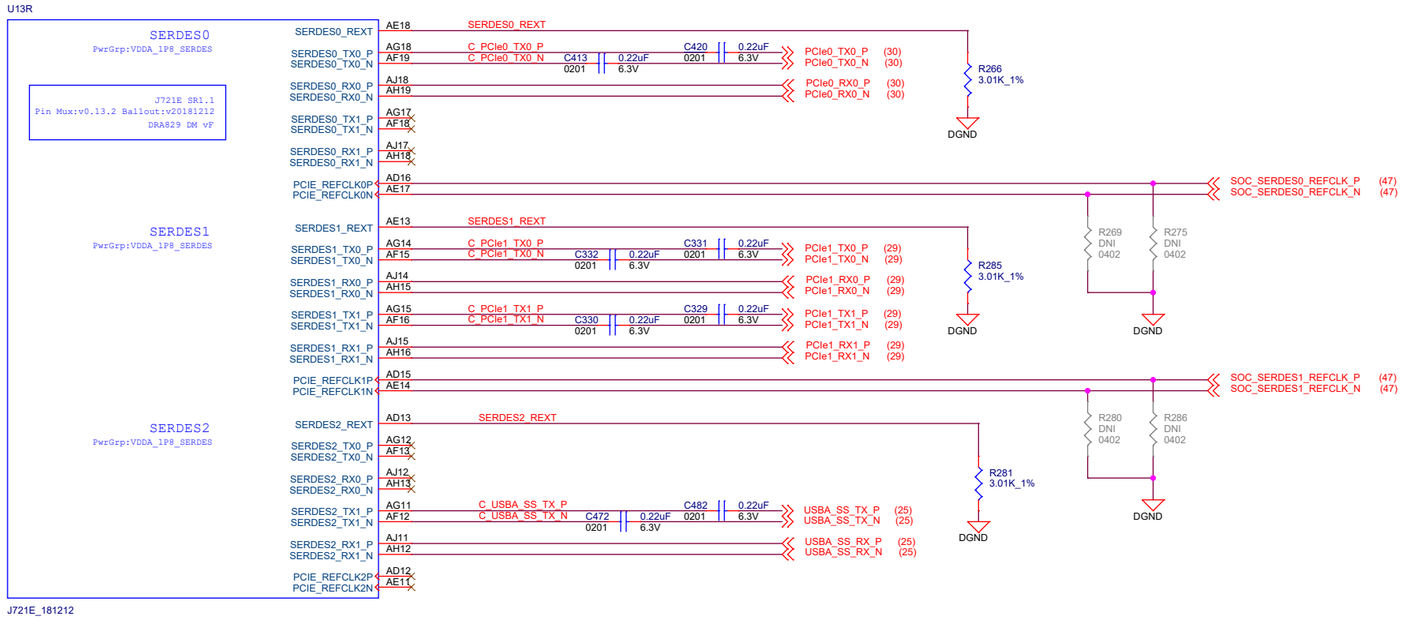
SERDES



Project : TDA4VM Edge AI Kit	Texas Instruments	Title: SERDES_INTERFACE
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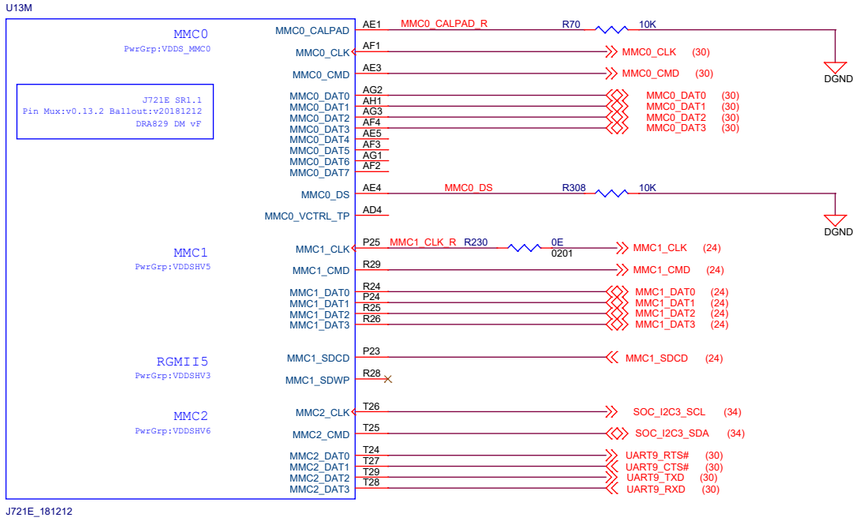
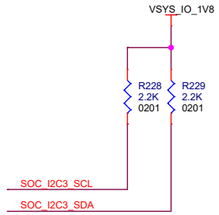
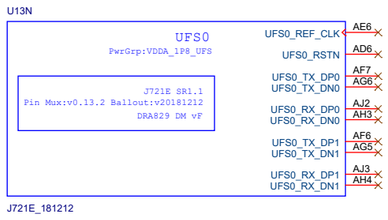
MMC Interface





UFS Interface



Project : TDA4VM Edge AI Kit	TEXAS INSTRUMENTS	Title: MMC,UFS_INTERFACE
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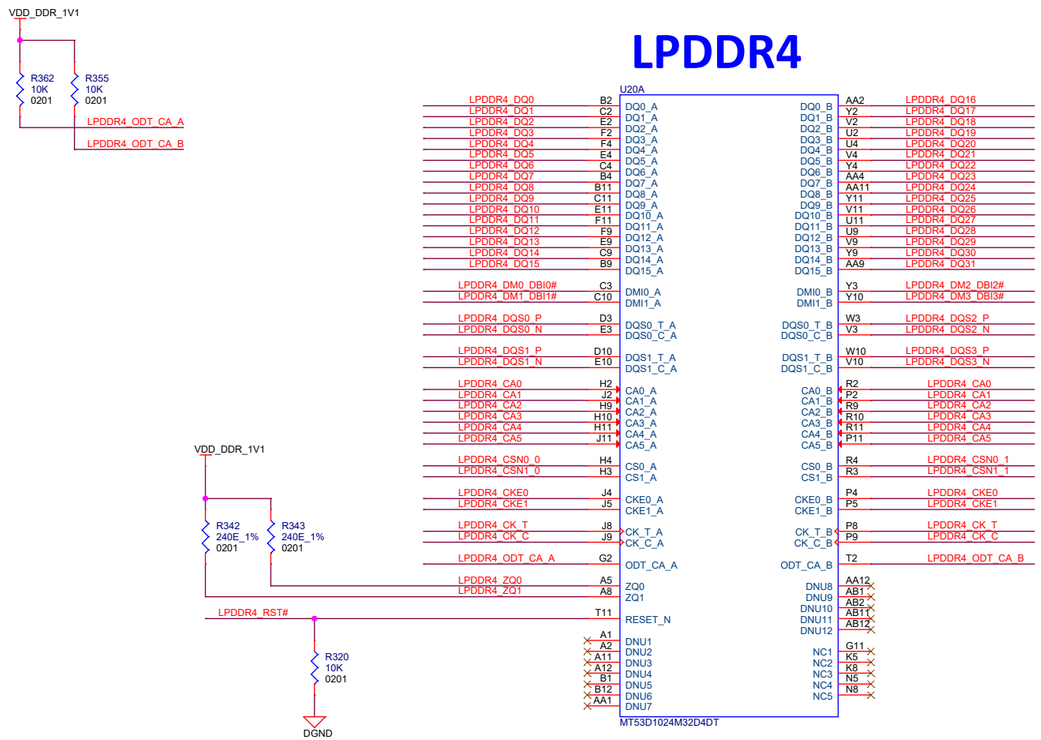
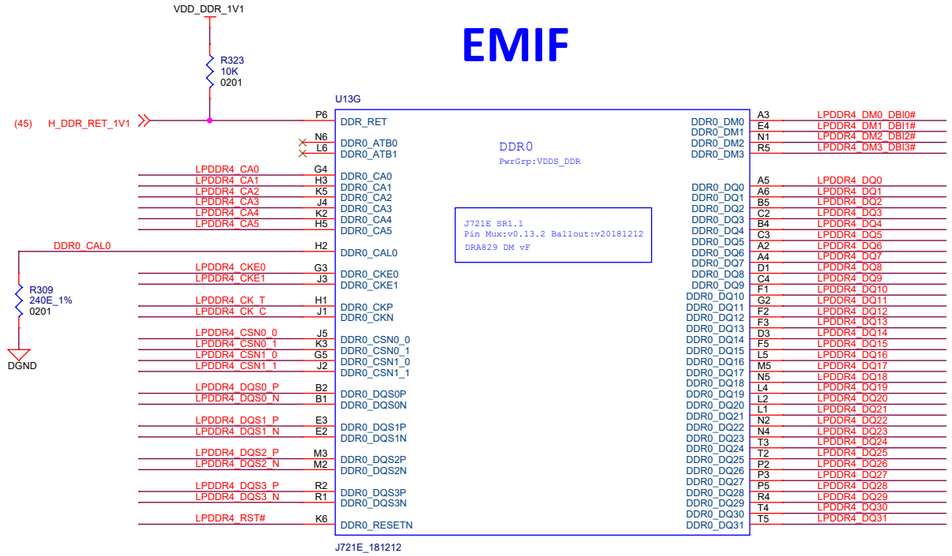
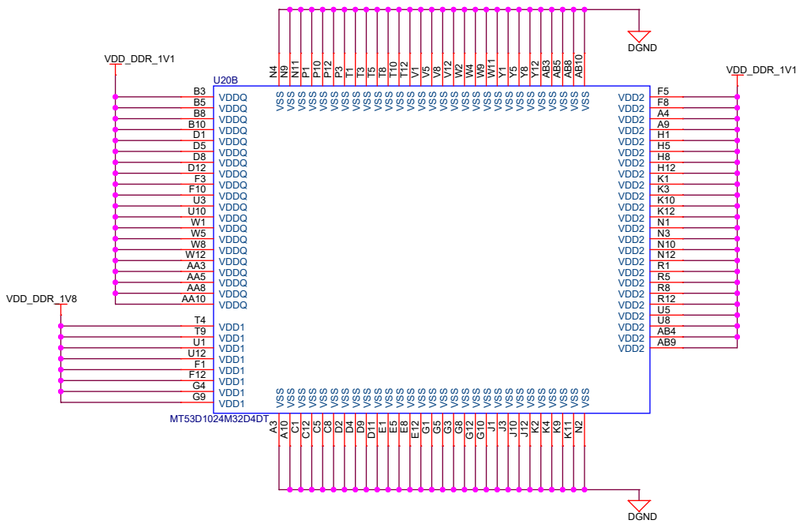
LPDDR4



EMIF





Project :

TDA4VM Edge AI Kit

Texas Instruments

Title: LPDDR4

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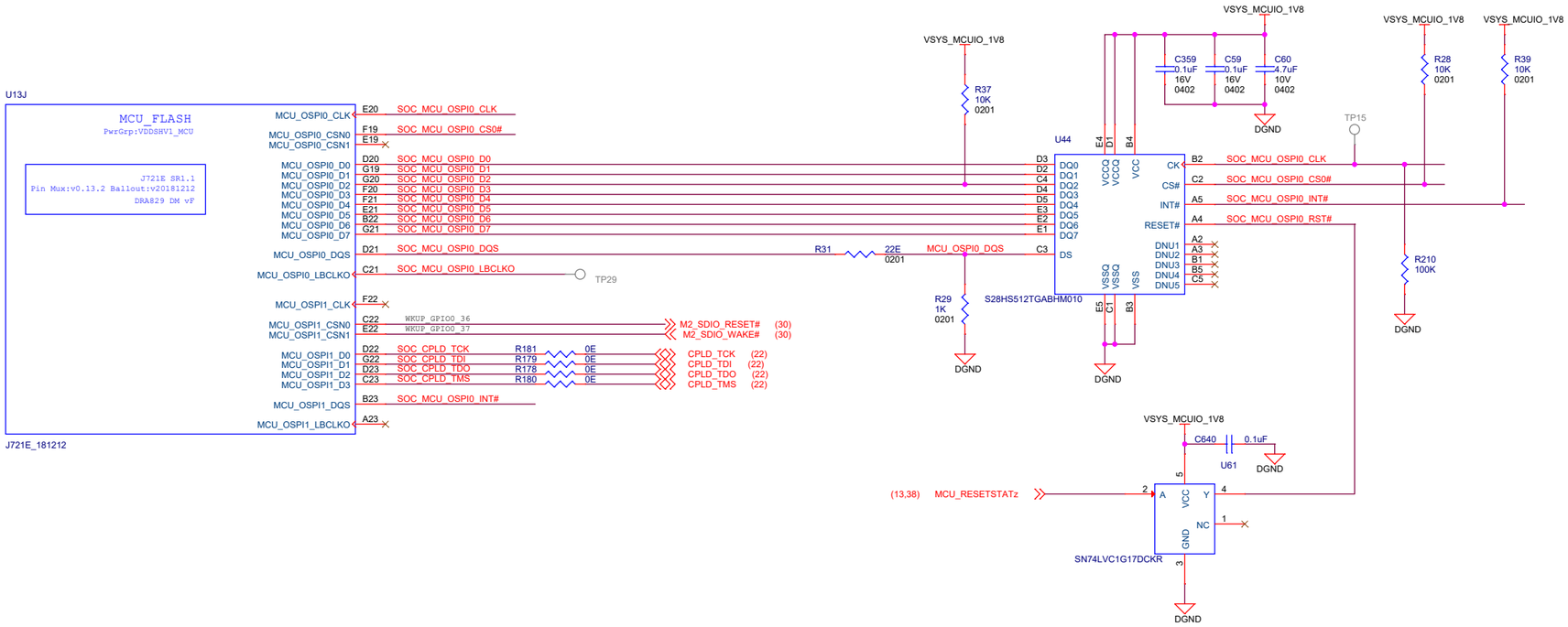
MCU FLASH

OSPI FLASH



Project : TDA4VM Edge AI Kit	TEXAS INSTRUMENTS	Title: MCU FLASH
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MCU & MAIN GENERAL IO, OSC CLKS

U13I

MCU_GENERAL
PwrGrp:VDDSHV0_MCU

J721E SR1.1
Pin Mux:v0.13.2 Ballout:v20181212
DRA829 DM vF

VDDA_MCU_PLLGRP0
PwrGrp:VDDA_MCU_PLLGRP0

J721E_181212

MCU_I2C0_SCL	J26	MCU_I2C0_SCL (44)
MCU_I2C0_SDA	H25	MCU_I2C0_SDA (44)
MCU_I3C0_SCL	D26	MCU_UART0_CTS# (38)
MCU_I3C0_SDA	D25	MCU_UART0_RTS# (38)
MCU_MCAN0_TX	D29	MCU_MCAN0_TX (37)
MCU_MCAN0_RX	C29	MCU_MCAN0_RX (37)
MCU_SPI0_CLK	E27	MCU_BOOTMODE00
MCU_SPI0_CS0	E25	SYS_MCU_PWRDN (21)
MCU_SPI0_D0	E24	MCU_BOOTMODE01
MCU_SPI0_D1	E28	MCU_BOOTMODE02
MCU_RESETSTATZ	C27	MCU_RESETSTATz (12,38)
MCU_RESETZ	D28	MCU_RESETZ (22)
MCU_PORZ_OUT	B28	MCU_PORZ_OUT (22)
WKUP_I2C0_SCL	J25	WKUP_I2C0_SCL (23,44)
WKUP_I2C0_SDA	H24	WKUP_I2C0_SDA (23,44)
WKUP_UART0_TXD	J28	WKUP_UART0_TXD (38)
WKUP_UART0_RXD	J29	WKUP_UART0_RXD (38)
WKUP_GPIO0_0	F26	MCU_BOOTMODE03
WKUP_GPIO0_1	F25	MCU_BOOTMODE04
WKUP_GPIO0_2	F28	MCU_BOOTMODE05
WKUP_GPIO0_3	F27	
WKUP_GPIO0_4	G25	MCU_MCAN0_STB (37)
WKUP_GPIO0_5	G24	SOC_WAKE (21)
WKUP_GPIO0_6	F29	SOC_INT2z
WKUP_GPIO0_7	G28	PMIC_MCU_INT# R221 0E H_MCU_INT# (44,45)
WKUP_GPIO0_8	G27	GPIO_uSD_PWR_EN (24)
WKUP_GPIO0_9	G26	SEL_SDIO_3V3_1V8n (45)
WKUP_GPIO0_10	H26	GPIO_MCU_RGMII_RST# (22)
WKUP_GPIO0_11	H27	SOC_PCIe1_M.2_RTSz (22)
WKUP_GPIO0_12	G29	MCU_UART0_TXD (38)
WKUP_GPIO0_13	H28	MCU_UART0_RXD (38)
WKUP_GPIO0_14	H29	MCU_BOOTMODE06
WKUP_GPIO0_15	J27	MCU_BOOTMODE07
TEMP_DIODE_P	F13	

VSYS_MCUIO_3V3: R153 2.2K 0201, R155 2.2K 0201
WKUP_I2C0_SCL
WKUP_I2C0_SDA

VSYS_MCUIO_3V3: R328 2.2K 0201, R329 2.2K 0201, R240 2.2K
MCU_I2C0_SCL
MCU_I2C0_SDA
MCU_RESETZ

TP16
R238 10K 0201
DGND

TP20
R43 10K 0201
DGND

VSYS_IO_3V3
R41 10K 0201

SOC_INT2z (22)
From Test Automation header

VSYS_IO_3V3: R239 10K, R40 10K, R256 10K 0201

TP23

U13C

MCU_GENERAL
PwrGrp:VDDSHV0_MCU

J721E SR1.1
Pin Mux:v0.13.2 Ballout:v20181212
DRA829 DM vF

GENERAL
PwrGrp:VDDSHV0

J721E_181212

EMU0	C26	SOC_EMU0
EMU1	B29	SOC_EMU1
TRSTN	F24	SOC_TRST#
RESET_REQZ	C28	SOC_RESET_REQZ R258 0E RESET_REQZ
PMIC_POWER_EN0	E26	
PMIC_POWER_EN1	G23	MCU_RGMII_INT# (31) PMIC_POWER_EN1 (44)
TCK	E29	SOC_TCK
TDI	V1	SOC_TDI
TDO	V3	SOC_TDO
TMS	V2	SOC_TMS
PORZ_OUT	U1	SOC_PORZ_OUT R69 10K 0201 SOC_PORZ_OUT (22,47)
TIMER_IO0	V6	SYSCLKOUT0
TIMER_IO1	V5	OBSCLK0
SOC_SAFETY_ERRORN	U4	SOC_SAFETY_ERRZ (44)
RESETSTATZ	T6	R306 0201 10K RESETSTATZ (22,24,25,29,34)
EXT_REFCLK1	U3	SYNC1_OUT (23)
ECAP0_IN_APWM_OUT	U2	

DGND

Default state of the bootmode pins from CPLD are pulled down

MCU_BOOTMODE00
MCU_BOOTMODE01
MCU_BOOTMODE02
MCU_BOOTMODE03
MCU_BOOTMODE04
MCU_BOOTMODE05
MCU_BOOTMODE06
MCU_BOOTMODE07
MCU_BOOTMODE08

MCU_BOOTMODE03 (22)
MCU_BOOTMODE04 (22)
MCU_BOOTMODE05 (22)

MCU_UART0_TXD R245 0201 1K
MCU_UART0_RXD R243 0201 1K MCU_BOOTMODE09

R223 10K 0201, R225 10K 0201, R222 10K 0201, R224 10K 0201, R244 10K 0201, R237 10K 0201, R246 10K 0201

DGND

Note: MCU_BOOTMODE[2:0] set to '000' for 19.2MHz input frequency.

cTI 20PIN JTAG HEADER

VSYS_IO_3V3
C57 0.1uF
DGND

VSYS_IO_3V3
R25 4.7K

SOC_TCK
R26 22E 1% 0402

J9

SOC_TMS	1	2	SOC_TRST#
SOC_TDI	3	4	cTI20_TDIS
	5	7	
SOC_TDO	8	10	
cTI20_RTCK	9	11	
SOC_EMU0	12	14	SOC_EMU1
(22) JTAG_RESETz	15	16	
	17	18	
	19	20	

FTR-110-51-S-D-06-P

DGND

R51 0E
R52 4.7K
DGND DGND

OSC

U13D

OSC0
PwrGrp:VDDS_OSC1

J721E SR1.1
Pin Mux:v0.13.2 Ballout:v20181212
DRA829 DM vF

OSC1
PwrGrp:VDDS_OSC1

J721E_181212

MCU_SAFETY_ERRORN	D27	MCU_SAFETY_ERRZ (44)
MCU_PORZ	H23	MCU_PORZ (22,44)
PORZ	J24	PORZ (22,44)
WKUP_LFOSC0_XI	N28	WKUP_LFOSC0_XI (44)
WKUP_LFOSC0_XO	N26	
WKUP_OSC0_XI	M29	WKUP_OSC0_XIN
WKUP_OSC0_XO	M27	WKUP_OSC0_XOUT
ATEST0	AJ29	
OSC1_XI	P29	OSC1_XI
OSC1_XO	P27	OSC1_XO
IFORCE	P26	
VSENSE	R27	
MAIN_ATEST	N25	

R30 0E 0402 R_WKUP_OSC0_XIN
Y2 ABM10W-19.2000MHZ-8-K1Z-T3 19.200MHz
C53 0402 12pF 50V
R27 0E 0402 R_WKUP_OSC0_XOUT
C43 0402 12pF 50V
DGND

R215 DNI 0402 R_OSC1_XI
Y4 DNI
C352 0402 DNI 50V
R214 DNI 0402 R_OSC1_XO
C338 0402 DNI 50V
DGND

CLKS

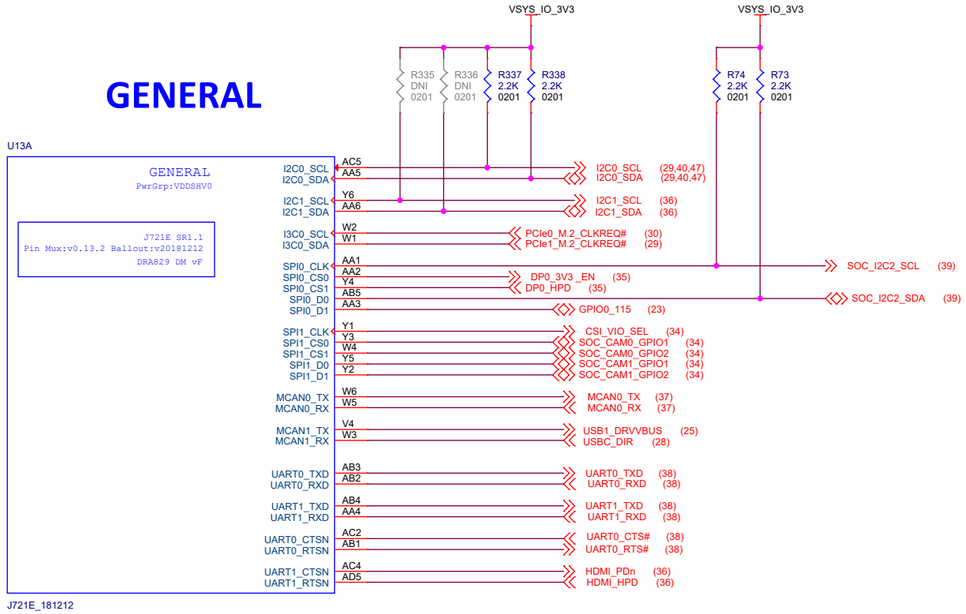
TP18
SYSCLKOUT0 R241 1K 0201 SYS_BOOTMODE4 (22)

TP17
OBSCLK0 R242 1K 0201 SYS_BOOTMODE5 (22)

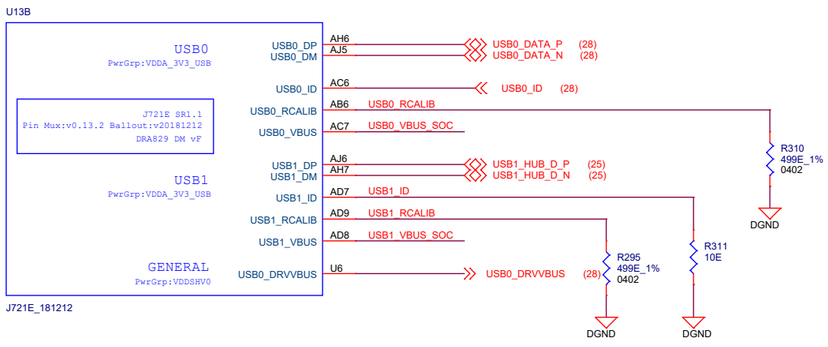
SOC_PORZ_OUT TP10
RESETSTATZ TP42

Project : TDA4VM Edge AI Kit		Title: SOC_GENERAL&MCU_GENERAL	
		Size: C	PROC112 001 J721EXSKG01EVM — Rev: E2
		Date: Wednesday, July 21, 2021	Sheet 13 of 48

GENERAL



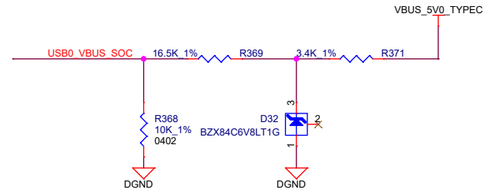
USB



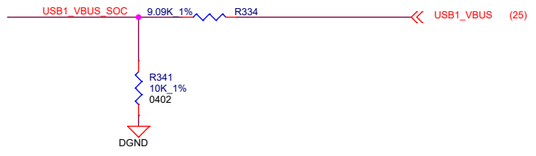
USB1_ID Pulled low. J7 SoC in Host Mode.

USB VBUS Resistor divider circuit

Note: Recommended VBUS circuit for USB connector. Supports 5V-30V VBUS

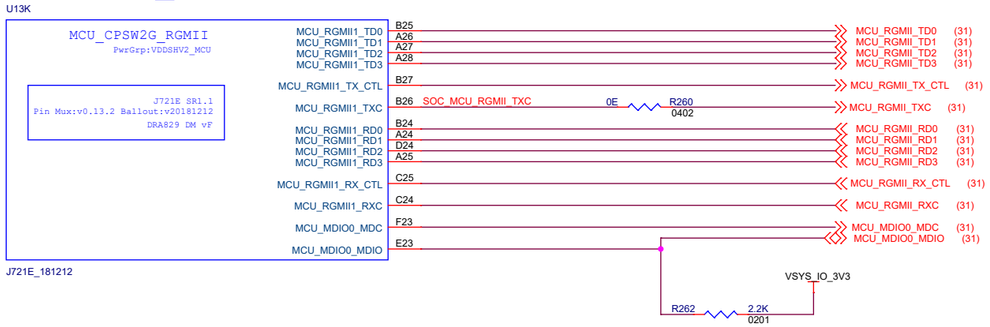


Note: Recommended VBUS circuit for embedded Hub

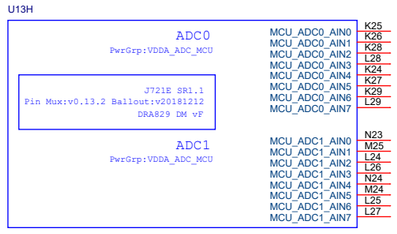


Project : TDA4VM Edge AI Kit	TEXAS INSTRUMENTS	Title: GENERAL_USB
	Size: C	PROC112 001 J721EXSKG01EVM — Rev: E2
	Date: Tuesday, July 20, 2021	Sheet 14 of 48

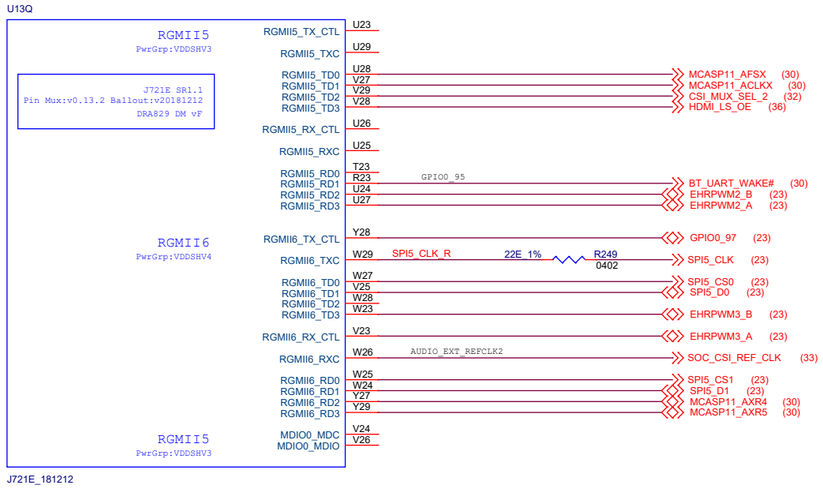
MCU_RGMII



MCU ADCs



MAIN RGMII



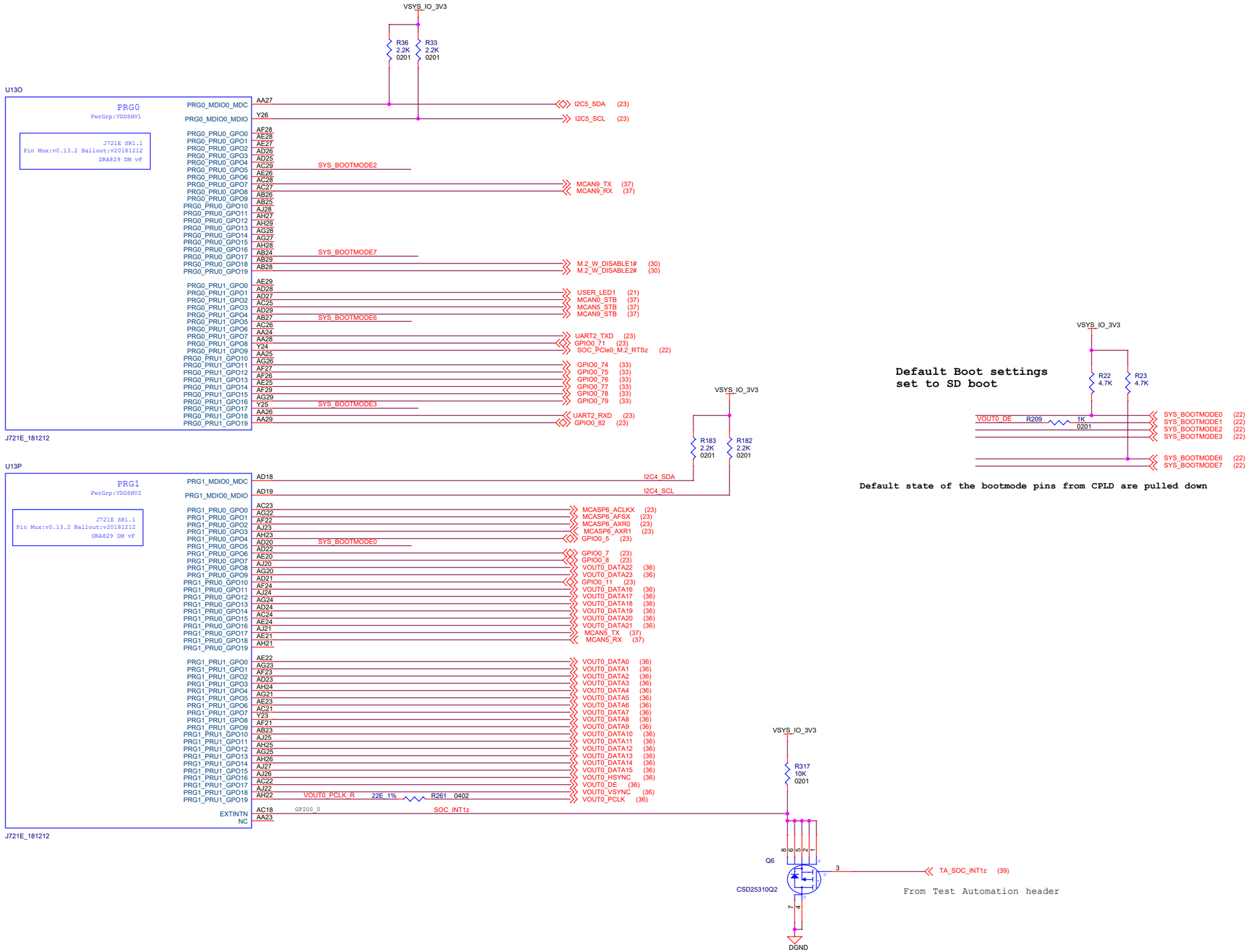
Project :

TDA4VM Edge AI Kit

Title
MCU_RGMII&MCU_ADC

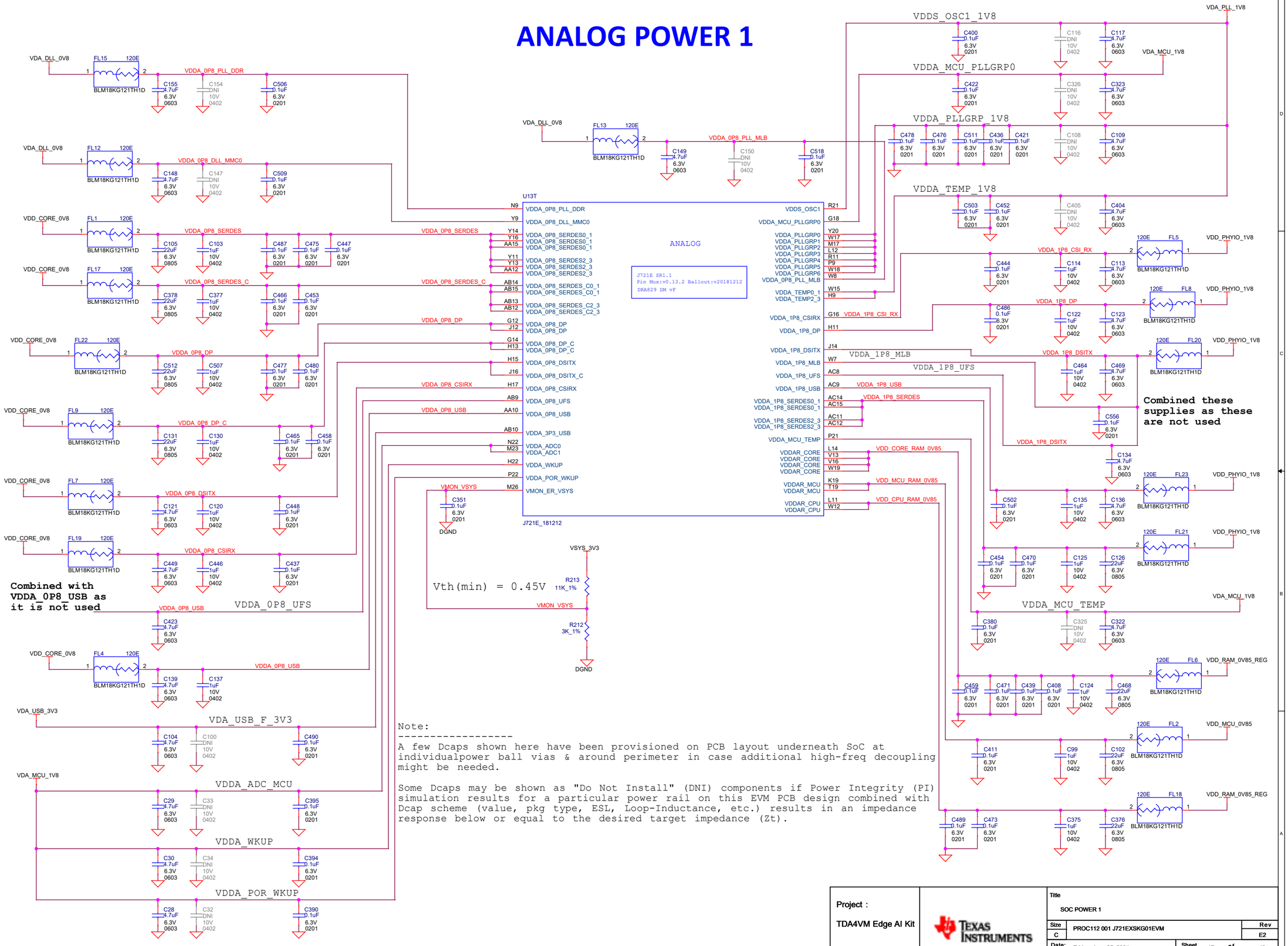
Size	PROC112 001 J721EXSKG01EVM	Rev
C		E2
Date: Wednesday, July 21, 2021	Sheet 15 of 48	

PRG0 & PRG1



Project : TDA4VM Edge AI Kit	TEXAS INSTRUMENTS	Title: PRG
	Size: C — PROC112 001 J721EXSKG01EVM	Rev: E2
	Date: Wednesday, July 21, 2021	Sheet 16 of 48

ANALOG POWER 1



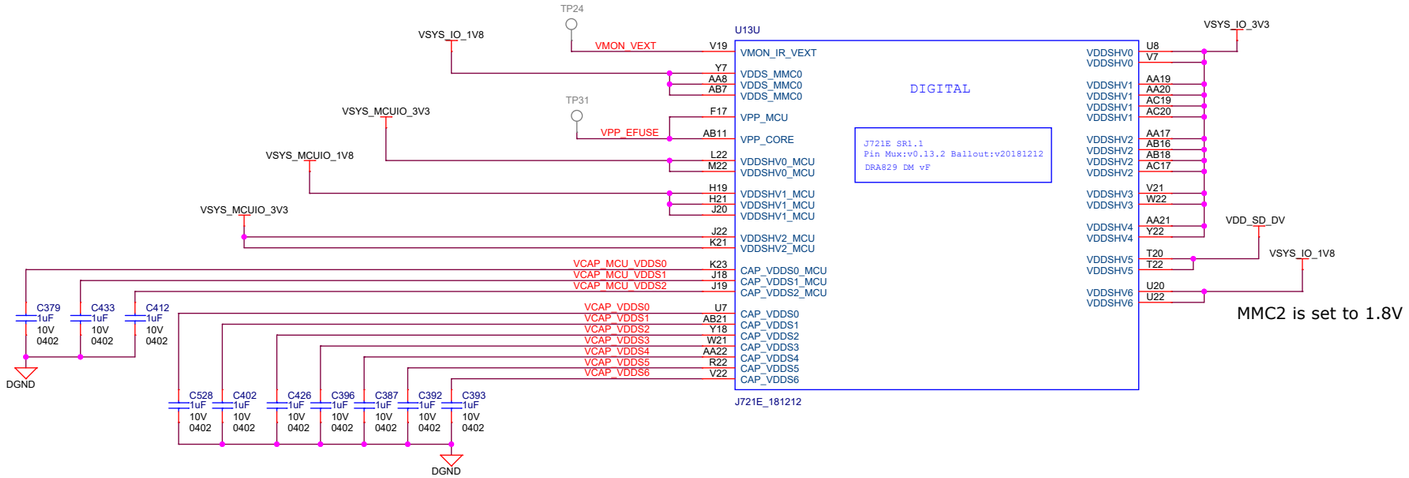
Note:

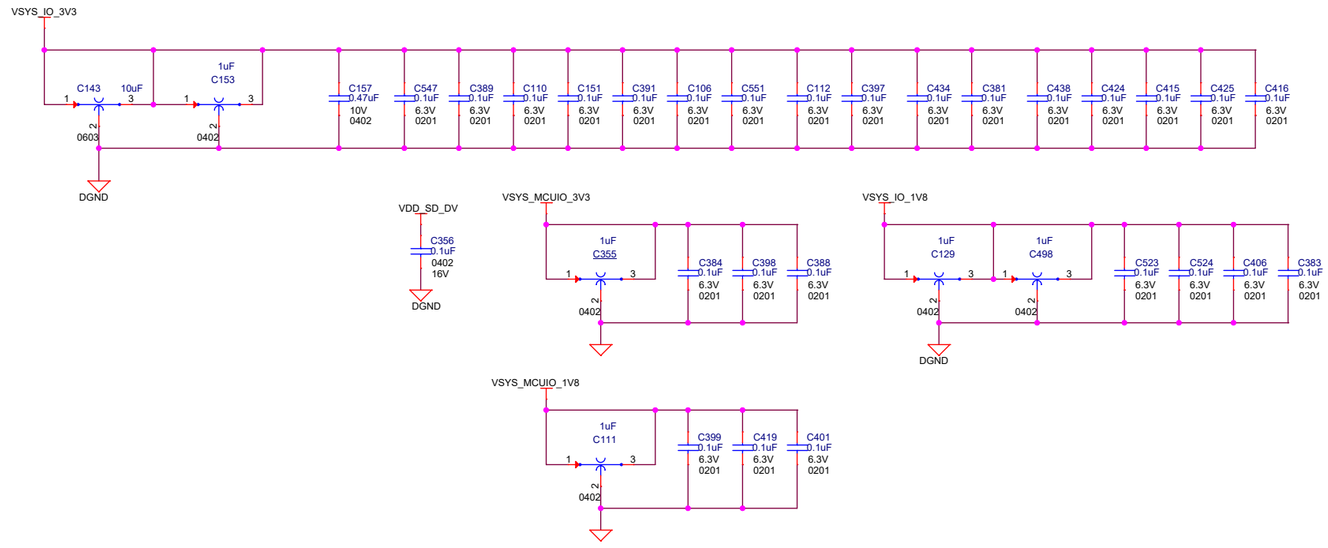
A few Dcaps shown here have been provisioned on PCB layout underneath SoC at individualpower ball vias & around perimeter in case additional high-freq decoupling might be needed.

Some Dcaps may be shown as "Do Not Install" (DNI) components if Power Integrity (PI) simulation results for a particular power rail on this EVM PCB design combined with Dcap scheme (value, pkg type, ESL, Loop-Inductance, etc.) results in an impedance response below or equal to the desired target impedance (Zt).

Project : TDA4VM Edge AI Kit		Title: SOC POWER 1	
		Size: C — PROC112 001 J721EXSKG01EVM	Rev: E2
		Date: Friday, June 25, 2021	Sheet 17 of 48

DIGITAL POWER 2





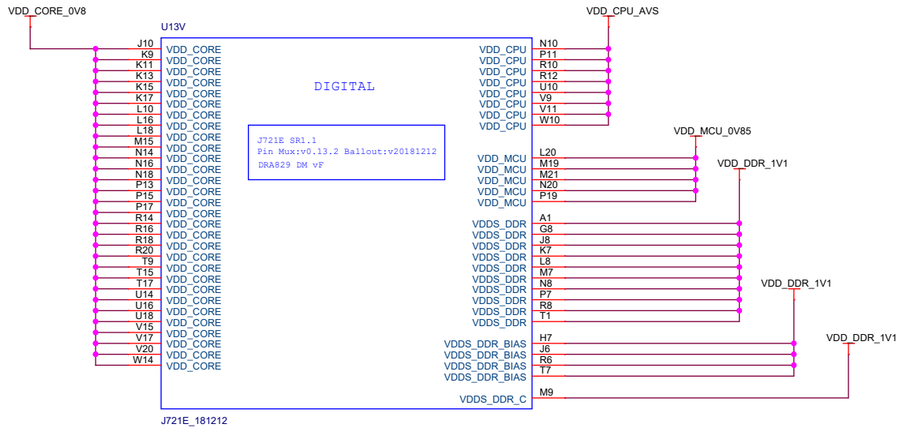
Note:

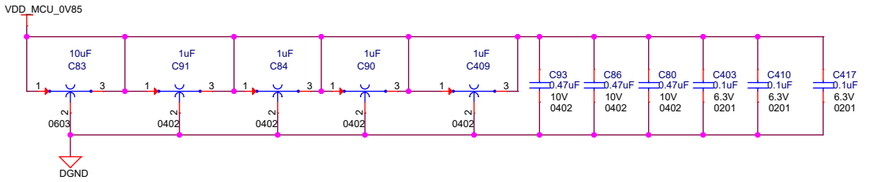
A few Dcaps shown here have been provisioned on PCB layout underneath SoC at individualpower ball vias & around perimeter in case additional high-freq decoupling might be needed.

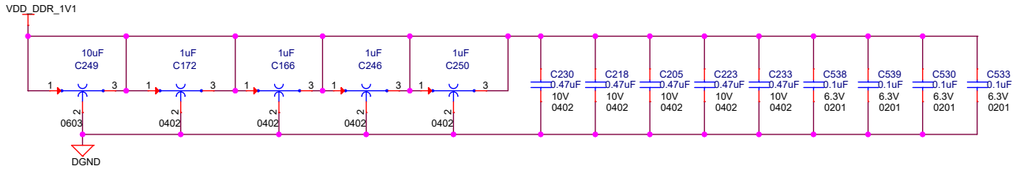
Some Dcaps may be shown as "Do Not Install" (DNI) components if Power Integrity (PI) simulation results for a particular power rail on this EVM PCB design combined with Dcap scheme (value, pkg type, ESL, Loop-Inductance, etc.) results in an impedance response below or equal to the desired target impedance (Zt).

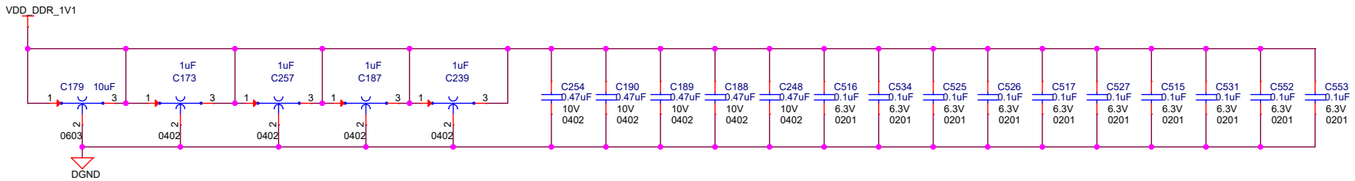
Project : TDA4VM Edge AI Kit	Texas Instruments	Title: SOC POWER 2
		Size: C — PROC112 001 J721EXSKG01EVM — Rev: E2
		Date: Wednesday, July 21, 2021 — Sheet 18 of 48

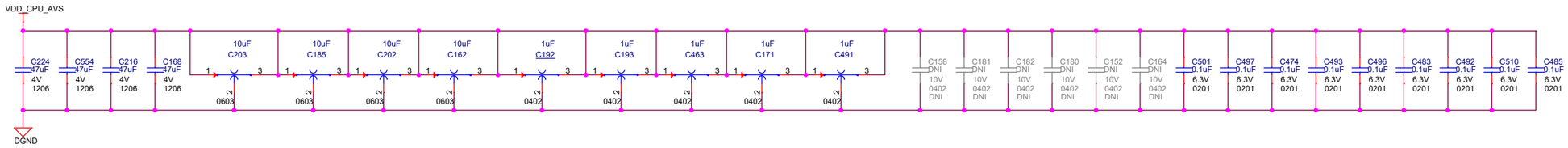
DIGITAL POWER 3

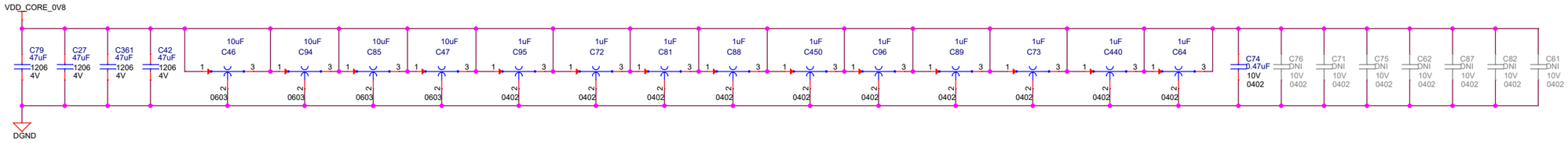


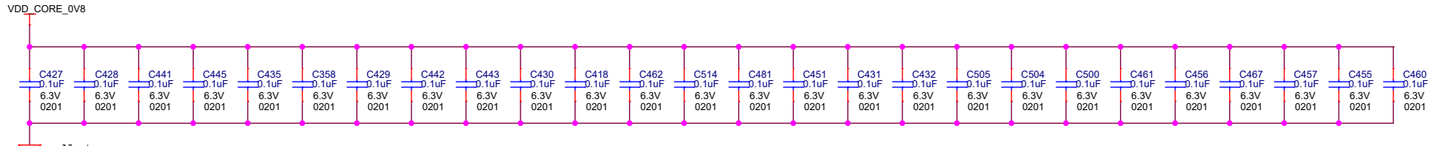












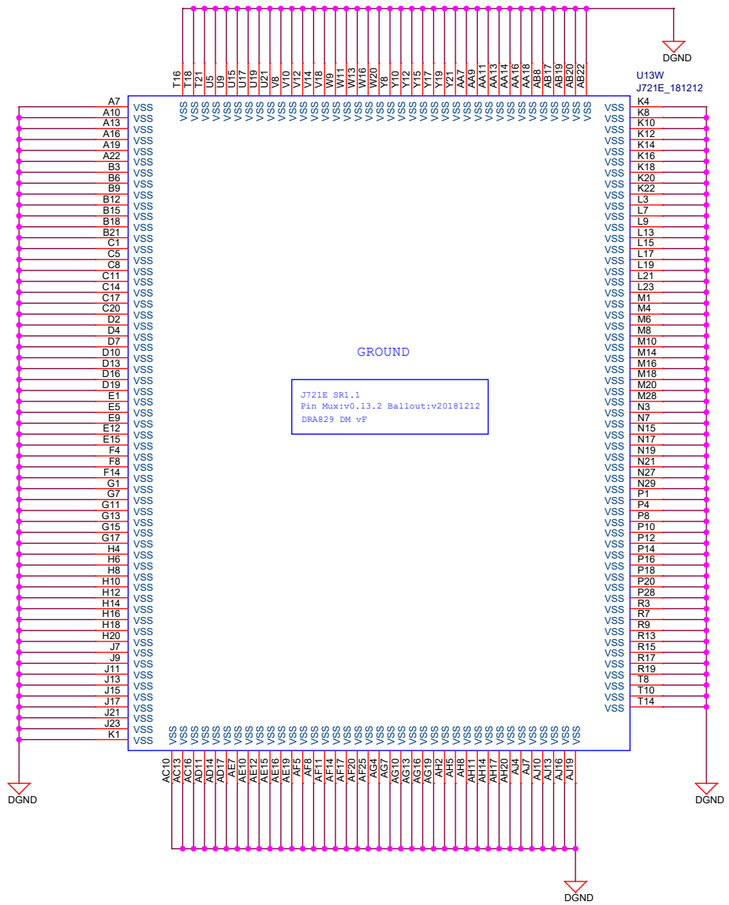
Note:

A few Dcaps shown here have been provisioned on PCB layout underneath SoC at individualpower ball vias & around perimeter in case additional high-freq decoupling might be needed.

Some Dcaps may be shown as "Do Not Install" (DNI) components if Power Integrity (PI) simulation results for a particular power rail on this EVM PCB design combined with Dcap scheme (value, pkg type, ESL, Loop-Inductance, etc.) results in an impedance response below or equal to the desired target impedance (Zt).

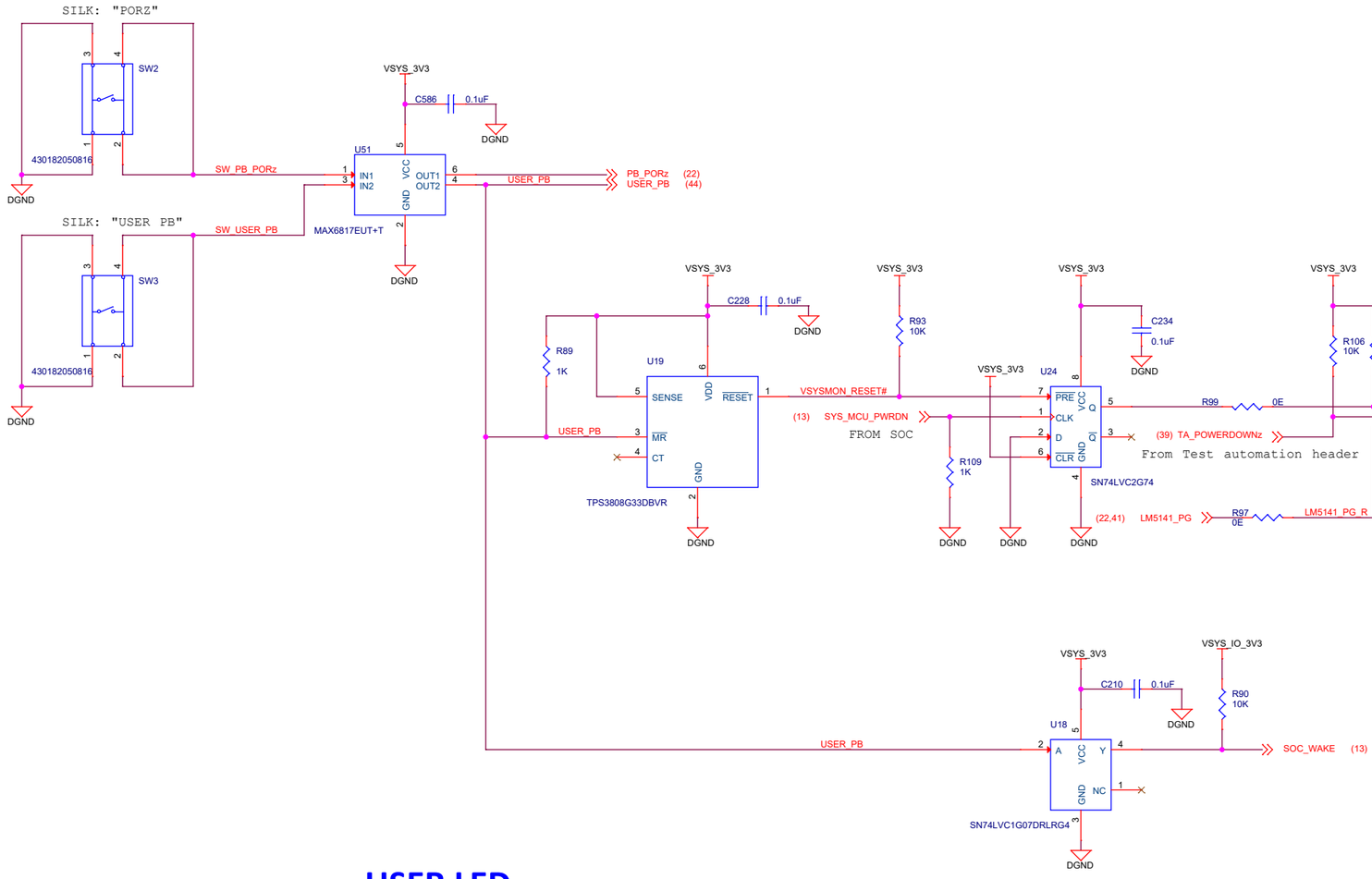
Project : TDA4VM Edge AI Kit	TEXAS INSTRUMENTS	Title: SOC POWER 3	
		Size: C — PROC112 001 J721EXSKG01EVM	Rev: E2
		Date: Friday, June 25, 2021	Sheet 19 of 48

SOC GROUND

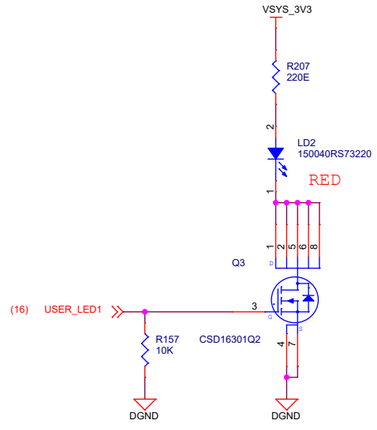


Project : TDA4VM Edge AI Kit	Texas Instruments	Title: SOC GROUND
	Size: C — PROC112 001 J721EXSKG01EVM	Rev: E2
	Date: Tuesday, June 22, 2021	Sheet 20 of 48

RESET BUTTONs



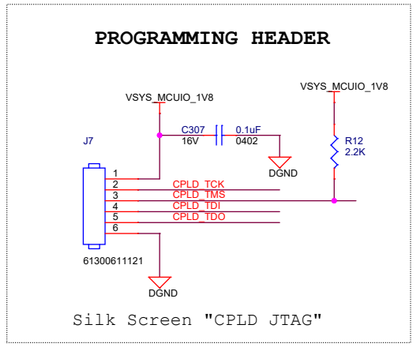
USER LED

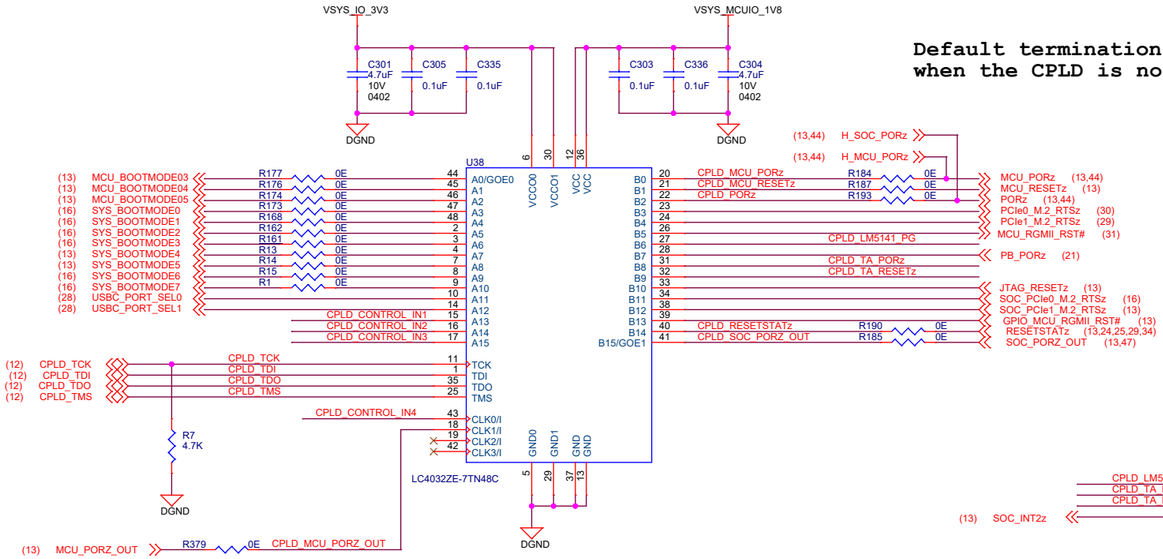


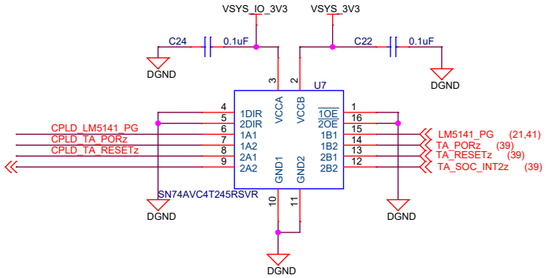
Project : TDA4VM Edge AI Kit	TEXAS INSTRUMENTS	Title: RESET BUTTONs
		Size: C — PROC112 001 J721EXSKG01EVM — Rev: E2
		Date: Wednesday, July 21, 2021 — Sheet 21 of 48

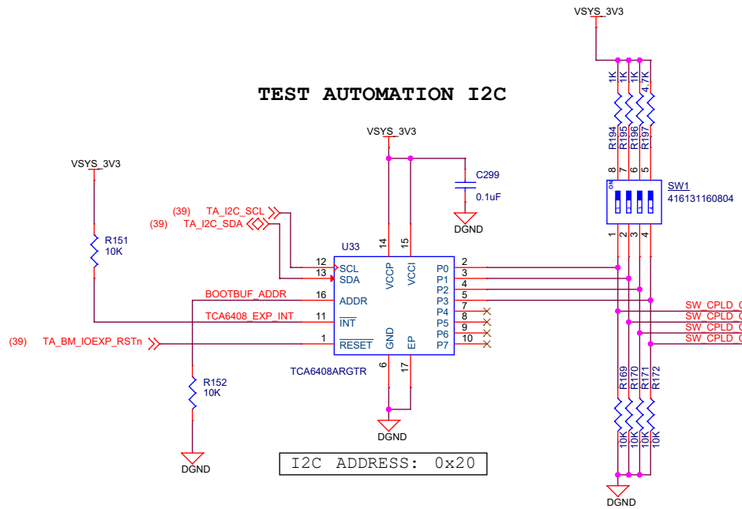
CPLD

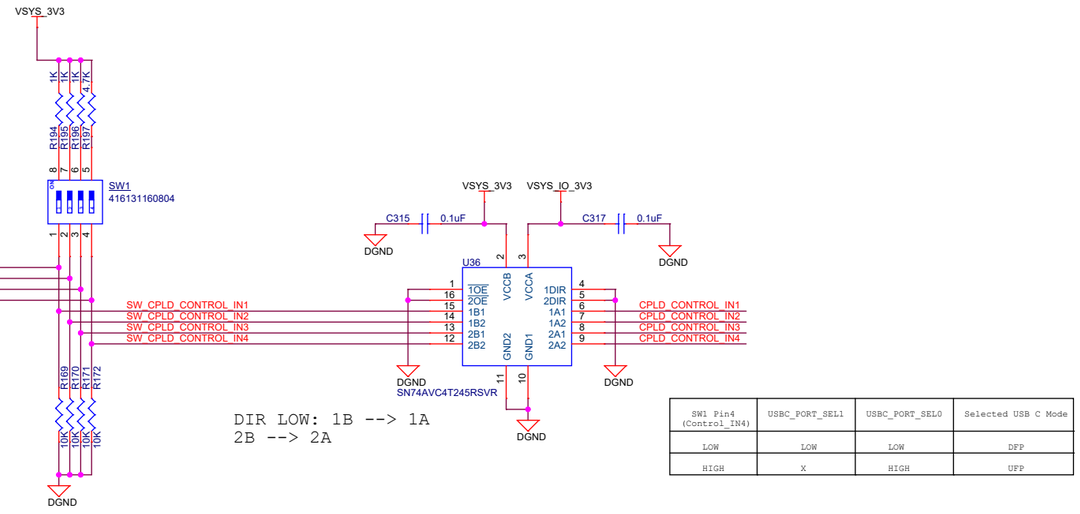
Default termination on IOs is Pull down, when the CPLD is not programmed.











DIR LOW: 1B --> 1A
2B --> 2A

Bootmode Table

SW1.3	SW1.2	SW1.1	BOOTMODE
0	0	0	SD
0	0	1	NO Boot
0	1	0	USB - 0 (DFU)
0	1	1	USB - 1 (DFU)
1	0	0	xSPI - 1S
1	0	1	UART
1	1	0	PCIe
1	1	1	xSPI SFDP

SW1 Pin4 (Control_IN4)	USBC_PORT_SEL1	USBC_PORT_SEL0	Selected USB C Mode
LOW	LOW	LOW	DFP
HIGH	X	HIGH	UFP

Project :
TDA4VM Edge AI Kit

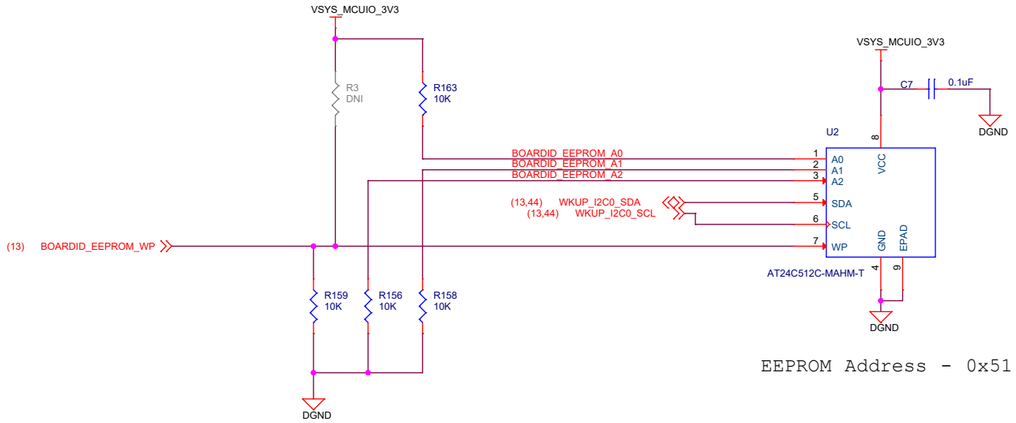
TEXAS INSTRUMENTS

Title: CPLD

Size		Rev
C	PROC112 001 J721EXSKG01EVM	E2

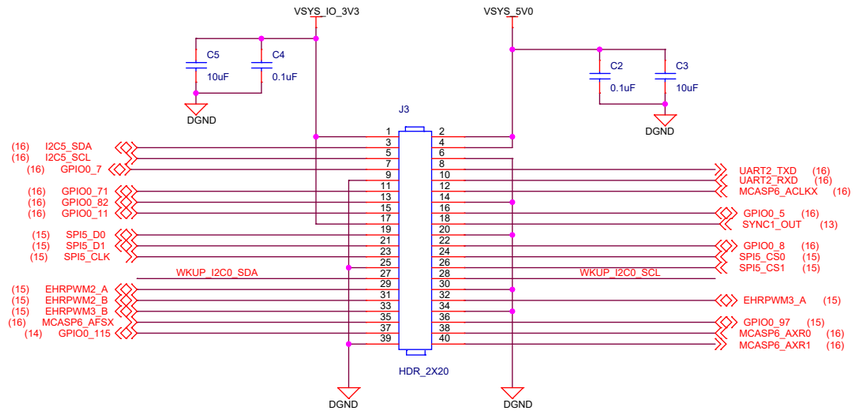
Date: Wednesday, July 21, 2021 | Sheet 22 of 48

BOARD ID EEPROM



EEPROM Address - 0x51

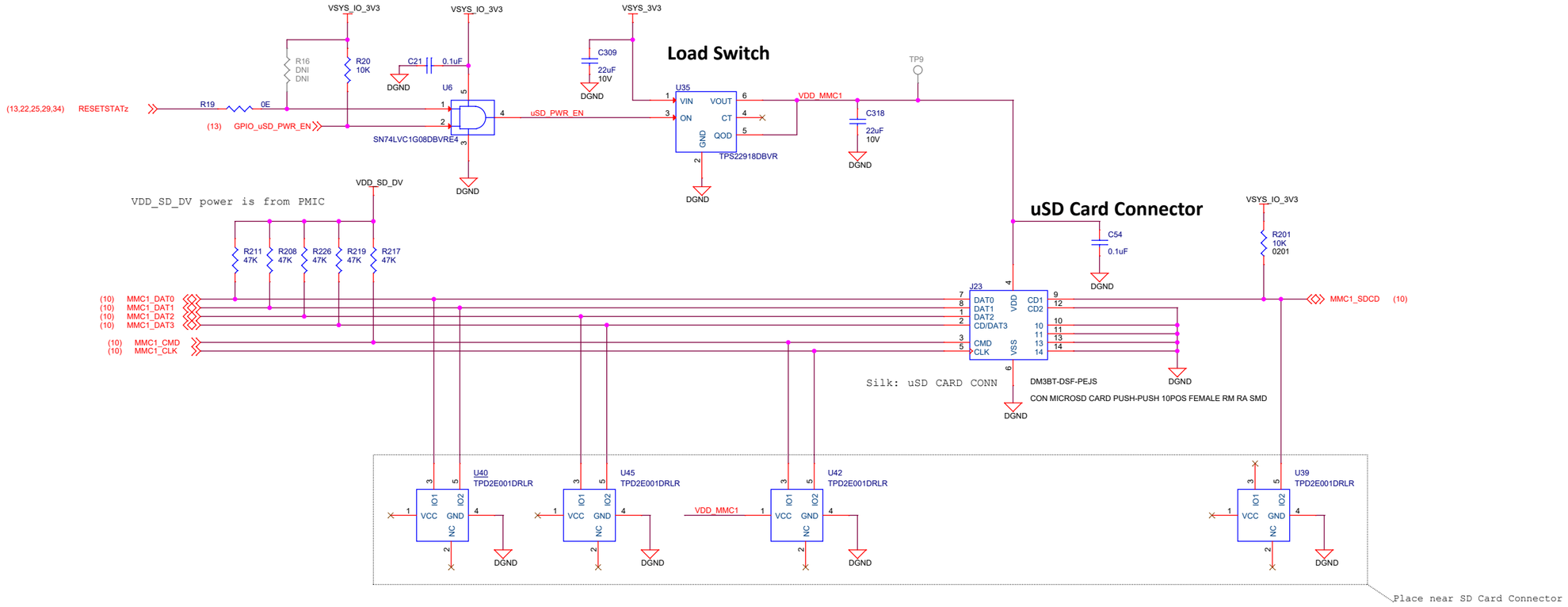
40Pin Expansion Header



Silk Screen "40p EXP HDR"

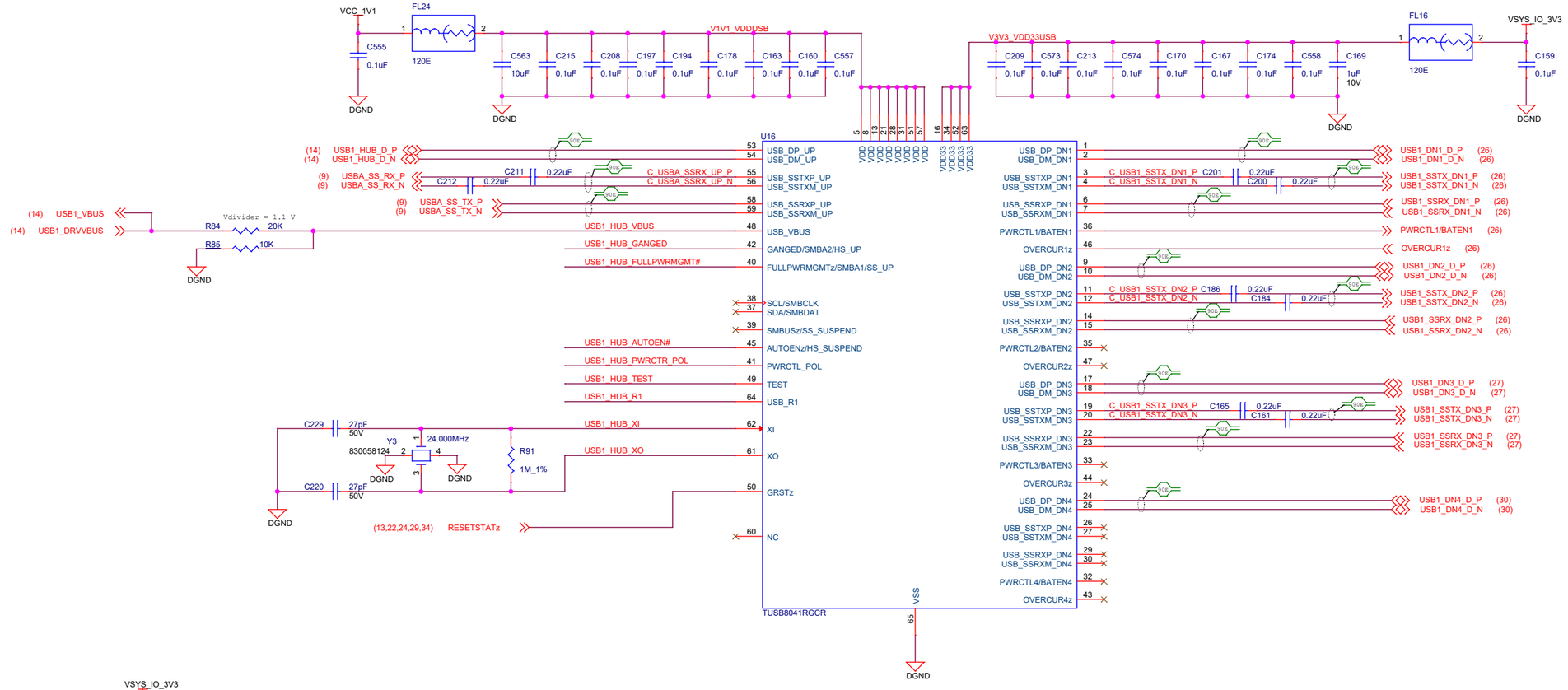
Project : TDA4VM Edge AI Kit	Texas Instruments	Title: Board ID EEPROM & 40 Pin EXP Header
		Size: C — PROC112 001 J721EXSKG01EVM — Rev: E2
		Date: Wednesday, July 21, 2021 — Sheet 23 of 48

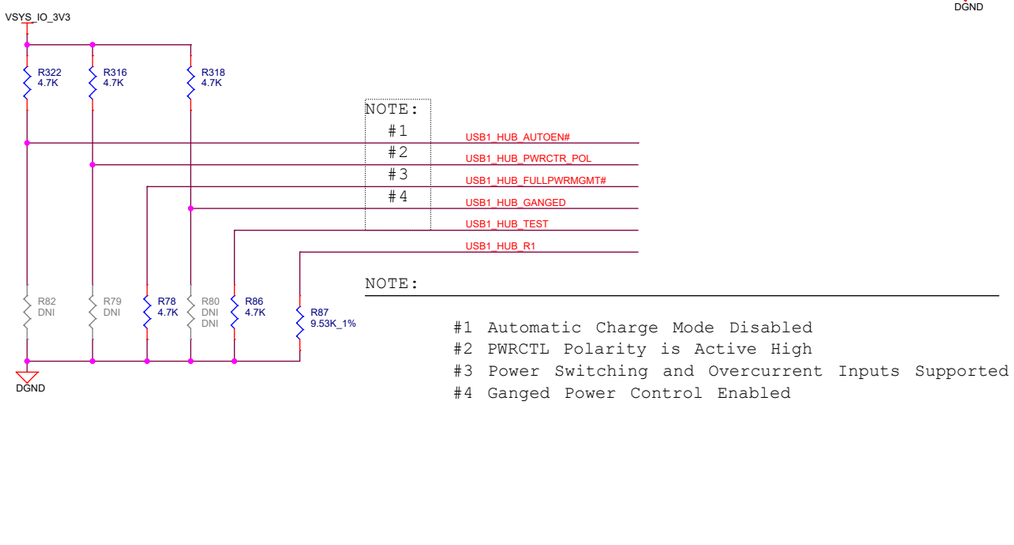
Micro SD CARD INTERFACE



Project : TDA4VM Edge AI Kit	Texas Instruments	Title: Micro SD CARD INTERFACE
		Size: C — PROC112 001 J721EXSKG01EVM — Rev: E2
		Date: Tuesday, July 20, 2021 — Sheet 24 of 48

USB3.0 HUB



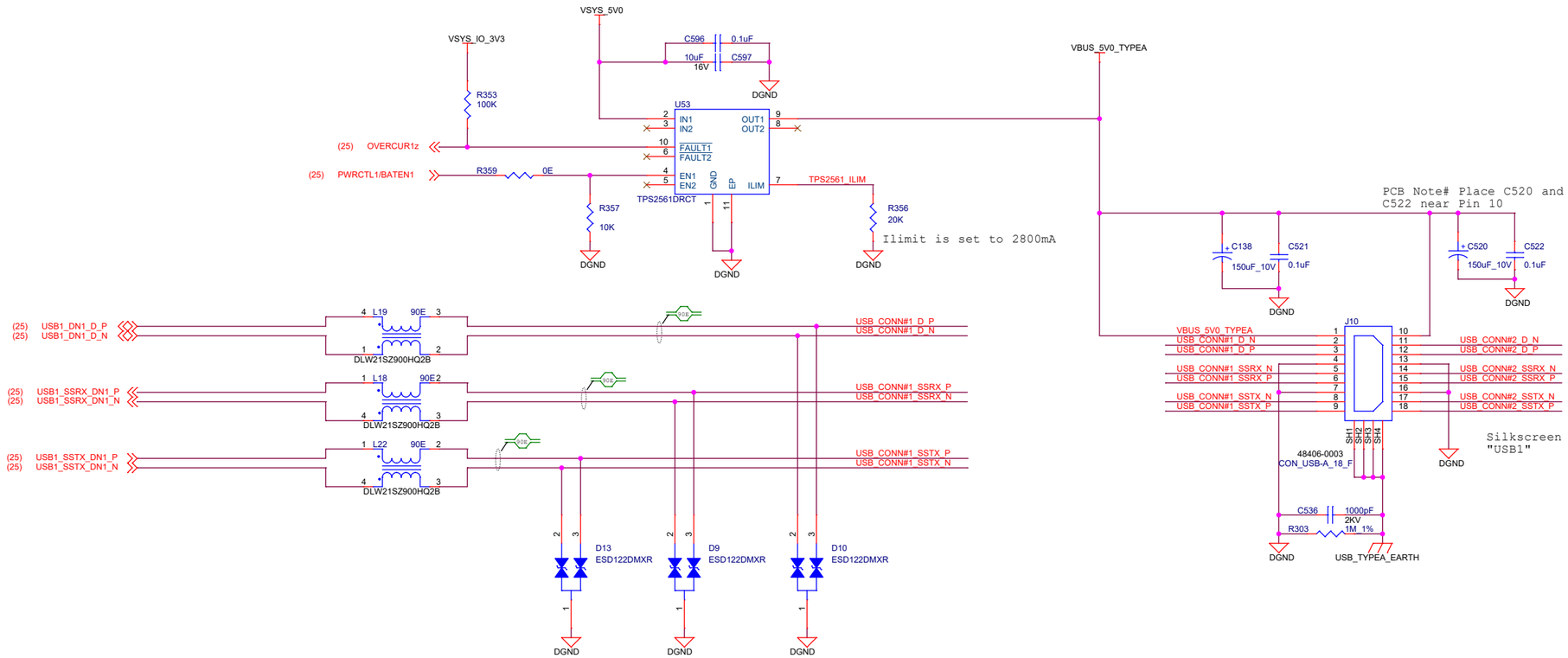


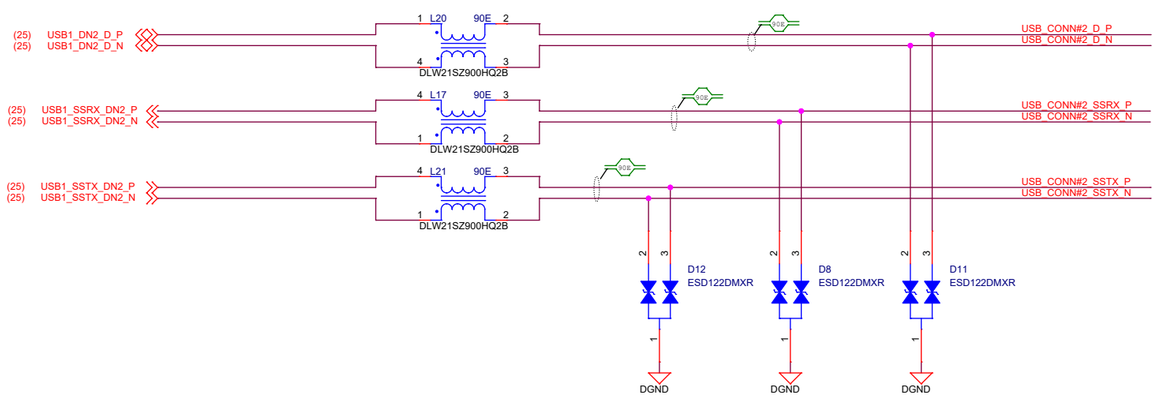
NOTE:

#1 Automatic Charge Mode Disabled
#2 PWRCTL Polarity is Active High
#3 Power Switching and Overcurrent Inputs Supported
#4 Ganged Power Control Enabled

Project : TDA4VM Edge AI Kit	TEXAS INSTRUMENTS	Title: USB3.0 HUB
		Size: C — PROC112 001 J721EXSKG01EVM — Rev: E2
		Date: Wednesday, July 21, 2021 — Sheet 25 of 48

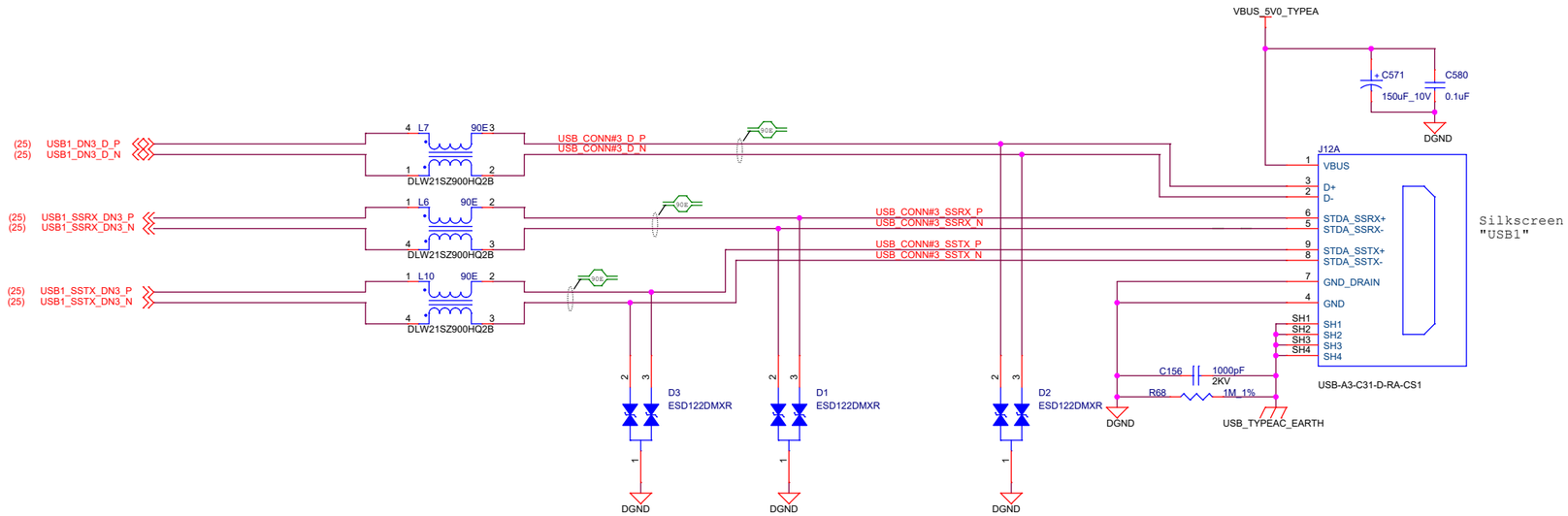
USB 3.0 TYPE-A CONNECTORS - 1





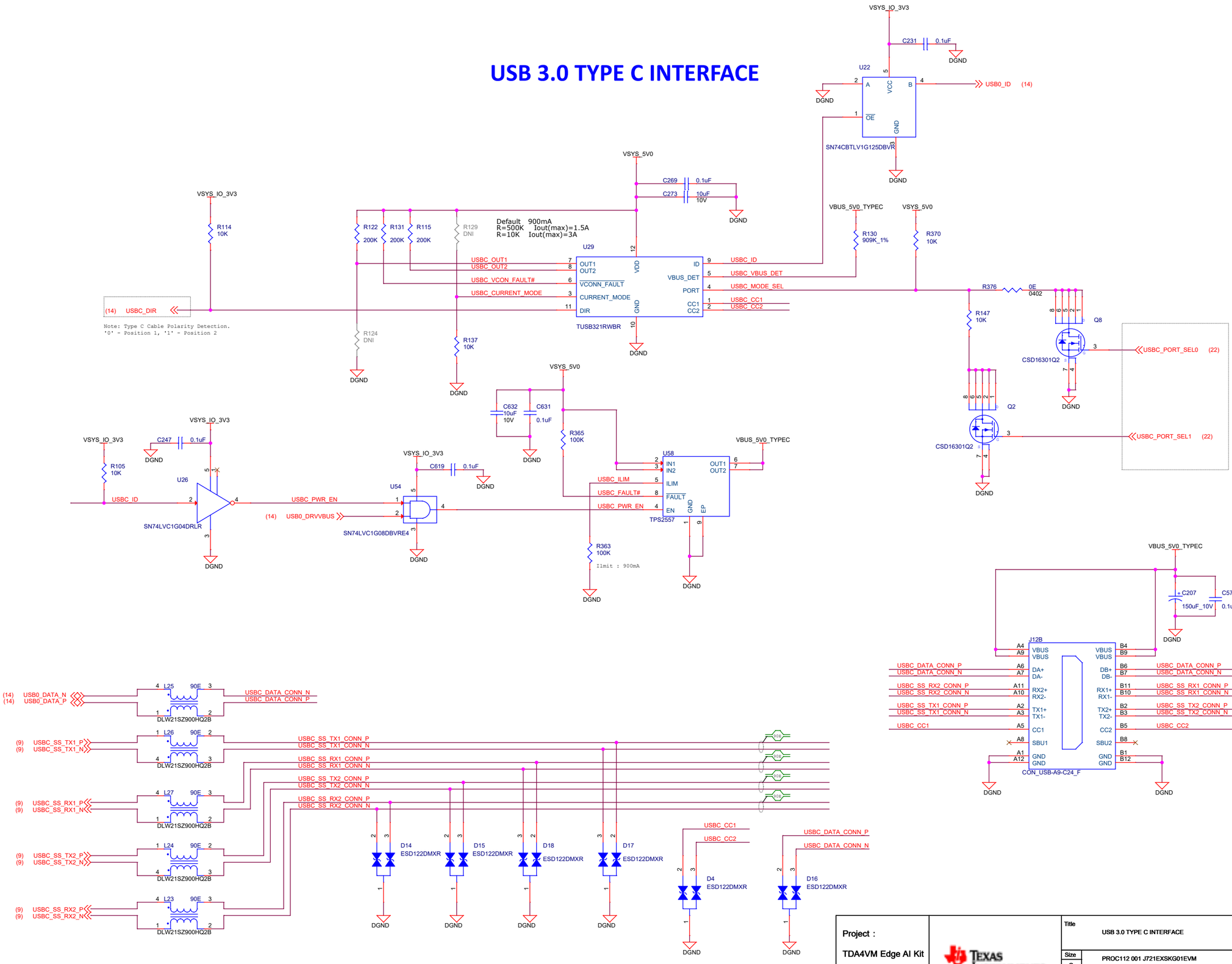
Project : TDA4VM Edge AI Kit	TEXAS INSTRUMENTS	Title: USB 3.0 TYPE-A CONNECTORS - 1
		Size: C — PROC112 001 J721EXSKG01EVM — Rev: E2
		Date: Wednesday, July 21, 2021 — Sheet 26 of 48

USB 3.0 TYPE-A CONNECTORS - 2



Project : TDA4VM Edge AI Kit		Title: USB 3.0 TYPE-A CONNECTORS - 2
		Size: C — PROC112 001 J721EXSKG01EVM — Rev: E2
		Date: Wednesday, July 21, 2021 — Sheet 27 of 48

USB 3.0 TYPE C INTERFACE

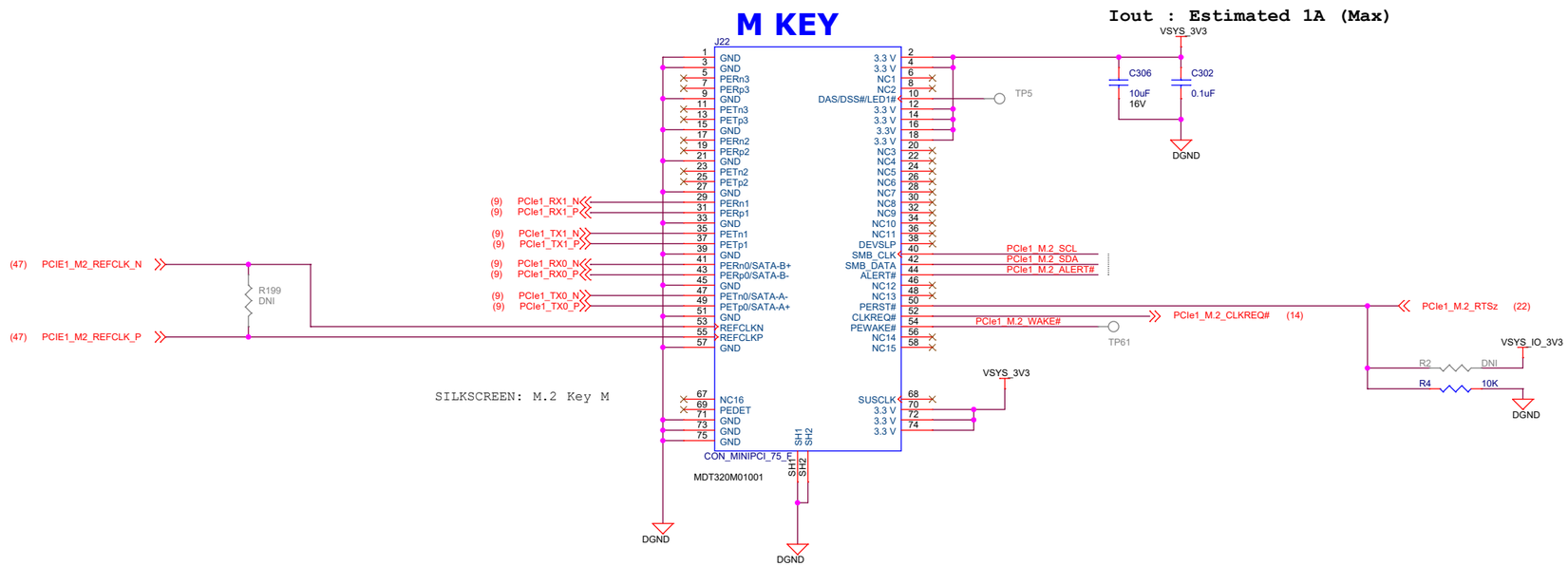


Project : TDA4VM Edge AI Kit	TEXAS INSTRUMENTS	Title: USB 3.0 TYPE C INTERFACE	
		Size: C	PROC112 001 J721EXSKG01EVM — Rev: E2
		Date: Tuesday, June 22, 2021	Sheet 28 of 48

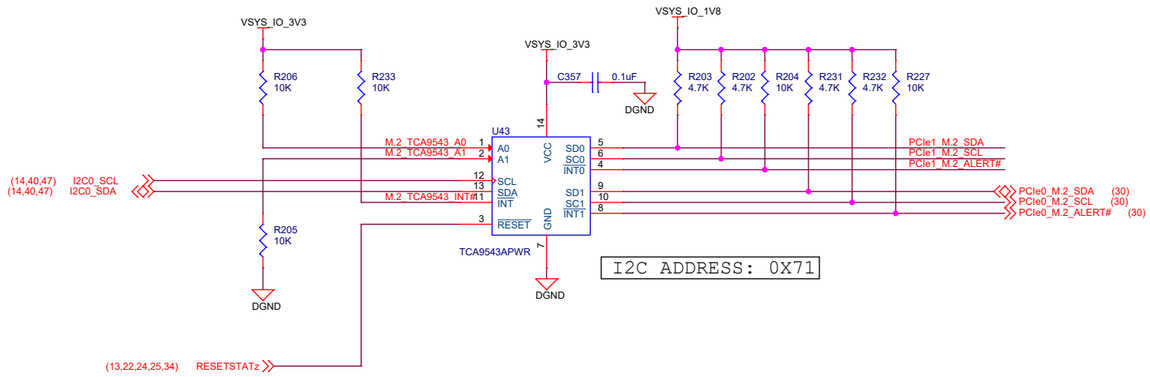
PCIe_M.2_INTERFACE SSD

M KEY

Iout : Estimated 1A (Max)



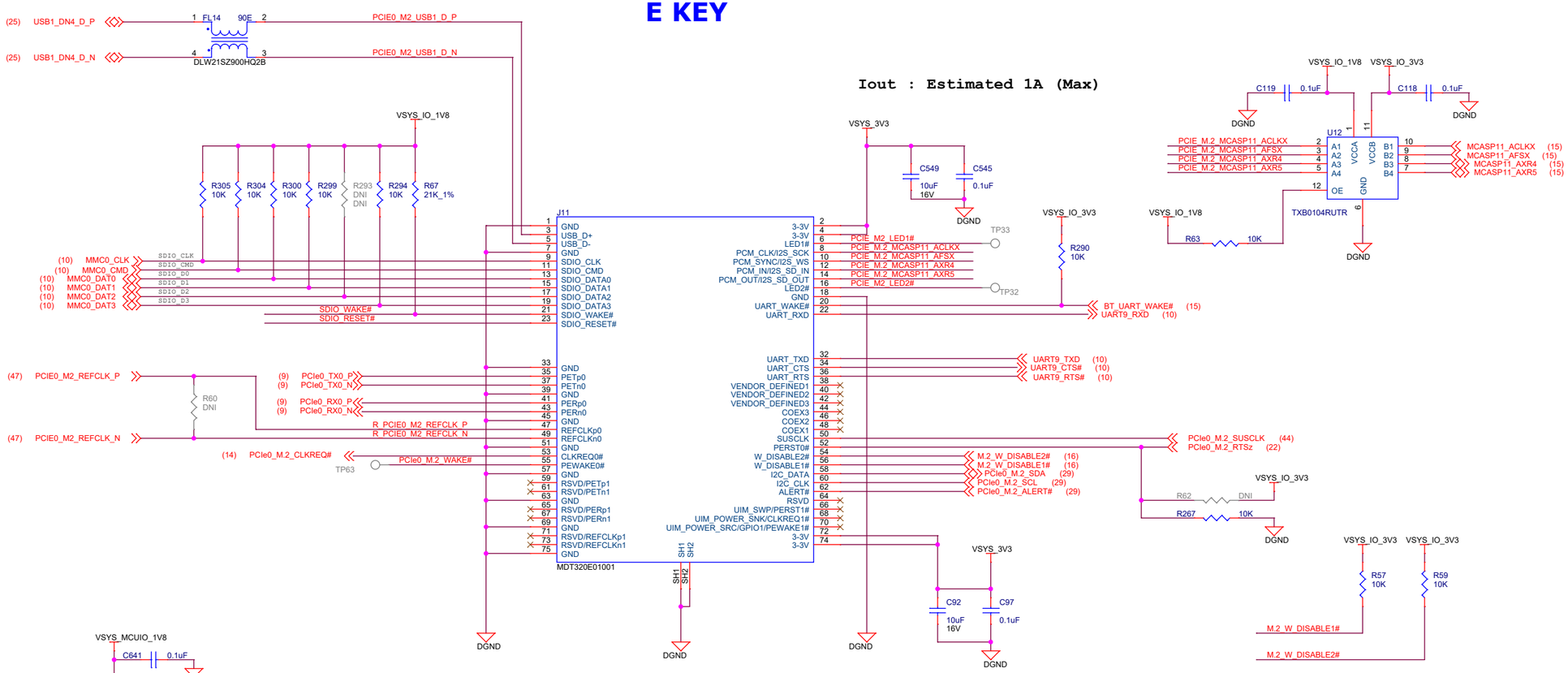
3.3V To 1V8 Level translator

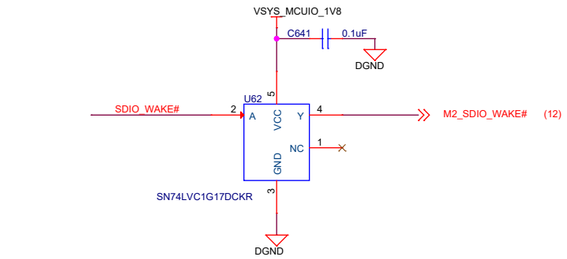


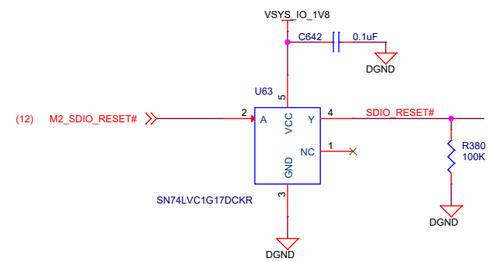
Project : TDA4VM Edge AI Kit	Texas Instruments	Title: PCIe_M.2_INTERFACE(M Key)
		Size: C — PROC112 001 J721EXSKG01EVM — Rev: E2
		Date: Tuesday, June 22, 2021 — Sheet 29 of 48

PCIe_M.2_INTERFACE - SDIO

E KEY



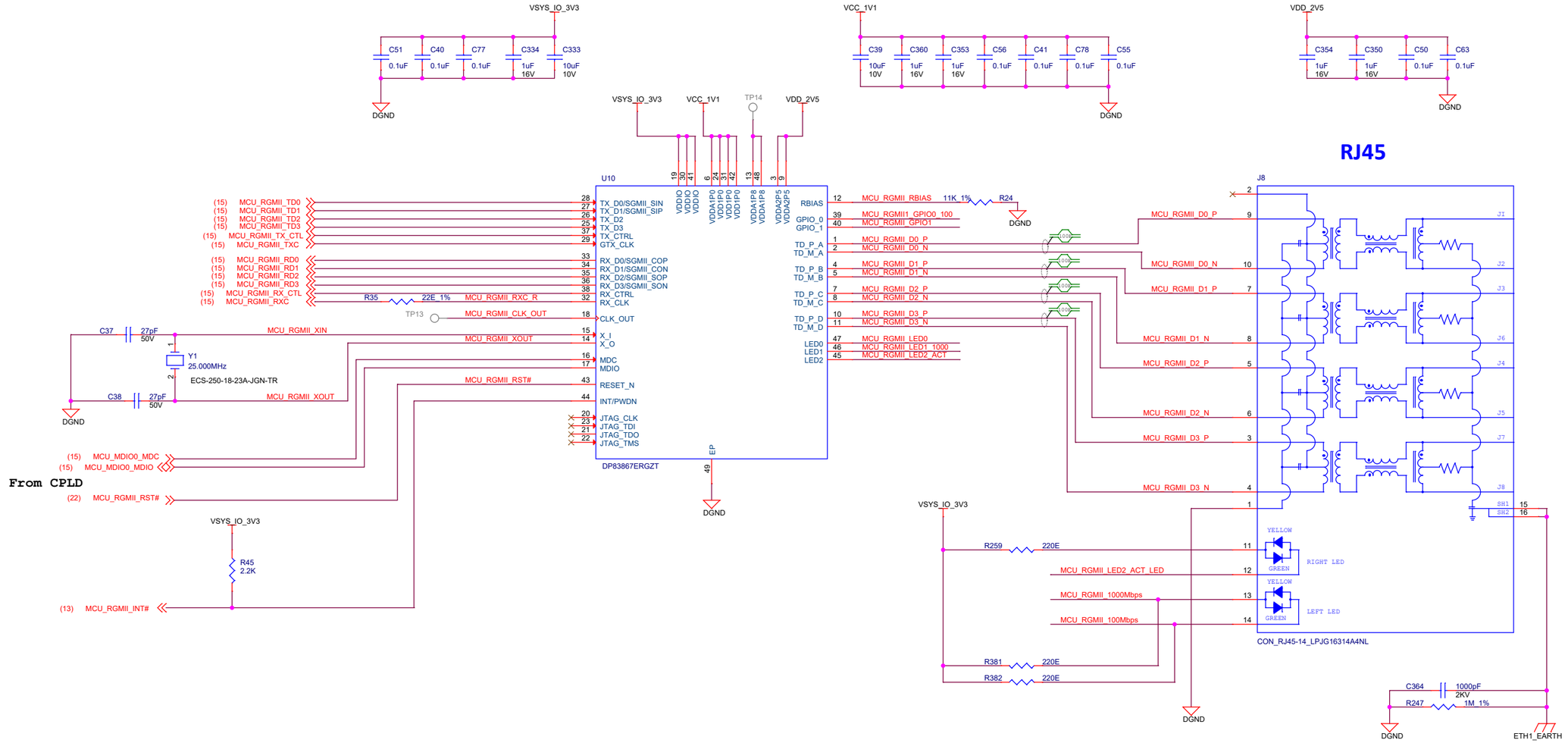




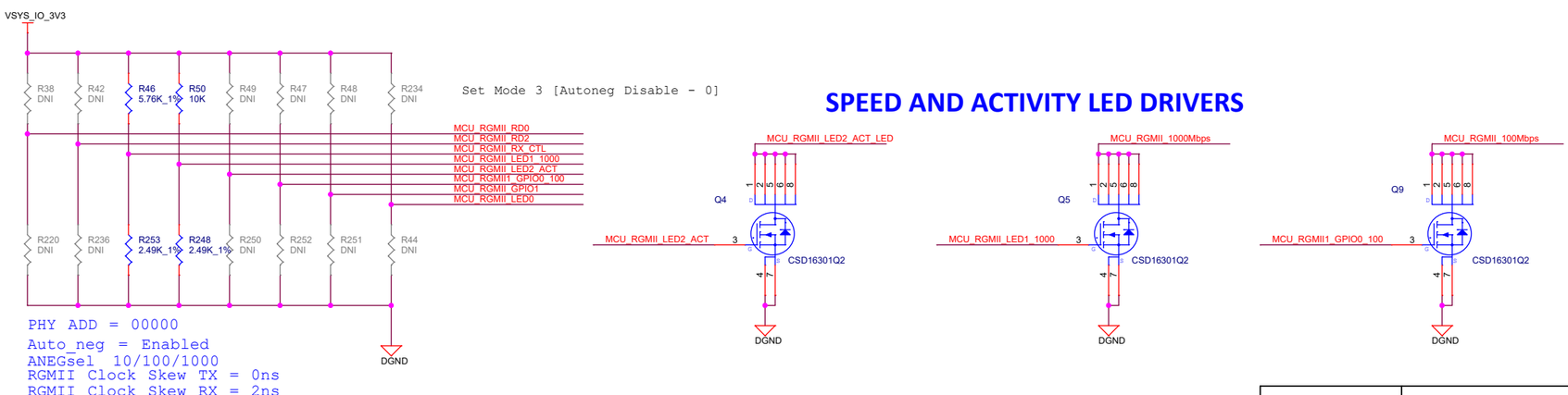
SILKSCREEN: M.2 Key E

Project : TDA4VM Edge AI Kit	Texas Instruments	Title: PCIe_M.2_INTERFACE(E Key)	
		Size: C	PROC112 001 J721EXSKG01EVM — Rev: E2
		Date: Friday, June 25, 2021	Sheet 30 of 48

MCU GB ETHERNET



SPEED AND ACTIVITY LED DRIVERS



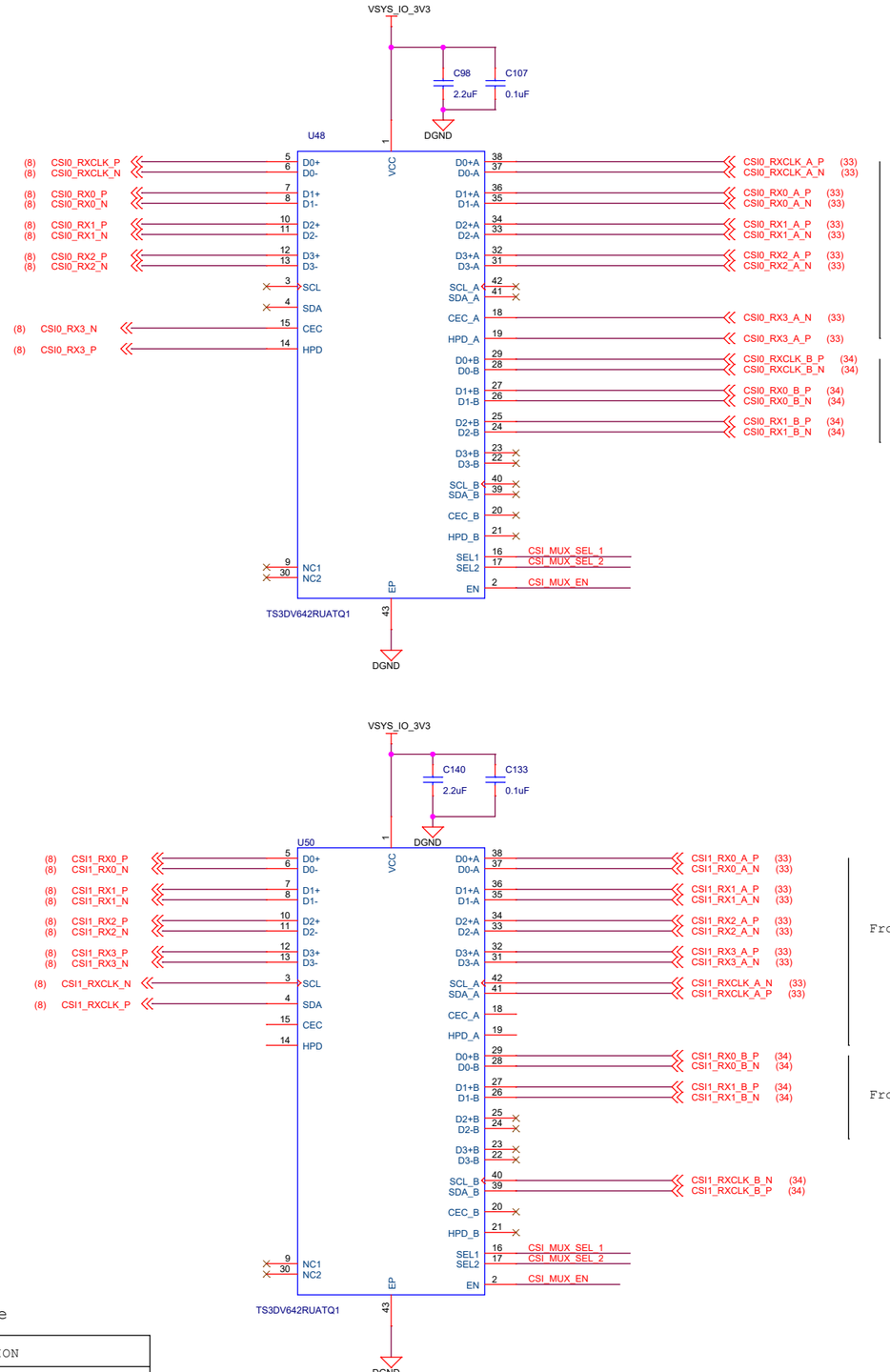
RJ45-LED	FUNCTION
RIGHT - GREEN	ACTIVITY
LEFT - GREEN	1000Mbps Speed
LEFT - YELLOW	100Mbps Speed

LED_2-MODE1 & LED_1-MODE2-TX SKEW=0nS
GPIO0-MODE1 & GPIO1-MODE1-RX SKEW=2nS

Project :
TDA4VM Edge AI Kit

Title: MCU GB ETHERNET
Size: C | PROC112 001 J721EXSKG01EVM | Rev: E2
Date: Wednesday, July 21, 2021 | Sheet 31 of 48

CSI MUX - DATA



CSI - 1:2 MUX : Truth Table

MUX_SEL_2	FUNCTION
LOW	INPUT<--A port [CSI2 Connector]
HIGH	INPUT<--B port [FPC Camera Connector]

(default)

Project :

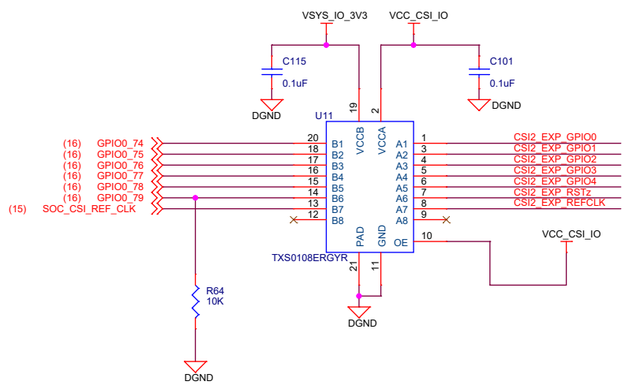
TDA4VM Edge AI Kit

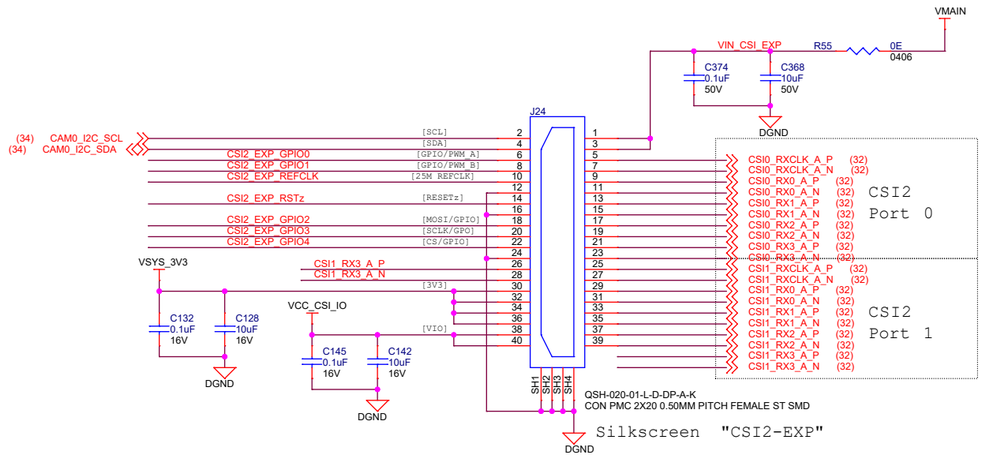
Texas Instruments

Title: CSI MUX - DATA

Size		Rev
C	PROC112 001 J721EXSKG01EVM	E2
Date: Tuesday, July 20, 2021	Sheet 32 of 48	

CSI2 EXPANSION CONNECTOR

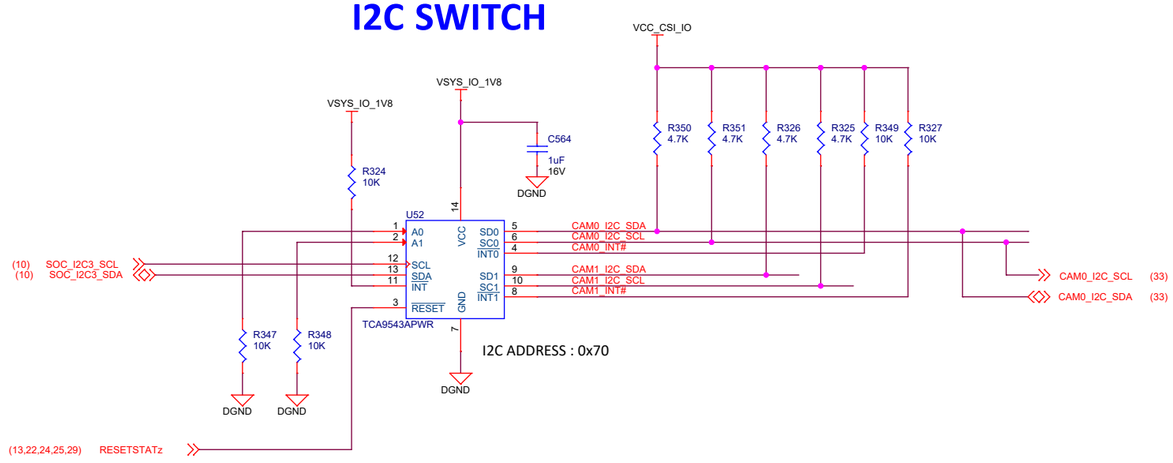




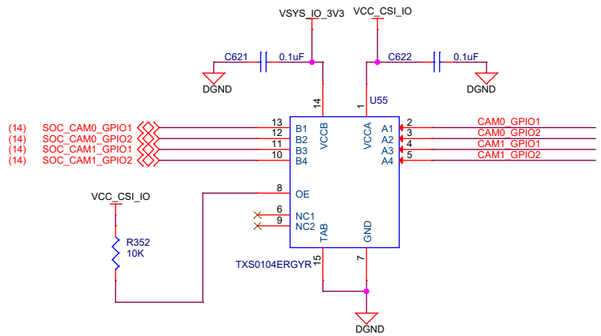
Project : TDA4VM Edge AI Kit		Title: CSI2 EXPANSION CONNECTOR
		Size: C — PROC112 001 J721EXSKG01EVM — Rev: E2
		Date: Wednesday, July 21, 2021 — Sheet 33 of 48

CSI FPC CAMERA CONNECTORS

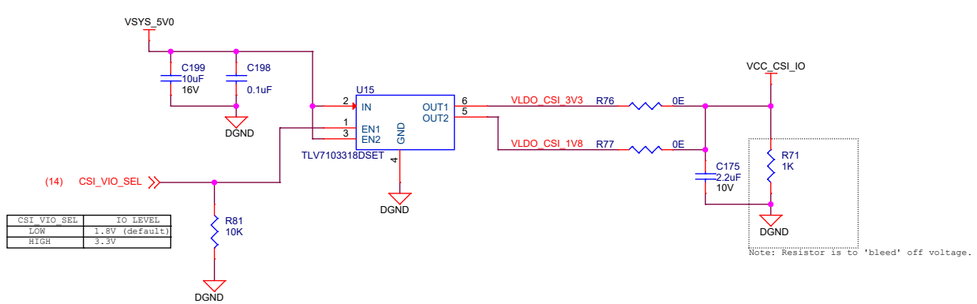
I2C SWITCH



GPIO LEVEL TRANSLATOR



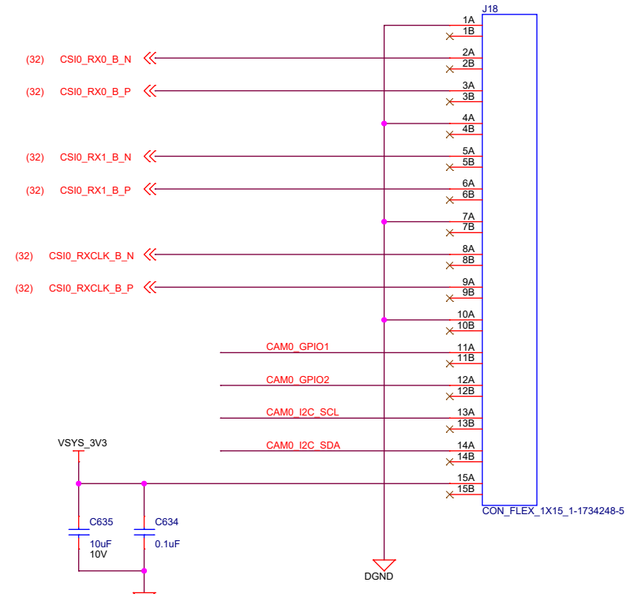
CAMERA IO SUPPLY



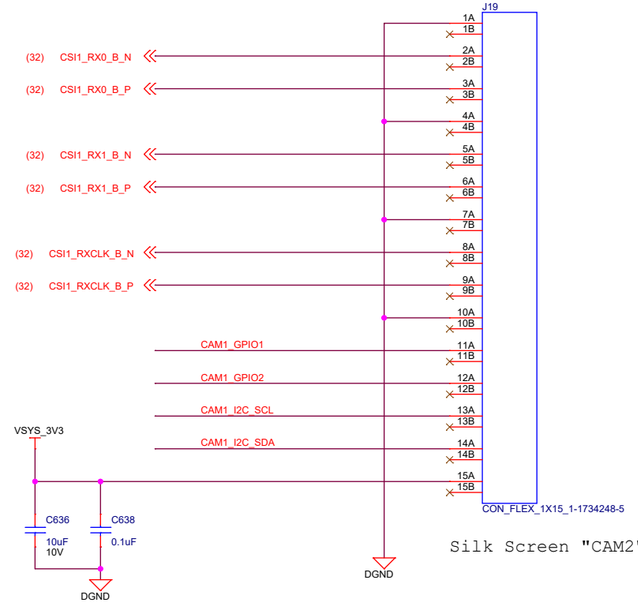
CSI_VIO_SEL	IO LEVEL
LOW	1.8V (default)
HIGH	3.3V

Silk Screen "CAM1"

FPC Camera Connector -1



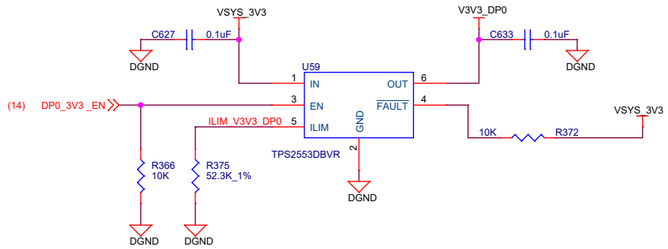
FPC Camera Connector -2

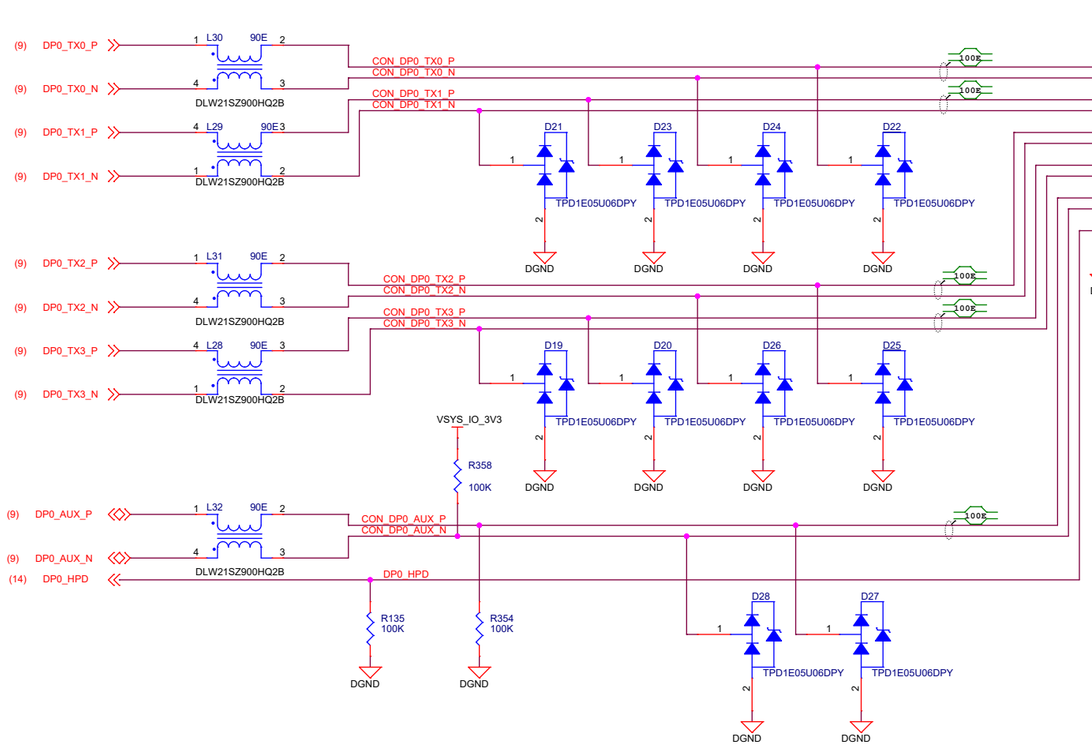


Silk Screen "CAM2"

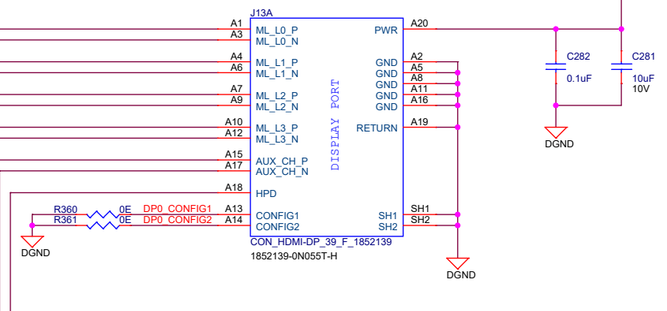
Project : TDA4VM Edge AI Kit		Title	CSI FPC CAMERA CONNECTORS
		Size: C	PROC112 001 J721EXSKG01EVM
		Rev	E2
		Date: Wednesday, July 21, 2021	Sheet 34 of 48

DISPLAY PORT INTERFACE





Display Port Connector

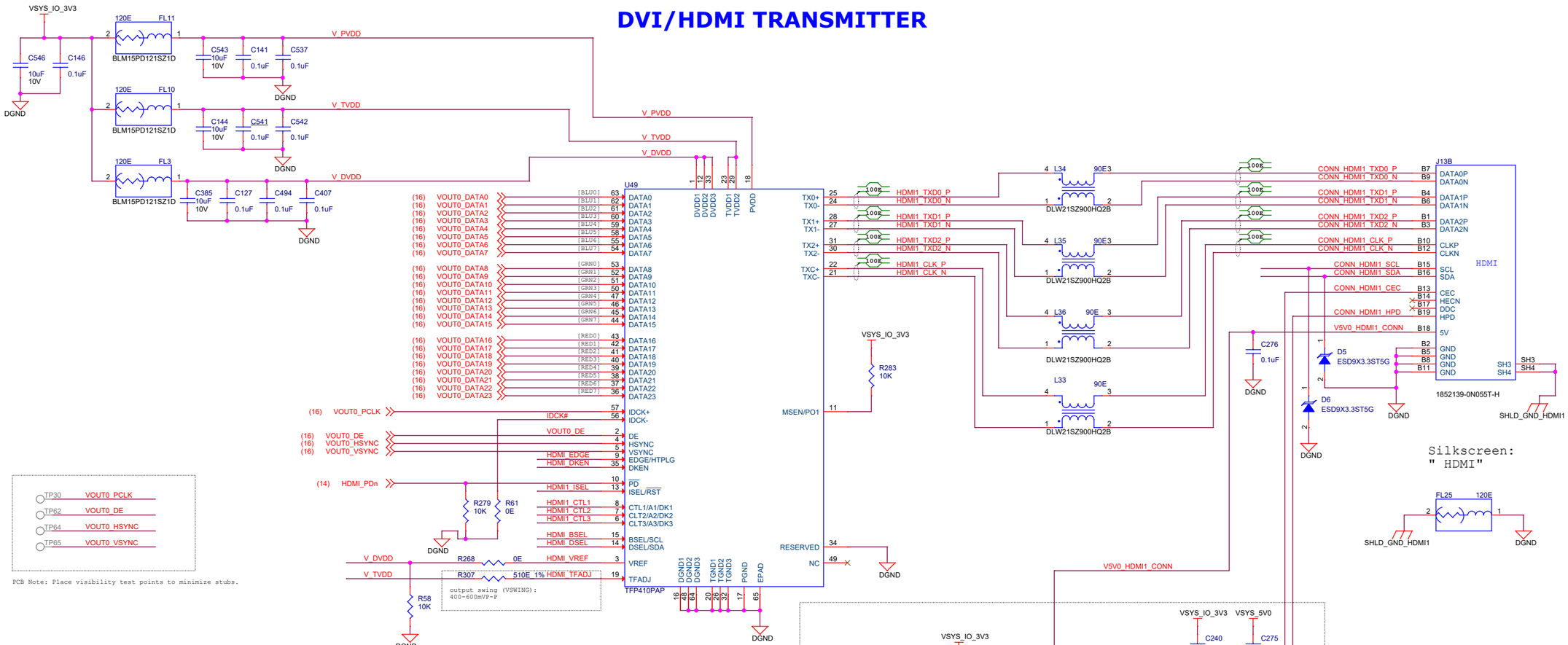


Silkscreen: "DISPLAY PORT+ HDMI"

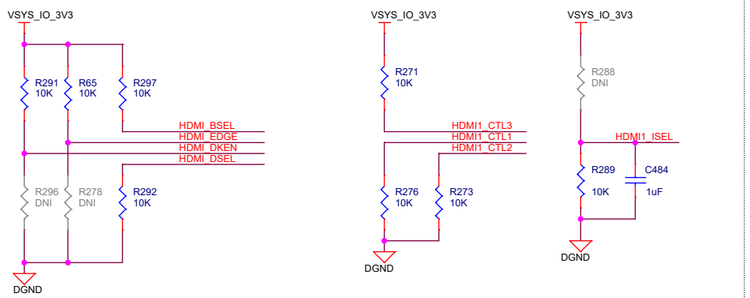
PCB Note: Place the ESD diodes close to DISPLAY PORT CONN

Project : TDA4VM Edge AI Kit	Texas Instruments	Title: DISPLAY_PORT_INTERFACE	
		Size: C	PROC112 001 J721EXSKG01EVM — Rev: E2
		Date: Wednesday, July 21, 2021	Sheet 35 of 48

DVI/HDMI TRANSMITTER



DVI Configuration Settings

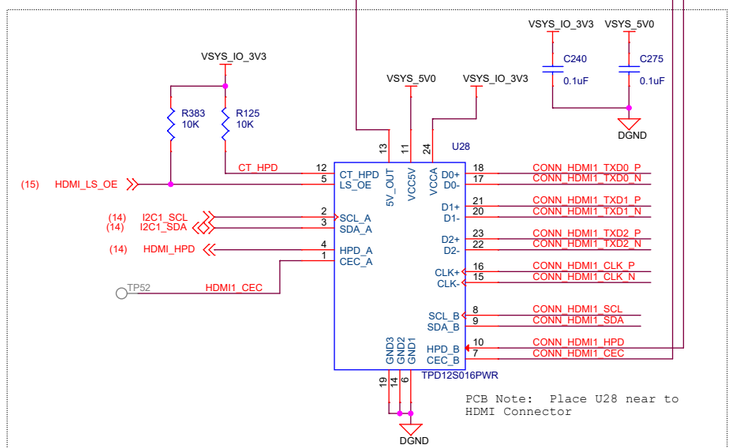


VREF	BSEL	EDGE	DSEL	BUS WIDTH	LATCH MODE	CLOCK MODE	CLOCK EDGE
0.55V-0.9V	1	0	0	24-bit	Single-ended	Falling	Single-ended
Default	1	1	0	24-bit	Single-ended	Raising	Single-ended

ISEL:- Low (default): I2C interface is disabled and chip configuration is specified by BSEL, DSEL, EDGE, VREF pins

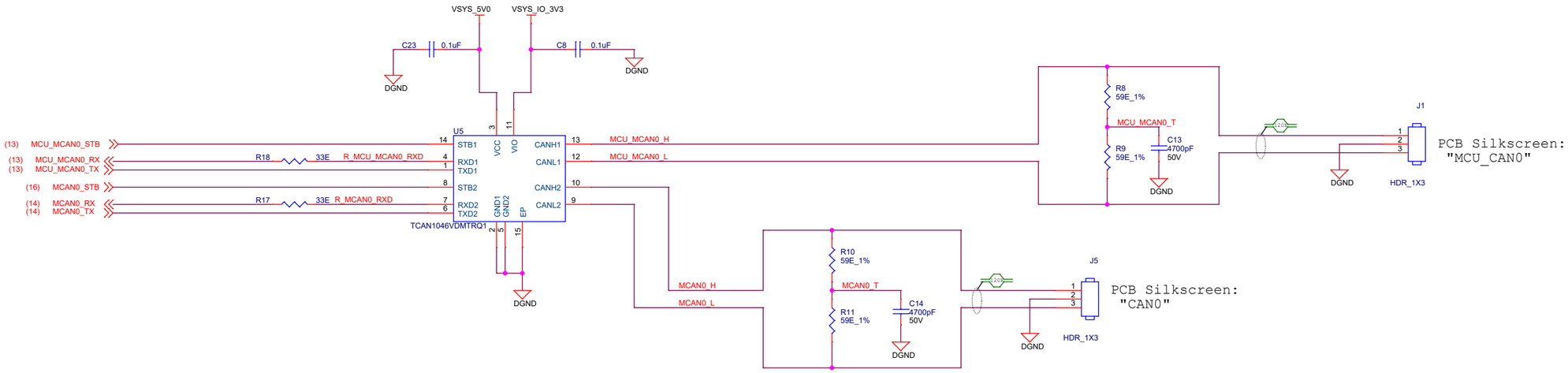
When ISEL: L, DSEL-H- enables de-skew function (default)

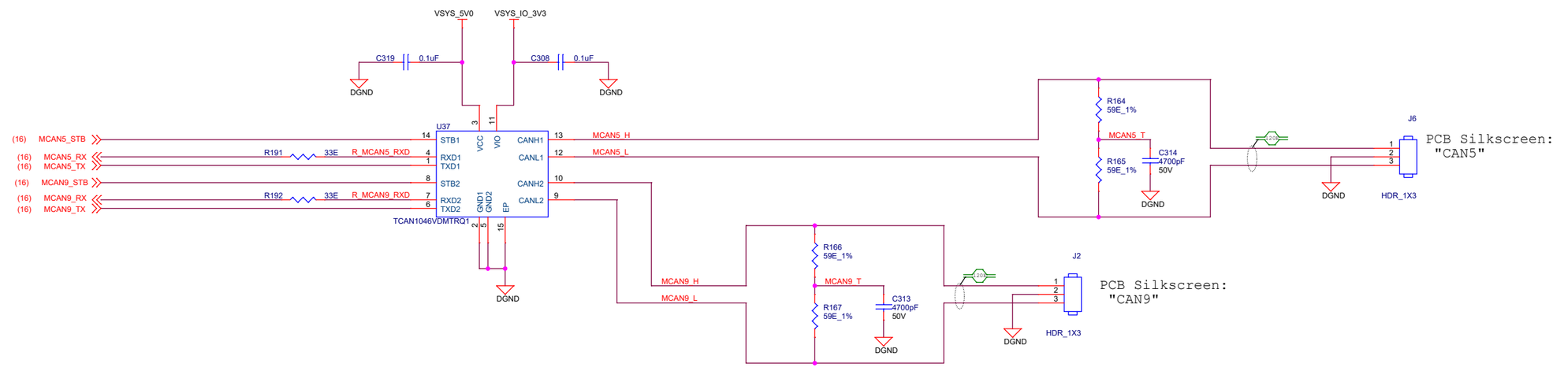
ESD Protection, Curent Limit Load switch



Project : TDA4VM Edge AI Kit		Title	HDMI BRIDGE
		Size C	PROC112 001 J721EXSKG01EVM — Rev E2
		Date: Wednesday, July 21, 2021	Sheet 36 of 48

CAN TRANSCEIVERS #2-MAIN DOMAIN





Project : TDA4VM Edge AI Kit	Texas Instruments	Title: CAN TRANSCEIVERS	
		Size: C — PROC112 001 J721EXSKG01EVM	Rev: E2
		Date: Tuesday, June 22, 2021	Sheet 37 of 48

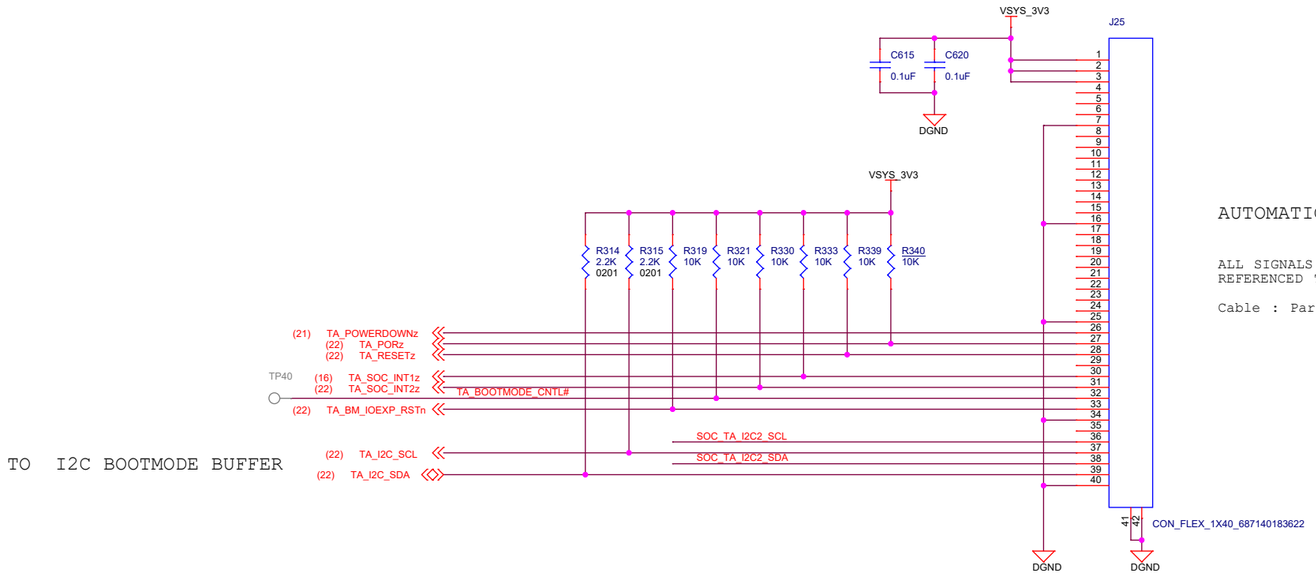
QUAD PORT CONSOLE

Silkscreen
"MAIN-UART"

TP2
VUSB_CP2108
J4
CON_MUSB-B_5_F
629105150521
USB_FT4232_EARTH
FB1
150E
LI0805H151R-10
USB_DM_CP2108
USB_DP_CP2108
U1
TPD2E001DRLR
VUSB_CP2108
USB_DP_CP2108
VDD_CP2108
C1
0.1uF
C300
1uF
16V
C9
1uF
16V
C11
0.1uF
C20
1uF
16V
C17
0.1uF
C31
0.1uF
C16
0.1uF
C18
1uF
10V
C324
1uF
10V
U4
CP2108-B02-GM
USB_DP_CP2108
USB_DM_CP2108
VDD_CP2108 R5 4.7K CP2108_RESET# 64
C6
0.1uF
RESET
CP2108_SUSPEND#
R154
220E
LD1
150040RS73220
RED
GPIO0
GPIO1
GPIO2
GPIO3
GPIO4
GPIO5
GPIO6
GPIO7
GPIO8
GPIO9
GPIO10
GPIO11
GPIO12
GPIO13
GPIO14
GPIO15
SUSPEND
SUSPEND
CP2108_SUSPEND#
CP2108_SUSPEND
TP6
RX0
TX0
RTS0
CTS0
DTR0
DSR0
DCD0
RI0
CP2108_UART0_RXD
CP2108_UART0_TXD
RX1
TX1
RTS1
CTS1
DTR1
DSR1
DCD1
RI1
CP2108_UART1_RXD
CP2108_UART1_TXD
CP2108_UART1_RTS#
CP2108_UART1_CTS#
RX2
TX2
RTS2
CTS2
DTR2
DSR2
DCD2
RI2
CP2108_UART2_RXD
CP2108_UART2_TXD
CP2108_UART2_RTS#
CP2108_UART2_CTS#
RX3
TX3
RI3
RTS3
CTS3
DTR3
DSR3
DCD3
CP2108_UART3_RXD
CP2108_UART3_TXD
NC1
NC2
VSS
VSS
VSSHD
EP
DGND
VSYS_IO_3V3
R21
10K
U41
SN74LVC1G06DCKT
CP2108_RXR_OE#
MCU_RESETSTATz (12,13)
C339
0.1uF
U9
SN74AVC4T245RSVR
CP2108_UART0_TXD
CP2108_UART3_TXD
CP2108_UART0_RXD
CP2108_UART3_RXD
WKUP_UART0_RXD (13)
UART1_RXD (14)
WKUP_UART0_TXD (13)
UART1_TXD (14)
C52
0.1uF
C58
0.1uF
R34
100K
R32
100K
DIR LOW: 1B --> 1A
HIGH: 2B <-- 2A
U3
SN74AVC4T245RSVR
CP2108_RXR_OE#
CP2108_UART1_TXD
CP2108_UART1_RTS#
CP2108_UART1_RXD
MCU_UART0_RXD (13)
MCU_UART0_CTS# (13)
MCU_UART0_RTS# (13)
MCU_UART0_TXD (13)
C15
0.1uF
C12
0.1uF
R6
100K
U34
SN74AVC4T245RSVR
CP2108_UART2_TXD
CP2108_UART2_RTS#
CP2108_UART2_RXD
CP2108_UART2_CTS#
UART0_RXD (14)
UART0_CTS# (14)
UART0_RTS# (14)
UART0_TXD (14)
C311
0.1uF
C312
0.1uF
R160
100K
DIR LOW: 1B --> 1A
HIGH: 2B <-- 2A

Project : TDA4VM Edge AI Kit	TEXAS INSTRUMENTS	Title: QUAD PORT UART	
		Size: C — PROC112 001 J721EXSKG01EVM	Rev: E2
		Date: Wednesday, July 21, 2021	Sheet 38 of 48

TEST AUTOMATION HEADER

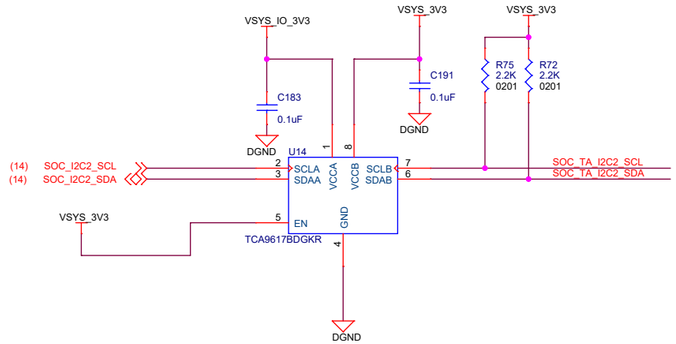


TO I2C BOOTMODE BUFFER

AUTOMATION INTERFACE

ALL SIGNALS SHOULD BE
REFERENCED TO EVM_3V3

Cable : Parlex-050R40-76B, .5mm 3"

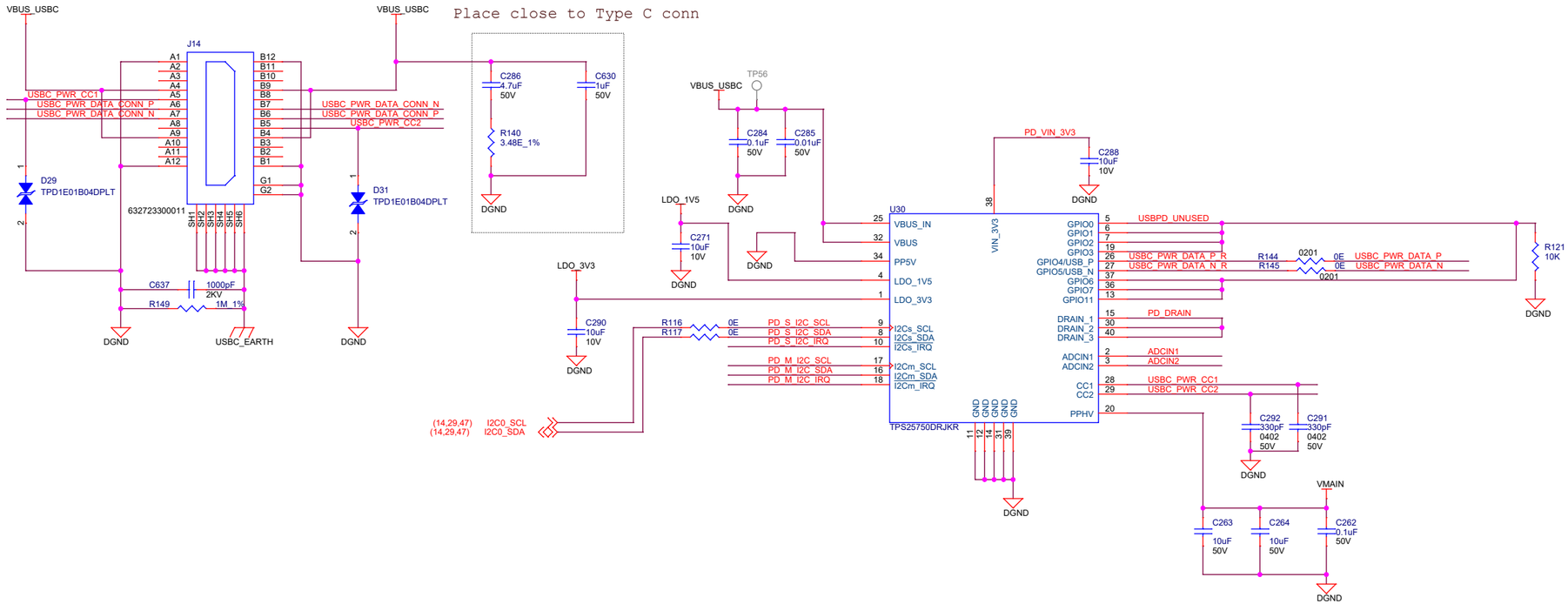


TEST AUTOMATION GPIO MAPPING

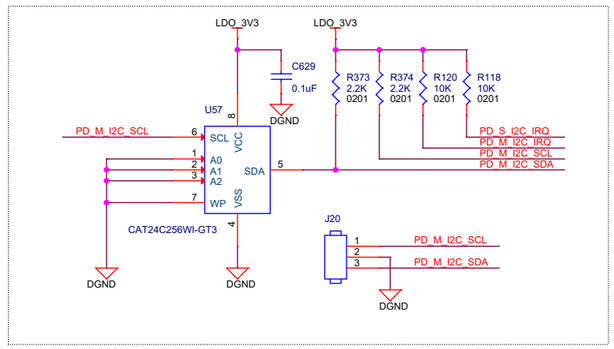
SIGNAL NAME	DESCRIPTION	Direction WRT CTRL	Internal/ External PU/PD states
TA_POWERDOWN	Used to Power down the system	OUTPUT	External Pullup
TA_PORZn	MCU & Main SoC domain Power ON Reset	OUTPUT	External Pullup
TA_RESETz	SoC Warmreset	OUTPUT	External Pullup
TA_SOC_INT1z	Interrupt to SOC	OUTPUT	External Pullup
TA_SOC_INT2z	Interrupt to SOC	OUTPUT	External Pullup
TA_BM_IOEXP_RSTn	Used to Reset the Bootmode IO Expander	OUTPUT	External Pullup

Project : TDA4VM Edge AI Kit		Title: TEST AUTOMATION HEADER
		Size: C — PROC112 001 J721EXSKG01EVM — Rev: E2
		Date: Wednesday, July 21, 2021 — Sheet 39 of 48

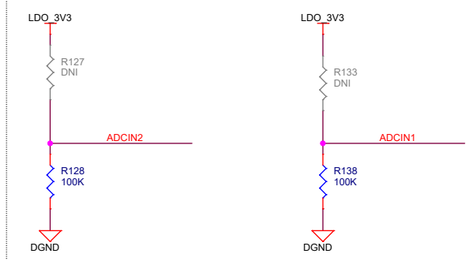
USB-C Power

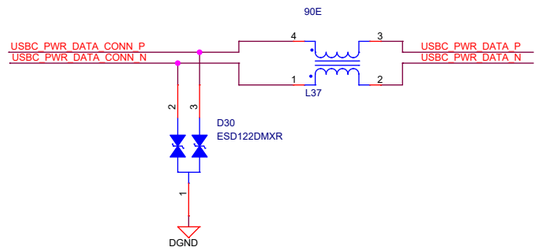


EEPROM & PROGRAMMING HEADER



ALWAYS ENABLE SINK
I2C SLAVE ADDRESS 0x20h (#01)





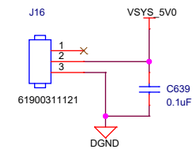
Project : TDA4VM Edge AI Kit	TEXAS INSTRUMENTS	Title: POWER INPUT
		Size: C — PROC112 001 J721EXSKG01EVM — Rev: E2
		Date: Wednesday, July 21, 2021 — Sheet 40 of 48

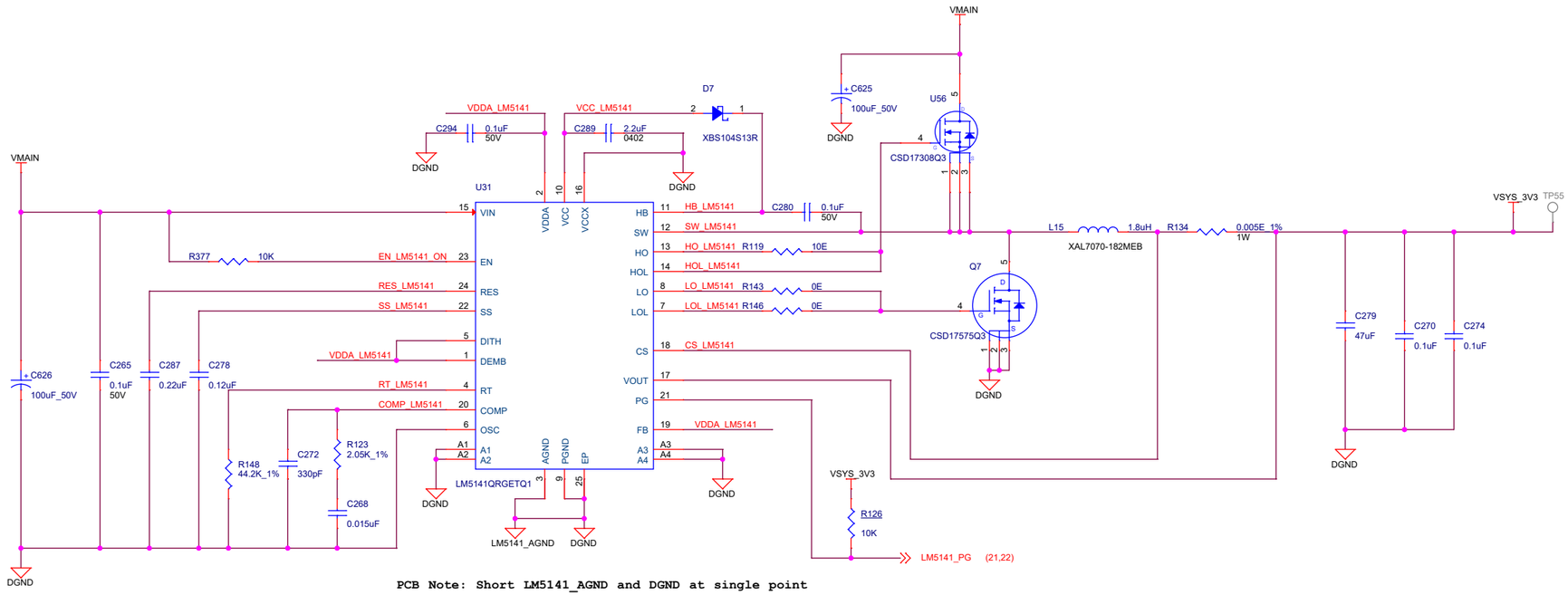
POWER SUPPLY #1

3.3V GENERATION

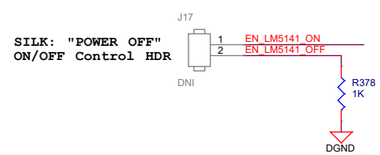
TI WEBENCH Simulation Inputs:
Vin (min) = 4.5V Vin (max) = 24V
Vout1 = 3.3V@10A
Ta = 25 deg

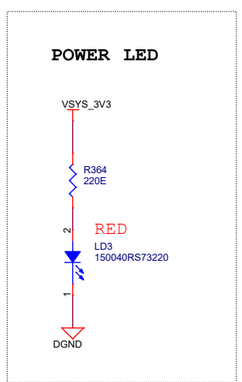
FAN HEADER





PCB Note: Short LM5141_AGND and DGND at single point

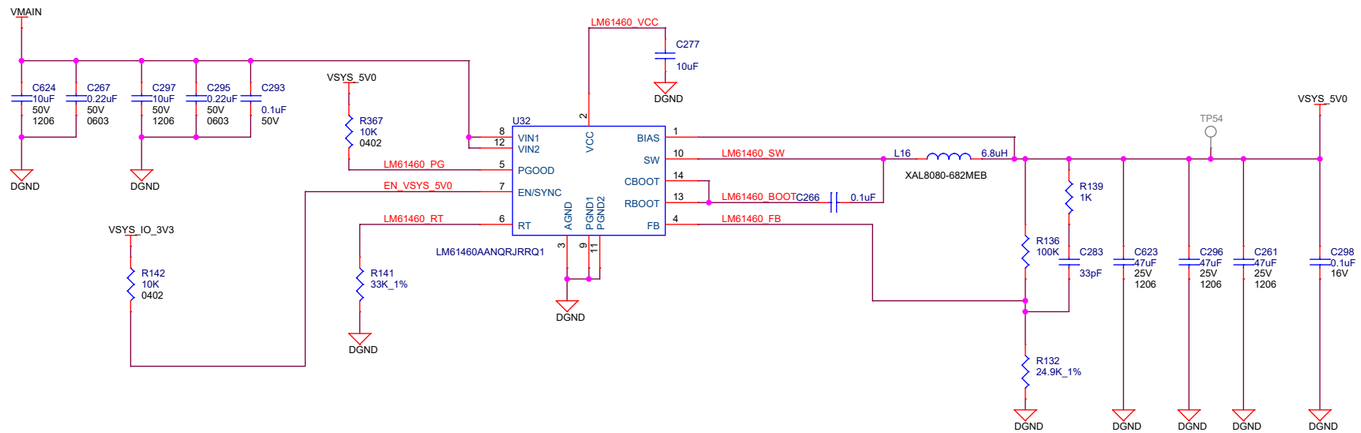




Project : TDA4VM Edge AI Kit	Texas Instruments	Title: POWER SUPPLY#1
		Size: C — PROC112 001 J721EXSKG01EVM — Rev: E2
		Date: Tuesday, June 22, 2021 — Sheet 41 of 48

POWER SUPPLY #2

LM61460 5V BUCK REGULATOR
VinMin = 12V
VinMax = 36V
Vout = 5.0V
Iout = 6A



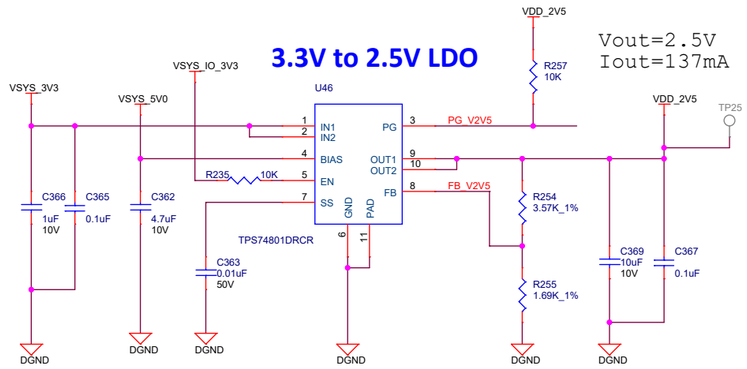
Project : TDA4VM Edge AI Kit	TEXAS INSTRUMENTS	Title: POWER SUPPLY #2
		Size: C — PROC112 001 J721EXSKG01EVM — Rev: E2
		Date: Wednesday, July 21, 2021 — Sheet 42 of 48

POWER SUPPLY #3

ETHERNET POWER

3.3V to 2.5V LDO

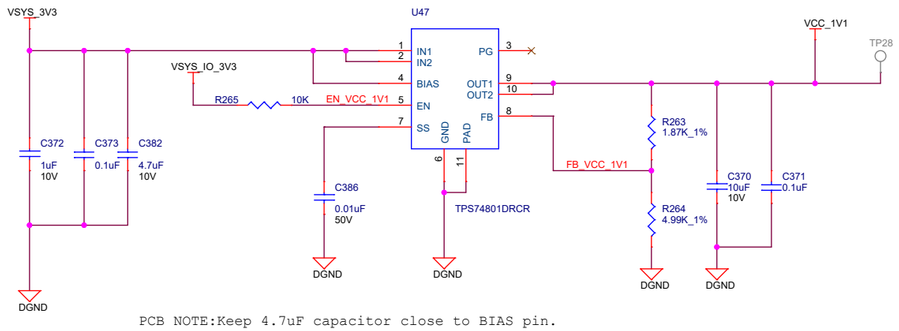
Vout=2.5V
Iout=137mA



USB HUB & ETHERNET POWER

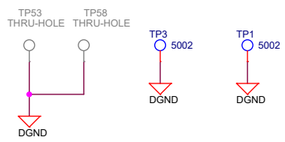
3.3V to 1.1V LDO

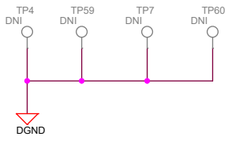
Vout=1.1V
Iout=888mA



PCB NOTE:Keep 4.7uF capacitor close to BIAS pin.

GROUND TEST POINTS





PCB NOTE: Spread the SMD test points Top and Bottom Side of PCB

Project : TDA4VM Edge AI Kit	TEXAS INSTRUMENTS	Title: POWER SUPPLY #3	
		Size: C — PROC112 001 J721EXSKG01EVM	Rev: E2
		Date: Tuesday, June 22, 2021	Sheet 43 of 48

EVM's 3-Phase DUAL PMIC Power Distribution Network (PDN)

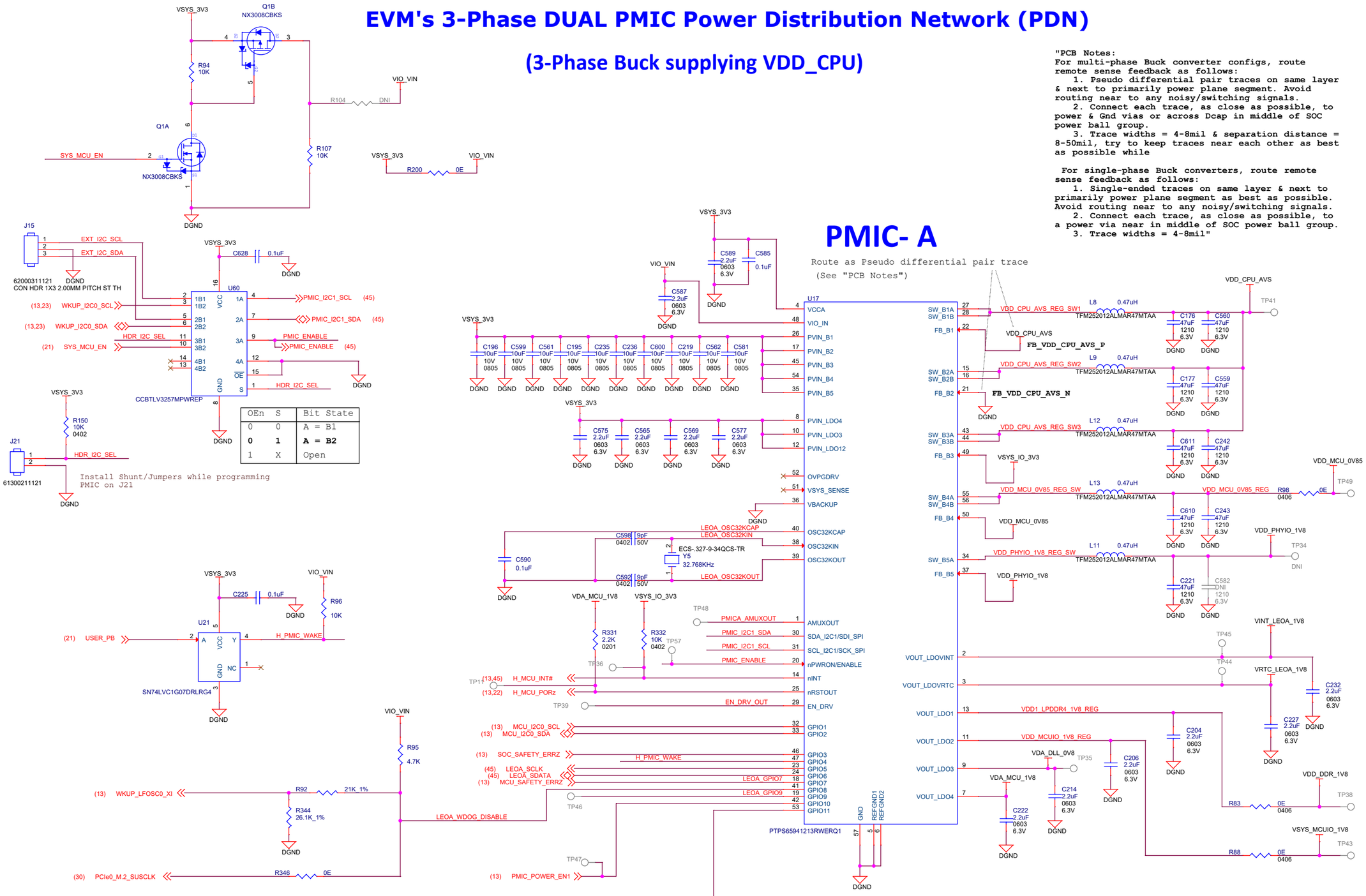
(3-Phase Buck supplying VDD_CPU)

"PCB Notes:
For multi-phase Buck converter configs, route remote sense feedback as follows:
1. Pseudo differential pair traces on same layer & next to primarily power plane segment. Avoid routing near to any noisy/switching signals.
2. Connect each trace, as close as possible, to power & Gnd vias or across Dcap in middle of SOC power ball group.
3. Trace widths = 4-8mil & separation distance = 8-50mil, try to keep traces near each other as best as possible while

For single-phase Buck converters, route remote sense feedback as follows:
1. Single-ended traces on same layer & next to primarily power plane segment as best as possible. Avoid routing near to any noisy/switching signals.
2. Connect each trace, as close as possible, to a power via near in middle of SOC power ball group.
3. Trace widths = 4-8mil"

PMIC- A

Route as Pseudo differential pair trace
(See "PCB Notes")



PMIC-A uses default I2C ADDR:
0x48, 0x49, 0x4A & 0x4B

(EVM Bd Setting Default):

LEOA_WDOG_DISABLE	PD (Low)	Enable WDOG
	PU (High)	Disable WDOG

Project :
TDA4VM Edge AI Kit

Texas Instruments

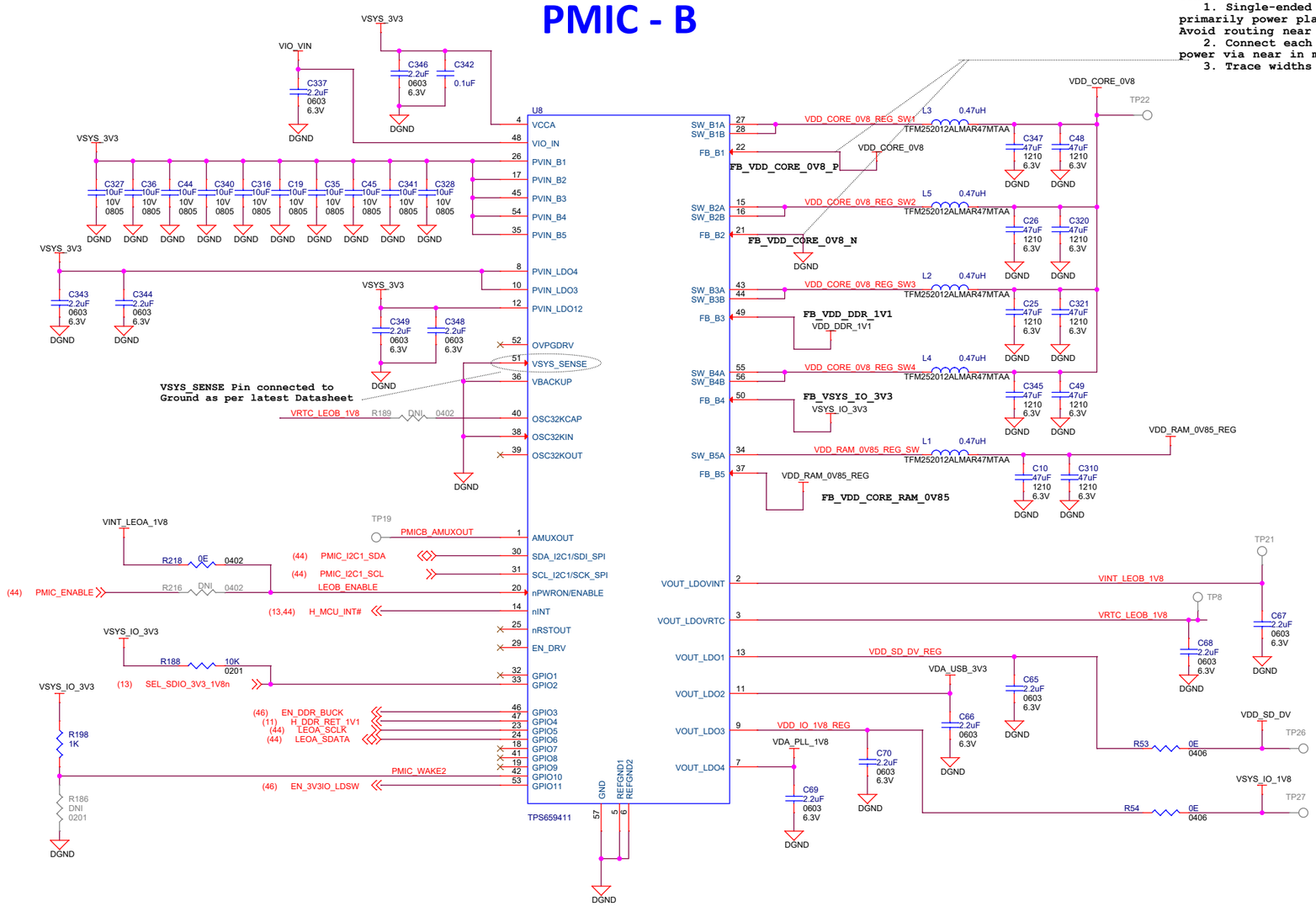
Title: PMIC A

Size		Rev
C	PROC112 001 J721EXSKG01EVM	E2
Date: Friday, June 25, 2021	Sheet 44 of 48	

PMIC - B

"PCB Notes:
For multi-phase Buck converter configs, route remote sense feedback as follows:
1. Pseudo differential pair traces on same layer & next to primarily power plane segment. Avoid routing near to any noisy/switching signals.
2. Connect each trace, as close as possible, to power & Gnd vias or across Dcap in middle of SOC power ball group.
3. Trace widths = 4-8mil & separation distance = 8-50mil, try to keep traces near each other as best as possible while

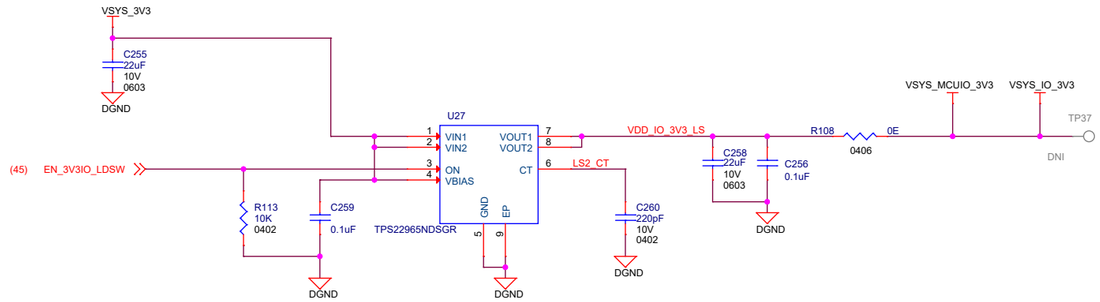
For single-phase Buck converters, route remote sense feedback as follows:
1. Single-ended traces on same layer & next to primarily power plane segment as best as possible. Avoid routing near to any noisy/switching signals.
2. Connect each trace, as close as possible, to a power via near in middle of SOC power ball group.
3. Trace widths = 4-8mil"



PMIC-B uses NVM to set I2C ADDR:
0x4C, 0x4D, 0x4E & 0x4F

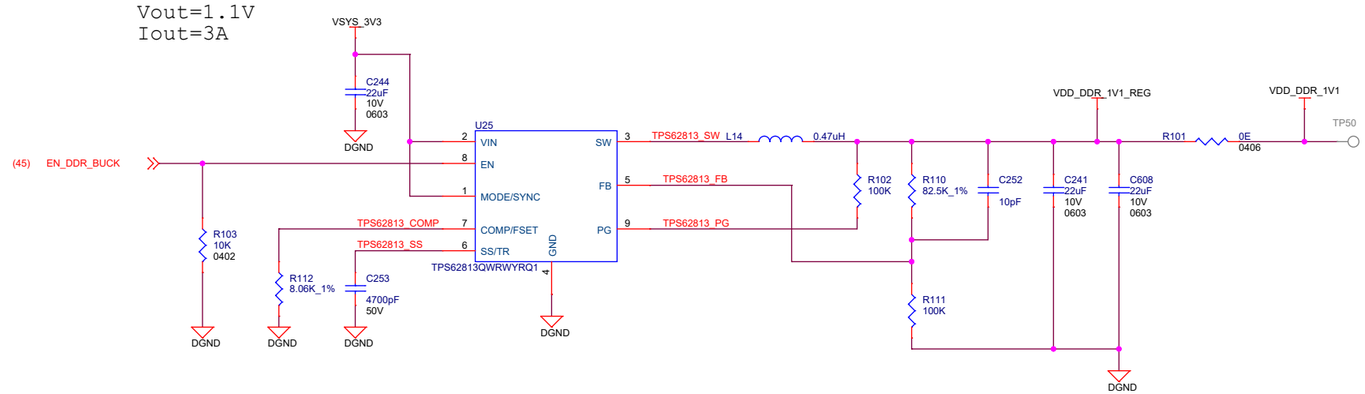
Project : TDA4VM Edge AI Kit	Texas Instruments	Title: PMIC B
		Size: C — PROC112 001 J721EXSKG01EVM — Rev: E2
		Date: Friday, June 25, 2021 — Sheet 45 of 48

3.3V LOAD SWITCH



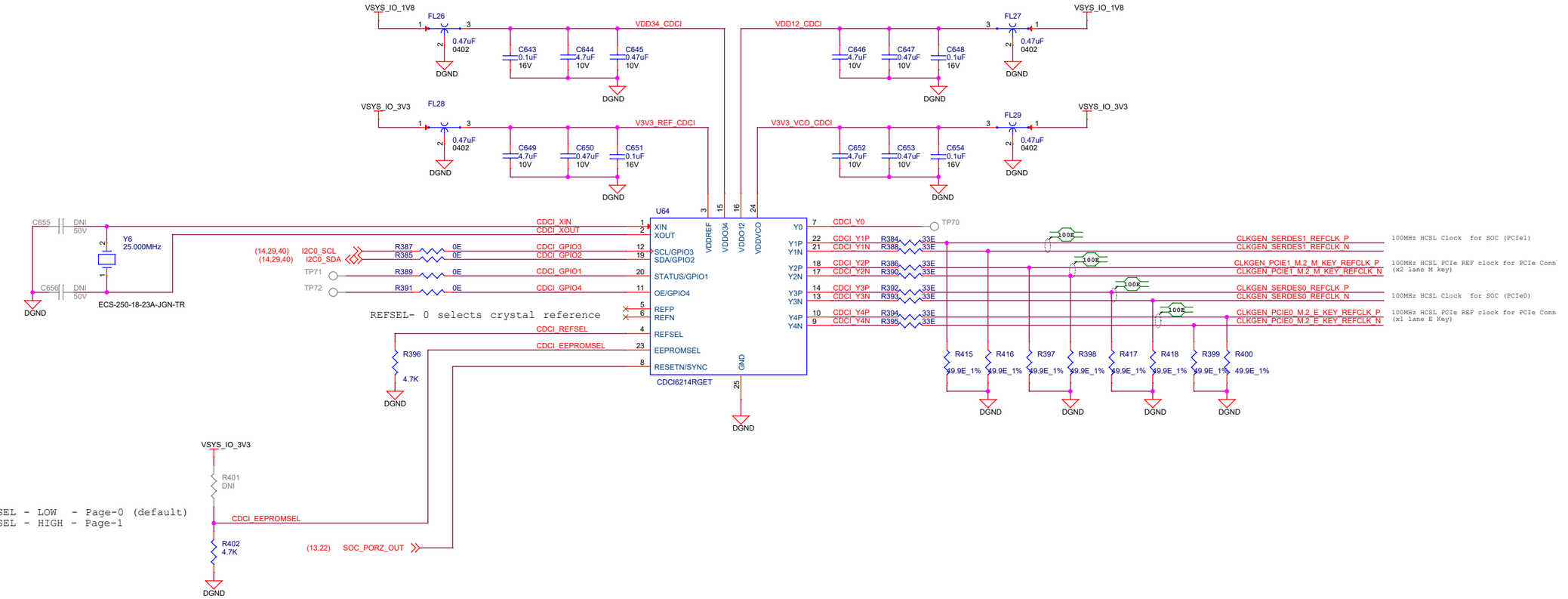
VDD_DDR_1V1 BUCK REG

Vout=1.1V
Iout=3A

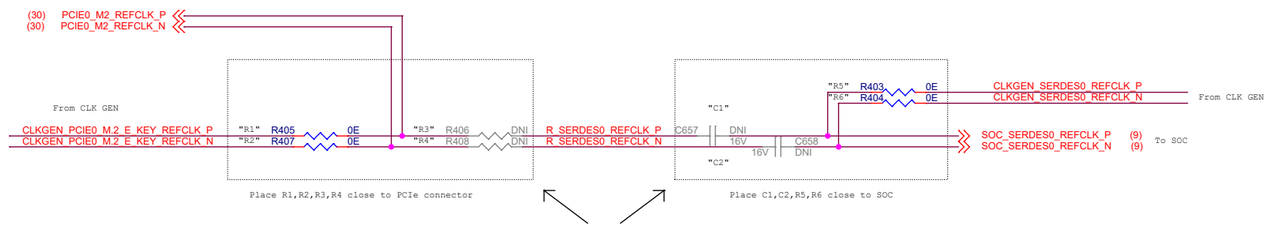


Project : TDA4VM Edge AI Kit	Texas Instruments	Title: LOAD SWITCHES
		Size: C — PROC112 001 J721EXSKG01EVM — Rev: E2
		Date: Tuesday, July 20, 2021 — Sheet 46 of 48

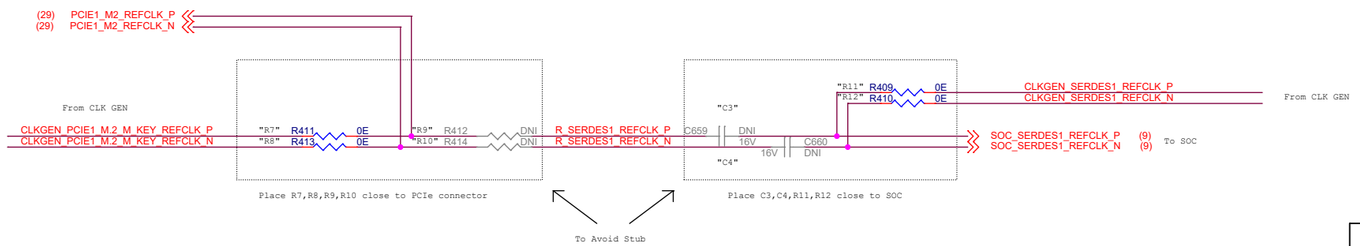
SERDES CLOCK GENERATOR



CLOCK ROOT SELECTION



Clock Source	Install	Remove
Clock Gen	R1,R2,R5,R6	C1,C2,R3,R4
SOC	C1,C2,R3,R4	R1,R2,R5,R6



Clock Source	Install	Remove
Clock Gen	R7,R8,R11,R12	C3,C4,R9,R10
SOC	C3,C4,R9,R10	R7,R8,R11,R12

Project : TDA4VM Edge AI Kit		Title: SERDES CLOCK GENERATOR
	Size: C	PROC112 001 J721EXSKG01EVM — Rev: E2
	Date: Wednesday, July 21, 2021	Sheet 47 of 48

NOTES, HW & LABELS

ASSEMBLY NOTES

1. All MSL components should be baked as per JEDEC standard.

2. PCB should be baked at 120 degree for 8 hours.

3. Board assembly must comply with workmanship standards. IPC-A-610 Class 2, unless otherwise specified.

4. These assemblies are ESD sensitive, ESD precautions shall be observed.

5. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

6. Provide serial numbers to the assembled boards for identification.

7. The assembled board are wrapped in ESD Covers(individual) and packed securely before shipment.

SCREWS

MH7 — PAN HEAD_M2.5 X 8

MH8 — PAN HEAD_M2.5 X 8

MH9 — PAN HEAD_M2.5 X 8

MH10 — PAN HEAD_M2.5 X 8

MH11 — PAN HEAD_M2.5 X 8

STANDOFFs

MH12 — HEX SPACER_M2.5 X 12

MH13 — HEX SPACER_M2.5 X 12

MH14 — HEX SPACER_M2.5 X 12

MH15 — HEX SPACER_M2.5 X 12

MH16 — HEX SPACER_M2.5 X 12

WASHER

ACC2 — PLAIN WASHER_M2.5

ACC3 — PLAIN WASHER_M2.5

ACC4 — PLAIN WASHER_M2.5

ACC5 — PLAIN WASHER_M2.5

ACC6 — PLAIN WASHER_M2.5

FIDUCIALS

FID1 DNI | FID2 DNI | FID3 DNI

FID4 DNI | FID5 DNI | FID6 DNI

BARE PCB

PCB1

PROC112E2

LABELS

Board Serial No.

LBL1

PCB LABEL

AM6-COMPROCEVM

Assembly Revision.

LBL2

PCB LABEL

AM6-COMPROCEVM

LOGOs

PCB LOGO DNI — Texas Instruments

PCB LOGO DNI — For Evaluation only; not FCC approved for resale

PCB LOGO DNI — WEEE Mark

PCB LOGO DNI — CE Mark

PCB LOGO DNI — High Temperature

SCREW & WASHER FOR PCIe M.2

MH2 — 9774015243R

MH3 — 3356

MH5 — MPMS 002 0005 PH

MH1 — 9774015243R

MH4 — 3356

MH6 — MPMS 002 0005 PH

HEATSINK AS ACCESSORIES

ACC1

374424B00035G

Project : TDA4VM Edge AI Kit	Texas Instruments	Title: HARDWARE SCHEMATICS
		Size: C — PROC112 001 J721EXSKG01EVM — Rev: E2
		Date: Tuesday, June 22, 2021 — Sheet 48 of 48