BQ24133, BQ24170, BQ24172, BQ24172 Schematic Review



Typical applications: Charger for 2S+ Lilon batteries in tablet PCs, Mobile Computers, Portable Printers, Portable Data Terminals, Battery Backup Systems

DESIGN CHECKLIST									
PIN N	AME	REQUIREMENT	COMPONENT	MIN	ТҮР	MAX	DESCRIPTION	COMMENTS AND RELEVANT EQUATIONS	PCB Placement
na	na	Recommended	RIN		2Ω		Input hot plug filter		
na	na	Recommended	CIN		2.2 uF				Place close to input adapater port
na	na	Recommended	Q1		*		Soft start FET		
na	na	Recommended	Q2		*		Reverse blocking FET	If not used, a reverse blocking diode is recommended	
		Optional					Soft start capacitor	To limit input surge current, external CGS at least 10 X FETs combined	
na	na		CGS		* uF			CGS can be added.	
na	na	Optional	RGS		499 kΩ		Pull down resistor	Required for 1S Lilon applications; recommended for all applications	
CMSRC	7	Required			4.02 kΩ		Common source connection for input		
			R12				NFETs		
	8	Required	544		4 02 1 0		Charge pump output for turning on		
ACDRV			RII		4.02 KΩ		INPUT NETS		
AVICC		Poquirod	C1		1 uF		IC input supply	C1 minimum voltage rating of 1.5 x maximum DC input voltage. R10 is 10 Ω unless input power is 5-V then reduce to 5 $\Omega.$	Place consciter close to IC ain and PCND, priority 1
			D1		10.0				Place capacitor close to ic pin and PGND, phonty 1
AVCC	7	Nequireu	ΝI		10 12			Low surrent diade (DATE4) to allow sharger to be newered from	
			D1 & D2		0.1 A		Schottky diode OR	batton when no input newer applied	
							3 3V reference voltage output for		
VREF	12	Required	C2		1 uF		resistor hias		Place near to IC pin and AGND, priority 3
								Sets the fast charge safety timer (5.6 min/nF). Pull the TTC to LOW to	
ттс	11	Required	C3		0.1 uF		Safety timer and termination control	disable the charge termination and safety timer. Pull the TTC to HIGH	Place near to IC pin and AGND, priority 3
								to disable the safety timer but allow the charge termination.	· · · · · · · · · · · · · · · · · · ·
							Input current limit common mode		Place from ACP pin to AGND. Kelvin connect to ACP
ACP	6	Optional	not shown		0.1 uF	i	filter capactior	if input current limit not used, do not install and short ACP=ACN.	pin.
ACN		Required		C12 0.1 uF			Input current limit common mode filter capactior	If input current limit not used, do not install and short ACP=ACN.	Place from ACN pip to ACND. Kelvin connect to ACN
	5		C12		0.1 uF				Place from ACN pill to AGND. Refuil connect to ACN
ACPtoACN	5 to 6 –	Required	RAC				Input current sense resistor	IDPM = VACSET/(20xRAC)	
					*Ω			If input current limit not used, do not install and short ACP=ACN. Use	
								current sense, low inductance resistor with appropriate current rating.	
		Required	C11		0.1E		Input current limit differential filter capacitor	antional 0.1 uE canacitar from ACN to ACND can be used for improved	Place across RAC input current limit resistor. Kelvin connect to ACP pin.
					0.1 UF			common mode filtering	
	10 -	Required	D9 (DT1)					(1)	
								$\left(\frac{1}{V_{T1}}-1\right)$	
TS					*0			$RT1 = \frac{1}{1}$	
			Ko (KII)		11			$\left(\frac{RT2}{RT2} + \frac{R_{NTC,T1}}{R_{NTC,T1}}\right)$	
							Resistor divider to set window for		
							thermistor temperature-based battery	If TS feature not used, use equations to set V(TS) to ~60% of VREF.	
		Required	R9 (RT2)				charging profile	$R_{NTCT1} \times R_{NTCTT} \times \left(\frac{1}{1} - \frac{1}{1}\right)$	
								$RT2 = \frac{RT2}{V_{T5} V_{T1}}$	Connect RT2 to AGND. Kelvin connect resistor
					*Ω			$\frac{1}{R} = \frac{1}{R} = \frac{1}$	divider midpoint to pin routed away from
								$(V_{T1} \land (V_{T1} \land (V_{T1} \land (V_{T5} \land (V_{$	traces/pours/planes with switching noise.
								See design xls at http://www.ti.com/lit/zip/sluc244	
OVPSET		Required					Resistor divider to set input over		Connect R7 to AGND. Kelvin connect resistor
			R6		*Ω			V _{ACOV} = 1.6V (R6/R7+1)	midpoint pin routed away from traces/pours/planes
	18							V _{ACUV} = 0.5V (R6/R7+1)	with switching noise. Add an optional 330pF
		Required	R7		*Ω		voitage and under voitage thresholds	Recommended to set R7 = 402k Ω and solve for R6	capacitor from OVPSET to ground if noisy supply or
								See design xls at http://www.ti.com/lit/zip/sluc244	fast transients.
ISET	13 -	Required	R2		*0		Resistor divider to set maximum charge current	V _{ISET} = VREF * R3/(R2+R3)	Connect R3 to AGND. Kelvin connect resistor divider midpoint to pin routed away from traces/pours/planes with switching noise.
			112		32			$I_{CHARGE} = V_{ISET} / (20 \text{xRSR})$	
		Required	B3		*∩	C		Recommended to set R2 = $100k\Omega$ and solve for R3	
		Required	КЭ		12			See design xls at http://www.ti.com/lit/zip/sluc244	

ACSET	17	Required	R4		*Ω		Resistor divider set maximum input	V _{ACSET} = VREF * R5/(R4+R5)	Connect R5 to AGND. Kelvin connect resistor divider midpoint to pin routed away from
								$I_{DPM} = V_{ACSET} / (20 x RAC)$	
		Dec. feed	55		*0		(adapater) current	Recommended to set R4 = $100k\Omega$ and solve for R5	traces/pours/planes with switching noise.
		Required	R5		*Ω *LΩ			See design xls at http://www.ti.com/lit/zip/sluc244	
STAT	10	Recommended	R10		*kΩ		LED pull up resistor		
		Optional	D3				Charging status indicating LED		
SW	1, 24	Required	L		3.3		Inductor connection	For BQ24133, refer to datasheet table 5	
								For BQ2417X, refer to datasneet table 3	Disco close to IC min and DCND priority 1. If alread
		Optional	D4				Low side Schottky diode	diada Sized for conduction only for duty $< 10\% * (1 D)$	Place close to ic pin and PGND, priority 1. If placed
					<u> </u>			603 footprint components, sized on working PCB using empirical	Place close to IC pip and PCND, priority 1. If placed
		Optional	RSNUB, CSNUB				RC snubber to reduce EMI	massurements. Decreases efficiency by ~0.5% when properly sized	an bettem layer, use multiple vise back to top
								incastrements. Decreases enciency by 0.5% when property sized	on bottom layer, use multiple vias back to top.
	, 21 to 1,24	Required	C5	0.047 uF					Place close to IC pin and PGND, priority 2.
BTST to SW								Slows down the FET turn on time which can reduce EMI. Sized	
		Optional	RBTST	1Ω		10 Ω		empirical. Will reduce efficiency by up to 1%.	
SRP	16								Place capacitor from IC pin to AGND. Kelvin connect
		Required	C7		0.1 uF		filter capactior	If input current limit not used, do not install and short ACP=ACN.	to IC pin and avoid traces/pours/planes with
									switching noise.
SRPtoSRN	↓ 15 to 16	Required	RSR		*Ω		Input current sense resistor	V _{1SET} = VREF * R3/(R2+R3)	-
								$I_{CHARGE} = V_{ISET}/(20 \text{xRSR})$	
								Recommended to set $R_2 = 100k\Omega$ and solve for R_3	
								See design xls at http://www.ti.com/lit/zip/sluc244	
		Required	C8		0.1 uF		Input current limit differential filter capacitor	If input current limit not used, do not install and short ACP=CAN. An	Place across RAC input current limit resistor. Kelvin connect to ACP pin.
								optional 0.1 uF capacitor from ACN to AGND can be used for improved	
								common mode filtering.	
	15	Optional	C _{DCP_BAT}	0.01 uF		0.1uF	Buck output decoupling capcaitor	Helpful in reducing output ripple and EMI	Place close to IC pin and PGND, priority 2.
SRN		Required	C9 & C10	10 uF	20 uF		Buck output bulk capacitance near	Minimum recommended is 10 uF; typical is 20 uF	Place close to IC pin and PGND, priority 3. Kelvin
5111								For BQ24133, refer to datasheet table 5	connect to IC pin and avoid traces/pours/planes with
							charger IC	For BQ2417x, refer to datasheet table 3	switching noise.
PVCC	23	Optional	C _{DCP_VCC}	0.01 uF		0.1uF	Buck input decoupling capacitance	Most important capacitor for minimizing EMI	Place close to IC pin and PGND, priority 1.
FVCC	2, 5	Required	C4	10 uF			Buck input bulk capacitance		Place close to IC pin and PGND, priority 1.
DECN	20	Poquirod	66	1E			REGN linear regulation output		Place close to IC pip and PCND, priority 1
REGIN		Requireu		IUF			capacitor		Place close to ic pill and PGND, priority 1.
CELL	14	Poquirod	22		22		Sats ()/ regulation point for 122/170	Set CELL pin LOW for 1-cell, Float for 2-cell (0.8 V - 1.8 V), and HIGH for	
		Requireu	na		IId		Sets CV regulation point for 155/170	3- cell with a fixed 4.2 V per cell.	
				Π				VBATREG = 2.1 V * (1 + RTOP/RBOT)	
FB	14	Required	RTOP, RBOT		*		Sets CV regulation point for 171/172	Recommended to set RBOT = 100k Ω and solve for RTOP	Place resistors close to IC pin and AGND.
								See design xls at http://www.ti.com/lit/zip/sluc244	