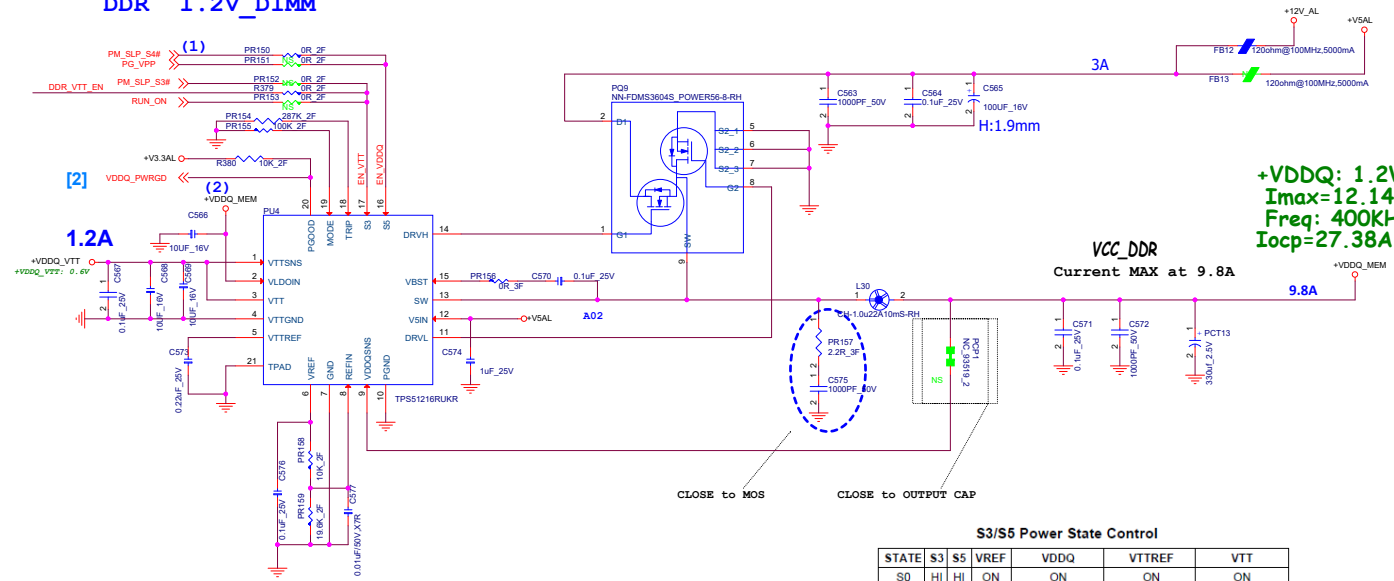


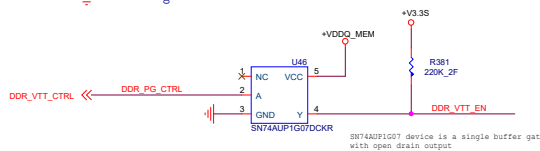
PM_SLP_S4#
 1: S0,S1,S3
 0: S4,S5

DDR 1.2V_DIMM



S3/S5 Power State Control

STATE	S3	S5	VREF	VDDQ	VTTREF	VTT
S0	HI	HI	ON	ON	ON	ON
S3	LO	HI	ON	ON	ON	OFF(High-Z)
S4/S5	LO	LO	OFF	OFF(Discharge)	OFF(Discharge)	OFF(Discharge)



SN74AUP1G07 device is a single buffer gate with open drain output.