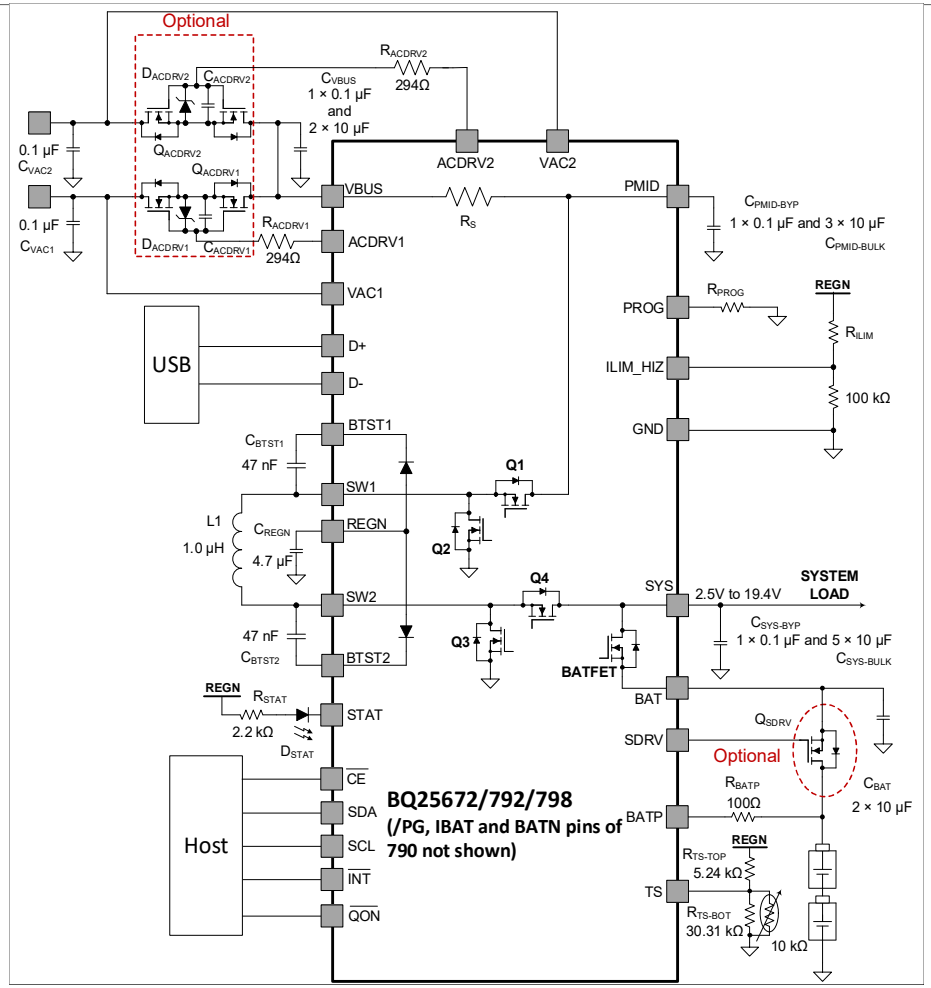
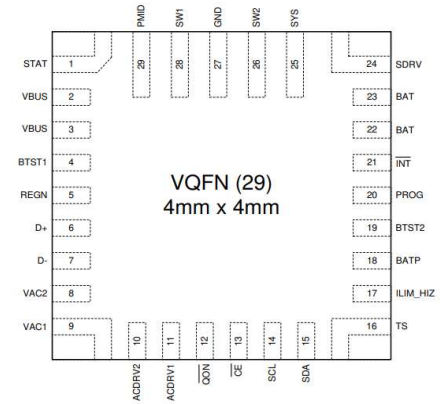
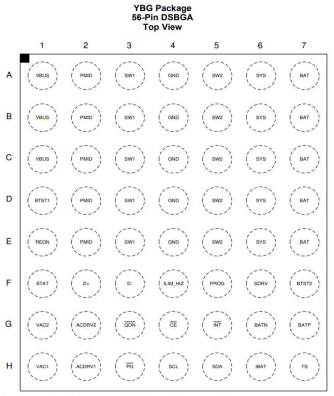
BQ25790/2/8 and BQ25672 Schematic Review



BQ25792/BQ25798/BQ25672



BQ25790



Top View = Xray through a soldered down part with A1 starting in upper left corner

NOTE: BQ25672 requires only 3x10uF

NOTE: All capacitors are assumed to be ceramic with voltage voltage rating = at least 2 x the pin's max expected voltage										
Pin	**QFN**	**WCSP**	**Opt/Rec/Req**	**Component**	**Min**	**Typ**	**Max**	**EXPLANATION**	**COMMENTS**	**LAYOUT GUIDANCE**
VAC1	9	H1	Optional	C_{VAC1}		100n F		VAC1 sense line filter capcacitor	Connect to VBUS if ACDRV1 not used.	
VAC2	8	G1	Optional	C_{VAC2}		100 nF		VAC2 sense line filter capcacitor	Connect to VBUS if ACDRV2 not used.	
ACDRV1	11	H2	Optional	Q_{ACDRV1}		30 V Nch		NFETs for input source MUX	Connect to ground if ACDRV1 not used.	
				D_{ACDRV1}		12V		Zener clamp to protect FET gate		
				R_{ACDRV1}		294 Ω		Softstart resistor		
				C_{ACDRV1}		1 nF		Softstart capacitor		
ACDRV2	10	G2	Optional	Q_{ACDRV2}		30 V Nch		NFETs for input source MUX	Connect to ground if ACDRV2 not used.	
				D_{ACDRV2}		12V		Zener clamp to protect FET gate		
				R_{ACDRV2}		294 Ω		Softstart resistor		
				C_{ACDRV2}		1 nF		Softstart capacitor		
VBUS	2,3	A1,B1, C1	Required	$C_{VBUS-BYP}$		0.1 uF		VBUS high frequency noise bypass capacitor		
			Required	$C_{VBUS-BULK}$		2 x 10uF		VBUS bulk capacitors		
REGN	5	E1	Required	C_{REGN}	4.7 uF			REGN linear regulation output capacitor		Place close to REGN pin and PGND, priority 2.
PMID	29	A2,B2,C2,D2,E2	Required	$C_{PMID-BYP}$		0.1 uF		PMID high frequency noise bypass capacitor	Critical for device operation and minimizing EMI.	Place as close as possible to PMID and GND pins using as few vias as possible, priority 1
			Required	$C_{PMID-BULK}$		3 x 10uF*		PMID bulk capacitors	Input capacitance for the converter *BQ25796 requires 2 additional, parallel 33 uF low ESR polarized capacitors	Place as close as possible to PMID and GND pins using as few vias as possible, priority 1
SYS	25	A6,B6,C6,D6,E6	Required	$C_{SYS-BYP}$		0.1 uF		SYS high frequency noise bypass capacitor	Critical for device operation and minimizing EMI	Place as close as possible to SYS and GND pins using as few vias as possible, priority 1
			Required	$C_{SYS-BULK}$		5 x 10uF -79x 3 x 10uF -672		SYS bulk capacitors	Output capacitance for the converter	Place as close as possible to SYS and GND pins using as few vias as possible, priority 1
BAT	22,23	A7,B7,C7,D7,E7	Required	C_{BAT}		2 x 10uF		BAT bulk capacitors		Place close to BAT pin and PGND, priority 2.
BATP	18	G7	Required	R_{BATP}		100 Ω		BAT+ remote sense isolation resistor	Can short to IC BAT pin if remote sense not needed.	
SW1	28	A3,B3,C3,D3,E3	Required	L1	1 uH		2.2 uH	Inductor buck side connection	1 uH for f_{SW} = 1.5 MHz and 2.2 uH for f_{SW} = 750 kHz	Required to route SWx traces under the IC and then uses vias to connect to inductor if on top layer.
			Optional	R_{SNUB1}, C_{SNUB1}		not shown		RC snubber to reduce EMI	603 footprint components, sized on working PCB using empirical measurements. Decreases efficiency by ~0.5% when properly sized	Place close to SWx and PGND, priority 1. If placed on bottom layer, use multiple vias back to top.
BTST1	4	D1	Required	C_{BTST1}		0.047 uF		Bootstrap capacitor for buck side FET gate drive		
SW2	26	A5,B5,C5,D5,E5	Required	L1	1 uH		2.2 uH	Inductor boost side connection	1 uH for f_{SW} = 1.5 MHz and 2.2 uH for f_{SW} = 750 kHz	Required to route SWx traces under the IC and then uses vias to connect to inductor if on top layer.
			Optional	R_{SNUB2}, C_{SNUB2}		not shown		RC snubber to reduce EMI	603 footprint components, sized on working PCB using empirical measurements. Decreases efficiency by ~0.5% when properly sized	Place close to SWx and PGND, priority 1. If placed on bottom layer, use multiple vias back to top.
BTST2	19	F7	Required	C_{BTST2}		0.047 uF		Bootstrap capacitor for boost side FET gate drive		
PROG	20	F5	Required	R_{PROG}		*Ω		Sets default converter switching frequency and either 1S, 2S, 3S or 4S charging	See datasheet section titled PROG Pin Configuration for resistor sizes	

ILIM_HIZ	17	F4	Required	R_{LIM}		*Ω		Program ILIM_HIZ voltage to set desired IINDPM by connecting a resistor divider from pull up rail to ILIM_HIZ pin then 100 kΩ resistor to ground. When the pin voltage is below 0.75V, the buck-boost converter enters non-switching mode with REGN on.	V_{ILIM_HIZ} = 1V + 800 mΩ x IINDPMmax IINDPM I2C register can be written to lower value. ILIM_HIZ can be disabled in I2C. ILIM_HIZ can be pulled directly to REGN to set max I2C register value (3.3A).	
TS	16	H7	Required (if not disabled in I2C register)	R_{TS-TOP}		*Ω		Resistor divider to set window for thermistor temperature-based battery charging profile	If TS feature not used, use equations to set V(TS) to ~60% of VREF to hardware disable or I2C bit to software disable.	
			Required (if not disabled in I2C register)	R_{TS-BOT}		*Ω			$RT2 = \frac{R_{NTC,T1} \times R_{NTC,T5} \times \left(\frac{1}{V_{T5}} - \frac{1}{V_{T1}}\right)}{R_{NTC,T1} \times \left(\frac{1}{V_{T1}} - 1\right) - R_{NTC,T5} \times \left(\frac{1}{V_{T5}} - 1\right)}$ $RT1 = \frac{\left(\frac{1}{V_{T1}} - 1\right)}{\left(\frac{1}{RT2} + \frac{1}{R_{NTC,T1}}\right)}$	Connect R_{TS_BOT} to AGND. Kelvin connect resistor divider midpoint to pin routed away from traces/pours/planes with switching noise.
STAT	1	F1	Recommended	R_{STAT}		2.2 kΩ		LED pull up resistor for open drain STAT pin.		
			Optional	D_{STAT}		green or red		Charging status indicating LED		
SDRV	24	F6	Optional	Q_{SDRV}		30 V Nch		The driver pin of the external ship FET. The ship FET is always turned on when ship mode is disabled, and it keeps off when the charger is in ship mode or shutdown mode.	Connect a 0402 / 50V / 1nF ceramic capacitor from SDRV to BAT or GND when the ship FET is not used.	
/CE	13	G4	Required	R_{PULLUP}	2.2 kΩ		10 kΩ	Active low, open drain charge enable	Can be tied to GND but recommended to be tied to host GPIO with pull up resistor. Cannot be left floating.	
/INT	21	G5	Optional	R_{PULLUP}	2.2 kΩ		10 kΩ	Active low, open drain INT pulse	Can be left floating but recommend to to tied to host GPIO with pull up resistor.	
/QON	12	G3	Optional					A logic low on this pin with t_{SM_EXIT} duration turns on ship FET to force the device to exit the ship mode. A logic low on this pin with t_{RST} duration resets system power by turning off the ship FET for t_{RST_SFET} (also setting the charger in HIZ mode when VBUS is high) and then turning on ship FET (also disabling the charger HIZ mode) to provide full system power reset	The pin has an internal pull up so it not used it should be left floating. Can be tied to a mechanical push button or host GPIO.	
SDA	15	H5	Required	R_{PULLUP}	2.2 kΩ		10 kΩ	I2C data line	Needs pull up resistor to 1.8 V to 3.3 V	
SCL	14	H4	Required	R_{PULLUP}	2.2 kΩ		10 kΩ	I2C clock like	Needs pull up resistor to 1.8 V to 3.3 V	
D+	6	F2	Optional					USB BC 1.2 communication lines	Connect to USB port in order to set charger input current (IINDPM) register to port capability per USB BC 1.2 spec. Host is expected to perform enumeration. If not used, leave floating for unkown adapter and IINDPM=3A. ILIM_HIZ resistor clamps maximum input current	
D-	7	F3	Optional							
BATN (790 only)	na	G6	Required	R_{BATN}		100 Ω		BAT- remote sense isolation resistor	Can short to IC GND pin if remote sense not needed.	
/PG (790 only)	na	H3	Optional	R_{PULLUP}	2.2 kΩ		10 kΩ	Active low, open drain input power good indicator	Can be left floating but recommend to to tied to host GPIO with pull up resistor.	
IBAT (790 only)	na	H6	Optional	R_{IBATP}		10 kΩ		Current source output proivding 25 uA per 1A charge current.	Parallel 100 pF capacitor is recommended to minimize ripple.	
GND	27	A4,B4,C4,D4,E4	Required					IC GND return	Separate PGND and AGND, connected only at GND pins is recommended by not required as long as power path (VBUS, PMID, SYS, BAT) grounds are routed away from AGND. REGN is technically PGND but difficult to route.	Required to route to internal/bottom layer under the IC but also provide GND trace on top layer for connecting PMID and SYS capacitor grounds