TPS65651/A/B Triple-Output AMOLED Display Power Supply

1 Features

- TPS65651:
  - $V_{(ELVSS)}$ startup delay = 40 ms
  - Short-circuit and OLP detect time = 4 ms
- TPS65651A/B:
  - $V_{(ELVSS)}$ startup delay = 10 ms
  - Short-circuit and OLP detect time = 1 ms
- 2.9-V to 4.8-V Input Voltage Range
- Synchronous Boost Converter (AVDD)
  - 6.1-V Output Voltage (TPS65651/A)
  - 7.6-V Output Voltage (TPS65651B)
  - 1% Accuracy
  - 80-mA Output Current Capability @ 6.1 V
  - 60-mA Output Current Capability @ 7.6 V
  - V_I to V_O and V_O to V_I Isolation
- Synchronous Boost Converter (ELVDD)
  - 4.6-V Output Voltage
  - 0.5% Accuracy
  - 300-mA Output Current Capability
  - External Output Voltage Sensing Pin for Load Drop Compensation
  - V_I to V_O and V_O to V_I Isolation
- Synchronous Inverting Buck-Boost Converter (ELVSS)
  - –5.4-V to –1.4-V Output Voltage (programmable)
  - –2.5-V Default Output Voltage
  - 1.2% Accuracy at –2.5 V (±30 mV)
  - 300-mA Output Current Capability
  - V_I to V_O and V_O to V_I Isolation
- Short Circuit Protection
- Thermal Shutdown
- Available in 3-mm × 3-mm x 0.75-mm 16-Pin WQFN Package

2 Applications

- Smartphones
- Small Size Tablets
- Active Matrix OLED Displays ≤ 8"

3 Description

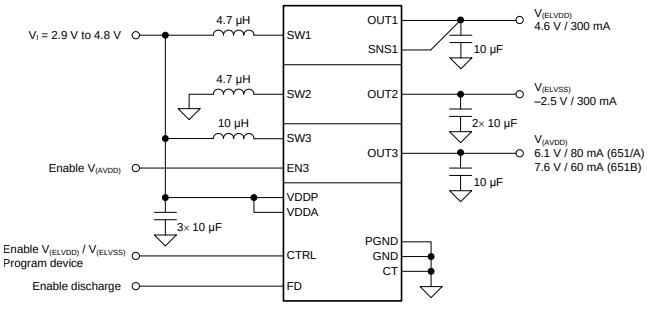
The TPS65651/A/B is designed to drive AMOLED displays (Active Matrix Organic Light Emitting Diode) requiring $V_{(AVDD)}$, $V_{(ELVDD)}$ and $V_{(ELVSS)}$. The device integrates a boost converter for $V_{(ELVDD)}$, an inverting buck-boost converter for $V_{(ELVSS)}$ and a boost converter for $V_{(AVDD)}$, which are suitable for battery operated products.

Device Information(1)

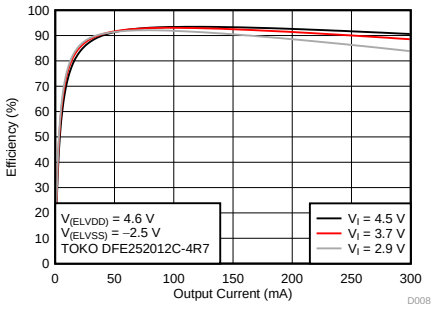
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS65651	WQFN (16)	3.00 mm x 3.00 mm
TPS65651A	WQFN (16)	3.00 mm x 3.00 mm
TPS65651B	WQFN (16)	3.00 mm x 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



Efficiency



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4 Pin Configuration and Functions

RTE Package
16-Pin WQFN
(Top View)

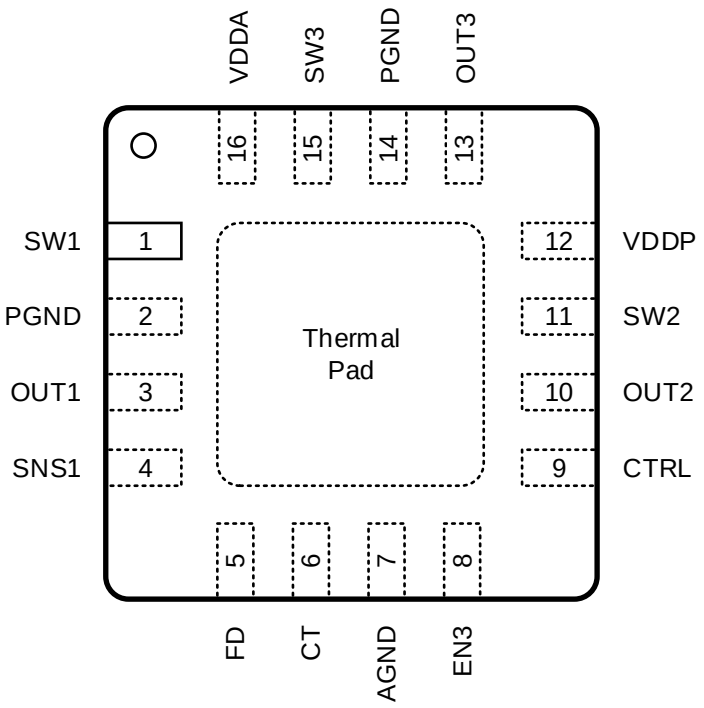


Table 1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	No.		
AGND	7	—	Analog ground.
CT	6	I / O	Control of the ELVSS transition time.
CTRL	9	I	Enable ELVDD boost converter and delayed ELVSS inverting buck-boost converter. Digital programming.
EN3	8	I	Enable AVDD boost converter.
FD	5	I	Active discharge enable / disable during shut-down.
OUT1	3	O	Output of the ELVDD boost converter.
OUT2	10	O	Output of the ELVSS inverting buck-boost converter.
OUT3	13	O	Output of the AVDD boost converter.
PGND	2	—	Power ground of the ELVDD boost converter.
PGND	14	—	Power ground of the AVDD boost converter.
SNS1	4	I	ELVDD sense input.
SW1	1	O	Switch pin of the ELVDD boost converter.
SW2	11	O	Switch pin of the ELVSS inverting buck-boost converter.
SW3	15	O	Switch pin of the AVDD boost converter.
VDDA	16	—	Supply for the internal analog circuits.
VDDP	12	—	Supply for ELVSS inverting buck-boost converter.
Exposed thermal pad		—	Connect this pad to AGND and PGND.

5 Specifications

5.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage(2)	VDDP, VDDA, EN3, CTRL, CT, FD, SW1, OUT1, SNS1	–0.3	6	V
	SW3, OUT3	–0.3	10	V
	OUT2	–6.5	0.3	V
	SW2	–6.5	5.5	V
Operating Junction temperature		–40	150	°C
Storage temperature range, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods my affect device reliability.
(2) All voltages are with respect to network ground pin.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_I	Supply input voltage range	2.9	3.7	4.8	V
T_J	Operating Junction temperature	–40		125	°C
ELVDD BOOST CONVERTER (OUT1)					
V_O	ELVDD boost converter output voltage range		4.6		V
L	Inductance	–30%	4.7	+30%	µH
C_I	Input capacitance placed at the inductor(1)	2.5	5		µF
C_O	Output capacitance placed at OUT1 pin(1)	2.5	5	24	µF
ELVSS INVERTING BUCK-BOOST CONVERTER (OUT2)					
V_O	ELVSS inverting buck-boost output voltage range	–5.4	–2.5	–1.4	V
L	Inductance	–30%	4.7	+30%	µH
$C_{(VDDP)}$	Input capacitance placed at VDDP pin(1)	2.5	5		µF
C_O	Output capacitance placed at OUT2 pin(1)	2.5	5	24	µF
$C_{(CT)}$	CT-pin capacitance(1)			300	nF
AVDD BOOST CONVERTER (OUT3)					
V_O	TPS65651/A AVDD boost converter output voltage range		6.1		V
	TPS65651B AVDD boost converter output voltage range		7.6		V
L	Inductance	–30%	10	+30%	µH
C_I	Input capacitance placed at the inductor(1)	2.5	5		µF
C_O	Output capacitance placed at OUT3 pin(1)	2.5	5	24	µF

(1) Note: The resulting capacitance of a capacitor changes over voltage and temperature. See the capacitors datasheet for more detail.

5.4 Thermal Information

THERMAL METRIC(1)		RTE (16 PINS)	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	42.9	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	44	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	14.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	14.1	°C/W
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance	3.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).

5.5 Electrical Characteristics

V_I = 3.7 V, CTRL = V_I, EN3 = V_I, $V_{(ELVDD)}$ = 4.6 V, $V_{(ELVSS)}$ = –2.5 V, $V_{(AVDD)}$ = 6.1 V, T_J = –40°C to 85°C, typical values are at T_J = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY AND THERMAL PROTECTION						
V_I	Operating Input Voltage		2.9	3.7	4.8	V
	Shutdown current into V_I	$V_{(CTRL)}$ = $V_{(EN3)}$ = GND, $V_{(FD)}$ = 3.7 V or GND		0.1	10	µA
$V_{IT–}$	Under-voltage lockout threshold (VDDA)	V_I falling	2.05	2.1	2.2	V
V_{IT+}		V_I rising	2.3	2.4	2.5	V
	Thermal shutdown temperature	Junction temperature rising		135		°C
	Thermal shutdown hysteresis	Junction temperature falling		5		°C
LOGIC SIGNALS (EN3, CTRL, FD)						
V_{IH}	High-level input voltage (EN3, CTRL, FD)	V_I = 2.9 V to 4.5 V	1.2			V
V_{IL}	Low-level input voltage (EN3, CTRL, FD)	V_I = 2.9 V to 4.5 V			0.4	V
	Pull-down resistance (EN3, CTRL)		250	500	900	kΩ
ELVDD BOOST CONVERTER (OUT1)						
V_O	Output voltage (OUT1)			4.6		V
	Output voltage accuracy (OUT1)	T_J = 25°C, no load	–0.5%		0.5%	
		–40°C ≤ T_J ≤ 85°C, no load	–0.8%		0.8%	
$r_{DS(on)}$	MOSFET on-state resistance (Q1)	I_{DS} = 100 mA		250		mΩ
$r_{DS(on)}$	MOSFET on-state resistance (Q2)	I_{DS} = 100 mA		350		mΩ
	Current limit (Q1)	Inductor valley current	0.8	1	1.3	A
	Short-circuit threshold in operation (SNS1)	Percentage of nominal V_O	85%	90%	95%	
	Voltage-sensing threshold (OUT1)	$V_{(OUT1)}$ – $V_{(SNS1)}$ increasing	200	300	450	mV
	Voltage-sensing threshold (SNS1)	$V_{(OUT1)}$ – $V_{(SNS1)}$ decreasing	100	200	350	mV
	Off current (combined) (OUT1, SNS1)	$V_{(FD)}$ = $V_{(CTRL)}$ = GND		0.8	5	µA
$R_{(SNS1)}$	Pull-down resistance (SNS1)		1.5	4	8	MΩ
	Discharge resistance (OUT1)	$V_{(CTRL)}$ = GND, I_O = 1 mA	15	30	55	Ω
	Line regulation	I_O = 100 mA, V_I = 2.9 V to 4.5 V		0.01		%/V
	Load regulation	1 mA ≤ I_O ≤ 300 mA		0.1		%/A

Electrical Characteristics (continued)

V_I = 3.7 V, CTRL = V_I, EN3 = V_I, $V_{(ELVDD)}$ = 4.6 V, $V_{(ELVSS)}$ = –2.5 V, $V_{(AVDD)}$ = 6.1 V, T_J = –40°C to 85°C, typical values are at T_J = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ELVSS INVERTING BUCK-BOOST CONVERTER (OUT2)						
V_O	Output voltage (OUT2)		–1.4	–2.5	–5.4	V
	Output voltage accuracy (OUT2)	T_J = 25°C, no load	–30		30	mV
		–40°C ≤ T_J ≤ 85°C, no load	–50		50	mV
$r_{DS(on)}$	MOSFET on-state resistance (Q3)	I_{DS} = 100 mA		250		mΩ
$r_{DS(on)}$	MOSFET on-state resistance (Q4)	I_{DS} = 100 mA		300		mΩ
	Current limit (Q3)	Inductor peak current	1.5	2.2	3	A
	Short-circuit threshold in operation (OUT2)	Voltage rise from nominal V_O	400	500	650	mV
	Off current (OUT2)	$V_{(FD)}$ = $V_{(CTRL)}$ = GND		0.01	5	µA
	Discharge resistance (OUT2)	$V_{(CTRL)}$ = GND, I_O = 1 mA	130	150	175	Ω
$R_{(CT)}$	Output resistance (CT)		150	325	500	kΩ
	Input threshold voltage (CT)	$V_{(CT)}$ rising	10	50	200	mV
	Line regulation	I_O = 100 mA, V_I = 2.9 V to 4.5 V		0.02		%/V
	Load regulation	1 mA ≤ I_O ≤ 300 mA		–0.5		%/A
AVDD BOOST CONVERTER (OUT3)						
V_O	TPS65651/A Output voltage (OUT3)			6.1		V
	TPS65651B Output voltage (OUT3)			7.6		V
	Output voltage accuracy (OUT3)	–40°C ≤ T_J ≤ 85°C, no load	–1%		1%	
$r_{DS(on)}$	MOSFET on-state resistance (Q5)	I_{DS} = 100 mA		500		mΩ
$r_{DS(on)}$	MOSFET on-state resistance (Q6)	I_{DS} = 100 mA		1200		mΩ
	Current limit (Q5)	Inductor peak current	0.25	0.4	0.55	A
	Short-circuit threshold voltage (OUT3)	Percentage of nominal V_O	85	90	95	%
	Off current (OUT3)	$V_{(FD)}$ = $V_{(EN3)}$ = GND		1.5	5	µA
	Discharge resistance (OUT3)	$V_{(EN3)}$ = GND, I_O = 1 mA	15	30	55	Ω
	Line regulation	I_O = 30 mA, V_I = 2.9 V to 4.5 V		0.02		%/V
	Load regulation	1 mA ≤ I_O ≤ 80 mA		–0.4		%/A

5.6 Timing Requirements

		MIN	TYP	MAX	UNIT
CTRL INTERFACE					
$t_{w(high)}$	High-level pulse duration (CTRL)	2	10	25	µs
$t_{w(low)}$	Low-level pulse duration (CTRL)	2	10	25	µs
$t_{d(reset)}$	Reset time to ensure proper logic reset	100			µs

5.7 Switching Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CTRL INTERFACE						
$t_{d(on)}$	Turn-on delay time			300	400	µs
$t_{d(off)}$	Turn-off delay time		30		80	µs
$t_{d(store)}$	Data storage / accept time period		30		80	µs
TPS65651 PROTECTION AND DISCHARGE						
$t_{d(short)}$	Short-circuit detection delay during start up (OUT1)		32	40	48	ms
	Short-circuit detection delay during operation (OUT1)		3.2	4	4.8	ms
	Short-circuit detection delay during start up (OUT2)		32	40	48	ms
	Short-circuit detection delay during operation (OUT2)		3.2	4	4.8	ms
	Short-circuit detection delay during operation (OUT3)		3.2	4	4.8	ms
$t_{d(overload)}$	Overload detection delay (OUT3)		3.2	4	4.8	ms
$t_{d(discharge)}$	Discharge time after CTRL goes high (OUT2)		32	40	48	ms
TPS65651A/B PROTECTION AND DISCHARGE						
$t_{d(short)}$	Short-circuit detection delay during start up (OUT1)		8	10	12	ms
	Short-circuit detection delay during operation (OUT1)		0.8	1	1.3	ms
	Short-circuit detection delay during start up (OUT2)		16	20	24	ms
	Short-circuit detection delay during operation (OUT2)		0.8	1	1.3	ms
	Short-circuit detection delay during operation (OUT3)		0.8	1	1.3	ms
$t_{d(overload)}$	Overload detection delay (OUT3)		0.8	1	1.3	ms
$t_{d(discharge)}$	Discharge time after CTRL goes high (OUT2)		8	10	12	ms
SWITCHING FREQUENCY						
	AVDD boost converter switching frequency	I_O = 30 mA	1.3	1.6	1.75	MHz
	ELVDD boost converter switching frequency	I_O = 100 mA	1.3	1.6	1.75	MHz
	ELVSS inverting buck-boost converter switching frequency	I_O = 100 mA		1.6		MHz

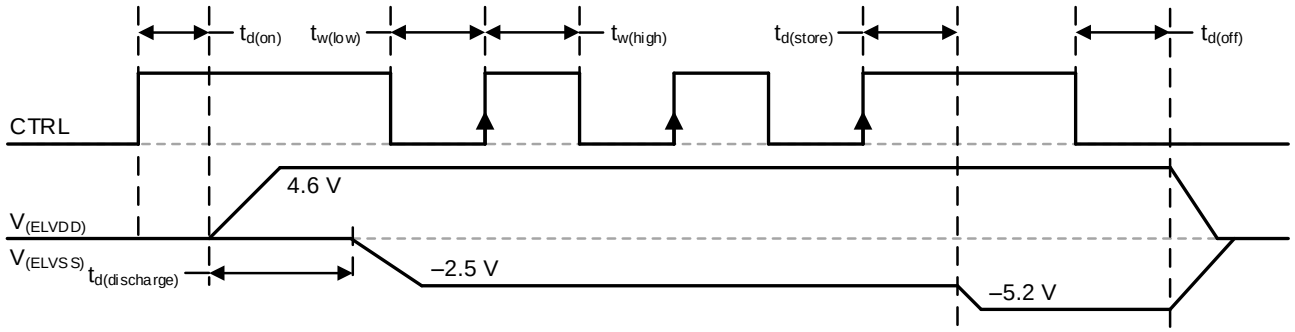


Figure 1. Timing Diagram

6 Typical Characteristics

V_I = 3.7 V unless otherwise noted.

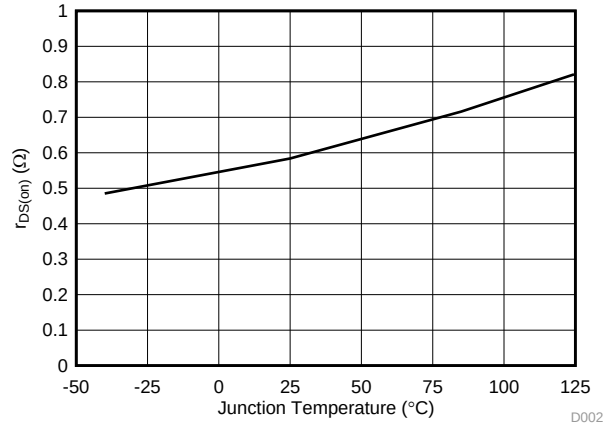


Figure 2. AVDD Boost Converter Switch $r_{DS(on)}$ (Q5)

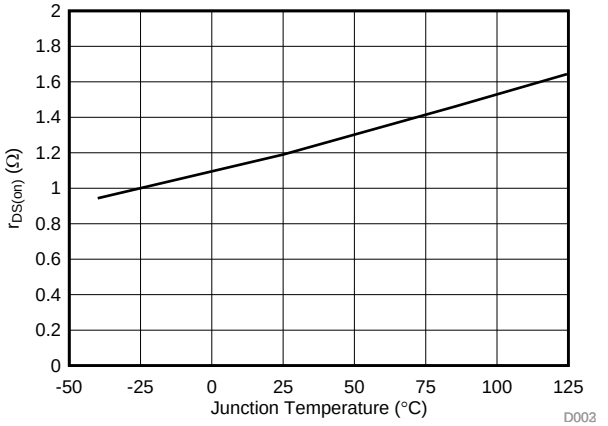


Figure 3. AVDD Boost Converter Rectifier $r_{DS(on)}$ (Q6)

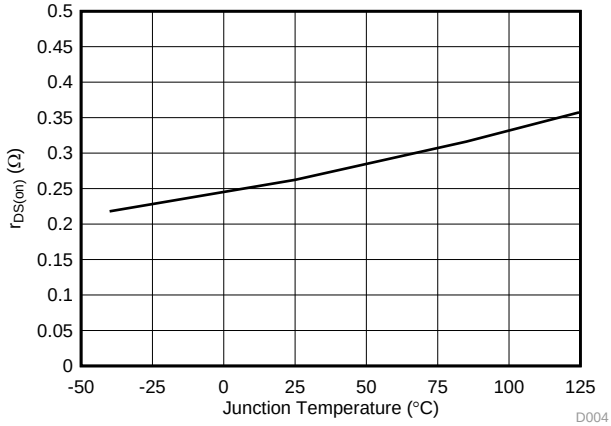


Figure 4. ELVDD Boost Converter Switch $r_{DS(on)}$ (Q1)

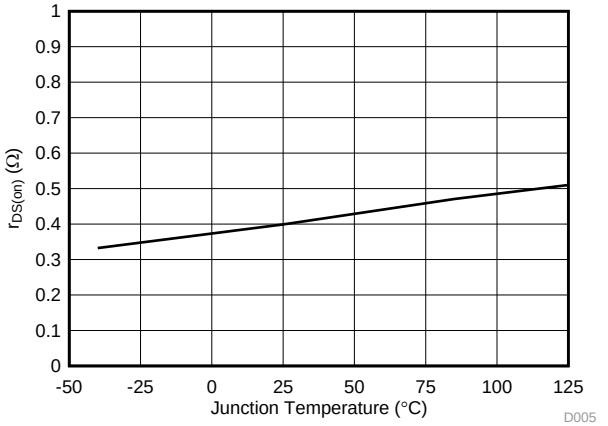


Figure 5. ELVDD Boost Converter Rectifier $r_{DS(on)}$ (Q2)

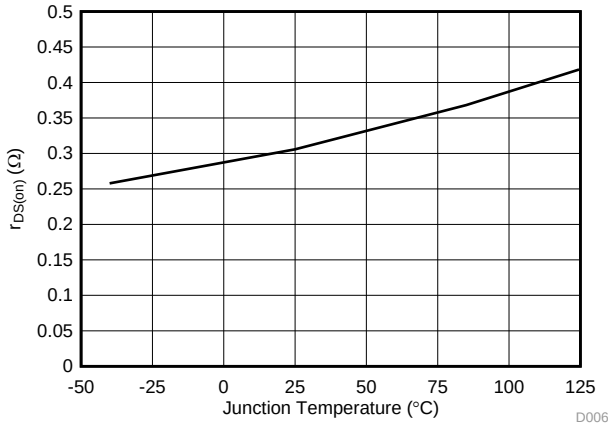


Figure 6. ELVSS Inverting Buck-Boost Converter Switch $r_{DS(on)}$ (Q3)

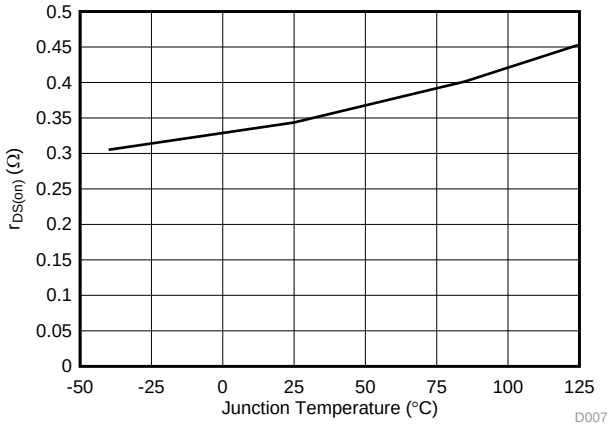


Figure 7. ELVSS Inverting Buck-Boost Converter Rectifier $r_{DS(on)}$ (Q4)

Typical Characteristics (continued)

V_I = 3.7 V unless otherwise noted.

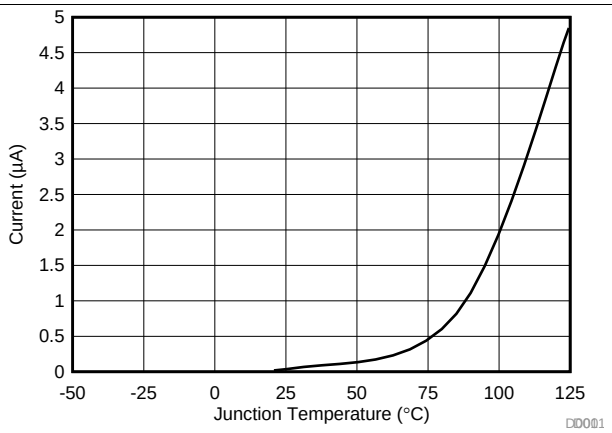


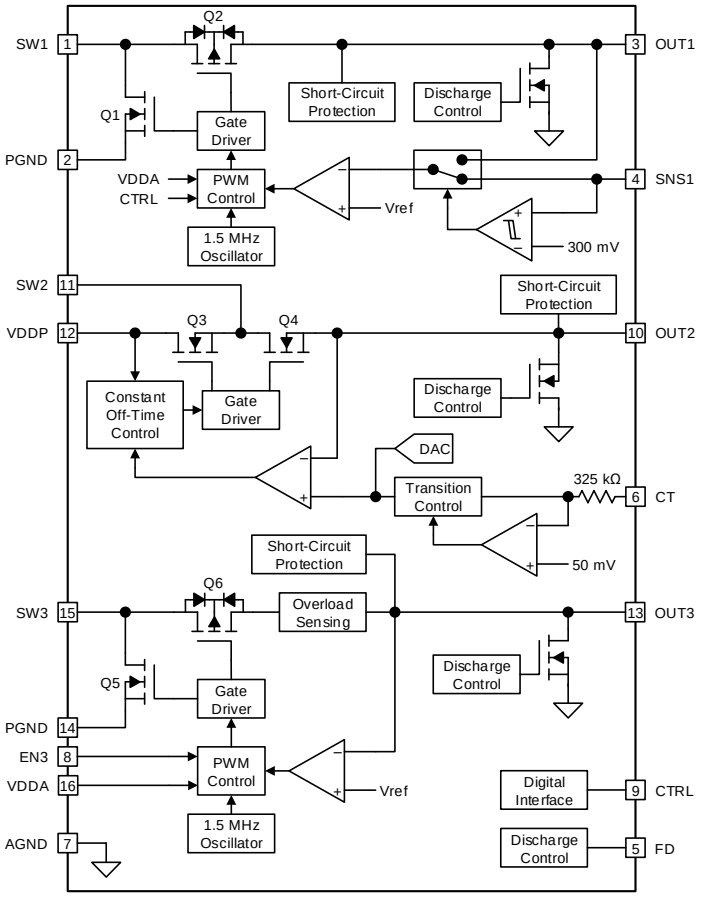
Figure 8. Shutdown Current into VDDA, VDDP, SW1 and SW3

7 Detailed Description

7.1 Overview

The TPS65651/A/B consists of two boost converters and an inverting buck-boost converter. $V_{(ELVDD)}$ is fixed at 4.6 V, $V_{(ELVSS)}$ is programmable in the range of –1.4 V to –5.4 V (default = –2.5 V) and $V_{(AVDD)}$ is fixed at 6.1 V for TPS65651/A or 7.6 V for TPS65651B. The transition time when $V_{(ELVSS)}$ is programmed to a different voltage is adjustable by the CT-pin capacitor.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Undervoltage Lockout

The device has a build in undervoltage lockout function that disables the device when the input supply voltage is too low for normal operation.

7.3.2 Thermal Shutdown

A thermal shutdown is implemented to prevent damage because of excessive heat and power dissipation. Once a temperature of typically 135°C is exceeded the device shuts down (the programming is not lost). When the temperature decreases to typ 130°C the device automatically restarts performing the start-up sequencing with the same voltages and programming as programmed before the thermal shutdown.

7.3.3 ELVDD Boost Converter (OUT1)

The ELVDD boost converter uses a fixed-frequency valley-current-mode topology. The output voltage $V_{(ELVDD)}$ is fixed at 4.6 V. In shutdown its output is fully isolated (input to output and output to input).

Feature Description (continued)

For the highest output voltage accuracy, connect the output sense pin (SNS1) directly to the positive pin of the output capacitor. If not used, the SNS1 pin can be left floating or connected to ground, then the output voltage is sensed at the OUT1 pin.

7.3.4 ELVSS Inverting Buck-Boost Converter (OUT2)

The ELVSS inverting buck-boost converter uses a constant-off-time peak-current-mode topology. The output voltage $V_{(ELVSS)}$ is adjustable between –5.4 V and –1.4 V with a default voltage of –2.5 V (see Table 2). In shutdown its output is fully isolated (input to output and output to input).

7.3.5 AVDD Boost Converter (OUT3)

The AVDD boost converter uses a fixed-frequency peak-current-mode topology. The output voltage $V_{(AVDD)}$ is fixed at 6.1 V for TPS65651/A and 7.6 V for TPS65651B . In shutdown its output is fully isolated (input to output and output to input).

7.3.6 Start-up Sequence, Soft-Start and Shut-down

The device has an implemented soft-start which limits the inrush current. When V_I is applied, the Output Discharge is undefined until the rising edge of CTRL sets the Output Discharge to follow the FD-pin setting. When the converters are disabled all outputs are discharged if FD = high or high impedant if FD = low. If only the AVDD converter is disabled (EN3 = low, CTRL = high) a forward biased diode charges the AVDD output to V_I until CTRL = low, then the AVDD output is disconnected from V_I. The typical start-up sequence is shown in Figure 9.

- Pulling EN3 high starts the AVDD boost converter. $V_{(AVDD)}$ follows a linear 1.5 ms long voltage ramp until it reaches 6.1 V (TPS65651/A) or 7.6 V (TPS65651B), then the switch current is limited to typ. 0.35 A.
- Pulling CTRL high starts the ELVDD boost converter. $V_{(ELVDD)}$ starts with a reduced switch current limit of 0.1 A until it reaches 4.6 V, then the full current limit is released.
- 40 ms (651) or 10 ms (651A/B) after CTRL is pulled high the ELVSS inverting buck-boost converter starts. $V_{(ELVSS)}$ starts with a reduced switch current limit of 0.4 A until it reaches its default voltage of –2.5 V, then the full current limit is released.

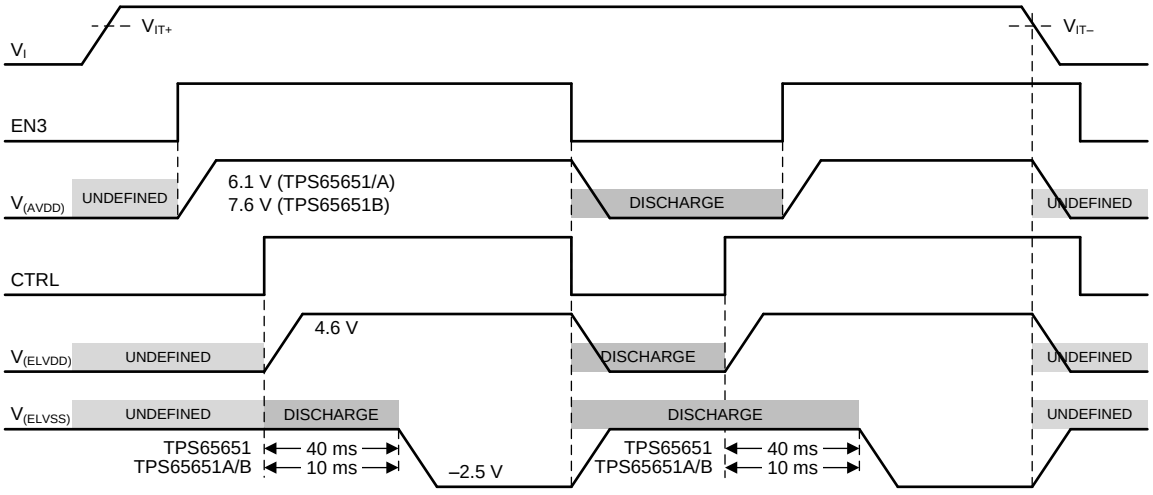


Figure 9. TPS65651/A/B Start-up Sequencing Active Discharge Enabled

Feature Description (continued)

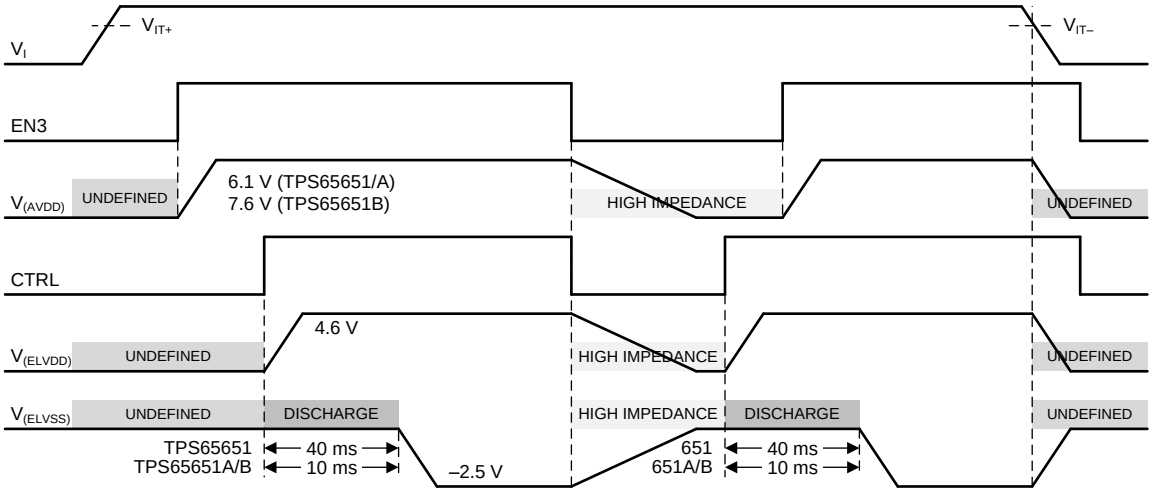


Figure 10. TPS65651/A/B Start-up Sequencing Active Discharge Disabled

7.3.7 $V_{(ELVSS)}$ Transition Time Control (CT Pin)

The transition time is the time required to move $V_{(ELVSS)}$ from the actual voltage level to the new programmed voltage level. The transition time can be controlled by an external capacitor connected to the CT pin. For the first $V_{(ELVSS)}$ voltage level change the transition time is as fast as possible, for all following $V_{(ELVSS)}$ changes the transition time is controlled by the capacitor connected to the CT pin. The typical 50 mV CT pin comparator detects when the CT pin is connected to GND or floating, then the fastest possible transition time is used. When a capacitor is connected the R-C time constant τ sets the transition time. The output voltage is almost settled after 3τ, which means 95% of the target voltage is reached.

$$\tau = \text{Internal CT resistance x external capacitor} = R_{(CT)} \times C_{(CT)} = 325\ k\Omega \times 100\ nF = 32.5\ ms \quad (1)$$

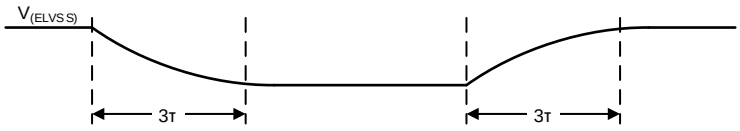


Figure 11. $V_{(ELVSS)}$ Transition Time Control

Feature Description (continued)

7.3.8 Digital Interface (CTRL Pin)

The digital interface allows programming of the negative output voltage $V_{(ELVSS)}$ in discrete steps. If programming is not required the CTRL pin can also be used as a standard enable pin. Once the device is enabled the device starts with its default values (blue marked values in Table 2). The interface counts the rising edges applied to the CTRL pin and sets the new values as shown in Table 2. The settings are stored in a volatile memory, the reset behavior is described in the Device Reset section.

Table 2. Programming Table

Rising Edges	$V_{(ELVSS)}$	Rising Edges	$V_{(ELVSS)}$
0 / no pulse	–2.5 V	21	–3.4 V
1	–5.4 V	22	–3.3 V
2	–5.3 V	23	–3.2 V
3	–5.2 V	24	–3.1 V
4	–5.1 V	25	–3.0 V
5	–5.0 V	26	–2.9 V
6	–4.9 V	27	–2.8 V
7	–4.8 V	28	–2.7 V
8	–4.7 V	29	–2.6 V
9	–4.6 V	30	–2.5 V
10	–4.5 V	31	–2.4 V
11	–4.4 V	32	–2.3 V
12	–4.3 V	33	–2.2 V
13	–4.2 V	34	–2.1 V
14	–4.1 V	35	–2.0 V
15	–4.0 V	36	–1.9 V
16	–3.9 V	37	–1.8 V
17	–3.8 V	38	–1.7 V
18	–3.7 V	39	–1.6 V
19	–3.6 V	40	–1.5 V
20	–3.5 V	41	–1.4 V

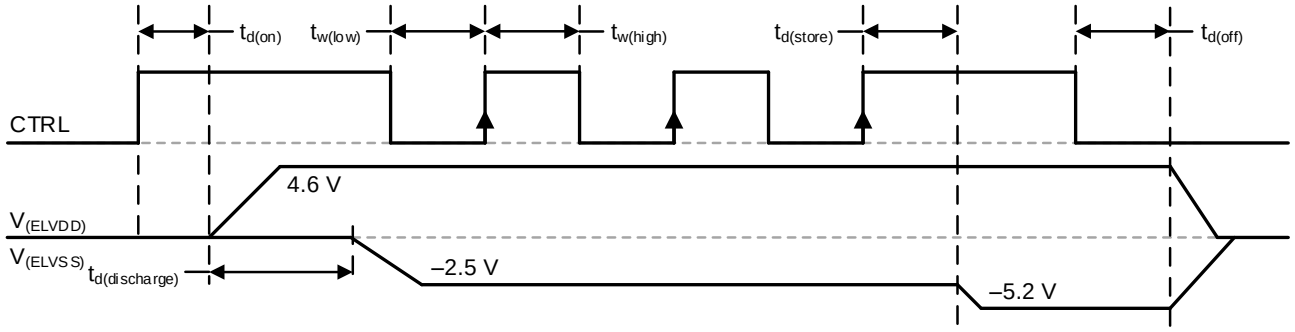


Figure 12. Timing Diagram

Feature Description (continued)

7.3.9 Short Circuit and Overload Protection

The device is protected against short of $V_{(AVDD)}$, $V_{(ELVDD)}$ and $V_{(ELVSS)}$ to ground. $V_{(ELVDD)}$ and $V_{(ELVSS)}$ are also protected when they are shorted together. A short at any converter shuts down the whole device, the shut-down state is latched, input and outputs are fully disconnected. To reset the whole device V_I has to cycle below Undervoltage Lockout or EN3 and CTRL have to be low at the same time for minimum $t_{d(reset)}$. The device detects a short when one of the below conditions is fulfilled:

Startup:

- $V_{(ELVDD)}$ is not in regulation 40 ms (651) or 10 ms (651A/B) after $V_{(ELVDD)}$ is enabled (40 ms or 10 ms CTRL = HIGH) → shut-down all
- $V_{(ELVSS)}$ is not in regulation 40 ms (651) or 10 ms (651A/B) after $V_{(ELVSS)}$ is enabled (80 ms or 20 ms after CTRL = HIGH) → shut-down all
- $V_{(AVDD)}$ protection is enabled when the soft-start is completed.

During Operation:

- $V_{(AVDD)}$ falls below 90% of its programmed voltage longer than 4 ms (651) or 1 ms (651A/B) → shut-down all
- $V_{(ELVDD)}$ falls below 90% of its programmed voltage longer than 4 ms (651) or 1 ms (651A/B) → shut-down all
- $V_{(ELVSS)}$ rises above 500 mV of its programmed voltage longer than 4 ms (651) or 1 ms (651A/B) → shut-down all

7.3.10 Enable / Disable Active Discharge During Shutdown

The Active Discharge during shutdown can be enabled and disabled by the FD pin.

- FD pin connected to GND
  → Active discharge is disabled and all outputs are high impedance.
- FD pin connected to HIGH (V_{IH} > 1.2 V)
  → Active discharge is enabled and all outputs are discharged.

7.3.11 Device Reset

- A power cycle resets all settings to default values as well as the short-circuit protection .
- When CTRL is low for $t_{d(reset)}$ then $V_{(ELVSS)}$ is reset to default value
  → –2.5 V.
- EN3 and CTRL are low at the same time for $t_{d(reset)}$
  → Short-circuit protection is reset.

7.4 Device Functional Modes

7.4.1 Operation with V_I < 2.9 V

The recommended minimum input supply voltage for full performance is 2.9 V. The device continues to operate with input supply voltages below 2.9 V, however, full performance is not ensured. The device does not operate with input supply voltages below the Undervoltage Lockout threshold.

7.4.2 Operation with V_I > 4.4 V (Diode Mode for $V_{(ELVDD)}$)

For V_I > 4.4 V the ELVDD boost converter cannot support the duty cycle anymore. It enables its build in Diode-Mode which enables the converter to regulate the output voltage even when the input supply is very close or higher than the output. When operating in Diode-Mode the converter's rectifier switch stops switching and regulates the output voltage. The efficiency during Diode-Mode operation is reduced. At low output current (< 2 mA), the converter automatically transitions from pulse-width modulation to pulse-skip mode. This ensures that $V_{(ELVDD)}$ stays in regulation, but increases the output voltage ripple.

8 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

Figure 13 shows a typical application circuit suitable for supplying AMOLED displays in smartphone applications. The circuit is designed to operate from a single-cell Li-Ion battery and generates positive output voltages $V_{(AVDD)}$ of 6.1 V (TPS65651/A) or 7.6 V (TPS65651B) and $V_{(ELVDD)}$ of 4.6 V as well as a negative output voltage $V_{(ELVSS)}$ of –2.5 V. ELVDD and ELVSS are capable of supplying up to 300 mA of output current.

8.2 Typical Application

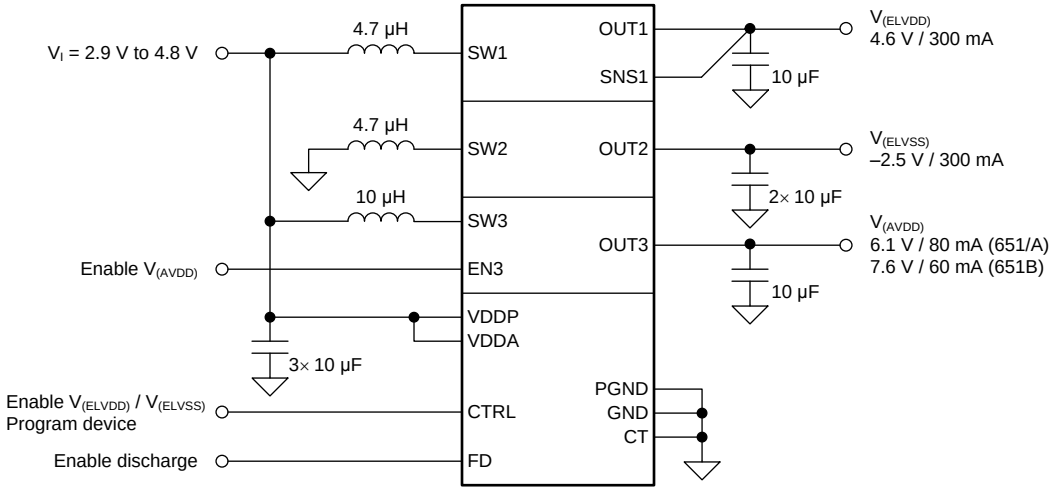


Figure 13. Typical Application Schematic

8.2.1 Design Requirements

For this design example, use the following input parameters in Table 3.

Table 3. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	2.9 V to 4.8 V
Output voltage	$V_{(AVDD)}$ = 6.1 V, $V_{(ELVDD)}$ = 4.6 V, $V_{(ELVSS)}$ = –2.5 V
Switching frequency	ELVDD, ELVSS and AVDD = 1.6 MHz

8.2.2 Detailed Design Procedure

In order to maximize performance, the device has been optimized for use with a relatively narrow range of component values. The $V_{(AVDD)}$ boost converter typically requires a 10-µH inductor, $V_{(ELVDD)}$ and $V_{(ELVSS)}$ require a 4.7-µH inductor. Ceramic capacitors are usually used for input and output capacitors. It is recommended to use the suggested values in all applications. Customers using other values are strongly recommended to characterize circuit performance on a case-by-case basis.

8.2.2.1 ELVDD Boost Converter (OUT1)

8.2.2.1.1 Inductor Selection

The main parameter for the inductor selection is the inductor saturation current, which must be higher than the peak switch current. Inductors with lower saturation current than the minimum switch current limit can be used when the maximum output current is not required, however a minimum saturation current of 0.5 A is required to ensure proper startup. The minimum required saturation current is calculated by the peak inductor current formula.

The inductors DC resistance as well as its core losses affect the efficiency. Lower DC resistance results in higher high load efficiency. The core losses are especially important for light load efficiency. The core material as well as the inductors physical size has an influence on the core losses. The higher the quality factor Q of the inductor at the switching frequency (1.6 MHz) the lower the core losses. Table 4 shows examples of suitable inductors, equivalent parts can be used.

- Minimum 3.3-µH, maximum 6.1-µH inductance.
- Minimum 0.5-A saturation current, for full output current capability 1.3 A.
- Minimum V_I and maximum I_O must be taken to calculate the required saturation current.
- Duty Cycle: $$D = \frac{V_O - V_I \times \eta}{V_O}$$
  where
  - V_I is the boost converter input supply voltage.
  - V_O is the boost converter output voltage.
  - η is the boost converter efficiency (taken from the Application Curves or 80% as an assumption).
- Peak Inductor Current: $$I_{(SW)M} = \frac{I_O}{1 - D} + \frac{V_I \times D}{2 \times f \times L}$$
  where
  - I_O is the boost converter output current.
  - f = 1.6 MHz (the boost converter switching frequency).
  - L is the boost converter inductance (4.7 µH).

Table 4. ELVDD Boost Converter (OUT1) Inductor Selection

INDUCTANCE	I_{SAT}	DCR	MANUFACTURER(1)	PART NUMBER	DIMENSIONS
4.7 µH	1.9 A	200 mΩ	TOKO	DFE252012C-4R7M	2.5 mm × 2.0 mm × 1.2 mm
	2.2 A	165 mΩ	TOKO	DFE252012P-4R7M	2.5 mm × 2.0 mm × 1.2 mm
	1.5 A	175 mΩ	ALPS	GLCLM4R701A	2.5 mm × 2.0 mm × 1.2 mm
	1.5 A	230 mΩ	ALPS	GLCLK4R701A	2.5 mm × 2.0 mm × 1 mm

(1) See Third-party Products disclaimer.

8.2.2.1.2 Capacitor Selection

The main parameter for the capacitor selection is the capacitance at the operating voltage. The more voltage is applied at the capacitor the lower is its resulting capacitance (DC-bias effect), also temperature and AC-Voltage changes the capacitance, however the DC-bias effect is dominant. For best voltage filtering (lowest voltage ripple), low ESR capacitors are recommended. Table 5 and Table 6 show examples of suitable capacitors, equivalent parts can be used.

Input Capacitor:

- Minimum 2.5-µF resulting capacitance.
- Minimum 6.3-V voltage rating.

Output Capacitor:

- Minimum 2.5-µF, maximum 24-µF resulting capacitance.
- Minimum 6.3-V voltage rating.

Table 5. Input Capacitor Selection ELVDD Boost Converter (OUT1)

CAPACITANCE	VOLTAGE RATING	MANUFACTURER(1)	PART NUMBER	SIZE
10 µF	6.3 V	muRata	GRM188R60J106ME84	0603
10 µF	10 V	muRata	GRM219R61A106ME47	0805
22 µF	10 V	Samsung	CL21A226MPCLRNC	0805

(1) See Third-party Products disclaimer.

Table 6. Output Capacitor Selection ELVDD Boost Converter (OUT1)

CAPACITANCE	VOLTAGE RATING	MANUFACTURER(1)	PART NUMBER	SIZE
10 µF	10 V	muRata	GRM219R61A106ME47	0805
22 µF	10 V	Samsung	CL21A226MPCLRNC	0805

(1) See Third-party Products disclaimer.

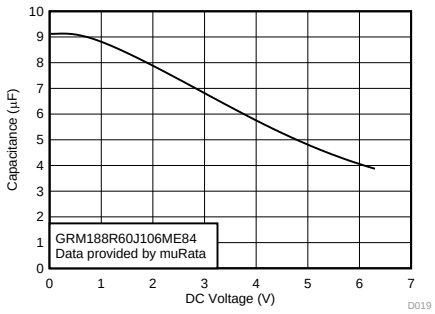


Figure 14. GRM188R60J106ME84

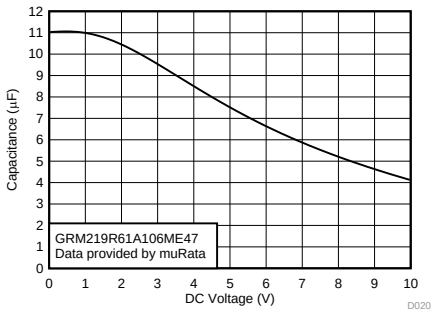


Figure 15. GRM219R61A106ME47

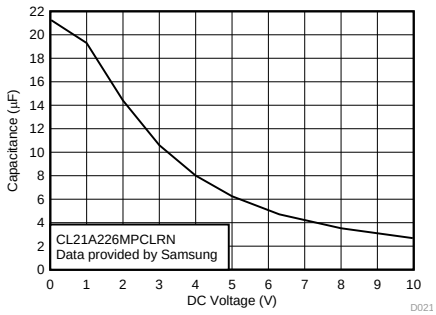


Figure 16. CL21A226MPCLRN

8.2.2.2 ELVSS Inverting Buck-Boost Converter (OUT2)

8.2.2.2.1 Inductor Selection

The main parameter for the inductor selection is the inductor saturation current, which must be higher than the peak switch current. Inductors with lower saturation current than the minimum switch current limit can be used when the maximum output current is not required, however a minimum saturation current of 0.5 A is required to ensure proper startup. The minimum required saturation current is calculated by the peak inductor current formula.

The inductors DC resistance as well as its core losses affect the efficiency. Lower DC resistance results in higher high load efficiency. The core losses are especially important for light load efficiency. The core material as well as the inductors physical size has an influence on the core losses. The higher the quality factor Q of the inductor at the switching frequency (1.6 MHz) the lower the core losses. Table 7 shows examples of suitable inductors, equivalent parts can be used.

- Minimum 3.3-µH, maximum 6.1-µH inductance.
- Minimum 0.5-A saturation current, for full output current capability 1.5 A.
- Minimum V_I and maximum I_O must be taken to calculate the required saturation current.
- Duty Cycle:

$$D = \frac{V_O}{V_O - V_I \times \eta}$$

  where
  - V_I is the inverting buck-boost converter input supply voltage.
  - V_O is the inverting buck-boost converter output voltage.
  - η is the inverting buck-boost converter efficiency (taken from the Application Curves or 80% as an assumption).

- Peak Inductor Current: $$I_{(SW)M} = \frac{I_O}{1 - D} + \frac{V_I \times D}{2 \times f \times L}$$
  where
  - I_O is the inverting buck-boost converter output current.
  - f = 1.6 MHz (the inverting buck-boost converter switching frequency).
  - L is the inverting buck-boost converter inductance (4.7 µH).

Table 7. ELVSS Inverting Buck-Boost Converter (OUT2) Inductor Selection

INDUCTANCE	I_{SAT}	DCR	MANUFACTURER(1)	PART NUMBER	DIMENSIONS
4.7 µH	1.9 A	200 mΩ	TOKO	DFE252012C-4R7M	2.5 mm × 2.0 mm × 1.2 mm
	2.2 A	165 mΩ	TOKO	DFE252012P-4R7M	2.5 mm × 2.0 mm × 1.2 mm
	1.5 A	175 mΩ	ALPS	GLCLM4R701A	2.5 mm × 2.0 mm × 1.2 mm
	1.5 A	230 mΩ	ALPS	GLCLK4R701A	2.5 mm × 2.0 mm × 1 mm

(1) See Third-party Products disclaimer.

8.2.2.2.2 Capacitor Selection

The main parameter for the capacitor selection is the capacitance at the operating voltage. The more voltage is applied at the capacitor the lower is its resulting capacitance (DC-bias effect), also temperature and AC-Voltage changes the capacitance, however the DC-bias effect is dominant. For best voltage filtering (lowest voltage ripple), low ESR capacitors are recommended. Table 8 and Table 9 show examples of suitable capacitors, equivalent parts can be used.

Input Capacitor:

- Minimum 2.5-µF resulting capacitance.
- Minimum 6.3-V voltage rating.

Output Capacitor:

- Minimum 2.5-µF, maximum 24-µF resulting capacitance.
- Minimum 10-V voltage rating, when maximum –6 V are used also 6.3 V rated capacitors can be used.

Table 8. Input Capacitor Selection ELVSS Inverting Buck-Boost Converter (OUT2)

CAPACITANCE	VOLTAGE RATING	MANUFACTURER(1)	PART NUMBER	SIZE
10 µF	6.3 V	muRata	GRM188R60J106ME84	0603
10 µF	10 V	muRata	GRM219R61A106ME47	0805
22 µF	10 V	Samsung	CL21A226MPCLRNC	0805

(1) See Third-party Products disclaimer.

Table 9. Output Capacitor Selection ELVSS Inverting Buck-Boost Converter (OUT2)

CAPACITANCE	VOLTAGE RATING	MANUFACTURER(1)	PART NUMBER	SIZE
10 µF	10 V	muRata	GRM219R61A106ME47	0805
22 µF	10 V	Samsung	CL21A226MPCLRNC	0805

(1) See Third-party Products disclaimer.

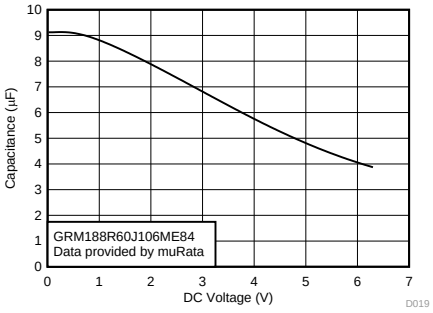


Figure 17. GRM188R60J106ME84

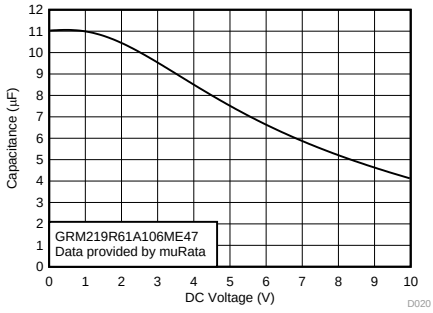


Figure 18. GRM219R61A106ME47

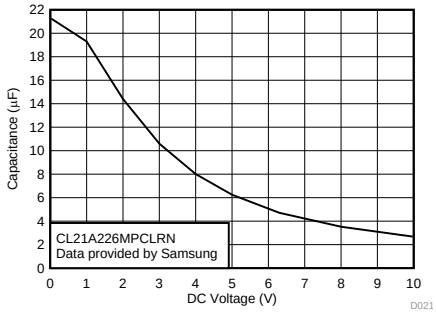


Figure 19. CL21A226MPCLRN

8.2.2.2.3 AVDD Boost Converter (OUT3)

8.2.2.2.3.1 Inductor Selection

The main parameter for the inductor selection is the inductor saturation current, which must be higher than the peak switch current. Inductors with lower saturation current than the minimum switch current limit can be used when the maximum output current is not required, however a minimum saturation current of 0.2 A is required to ensure proper startup. The minimum required saturation current is calculated by the peak inductor current formula.

The inductors DC resistance as well as its core losses affect the efficiency. Lower DC resistance results in higher high load efficiency. The core losses are especially important for light load efficiency. The core material as well as the inductors physical size has an influence on the core losses. The higher the quality factor Q of the inductor at the switching frequency (1.6 MHz) the lower the core losses. Table 10 shows examples of suitable inductors, equivalent parts can be used.

- Minimum 7-µH, maximum 13-µH inductance.
- Minimum 0.2-A saturation current, for full output current capability 0.25 A.
- Minimum V_I and maximum I_O must be taken to calculate the required saturation current.

- Duty Cycle:

$$D = \frac{V_O - V_I \times \eta}{V_O}$$

  where
  - V_I is the boost converter input supply voltage.
  - V_O is the boost converter output voltage.
  - η is the boost converter efficiency (taken from the Application Curves or 80% as an assumption).

- Peak Inductor Current:

$$I_{(SW)M} = \frac{I_O}{1 - D} + \frac{V_I \times D}{2 \times f \times L}$$

  where
  - I_O is the boost converter output current.
  - f = 1.6 MHz (the boost converter switching frequency).
  - L is the boost converter inductance (10 µH).

Table 10. AVDD Boost Converter (OUT3) Inductor Selection

INDUCTANCE	I_{SAT}	DCR	MANUFACTURER(1)	PART NUMBER	DIMENSIONS
10 µH	1.3 A	400 mΩ	TOKO	DFE252012C-100M	2.5 mm × 2.0 mm × 1.2 mm
	1.2 A	530 mΩ	TOKO	DFE252010C-100M	2.5 mm × 2.0 mm × 1 mm
	0.75 A	600 mΩ	Taiyo Yuden	MDKK2020T-100MM	2 mm × 2 mm × 1 mm
	0.8 A	359 mΩ	CYNTEC	SDET25201B-100MS	2.5 mm × 2 mm × 1.2 mm
	0.48 A	817 mΩ	CYNTEC	SDER20121T-100MS	2.0 mm × 1.2 mm × 1 mm

(1) See Third-party Products disclaimer.

8.2.2.2.3.2 Capacitor Selection

The main parameter for the capacitor selection is the capacitance at the operating voltage. The more voltage is applied at the capacitor the lower is its resulting capacitance (DC-bias effect), also temperature and AC-Voltage changes the capacitance, however the DC-bias effect is dominant. For best voltage filtering (lowest voltage ripple), low ESR capacitors are recommended. Table 11 and Table 12 show examples of suitable capacitors, equivalent parts can be used.

Input Capacitor:

- Minimum 2.5-µF resulting capacitance.
- Minimum 6.3-V voltage rating.

Output Capacitor:

- Minimum 2.5-µF, maximum 24-µF resulting capacitance.
- Minimum 10-V voltage rating.

Table 11. Input Capacitor Selection AVDD Boost Converter (OUT3)

CAPACITANCE	VOLTAGE RATING	MANUFACTURER(1)	PART NUMBER	SIZE
10 µF	6.3 V	muRata	GRM188R60J106ME84	0603
10 µF	10 V	muRata	GRM219R61A106ME47	0805
22 µF	10 V	Samsung	CL21A226MPCLRNC	0805

(1) See Third-party Products disclaimer.

Table 12. Output Capacitor Selection AVDD Boost Converter (OUT3)

CAPACITANCE	VOLTAGE RATING	MANUFACTURER(1)	PART NUMBER	SIZE
10 µF	10 V	muRata	GRM219R61A106ME47	0805
22 µF	10 V	Samsung	CL21A226MPCLRNC	0805

(1) See Third-party Products

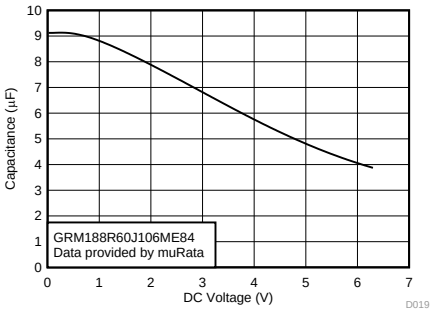


Figure 20. GRM188R60J106ME84

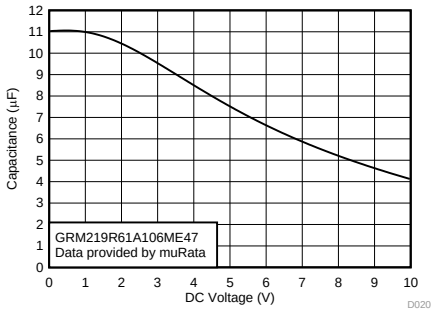


Figure 21. GRM219R61A106ME47

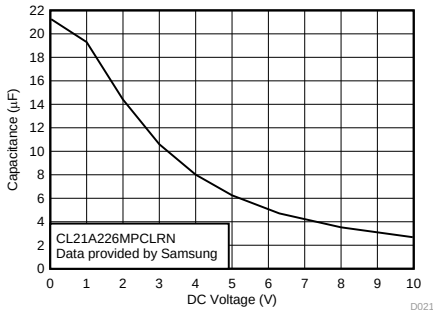


Figure 22. CL21A226MPCLRN

8.2.3 $V_{(ELVDD)}$ & $V_{(ELVSS)}$ Output Current > 300 mA

The TPS65651/A/B is designed to supply output currents up to 300 mA on $V_{(ELVDD)}$ & $V_{(ELVSS)}$ for the full recommended V_I and V_{OUT} range. For special conditions the device can support higher currents as well. Figure 23 shows the maximum supported output current for different V_I and $V_{(ELVSS)}$ voltages. The output current depends on:

- The used inductor → low DCR < 200 mΩ as well as sufficient I_{SAT} is needed.
- The input voltage V_I → the higher V_I the more output current can be supported.
- The $V_{(ELVSS)}$ output voltage → the lower the voltage (more negative) the lower the supported output current.

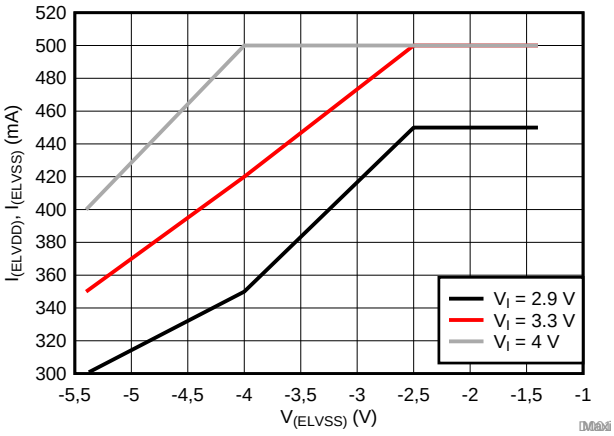
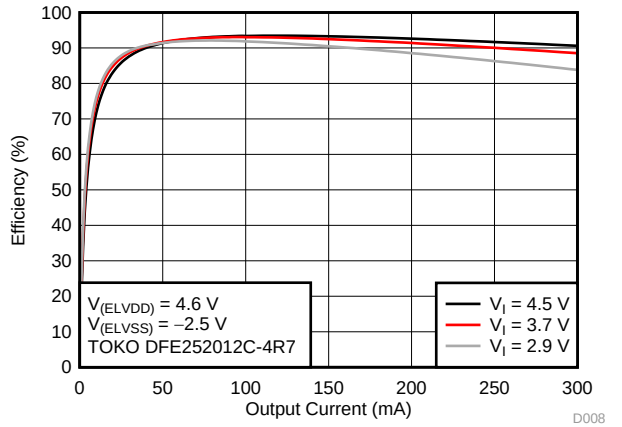


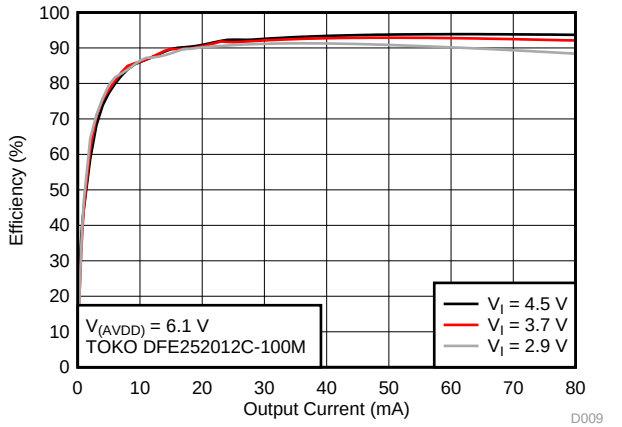
Figure 23. Supported Output Current

8.2.4 Application Curves



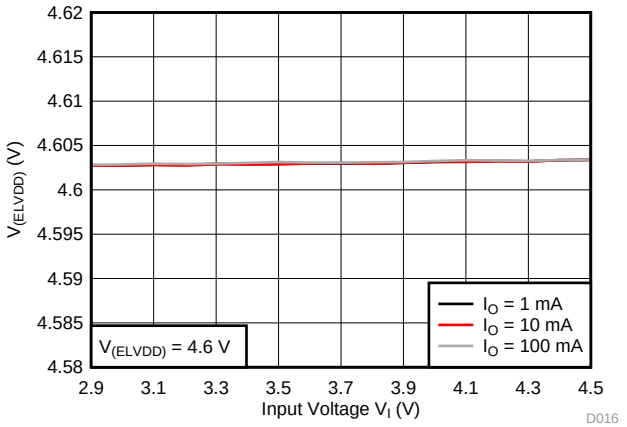
$V_{(ELVDD)}$ = 4.6 V $V_{(ELVSS)}$ = –2.5 V V_I = 2.9 V, 3.7 V, 4.5 V
EN3 = GND CTRL = V_I

Figure 24. $V_{(ELVDD)}$ and $V_{(ELVSS)}$ Combined Efficiency



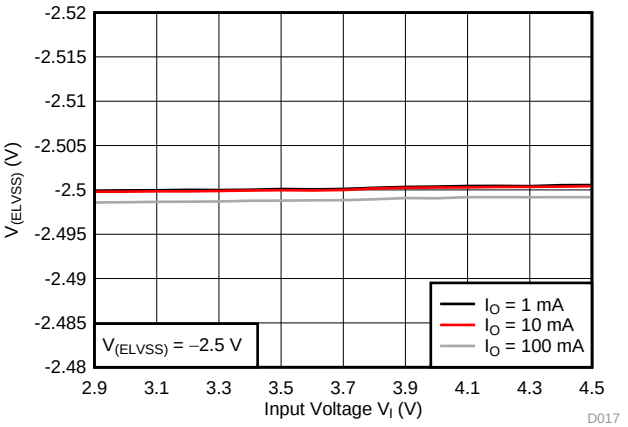
$V_{(AVDD)}$ = 6.1 V V_I = 2.9 V, 3.7 V, 4.5 V
EN3 = V_I CTRL = GND

Figure 25. $V_{(AVDD)}$ Efficiency



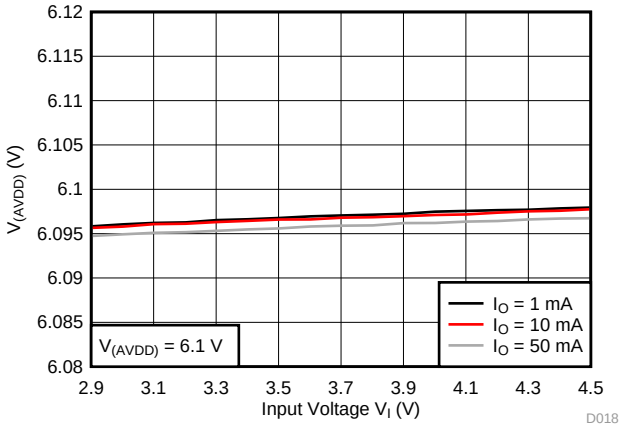
$V_{(ELVDD)}$ = 4.6 V V_I = 2.9 V to 4.5 V
EN3 = GND CTRL = V_I

Figure 26. $V_{(ELVDD)}$ Line Regulation



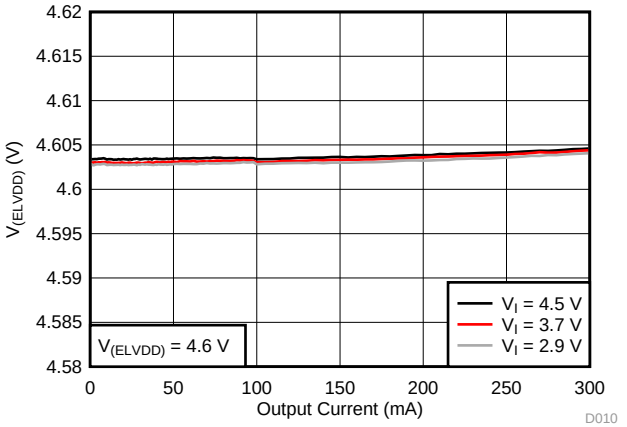
$V_{(ELVSS)}$ = –2.5 V V_I = 2.9 V to 4.5 V
EN3 = GND CTRL = V_I

Figure 27. $V_{(ELVSS)}$ Line Regulation



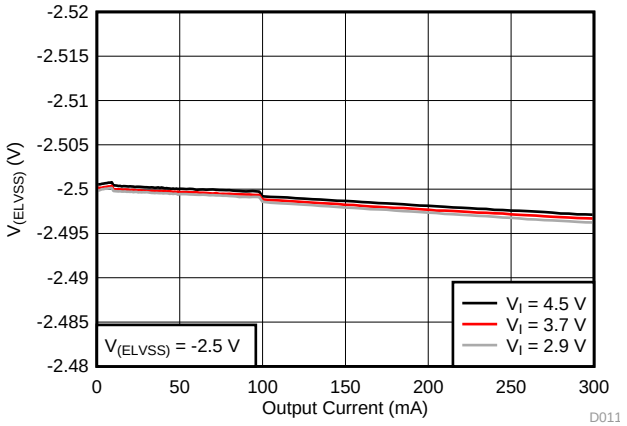
$V_{(AVDD)}$ = 6.1 V V_I = 2.9 V to 4.5 V
EN3 = V_I CTRL = GND

Figure 28. $V_{(AVDD)}$ Line Regulation



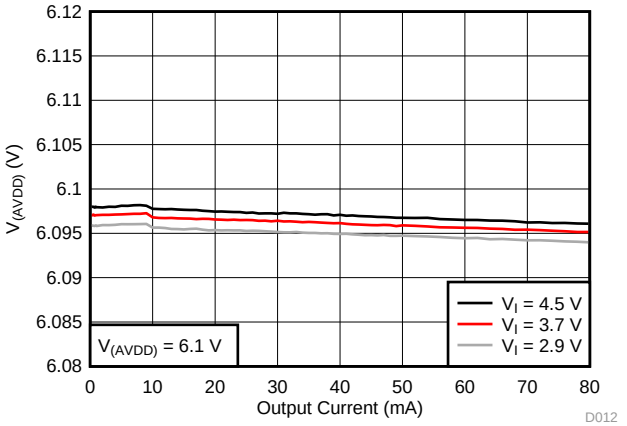
$V_{(ELVDD)}$ = 4.6 V V_I = 2.9 V, 3.7 V, 4.5 V
EN3 = GND CTRL = V_I

Figure 29. $V_{(ELVDD)}$ Load Regulation



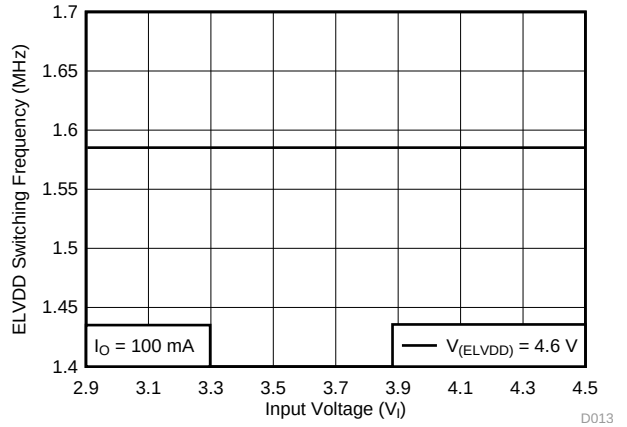
$V_{(ELVSS)}$ = –2.5 V V_I = 2.9 V, 3.7 V, 4.5 V
EN3 = GND CTRL = V_I

Figure 30. $V_{(ELVSS)}$ Load Regulation



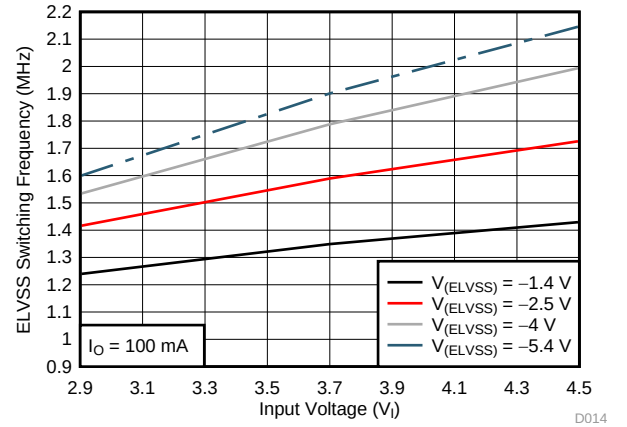
$V_{(AVDD)}$ = 6.1 V V_I = 2.9 V, 3.7 V, 4.5 V
EN3 = V_I CTRL = GND

Figure 31. $V_{(AVDD)}$ Load Regulation



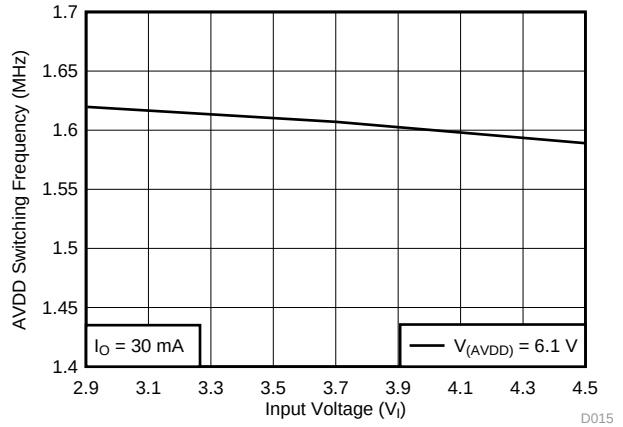
$V_{(ELVDD)}$ = 4.6 V V_I = 2.9 V to 4.5 V
EN3 = GND CTRL = V_I

Figure 32. ELVDD Converter Switching Frequency



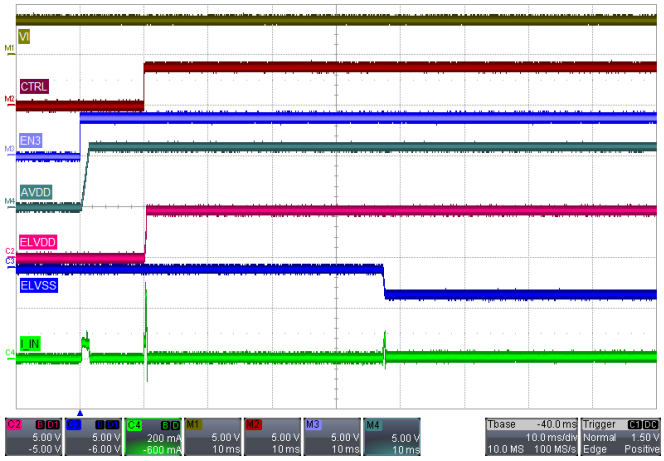
$V_{(ELVSS)}$ = –5.4 V to –1.4 V V_I = 2.9 V to 4.5 V
EN3 = GND CTRL = V_I

Figure 33. ELVSS Converter Switching Frequency



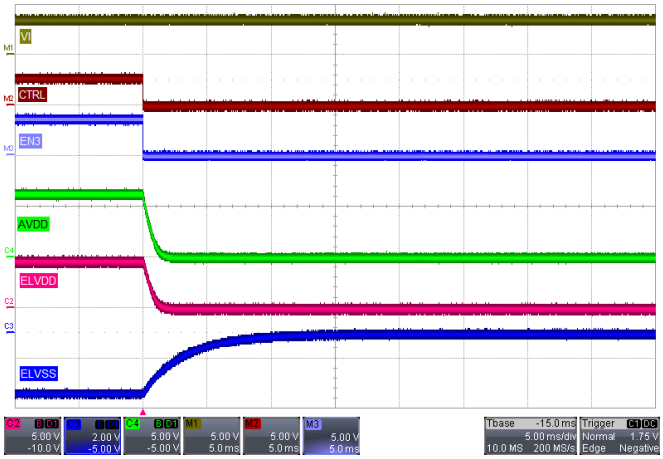
$V_{(AVDD)}$ = 6.1 V V_I = 2.9 V to 4.5 V
EN3 = V_I CTRL = GND

Figure 34. AVDD Converter Switching Frequency



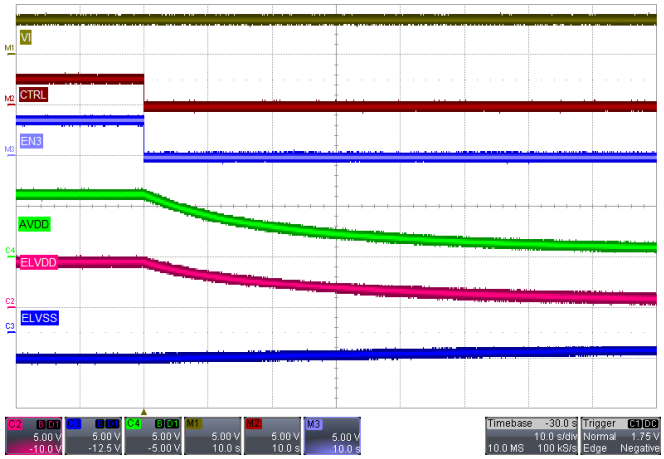
$V_{(AVDD)}$ = 6.1 V $V_{(ELVDD)}$ = 4.6 V $V_{(ELVSS)}$ = –2.5 V
EN3 = 3.3 V CTRL = 3.3 V FD = V_I

Figure 35. Startup Sequence



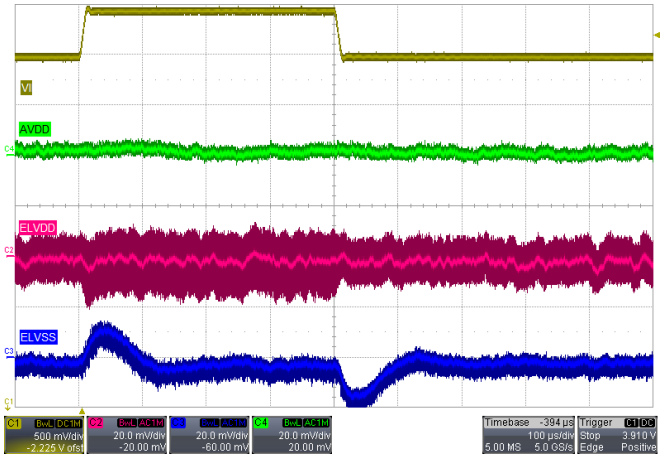
V_I = 3.7 V
$V_{(AVDD)}$ = 6.1 V $V_{(ELVDD)}$ = 4.6 V $V_{(ELVSS)}$ = –2.5 V
EN3 = 3.3 V CTRL = 2.5 V FD = V_I

Figure 36. Shutdown Sequence Discharge = ON



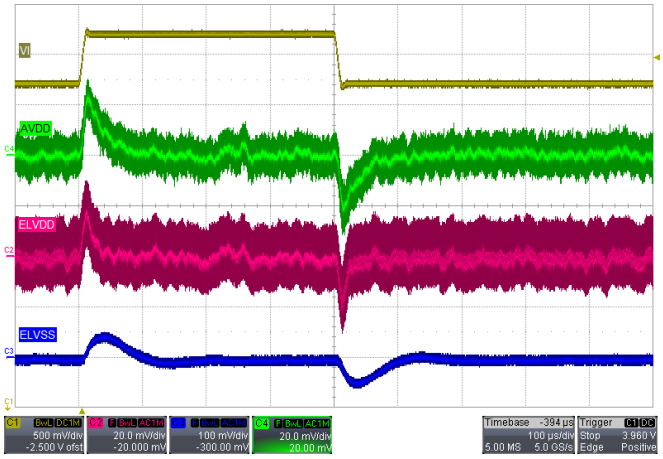
V_I = 3.7 V
$V_{(AVDD)}$ = 6.1 V $V_{(ELVDD)}$ = 4.6 V $V_{(ELVSS)}$ = –2.5 V
EN3 = 3.3 V CTRL = 2.5 V FD = GND

Figure 37. Shutdown Sequence Discharge = OFF



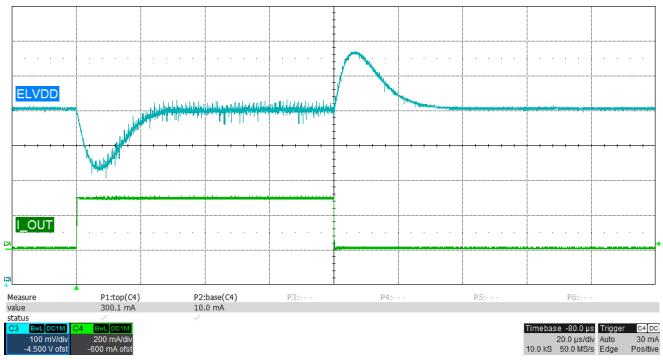
V_I = 3.7 V to 4.2 V
$I_{(AVDD)}$ = 0 mA
$I_{(ELVDD)}$ = 0 mA
$I_{(ELVSS)}$ = 0 mA
EN3 = V_I
CTRL = V_I
FD = V_I

Figure 38. Line Transient no load



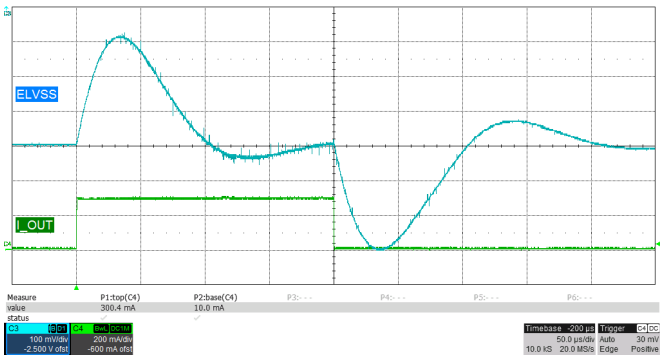
V_I = 3.7 V to 4.2 V
$I_{(AVDD)}$ = 55 mA
$I_{(ELVDD)}$ = 300 mA
$I_{(ELVSS)}$ = 300 mA
EN3 = V_I
CTRL = V_I
FD = V_I

Figure 39. Line Transient maximum load



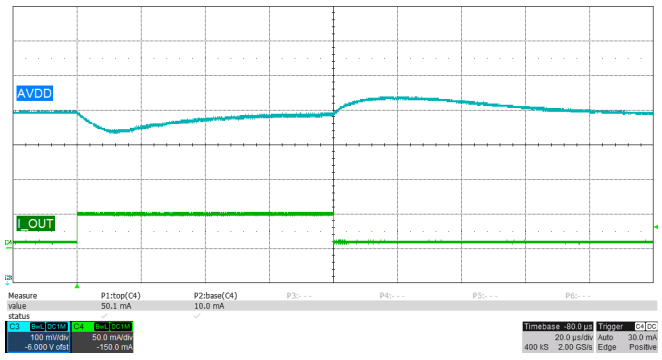
V_I = 3.7 V
$I_{(ELVDD)}$ = 10 mA to 300 mA
$I_{(ELVSS)}$ = 0 mA
$I_{(AVDD)}$ = 0 mA
EN3 = V_I
CTRL = V_I
FD = V_I

Figure 40. ELVDD Load Transient



V_I = 3.7 V
$I_{(ELVDD)}$ = 0 mA
$I_{(ELVSS)}$ = 10 mA to 300 mA
$I_{(AVDD)}$ = 0 mA
EN3 = V_I
CTRL = V_I
FD = V_I

Figure 41. ELVSS Load Transient



V_I = 3.7 V
$I_{(ELVDD)}$ = 0 mA
$I_{(ELVSS)}$ = 0 mA
$I_{(AVDD)}$ = 10 mA to 50 mA
EN3 = V_I
CTRL = V_I
FD = V_I

Figure 42. AVDD Load Transient

9 Power Supply Recommendations

The TPS65651/A/B device is designed to operate with input supplies from 2.9 V to 4.8 V. The input supply should be stable and free of noise if the device's full performance is to be achieved. If the input supply is located more than a few centimeters away from the device, additional bulk capacitance may be required. The input capacitance shown in the application schematics is sufficient for typical applications.

10 Layout

10.1 Layout Guideline

The PCB layout is an important step in the power supply design. An incorrect layout could cause converter instability, load regulation problems, noise, and EMI issues. Especially with a switching DC-DC converter at high load currents, too thin PCB traces can cause significant voltage spikes. Good grounding becomes important as well. If possible a common ground plane to minimize ground shifts between analog ground (GND) and power ground (PGND) is recommended.

- Place the input capacitor on VDDP and the output capacitor on OUT2 as close as possible to the device. Use short and wide traces to connect the input capacitor on VDDP and the output capacitor on OUT2.
- Place the output capacitor on OUT1 and OUT3 as close as possible to the device. Use short and wide traces to connect the output capacitor on OUT1 and OUT3.
- Connect the ground of the CT capacitor with AGND (pin 7) directly.
- Connect input ground and output ground on the same board layer, not through via hole.
- Connect AGND and PGND with the exposed thermal pad.

10.2 Layout Example

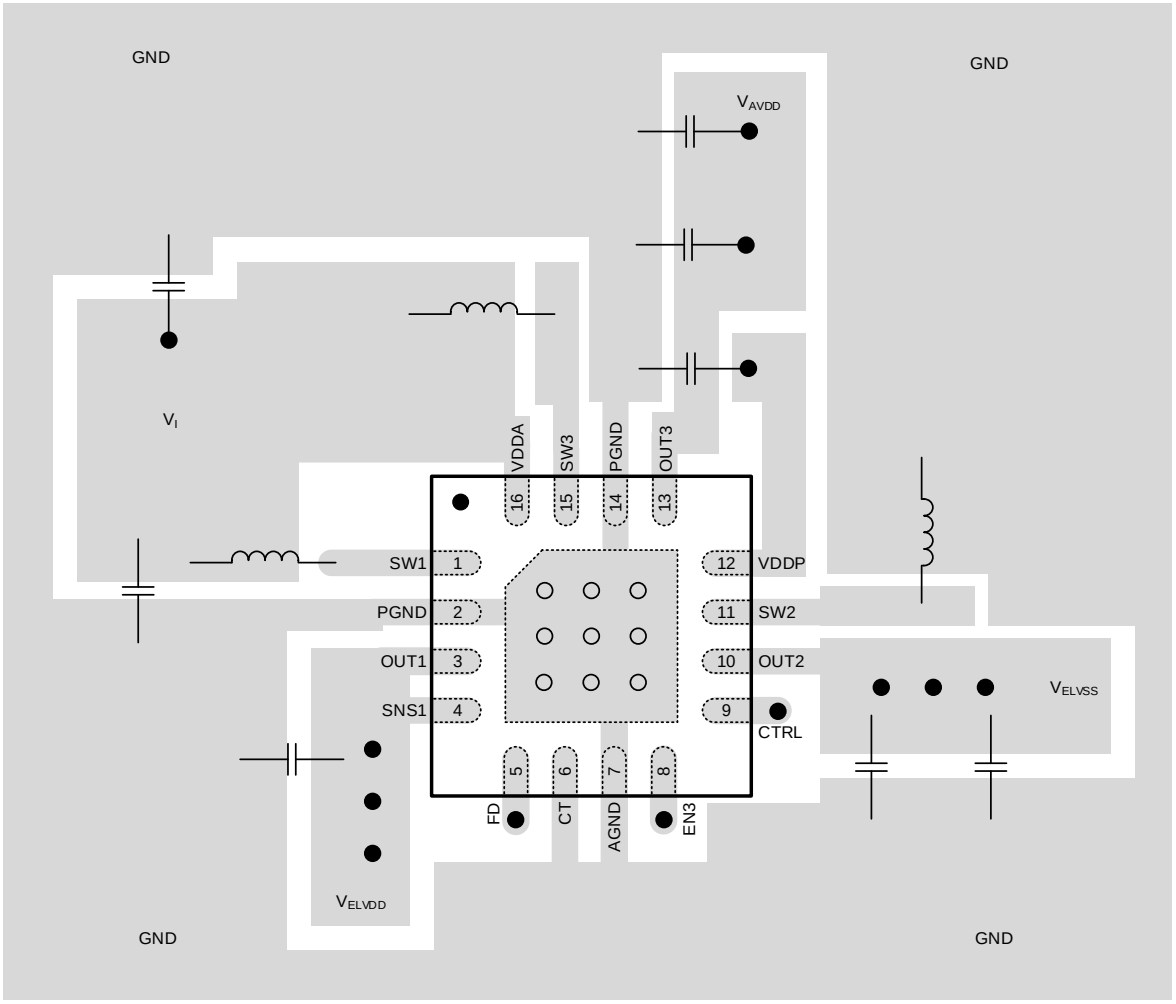


Figure 43. PCB Layout Example

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.2 Documentation Support

11.2.1 Related Documentation

PowerPAD™ Thermally Enhanced Package application report (SLMA002)
PowerPAD™ Made Easy application report (SLMA004)
QFN Layout Guidelines application report (SLOA122)
QFN/SON PCB Attachment application report (SLUA271)

11.3 Trademarks

All trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

12.1 Package Option Addendum

12.1.1 Packaging Information

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4) (5)
TPS65651RTER	ACTIVE	WQFN	RTE	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	T65651
TPS65651RTET	ACTIVE	WQFN	RTE	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	T65651
TPS65651ARTER	ACTIVE	WQFN	RTE	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	65651A
TPS65651BRTER	ACTIVE	WQFN	RTE	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	65651B
TPS65651BRTET	ACTIVE	WQFN	RTE	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	65651B

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

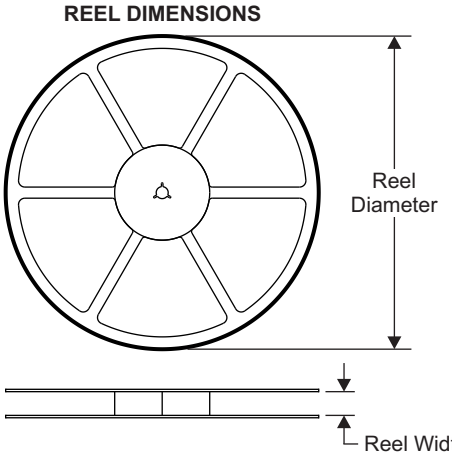
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

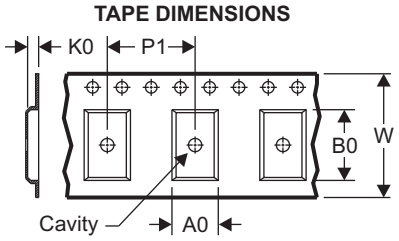
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device

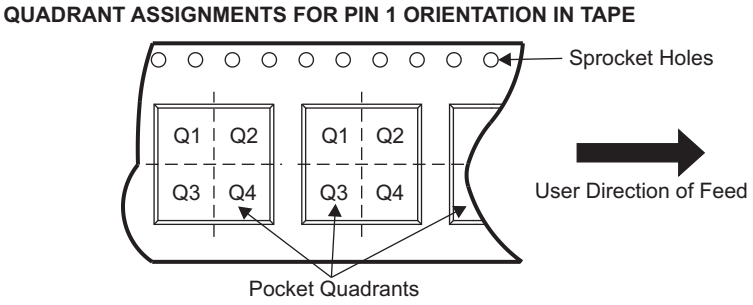
(5) Multiple Device markings will be inside parentheses. Only on Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

12.1.2 Tape and Reel Information



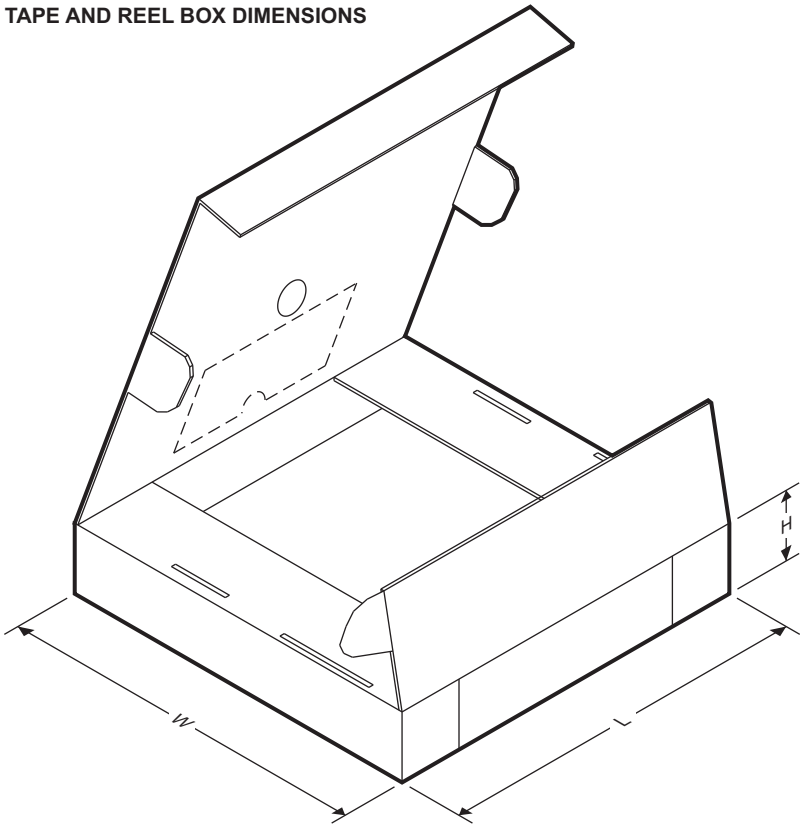


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65651RTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS65651RTET	WQFN	RTE	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS65651ARTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS65651BRTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS65651BRTET	WQFN	RTE	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



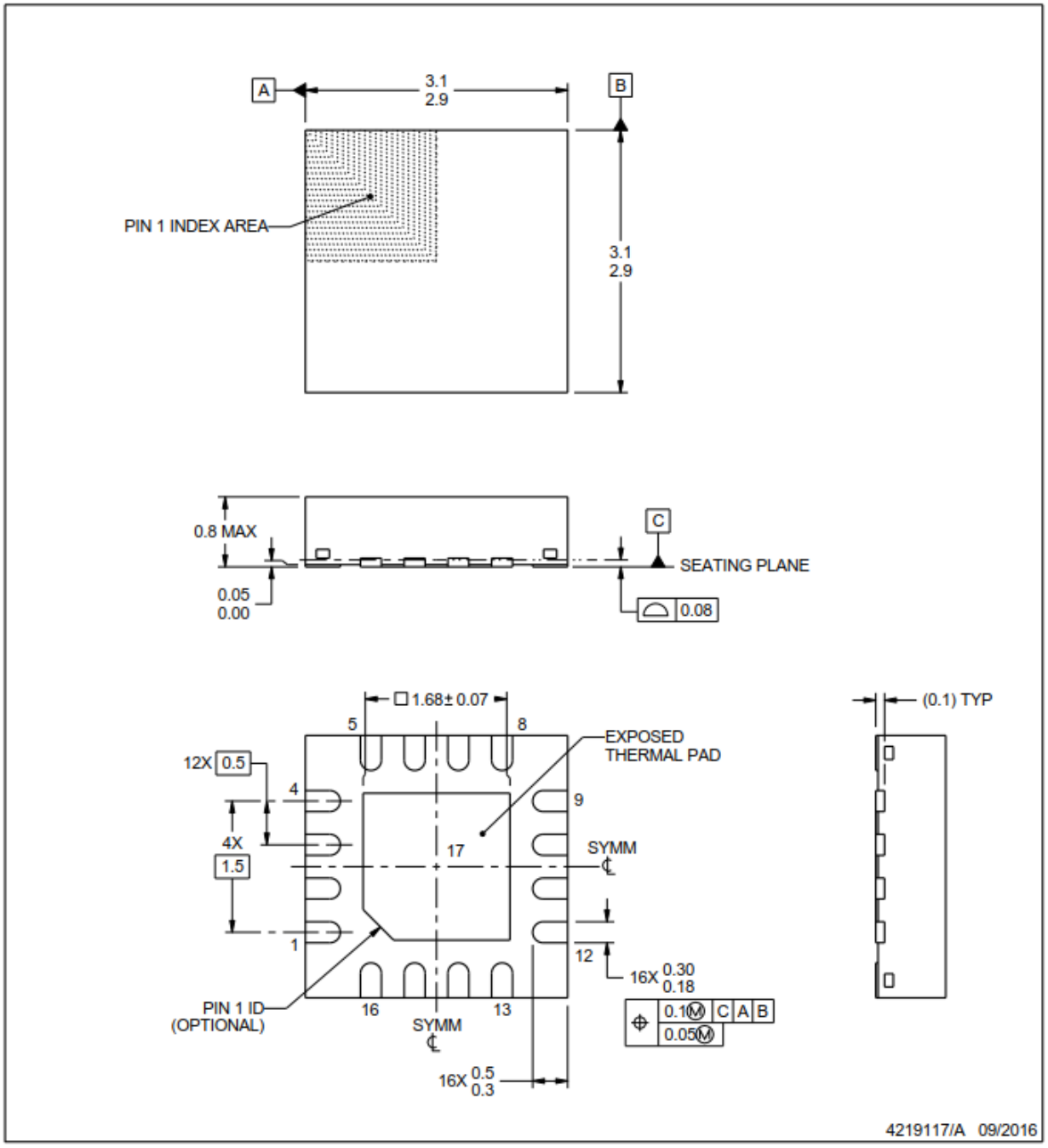
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65651RTER	WQFN	RTE	16	3000	367.0	367.0	35.0
TPS65651RTET	WQFN	RTE	16	250	210.0	185.0	35.0
TPS65651ARTER	WQFN	RTE	16	3000	367.0	367.0	35.0
TPS65651BRTER	WQFN	RTE	16	3000	367.0	367.0	35.0
TPS65651BRTET	WQFN	RTE	16	250	210.0	185.0	35.0

PACKAGE OUTLINE

RTE0016C

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



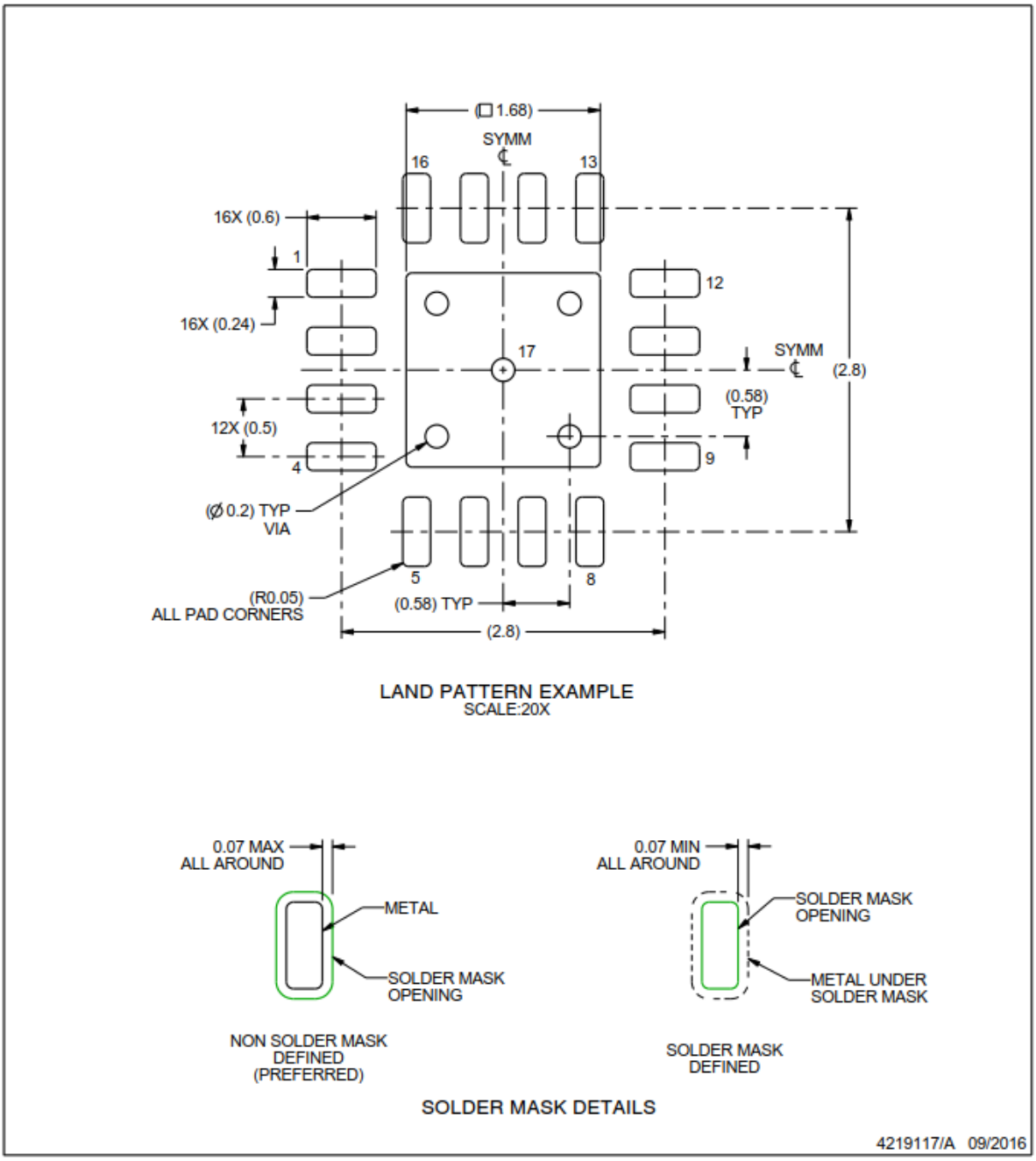
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

RTE0016C — **WQFN - 0.8 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



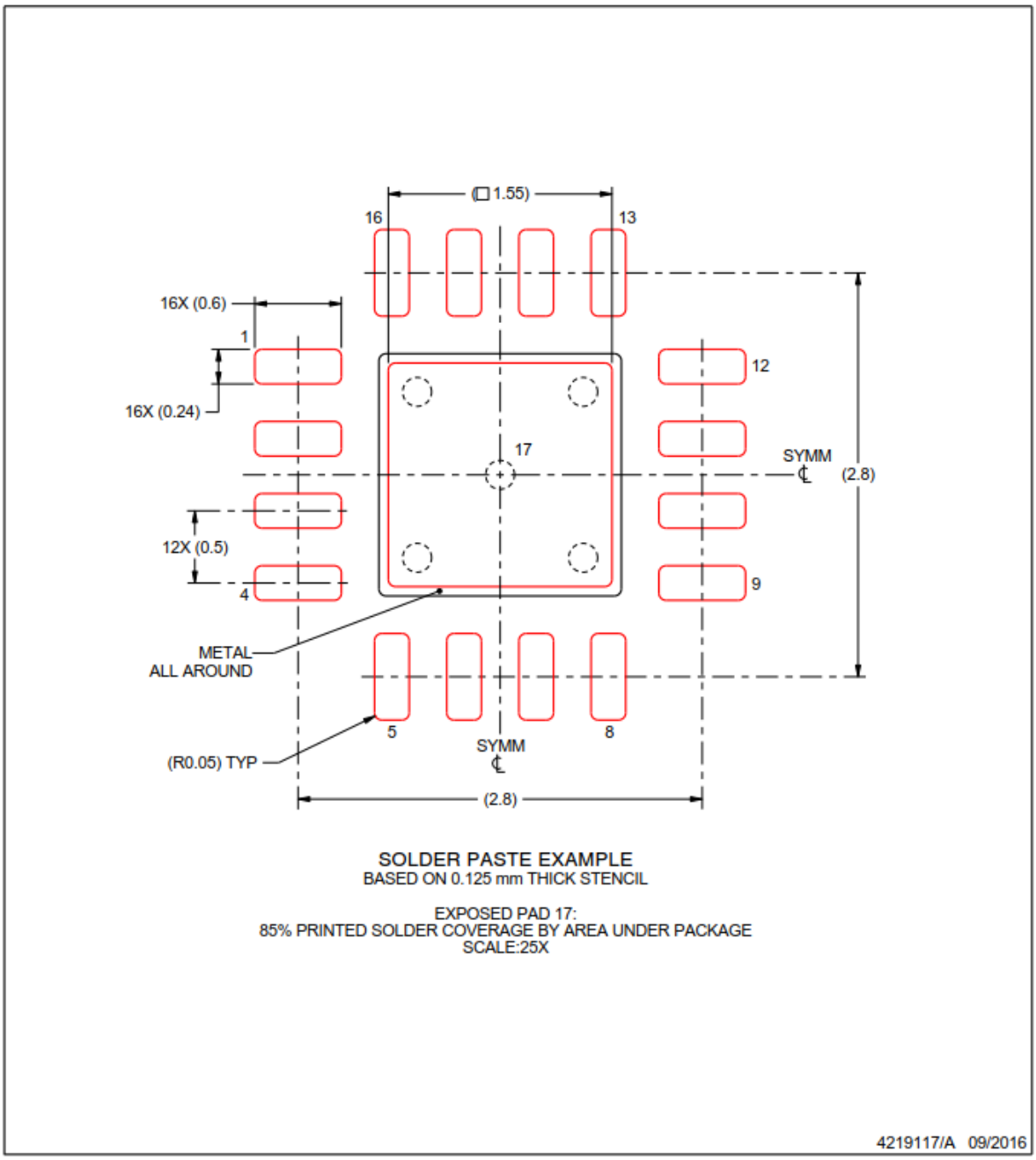
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RTE0016C — **WQFN - 0.8 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4219117/A 09/2016

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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