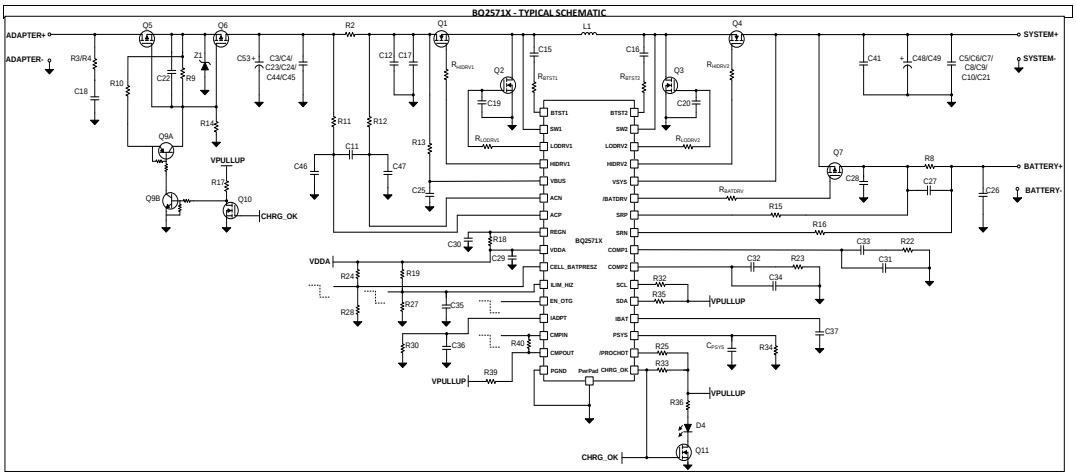
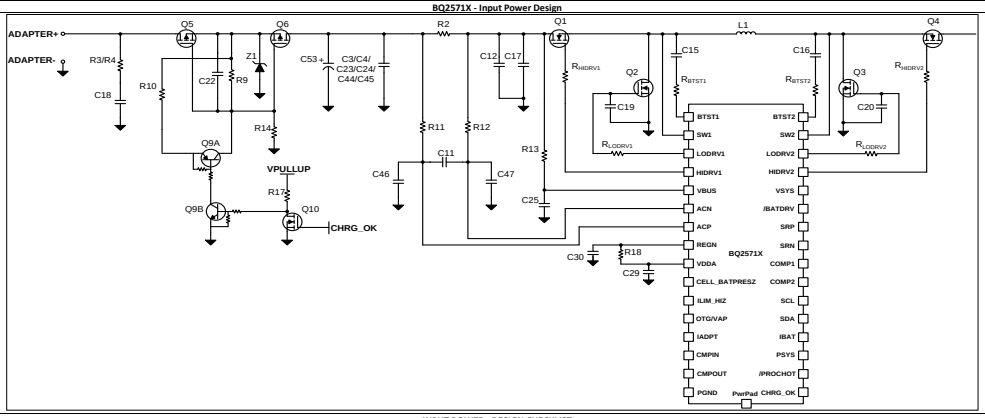

BQ2571X - TYPICAL SCHEMATIC
ADAPTER+
ADAPTER-
SYSTEM+
SYSTEM-
BATTERY+
BATTERY-
BQ2571X
BTST1
SW1
LODRV1
HIDRV1
VBUS
ACN
ACP
REGN
VDDA
CELL_BATPRESZ
ILIM_HIZ
EN_OTG
IADPT
CMPIN
CMPOUT
PGND
BTST2
SW2
LODRV2
HIDRV2
VSYS
/BATDRV
SRP
SRN
COMP1
COMP2
SCL
SDA
IBAT
PSYS
/PROCHOT
CHRG_OK
PwrPad
VPULLUP
CHRG_OK

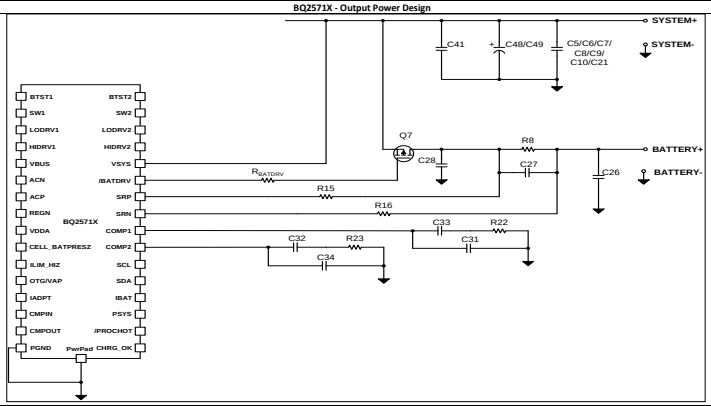
BQ2571X - Input Power Design



INPUT POWER - DESIGN CHECKLIST

PIN NAME		REQUIREMENT	COMPONENT	MIN	TYP	MAX	DESCRIPTION	COMMENTS AND RELEVANT EQUATIONS
			Input source to the charger					
ADAPTER+ / ADAPTER-	-	Required	C3+C4+C23+C24 +C44+C45	40 uF	60 uF		Forward Mode: Ceramic high frequency filtering input capacitors; Reverse Mode: Converter ceramic output filtering capacitors	For a 45 W to 65 W SYS load, use at least (4x) 10 uF capacitors with an extra (2x) 10 uF DNP. For a 90 W to 65 W SYS load, use at least (6x) 10 uF capacitors with an extra (2x) 10 uF DNP. X7R capacitors are recommended.
		Required	CS3		33 uF		Forward Mode: Tantalum polymer high frequency filtering input capacitor; Reverse Mode: Converter tantalum polymer output filtering capacitor	For > 65W SYS loads, with a 45 battery configuration, use at least (1x) 33 uF tantalum polymer capacitor.
		Recommended-DNP	R3, R4		3.9 Ω		Input hot-plug snubber circuit	For systems with high input cable or trace inductance and hot plug use cases, add experimentally derived RC snubber to limit inrush current and input voltage overshoot. R3 and R4 in parallel should be sized appropriately to handle the inrush current. $R3 \| R4 = \frac{1}{2\pi}\sqrt{\frac{L_{input}}{C_{input}}}, where\ 0 < L_{(Damping\ Factor)} < 1$
		Recommended-DNP	C18		1 uF			$C_{18,min} = \frac{I_{inrush,peak}}{(V_{input} + \Delta V_{overshoot,max})} * \frac{1}{\omega_{input,resonant}}, where\ \omega_{input,resonant} = \frac{1}{2\pi\sqrt{L_{input}C_{input}}}$
		Optional	Q5, Q6				Back-to-Back input protection P-Ch. MOSFETs	Size Q5 and Q6 appropriately to handle input power, optimize losses, and allow for smooth turn-on and turn off. Select delay and control circuits to avoid conflicts with charger timing. **Note**: If the Q5 and Q6 input protection circuit and is to function correctly, R13 (*See VBUS*) must be connected to the Drain of Q5.
		Optional	R10				Input protection turn-on/turn-off delay	
			R14					
			C22					
			R9					
		Optional	Q9A/Q9B				Input protection turn-on/turn-off control	
			Q10					
			R17		10 kΩ			
		Optional	Z1				Input protection gate-source Zener clamping diode	Size to clamp maximum allowable VGS for Q5 and Q6
			Differential input current sensing					
ACP-ACN	3-2	Required	R2 (R_{AC})	10 mΩ	10 mΩ	20 mΩ	Input current sensing resistor. This is used for both input current limit regulation and for inductor current sensing of the average current mode control architecutre of the charger.	For higher accuracy at light loads, increase to 20 mOhm. This will impact the IADPT and PSYS pin measurements. In IINDPM regulation, the input current limit is regulated as a differential voltage across R_{AC}, such that: $V_{IAC} = R_{AC}$ x Minimum(IIN_HOST() Register Setting, IIN_DPM() Register Setting, ILIM_HIZ pin setting).
		Recommended	R11, R12		4.99 Ω		Input current sense switching noise and common mode noise filtering	Select R11 / C46 and R12 / C47 such that the filter time constant is between 47 ns and 200 ns
			C46, C47		33 nF			
		Recommended	C12		10 nF	100 nF	High frequency switching currnet spike filtering	**Note** Too high of a capacitance on this side of RAC could impact the converter stability. This is the reason for limiting the maximum capacitance to 100nF.
			C17		1 nF	100 nF		
		Recommended-DNP	C11		0.01 uF		Differential mode noise filtering	
			IC input voltage rail					
VBUS	1	Required	C25	0.47 uF	0.47 uF		Input voltage noise decoupling capacitor	Placed close to the IC VBUS pin. X7R capacitor is recommended.
		Recommended	R13		1 Ω		Input voltage rail inrush current limiting	Size appropriately to handle large input overshoots and current spikes.
			Internal LDO output					
REGN	28	Required	C30	2.2 uF	2.2 uF		Internal LDO output stabilizing capacitor	Placed close to the IC REGN pin. X7R capacitor is recommended.
			Internal reference bias					
VDDA	7	Required	C29		1 uF		Noise decoupling capacitor	Placed close to the IC VDDA pin. X7R capacitor is recommended.
		Recommended	R18		10 Ω		Current limitine resistor	
			Converter (Forward Buck Mode) High-Side N-Channel MOSFET gate driver					
HIDRV1	31	Required	Q1				Converter (forward buck mode) active High-Side N-Channel MOSFET	Recommended MOSFET is the CSD17578Q3A. This is also the reverse boost mode synchronous High-Side MOSFET. Refer to section *10.2.2.5 Power MOSFETs Selection* in the BQ2571X datasheet for more details on the Power Stage MOSFET selection criterion.
		Recommended	R_{HIDRV1}	0 Ω			Q1 High-Side MOSFET gate drive strength limiting resistor	For non-ideal layouts with EMI contraints, add an experimentally derived resistance to slow down the Q1 turn-on and turn-off.
			Converter (Forward Buck Mode) Low-Side N-Channel MOSFET gate driver					
LODRV1	29	Required	Q2				Converter (forward buck mode) synchronous Low-Side N-Channel MOSFET	Recommended MOSFET is the CSD17578Q3A. This is also the reverse boost mode active Low-Side MOSFET. Refer to section *10.2.2.5 Power MOSFETs Selection* in the BQ2571X datasheet for more details on the Power Stage MOSFET selection criterion.
		Recommended	R_{LODRV1}	0 Ω			Q2 Low-Side MOSFET gate drive strength limiting resistor	For non-ideal layouts with EMI contraints, add an experimentally derived resistance to slow down the Q2 turn-on and turn-off.
		Recommended	C19		150 pF		Low-Side MOSFET Gate-Source holding capacitor	Sized to increase the effecive Cgs in comparison to the Cgd of Q2. This helps prevent the Miller capacitance from driving the MOSFET gate during a high dV/dt event. This is more important when Qgs and Qgd of Q2 are similar in magnitude.
			Buck-boost switching nodes and High-Side MOSFET bootstrap network					
SW1-SW2, BTST1, BTST2	32-23, 30, 25	Required	L1	1 uH	2.2 uH	3.3 uH	Converter inductor	SW1 and SW2 should be connected to minimize the inductive path from the IC pin to the inductor, L1. Refer to section *10.2.2.2 Inductor Selection* in the BQ2571X datasheet for more details on the inductor selection criterion.
		Required	C15		47 nF		Converter bootstrap capacitor for Q1 High-Side N-Channel MOSFET gate driver	
		Recommended	R_{BTST1}	0 Ω			Bootstrap capacitor discharge current limiting resistor	For non-ideal layouts with EMI contraints, add an experimentally derived resistance to slow down the Q1 turn-on.
		Required	C16		47 nF		Converter bootstrap capacitor for Q4 High-Side N-Channel MOSFET gate driver	
		Recommended	R_{BTST2}	0 Ω			Bootstrap capacitor discharge current limiting resistor	For non-ideal layouts with EMI contraints, add an experimentally derived resistance to slow down the Q4 turn-on.
			Converter (Forward Boost Mode) High-Side N-Channel MOSFET gate driver					
HIDRV2	24	Required	Q4				Converter (forward boost mode) synchronous High-Side N-Channel MOSFET	Recommended MOSFET is the CSD17578Q3A. This is also the reverse buck mode active MOSFET. Refer to section *10.2.2.5 Power MOSFETs Selection* in the BQ2571X datasheet for more details on the Power Stage MOSFET selection criterion.
		Recommended	R_{HIDRV1}	0 Ω			Q4 High-Side MOSFET gate drive strength limiting resistor	For non-ideal layouts with EMI contraints, add an experimentally derived resistance to slow down the Q4 turn-on and turn-off.
			Converter (Forward Boost Mode) Low-Side N-Channel MOSFET gate driver					
LODRV2	26	Required	Q3				Converter (forward boost mode) active Low-Side N-Channel MOSFET	Recommended MOSFET is the CSD17578Q3A. This is also the reverse buck mode synchronous MOSFET. Refer to section *10.2.2.5 Power MOSFETs Selection* in the BQ2571X datasheet for more details on the Power Stage MOSFET selection criterion.
		Recommended	R_{LODRV1}	0 Ω			Q3 Low-Side MOSFET gate drive strength limiting resistor	For non-ideal layouts with EMI contraints, add an experimentally derived resistance to slow down the Q3 turn-on and turn-off.
		Recommended	C19		150 pF		Low-Side MOSFET Gate-Source holding capacitor	Sized to increase the effecive Cgs in comparison to the Cgd of Q3. This helps prevent the Miller capacitance from driving the MOSFET gate during a high dV/dt event. This is more important when Qgs and Qgd of Q3 are similar in magnitude.

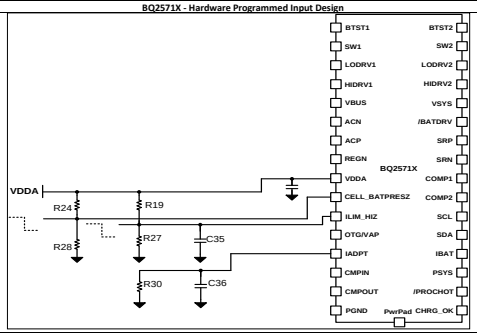
BQ2571X - Output Power Design



OUTPUT POWER - DESIGN CHECKLIST

PIN NAME		REQUIREMENT	COMPONENT	MIN	TYP	MAX	DESCRIPTION	COMMENTS AND RELEVANT EQUATIONS
							System output either from converter regulation of input source or battery	
SYSTEM+ / SYSTEM-	-	Required	C5+C6+C7+C8+C9+C10+C21 ($C_{SYSTEM+}$)	60 uF	80 uF		Forward Mode: Converter ceramic output filtering capacitors; Reverse Mode: Ceramic high frequency filtering input capacitors	For a 45 W to 65 W SYS load, use at least (6x) 10 uF capacitors with an extra (2x) 10 uF DNP. For a 90 W to 65 W SYS load, use at least (8x) 10 uF capacitors with an extra (2x) 10 uF DNP. X7R capacitors are recommended.
		Required	C48+C49 ($C_{SYSTEM+}$)	33 uF	66 uF		Forward Mode: Converter tantalum polymer output filtering capacitors; Reverse Mode: Tantalum polymer high frequency filtering input capacitor	For > 65W SYS loads, with a 4S battery configuration, use at least (1x) 33 uF tantalum polymer capacitor. For > 90W SYS loads, with a 4S battery configuration, use at least (2x) 33 uF tantalum polymer capacitors.
							System output regulation sensing point	
VSYS	22	Required	-		-		-	VSYS must be Kelvin connected to the output filter stage connected to SYSTEM+. The connection should be tied as close the output resonant filter portion of the system rail ($C_{SYSTEM+}$) as possible. Take precaution to not Kelvin connect this pin significantly far away from the output filter and/or IC SYS pin, such that a large IR loss from the system load is sensed by VSYS.
		Recommended-DNP	C41		10 nF		Noise decoupling capacitor	Placed close to the IC VSYS pin.
							Battery or battery pack connection to the charger	
BATTERY+ / BATTERY-	-	Required	C26	10 uF	10 uF		Charge current regulation stability and filtering capacitor	Connected to the SRN pin, this capacitor is critical for accurate battery voltage sensing. From the SRN pin, the Constant Voltage (CV) phase of charging will regulate the voltage to the MaxChargeVoltage() Register setting. When charging is disabled and the SRN voltage is above the MinSysVoltage() Register setting, the sensed voltage on the SRN pin is also used as a reference to regulate the SYS pin voltage such that: **$V_{SYS} = V_{SRN}$ + 160 mV.** X7R capacitor is recommended.
							Differential charge current sensing	
SRP-SRN	20-19	Required	R8 (R_{SR})		10 mΩ	20 mΩ	Charge current sensing resistor	For higher accuracy at light loads, increase to 20 mOhm. This will impact the IBAT and PSYS pin measurements. In Charge Current regulation for the Constant Current (CC) phase of charging, the ICHG current is regulated as a differential voltage across R_{SR}, such that **$V_{SRX} = R_{SR}$ x ChargeCurrent() Register setting**. If the charger is either in IINDPM, VINDPM, Supplement Mode, or Thermal Foldback, the regulated charge current will be lower than the programmed value.
		Required	C28	1 uF	1 uF		Noise filter capacitor	
		Recommended	C27		0.1 uF		Differential mode noise filterine	
		Recommended	R15, R16		10 Ω	10 Ω	Battery reverse polarity protection resistors	Sized with a low power rating such that in the event of a reverse polarity event with the battery pack, the resulting unintended current flow will damage R15 or R16 first rather than the charger or the system. This acts as a crude form of reverse polarity protection.
							External battery MOSFET driver	
/BATDRV	21	Required	Q7		-		External battery to system power path P-Channel MOSFET (BATFET)	Recommended MOSFET is the CSD25402Q3A
		Recommended	R_{BATDRV}		0 Ω		Q7 gate drive strength limiting resistor.	
							Converter external compensation networks	
COMP1, COMP2	16, 17	Required	C33		1800 pF		Average current control outer loop compensation network	Place close to the IC COMP1 pin. Ideally connect the ground return of these components to a signal ground, rather than a power ground. If not possible, connect the ground return as close to the IC PGND pin as possible.
		Required	R22		40.2 kΩ			
		Required	C31		33 pF		Average current control outer loop high frequency filtering capacitor	
		Required	C32		680 pF		Average current control inner loop compensation network	Place close to the IC COMP2 pin. Ideally connect the ground return of these components to a signal ground, rather than a power ground. If not possible, connect the ground return as close to the IC PGND pin as possible. When not using L = 2.2uH, scale R23 using R23 = 10kOhm x Lnew / 2.2uH
		Required	R23		10 kΩ			
		Required	C34		15 pF		Average current control inner loop high frequency filtering capacitor	

BQ2571X - Hardware Programmed Input Design



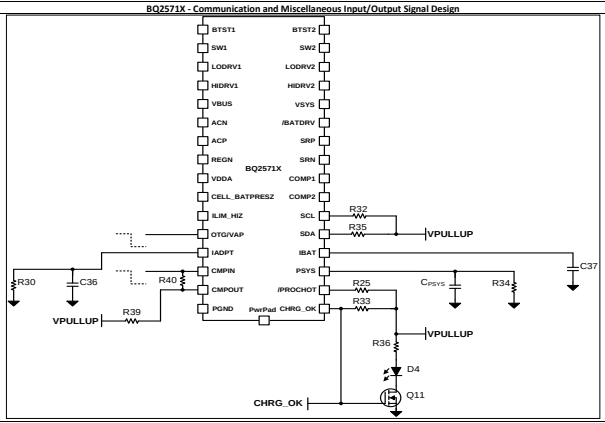
HARDWARE PROGRAMMED INPUT - DESIGN CHECKLIST

PIN		REQUIREMENT	COMPONENT	MIN	TYP	MAX	DESCRIPTION	COMMENTS AND RELEVANT EQUATIONS
							Default charging and system parameter setting	
CELL_BATPRESZ	18	Required	R24		*kΩ		Resistor divider network referenced to the VDDA rail to set the default charging voltage, default minimum system voltage, and maximum system voltage. Also input to signal charger of a battery absense.	The CELL_BATPRESZ cell count settings is determined once VDDA is powered, typically after a valid input source is applied. If CELL_BATPRESZ is pulled LOW externally, this indicates to the charger that the battery has been removed. This will reset the ChargeCurrent() Register setting to 0mA. If enabled in the ProchotOption1() Register setting, this will also trigger the ProchotStatus() register flag.
			R28		*kΩ			
							External input current limit setting and converter high impedance control	
ILIM_HIZ	6	Required	R19		*kΩ		Resistor divider network to set an external input current limit.	The voltage set at this pin through the resistor divider network determines the externally set input current limit setting.
			R27		*kΩ			$V_{ILIM\_HIZ} = 1V + 40 \times IINDPM_{setting} \times R_{AC}, where\ 1.2V < V_{ILIM\_HIZ} < 4.0V$
		Recommended-DNP	C35		*uF		Noise decoupling capacitor	Place close to the IC ILIM_HIZ pin.
							Inductor selection setting and input current measurement output	
IADPT	8	Required	R30	-3%	*Ω	+3%	Resistor used to indicate inductor selection and output an analog input current measurement	
		Recommended	C36		100 pF		Noise decoupling capacitor	Place close to the IC IADPT pin.

CELL COUNT	PIN VOLTAGE w.r.t. VDDA	BATTERY VOLTAGE MaxChargeVoltage() Register	MINIMUM SYSTEM VOLTAGE MinSystemVoltage() Register	SYSOVP
4S	75%	16.800 V	12.288 V	19.5 V
3S	55%	12.592 V	9.216 V	19.5 V
2S	40%	8.400 V	6.144 V	12 V
1S	25%	4.192 V	3.584 V	5 V

INDUCTOR IN USE	RESISTOR ON IADPT PIN
1 µH	93 kΩ
2.2 µH	137 kΩ
3.3 µH	169 kΩ

BQ2571X - Communication and Miscellaneous Input/Output Signal Design



COMMUNICATION AND MISC INPUT/OUTPUT SIGNAL - DESIGN CHECKLIST

PIN NAME		REQUIREMENT	COMPONENT	MIN	TYP	MAX	DESCRIPTION	COMMENTS AND RELEVANT EQUATIONS
							Reverse mode On-The-GO (OTG) or Vmin Active Protection (VAP) mode enable	
OTG/VAP	5	Optional	-		-		OTG or VAP mode	Pull HIGH to enable OTG or VAP mode, based on the ChargeOption3(), OTGVoltage(), and OTGCurrent() registers. Pull LOW to disable OTG or VAP mode.
							Inductor selection setting and analog calculated input current measurement output	
IADPT	8	Required	R30	-3%	*Ω	+3%	Resistor used to indicate inductor selection and output an analog input current measurement	Place close to the IC IBAT pin. The IADPT_GAIN setting is programmable in the ChargeOption0() Register. $V_{IADPT} = IADPT\_GAIN \times V_{ACP-ACN}, when\ in forward\ mode$ $V_{IADPT} = IADPT\_GAIN \times V_{ACN-ACP}, when\ in\ reverse\ OTG\ mode$
		Recommended	C36		100 pF		Noise decoupling capacitor	Place close to the IC IADPT pin.
							Independent comparator input and output	
CMPIN, CMPOUT	14, 15	Optional	R39		10 kΩ		Pullup resistor for CMPOUT open-drain output	Independent comparator reference voltage, polarity and deglitch time programmable in the ChargeOption1() register.
			R40		1 MΩ		Resistor tie when inpendent comparator is not used	
							I2C or SMBus Open-drain communication input and output	
SCL, SDA	13, 12	Required	R32, R35		10 kΩ		Pullup resistors for the open-drain I2C or SMBus clock and data communication bus	I2C or SMBus communication is required for charging to operate on this device as intended. This is a host controlled charging buck-boost controller. Charging is not autonomous without host intervention.
							Analog battery current measurement output	
IBAT	9	Optional	C37		100 pF		Analog voltage output representing the battery charge or discharge current measurement	Place close to the IC IBAT pin. The IBAT_GAIN setting is programmable in the ChargeOption0() Register. $V_{IBAT} = IBAT\_GAIN \times V_{SRP-SRN}, when\ battery\ is\ charging$ $V_{IBAT} = IBAT\_GAIN \times V_{SRN-SRP}, when\ battery\ is\ discharging$
							Analog system power measurement output	
PSYS	10	Optional	R34		30.1 kΩ		Analog current output representing the system power, measured as a voltage across R34.	The PSYS_RATIO setting is programmble in the ChargeOption1() Register. Proper PSYS functionality is limited to use with either a 10 mΩ or 20 mΩ for either R_{AC} and R_{SR}. Select the appropriate R_{AC}/R_{SR} resistance value in the ChargeOption1() Register. In reverse OTG mode, PSYS either measure the total battery output power or the system power, which can be set in the ChargeOption3() register. The PSYS calculation assumes 100% efficiency. $V_{PSYS} = R34 \times PSYS\_RATIO \times (V_{ACP} I_{IN} + V_{SRN} I_{BAT})$
		Optional	C_{PSYS}		100 pF		Noise decoupling capacitor	Place close to the IC PSYS pin.
							Active LOW open-drain output signal for Proccessor Hot flags	
/PROCHOT	11	Optional	R25		10 kΩ		Pullup resistor for/PROCHOT open-drain output	
							Active HIGH open-drain output signal of input source status	
CHRG_OK	4	Optional	R33				Pullup resistor for CHRG_OK open-drain output	Pulls HIGH when **3.2 V < VBUS < 26 V** and no Faults are present. Pulls LOW otherwise.
		Optional	R36				CHRG_OK LED indictation control	
			D4					
			Q11					
							IC Thermal dissipation pad	
PwrPad	-	Required	-		-		Main point of heat dissipation for the IC	Connect to a large Power Ground plane(s) and/or layer(s) with at least 5-point via connections