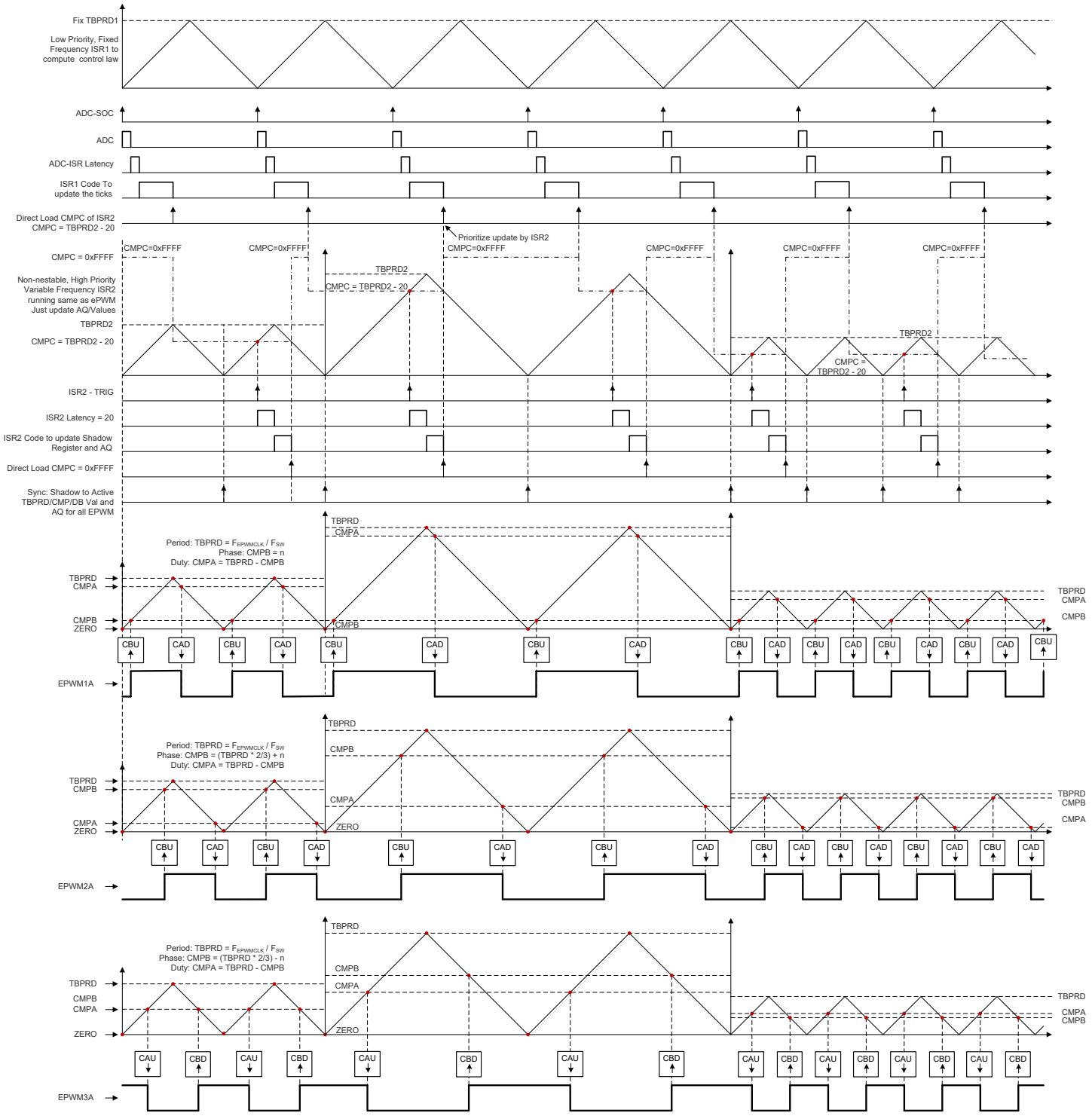
3-phase Interleaved LLC PWM update using two ISR



The figure above shows HRPWM configuration and timing diagram for three phase LLC implementation with variable frequency, phase, duty, dead band control. This implementation overcomes any limitation that HRPWM poses in interleaved LLC applications. On the top of standard C2000 digital power control following steps are taken for the implementation. Please see the sysconfig based CCS project that implements these steps.

1. In HRPWM mode, do not use sync function using TBPHS since that is also limitation of HRPWM method it may cause jitters (jitter in PWM is step variation of 3 TBCLK if counter or phase shift is within 3TBCLK around PRD and ZERO event). When configuring the ePWM follow the steps below to maintain synchronization:

    a. First disable TBCLK (using API: SysCtl_disablePeripheral(*SYSCTL_PERIPH_CLK_TBCLKSYNC*);).

b. Second, do the ePWM configuration.

c. In the last enable TBCLK (using API:SysCtl_enablePeripheral(*SYSCTL_PERIPH_CLK_TBCLKSYNC*);).

2. To mimic one shot, there will be two ISRs implemented,

   a. High Priority non-nestable variable frequency ISR1 (running at F_{SW} of LLC) which will only update ePWM values and action qualifier register considering this code operation has deterministic response. It means that you can profile this ISR1 and know how much exact time needed to update register. That time should be shorter than min TBPRD (or Max F_{SW} of LLC) of this ISR1. This ISR1 is triggered by CMPC event when counter is counting upwards. Once register update is finished DIRECT WRITE (not shadow) CMPC = 0xffff (saturation) so that it doesn't trigger next cycle unless fixed frequency ISR2 updates CMPC to trigger this ISR1 to update the register.

   b. Fixed frequency ISR2 which performs control law calculations and has lower priority than variable frequency ISR1. When it finishes the all the computation then it DIRECT WRITES (not shadow) "CMPC=TBPRD-20" of variable of ISR1 (where 20 counts are ISR latency)

3. This configuration uses up-down counter method with CMPB is used for phase shift and CMPA is used for duty control. Since both edge positions are controlled in HR steps, both phase shift and duty will be precise.

4. HRPWM method have limitations that CMP values cannot be close to TBPRD or ZERO by ~3TBCLK. This method also takes care of that limitation.

5. HRPWM methods other limitation is that you can either use Period/Duty in HR mode or Phase shift in HR mode. You can't use all three at the same time. In the following method, we are only using Period / Duty control by updating TBPRD/CMPA/CMPB and still achieve phase shift, 50% duty and period control in HR mode without jitter.