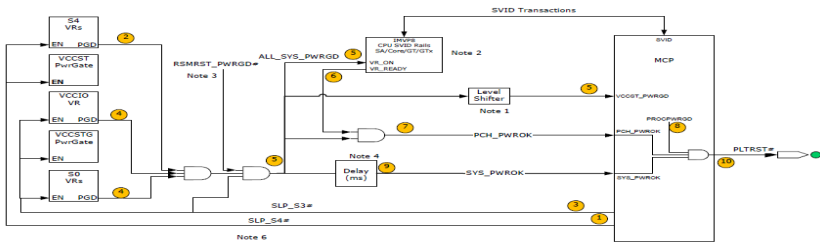
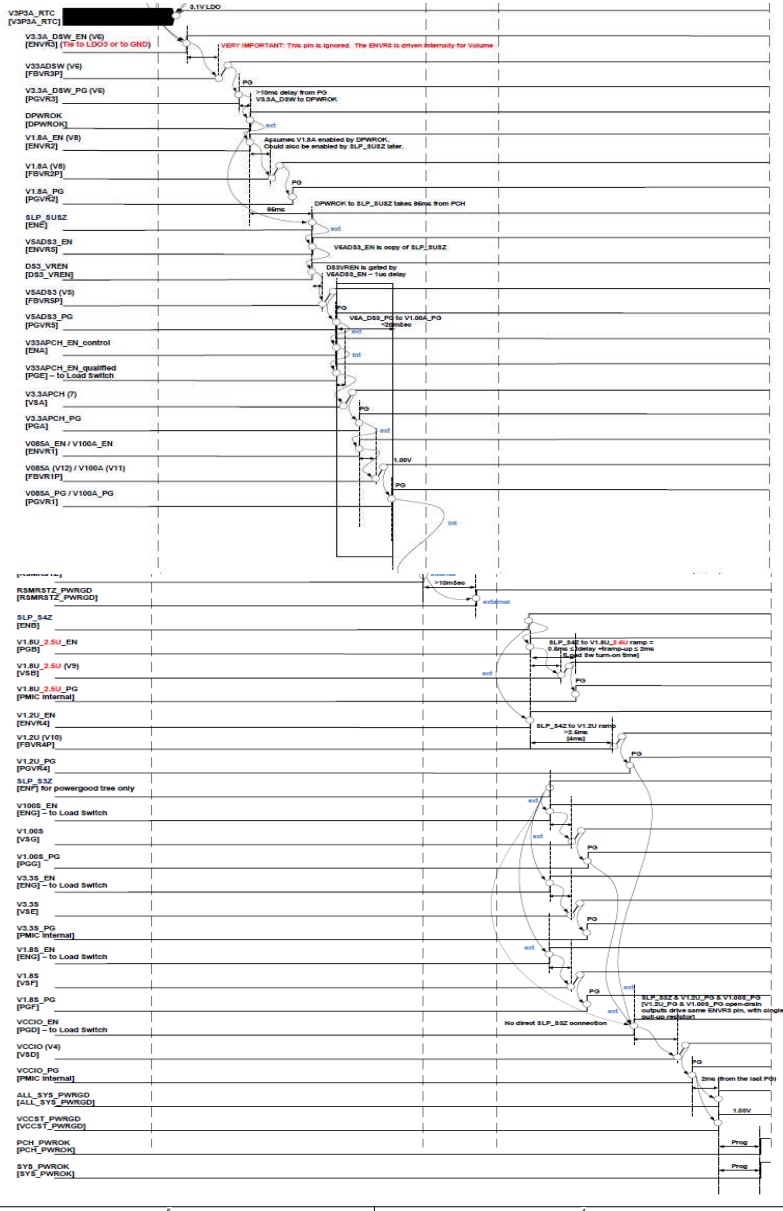


SKL U/Y (Volume Segment) Flow Diagram for SYS_PWROK/PCH_PWROK



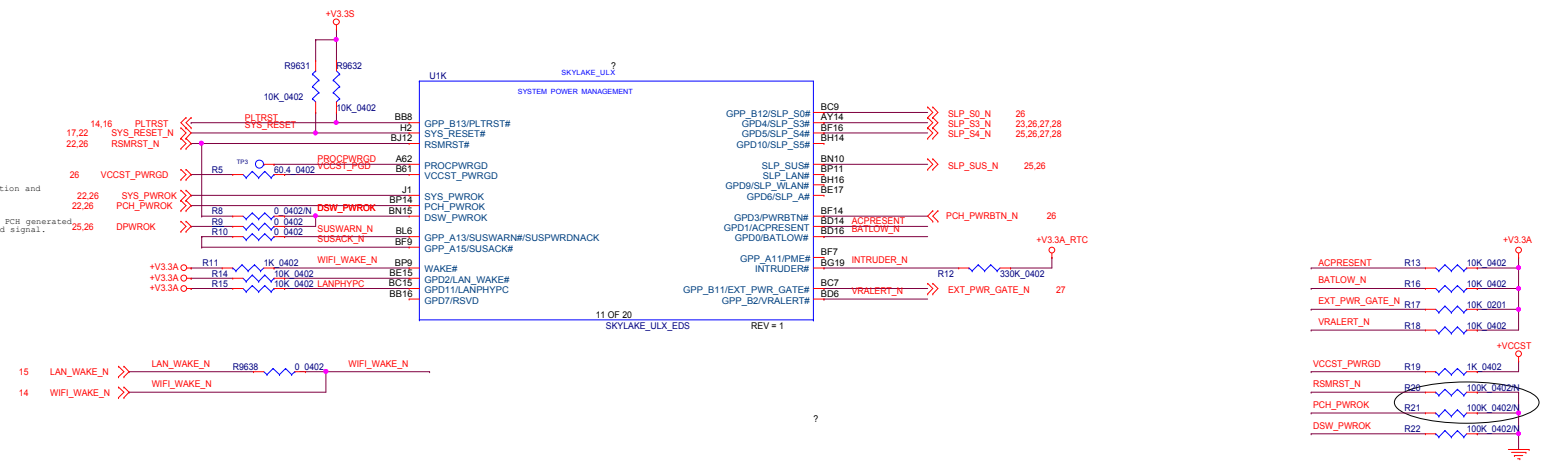
TPS650830 Timing diagram



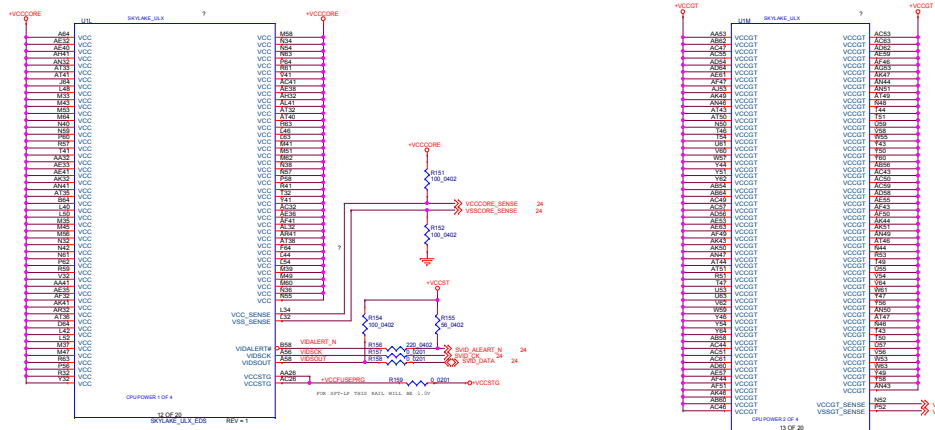
| | | |
|---------------------------|--------------|---------------------------|
| PC Partner | | |
| Power Delivery & Sequence | | |
| File | | |
| Size | Module Name: | B403 |
| C | Date: | Friday, December 07, 2018 |
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It is recommended that SYS_PWROK be asserted after both BCH_PWROK assertion and processor core VR_PWRGD assertion.

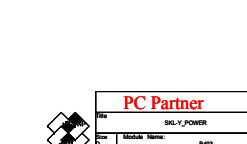
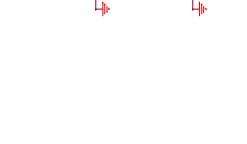
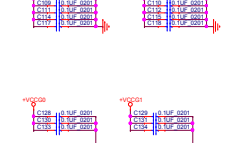
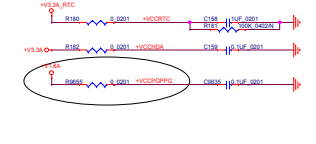
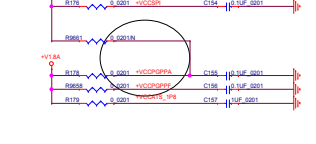
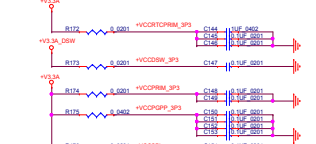
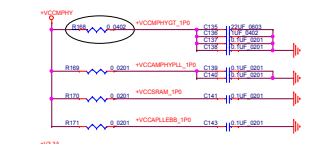
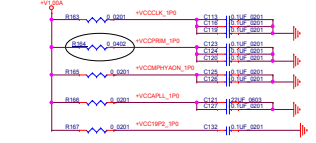
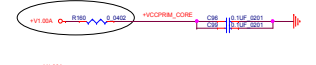
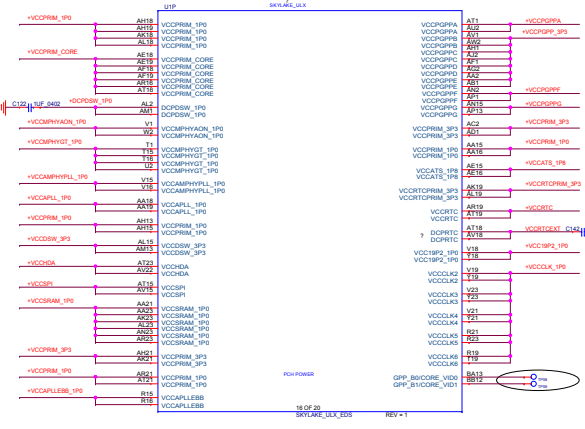
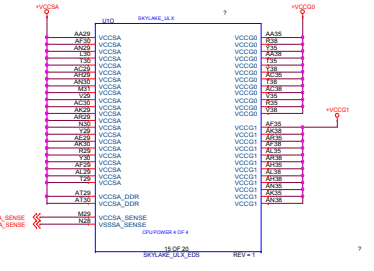
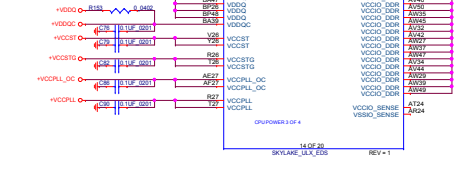
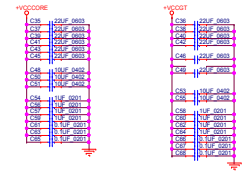
BCH_PWROK is an input signal to the PCH generated by EC or PMIC based on VR power good signal.



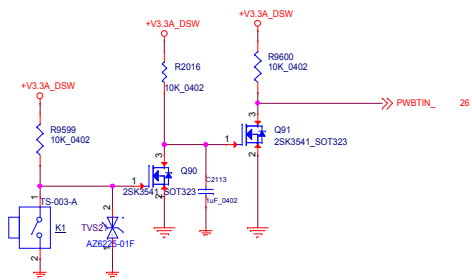
| | | |
|---------------------------------|-------------------|--------|
| PC Partner | | |
| Title: SKL_Y_DISPLAY/PWR_MANAGE | | |
| Size C | Module Name: B403 | Rev 01 |
| Date: Friday, December 07, 2018 | Sheet 4 of 28 | |



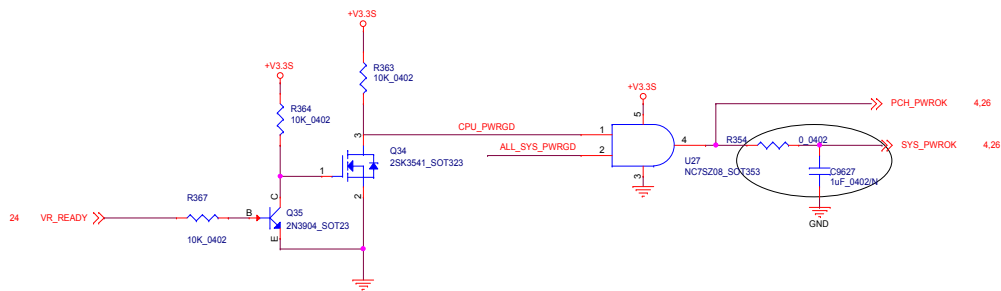
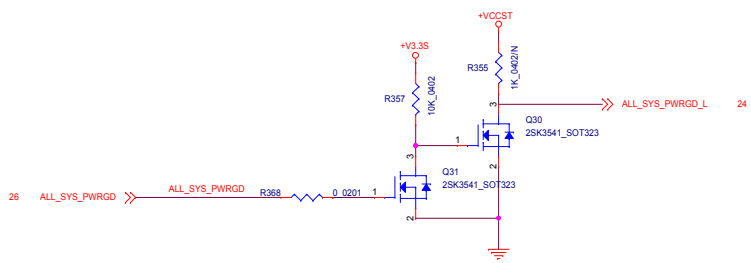
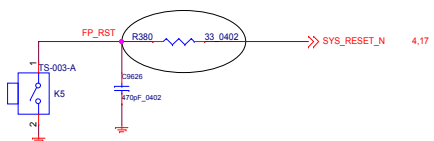
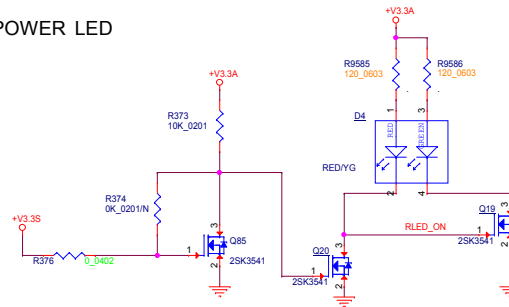
NOTE: SENSE WILL BE DERIVED FROM VCCGT
 THIS BALL WILL HAVE A DIFFERENT TRACK



Power Button



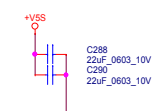
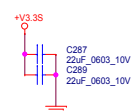
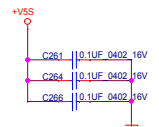
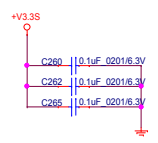
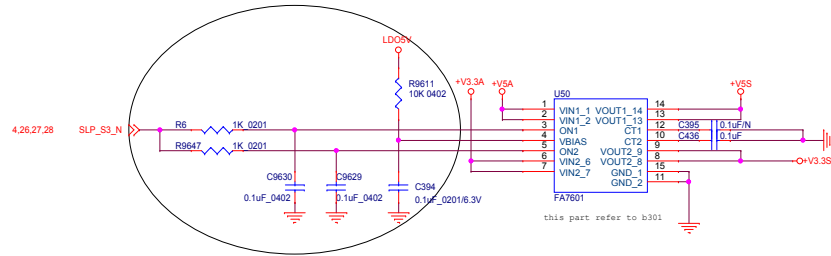
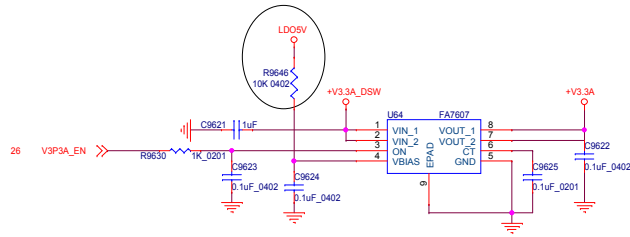
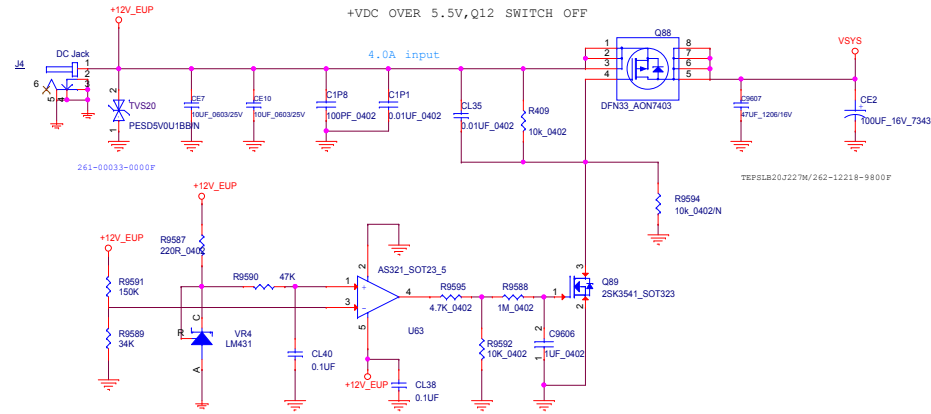
POWER LED



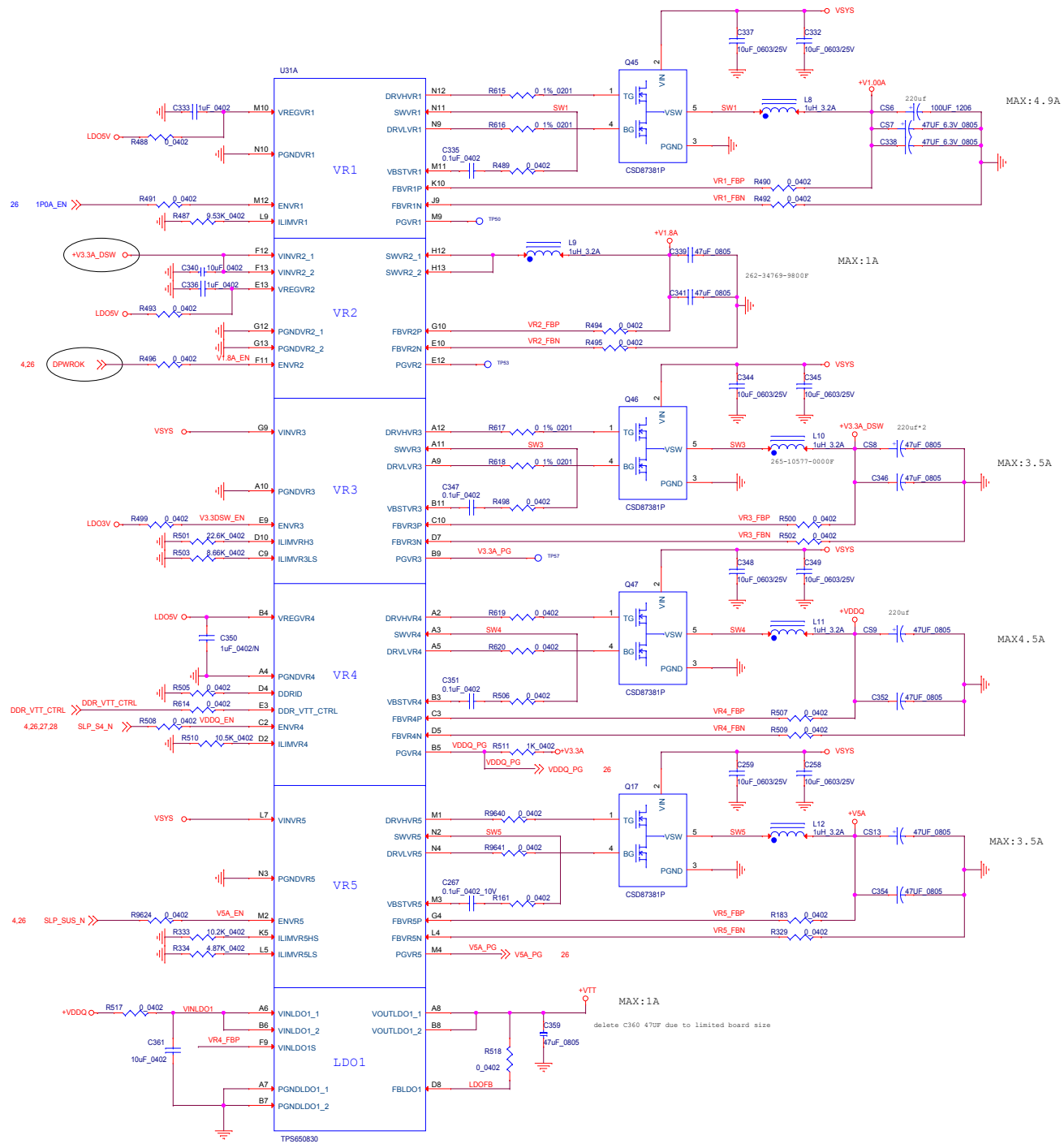
| | | |
|-------------------------|---------------------------|----------------|
| PC Partner | | |
| BL PWR & power sequence | | |
| File | | |
| Module Name: | B403 | Rev 01 |
| Date: | Friday, December 07, 2018 | Sheet 22 of 28 |

12V DC IN PART

12V / 1.5A DC IN

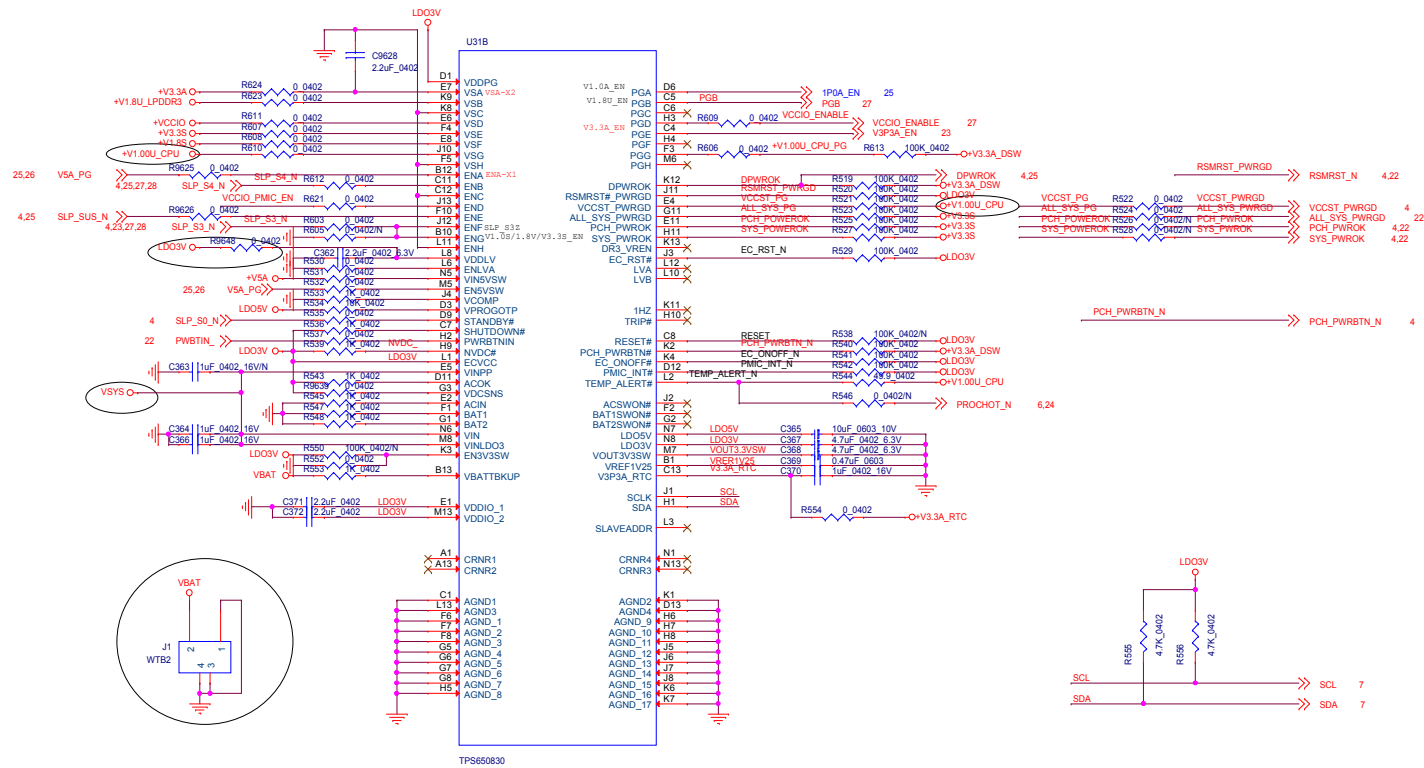
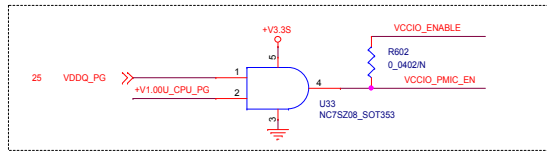


| | | |
|---------------------------------|-------------------|---------|
| PC Partner | | |
| Title: SYSTEM POWER IN | | |
| Size: C | Module Name: B403 | Rev: 01 |
| Date: Friday, December 07, 2018 | Sheet: 23 | of 28 |



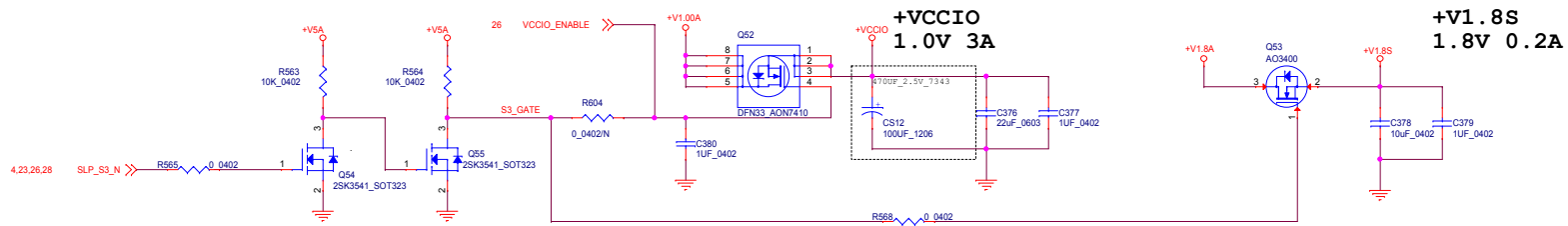
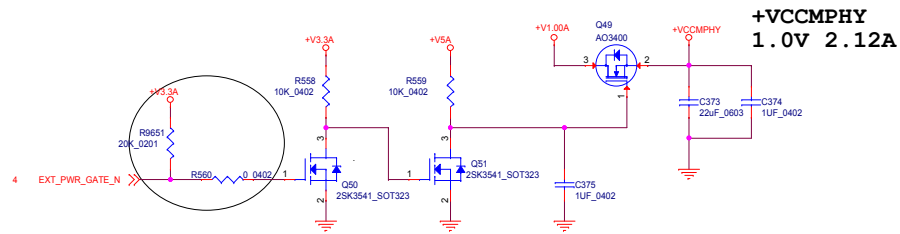
| | | |
|---------------------------------|-------------------|--------|
| PC Partner | | |
| Title: TPS650830_PMIC_1 | | |
| Size C: | Module Name: B403 | Rev 01 |
| Date: Friday, December 07, 2018 | Sheet 25 | of 28 |

VCCIO Enable circuit



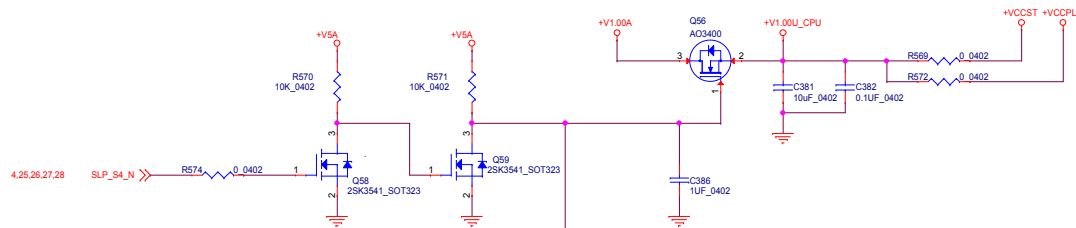
PC Partner

| | | |
|------------------|---------------------------|----------------|
| Title | | |
| TPS650830_PMIC_2 | | |
| Size | Module Name: | Rev |
| C | B403 | 01 |
| Date: | Friday, December 07, 2018 | Sheet 26 of 28 |

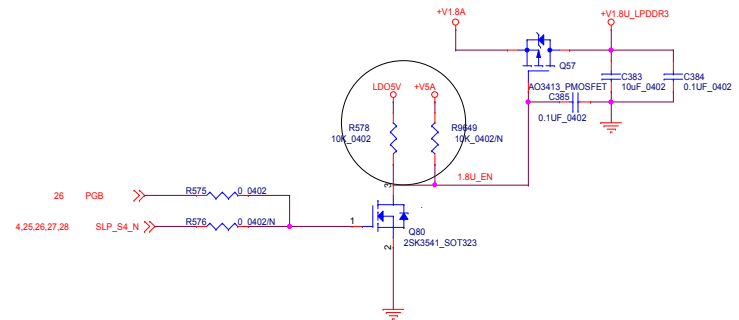


VCCST ramping and stable before VCCSTG > 100ns

+VCCST (include +VCCPLL)
1.0V 0.1A

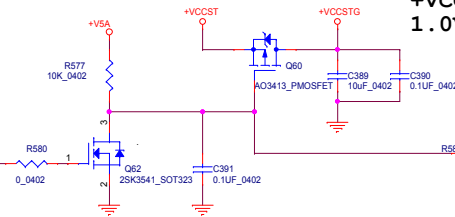


+V1.8U LPDDR3
1.8V 0.62A

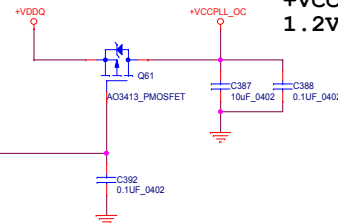


SLP_S0# de-assertion to VCCSTG stable should in 10-65us

+VCCSTG
1.0V 0.16A



+VCCPLL_OC
1.2V 0.35A



PC Partner

| | | |
|-------|---------------------------|----------------|
| File | 1.0S/1.8S/VCCSTG | |
| Size | Module Name: | B403 |
| Date: | Friday, December 07, 2018 | Sheet 27 of 28 |
| Rev | 01 | |