BQ25606 TYPICAL SCHEMATIC

BQ25606 WQFN Package 24-Pin WQFN Top View
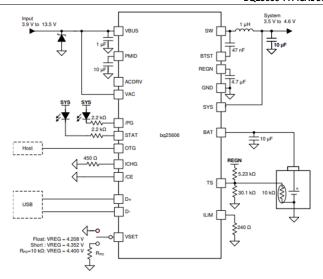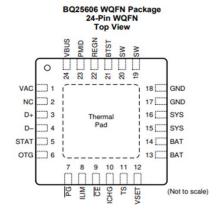
Addional Information: http://www.ti.com/lit/an/slva924/slva924.pdf Designing A Standalone Single Cell 3-A Charger with the bq25606

BQ25606 SCHEMATIC CHECKLIST

PIN NAME		REQUIREMENT	COMPONENT	MIN	TYP	MAX	DESCRIPTION	COMMENTS AND RELEVANT EQUATIONS
D+/D-	3,4						**USB data line pair**	
		Optional					Positive line of the USB data line pair.	D+/D- based USB host/charging port detection. The detection includes data contact detection (DCD), primary and secondary detection in BC1.2 and nonstandard adaptors.
		Optional					Negative line of the USB data line pair.	
STAT	5						**Open drain charge status output**	
		Optional	STAT resistor		2.2 kΩ	10 kΩ	Connect to the pull up rail via 2.2-kΩ or 10-kΩ resistor.	1. If not used, leave it float. 2. The STAT pin indicates charger status. Collect a current limit resister and a LED from a rail to this pin. 3. Charge in progress: LOW; Charge complete or charger in SLEEP mode: HIGH; Charge suspend (fault response): 1-Hz, 50% duty cycle Pulses 4.This pin can be disabled via EN_ICHG_MON[1:0] register bits.
OTG	6						**Active high boost mode enable pin**	
		Optional						1. If OTG boost mode is not used, short it to ground. 2. When this pin is pulled HIGH, OTG is enabled. 3. OTG cannot be floating
/PG	7						**Open drain active low power good indicator.**	
		Optional	PG resistor		2.2 kΩ	10 kΩ	Connect to the pull up rail via 10-kΩ resistor.	LOW indicates a good input source if the input voltage is between UVLO and ACOV, above SLEEP mode threshold, and current limit is above 30 mA.
NC	2						**No connect**	
		Optional						The pin must be floating
/CE	9						**Active low Charge Enable pin**	
		Required						When this pin is driven low, battery charging is enabled.
ILIM	8						**Input current limit setting**	
		Required	ILIM resistor		* Ω		A resistor is connected from ILIM pin to ground to set the input current limit as IINDPM = KILIM/RILIM	1.The acceptable range for ILIM current is 500 mA - 3200 mA. 2. The resistor based input current limit is effective only when the input adapter is detected as unknown. Otherwise, the input current limit is determined by D+/D– detection outcome.
ICHG	10						**Charge current limit setting**	
		Required	ICHG resistor		* Ω		A resistor is connected from ICHG pin to ground to set charge current limit as ICHG = KICHG/RICHG.	The acceptable range for charge current is 300 mA – 3000 mA
TS	11						**Temperature qualification voltage inputs for JEITA**	
		Required	TS resistors and thermistor				Connect a negative temperature coefficient thermistors. Recommend 103AT-2 thermistors.	1. If thermistor is not used, set TS pin voltage within normal range. 2. If thermistor is used, program temperature window with a resistor divider from REGN to TS to GND. Charge suspends when TS pin is out of range.
VSET	12						**Default battery charge voltage isetting**	
		Required	VSET resistor		* Ω		Program battery regulation voltage with a resistor pull-down from VSET to GND.	RPD > 50kΩ (float pin) = 4.208 V RPD < 500Ω (short to GND) = 4.352 V 5kΩ < RPD < 25kΩ = 4.400 V
VAC	1						**Charge input voltage sense**	
		Required						Charge input voltage sense. This pin must be connected to VBUS pin.
VBUS	24						**Charge input voltage**	
		Required	VBUS caps	1uF				1. Place a 1-µF ceramic capacitor from VBUS to PGND and place it as close as possible to IC. 2. It is recommended to have a total of ~10uF capacitance at VBUS & PMID for USB input compliance.
PMID	23						**Actual input source to the charger**	
		Required	PMID caps	8.2uF	10uF			Connected to the drain of the reverse blocking MOSFET (RBFET) and the drain of HSFET. Put 10 µF ceramic capacitor on PMID to GND.
BAT	13-14						**Positive battery connection point**	
		Required	BAT caps	10uF	10uF			Battery connection point to the positive terminal of the battery pack. The internal BATFET and current sensing is connected between SYS and BAT. 1. Connect a 10 µF closely to the BAT pin. 2. Charger may operate normally when battery is not connected.
SYS	15-16						**Converter output connection point**	
		Required	SYS caps	10uF	20uF	20uF		Connect a 20 µF closely to the SYS pin. The preferred ceramic capacitor is 6V or higher rating, X7R or X5R.
SW	19-20						**Switching node connecting to output inductor**	
		Required	Output inductor	1uH		2.2uH		Switching node output. Connected to output inductor. The charger device has internal loop compensator.
		Optional	SW Resistor		* Ω		Switching converter snubber circuit	Snubber circuit values empirically determined if required. Recommend unpopulated footprint on new designs.
		Optional	SW Cap		* F			
BTST	21						**PWM high side driver positive supply.**	
		Required	BTST-SW cap	0.047uF	0.047uF	0.047uF		Connect the 0.047µF bootstrap capacitor from SW to BTST.
		Optional	BTST resistor		* Ω		Bootstrap capacitor snubbing resistor	Help with EMI performance. Recommend unpopulated footprint on new designs.
REGN	22						**PWM low side driver positive supply output.**	
		Required	REGN cap	4.7uF	4.7uF	4.7uF		Connect a 4.7 µF (10 Vrating) ceramic capacitor from REGN to analog GND. The capacitor should be placed close to the IC. REGN also serves as bias rail of the TS pin.
GND	17-18						**Power ground**	
		Required						Power ground and signal ground
Thermal PAD		Required						Ground reference for the device that is also the thermal pad used to conduct heat from the device. This connection serves two purposes. 1) Provide an electrical ground connection for the device. 2. Provide a low thermal-impedance path from the device die to the PCB. This pad should be tied externally to a ground plane.