Description

The GT55N06 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

VDSS	RDS(ON) @10V (typ)	RDS(ON) @4.5V (typ)	ID
60V	6.8mΩ	9.5 mΩ	53A

- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation
- Special process technology for high ESD capability
- Totally Lead-Free&Fully RoHS Compliant

Application

Synchronus Rectification in DC/DC and AC/DC Converters
· Industrial and Motor Drive applications
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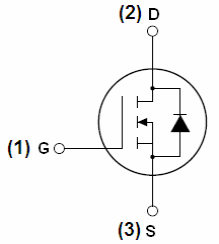
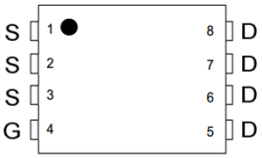
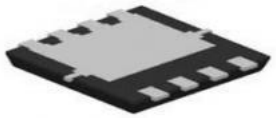
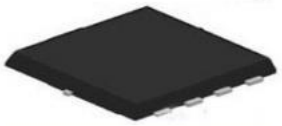


Schematic diagram



Marking and pin assignment





DFN 5x6-8L

Absolute Maximum Ratings T_A =25°C unless otherwise noted

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current [G]	T_A=25°C	I_D	53	A
	T_A=100°C		34	
Pulsed Drain Current [C]		I_{DM}	110	A
Avalanche energy L=0.5mH [C]		E_{AS}	195	mJ
Power Dissipation [A]	T_A=25°C	P_{DSM}	70	W
	T_A=70°C		28	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	°C

Thermal Characteristics

Parameter		Symbol	Maximum		Units
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	14	17	°C/W
Maximum Junction-to-Ambient [A D]	Steady-State		40	55	°C/W
Maximum Junction-to-Case	Steady-State	$R_{\theta JC}$	1.3	1.8	°C/W

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250μA, V_{GS}=0V	60	65		V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=60V, V_{GS}=0V			1	μA
		T_J=55°C			5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}=±20V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	1.1	1.7	2.5	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=20A		6.8	8.2	mΩ
		V_{GS}=4.5V, I_D=20A		9.5	12.0	mΩ
g_{FS}	Diode Forward Voltage	V_{DS}=5V, I_D=20A	30			S
V_{SD}	Diode Forward Voltage	I_S=20A,V_{GS}=0V		0.85	0.99	V
I_S	Maximum Body-Diode Continuous Current [G]				53	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=30V, f=1MHz		1988		pF
C_{oss}	Output Capacitance			470		pF
C_{rss}	Reverse Transfer Capacitance			14		pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz		1.6		Ω
SWITCHING PARAMETERS						
Q_g(10V)	Total Gate Charge	V_{GS}=10V, V_{DS}=30V, I_D=20A		31		nC
Q_g(4.5V)	Total Gate Charge			16		nC
Q_{gs}	Gate Source Charge			6		nC
Q_{gd}	Gate Drain Charge			5		nC
$t_{D(on)}$	Turn-on Delay Time	V_{GS}=10V, V_{DS}=15V, R_L=2.5Ω, R_{GEN}=3Ω		10.5		ns
t_r	Turn-on Rise Time			4.5		ns
$t_{D(off)}$	Turn-off Delay Time			29.5		ns
t_f	Turn-off Fall Time			8		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=20A,di/dt=500A/μs		17		ns
Q_{rr}	Body Diode Reverse Recovery charge	I_F=20A,di/dt=500A/μs		58		nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25° C. The Power dissipation P_{DSM} is based on $R_{\theta JA}$ t≤ 10s and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on $T_{J(MAX)}$=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Single pulse width limited by junction temperature TJ(MAX)=150° C.

D. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=150° C. The SOA curve provides a single pulse rating.

G. The maximum current rating is package limited.

Typical Performance Characteristics

Fig 1: Output Characteristics

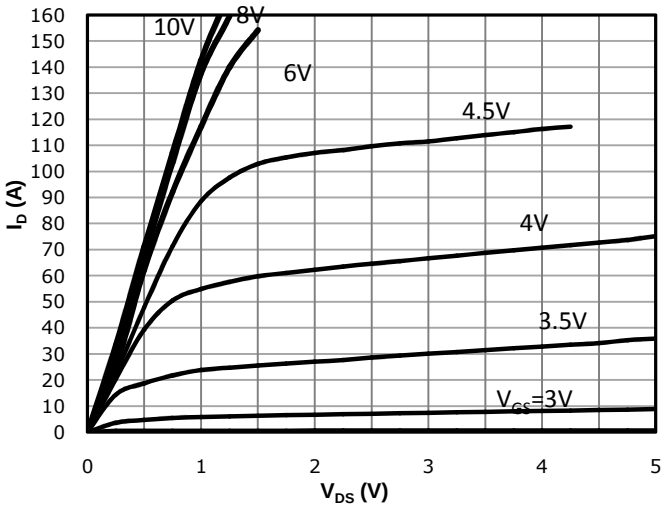


Fig 2: Transfer Characteristics

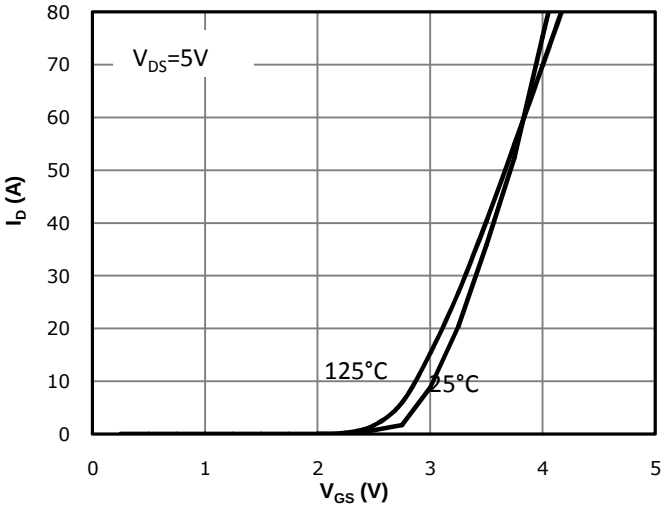


Fig 3: Rds(on) vs Drain Current and Gate Voltage

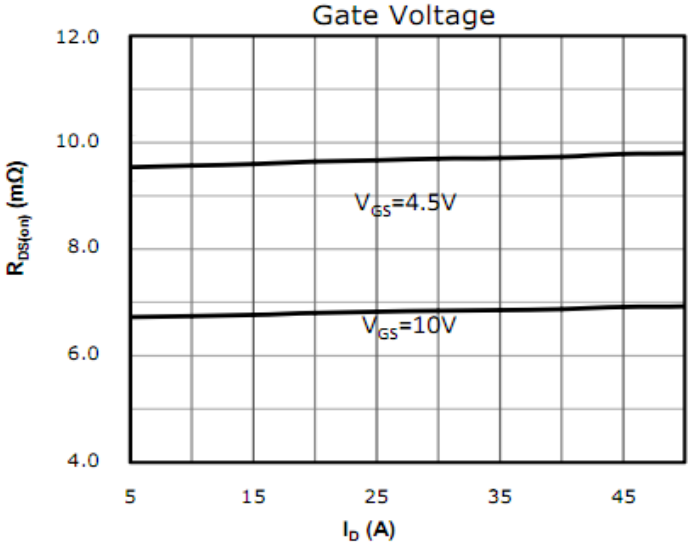


Fig 4: Rds(on) vs Gate Voltage

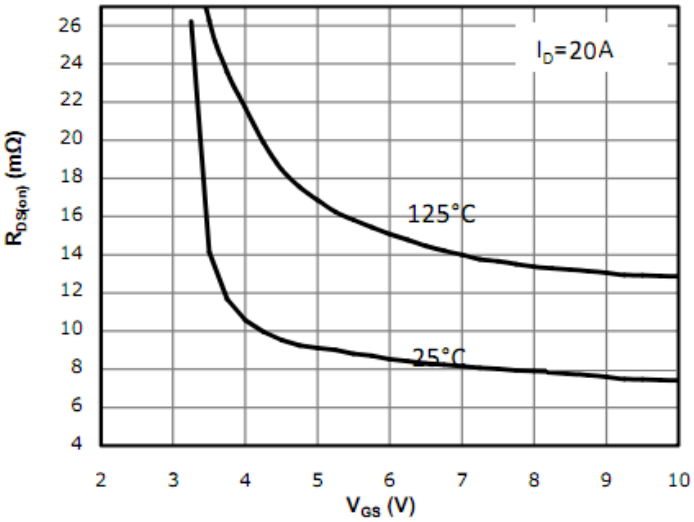


Fig 5: Rds(on) vs. Temperature

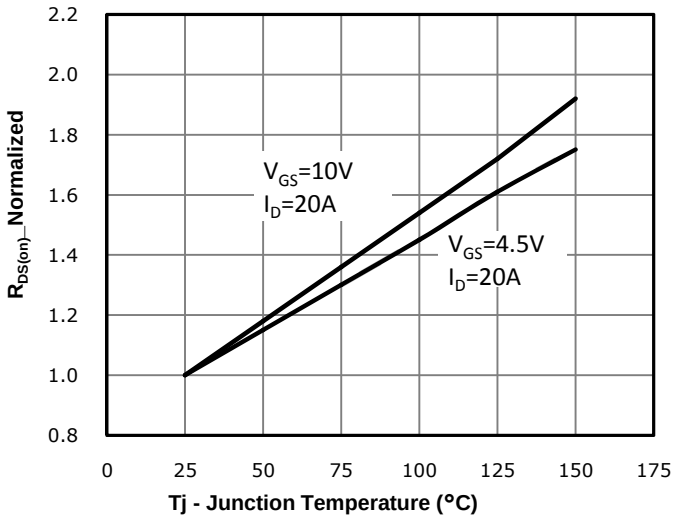


Fig 6: Capacitance Characteristics

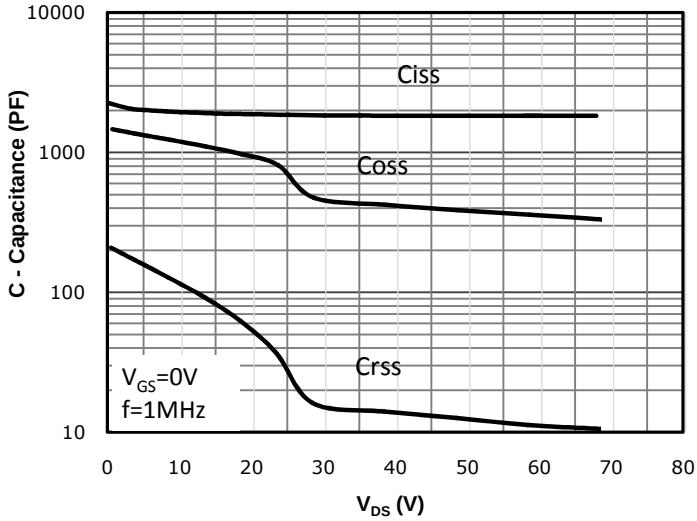


Fig 7: Gate Charge Characteristics

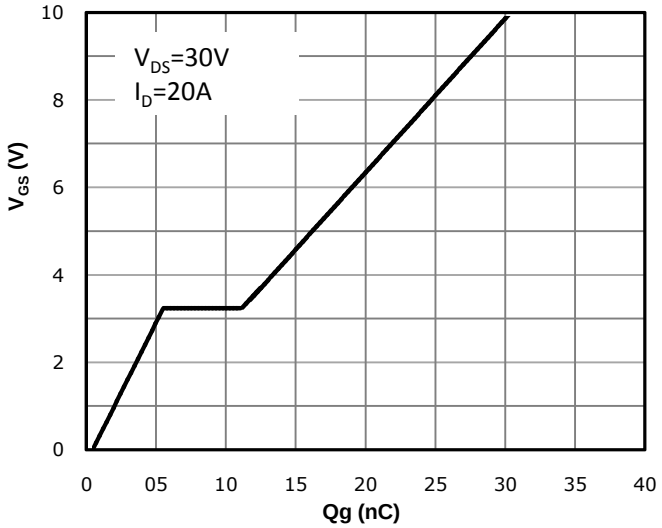


Fig 8: Body-diode Forward Characteristics

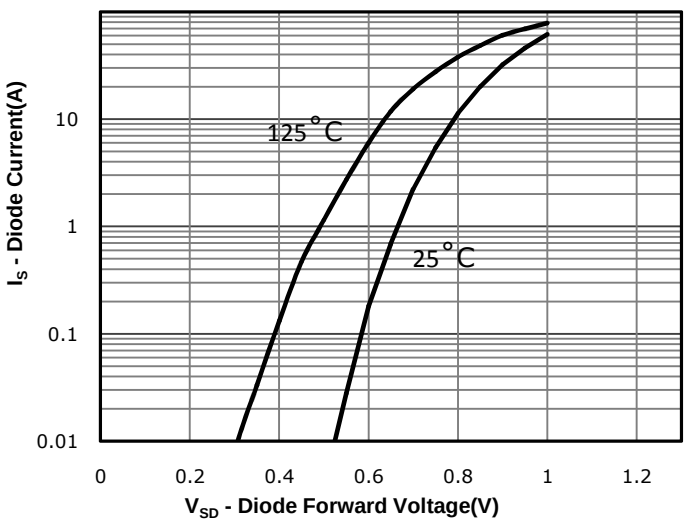


Fig 9: Power Dissipation

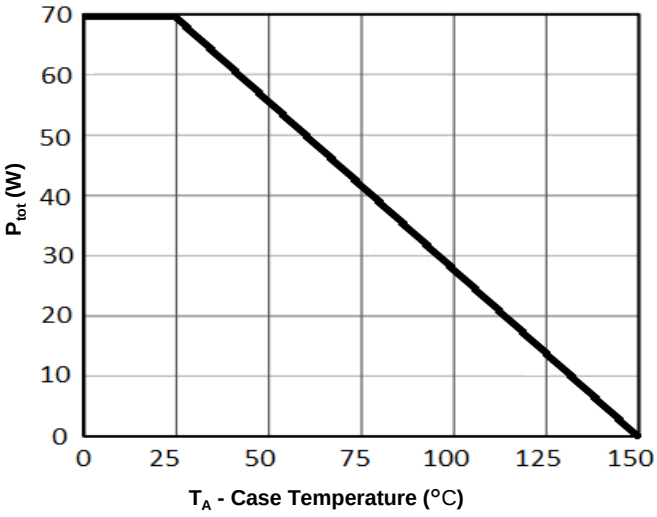


Fig 10: Drain Current Derating

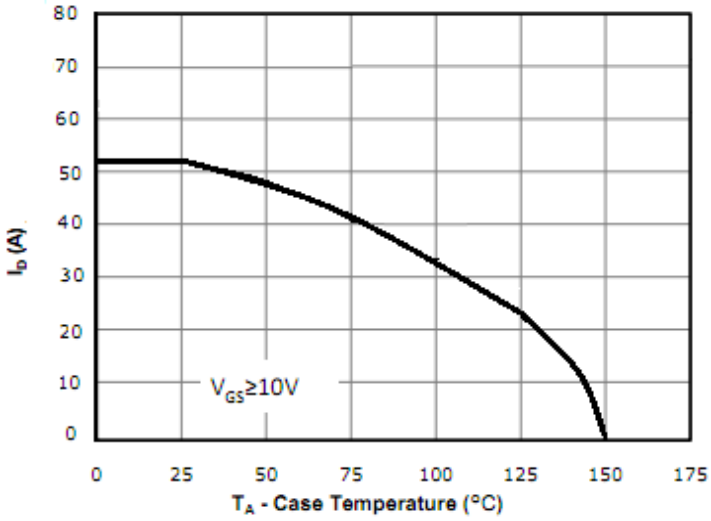


Figure A: Gate Charge Test Circuit & Waveforms

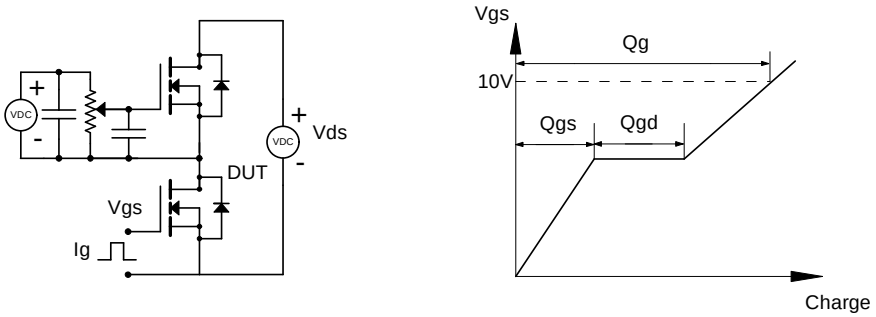


Figure B: Resistive Switching Test Circuit & Waveforms

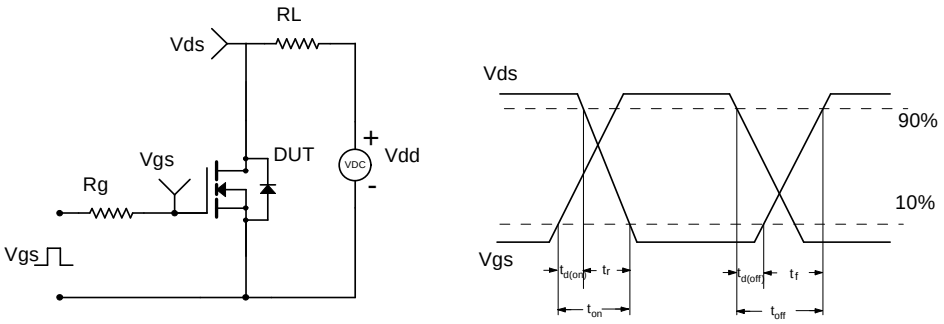


Figure C: Unclamped Inductive Switching (UIS) Test

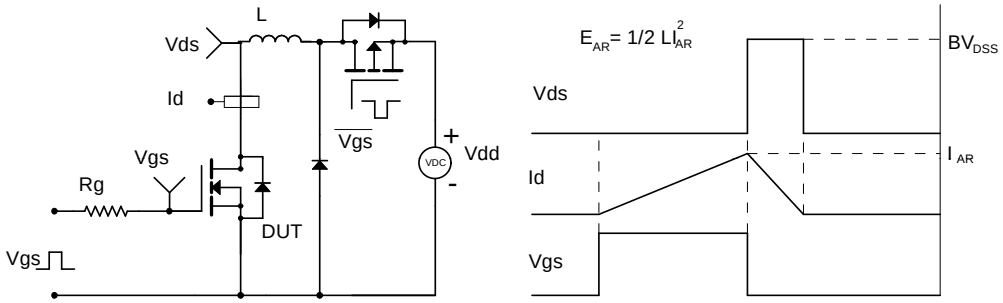
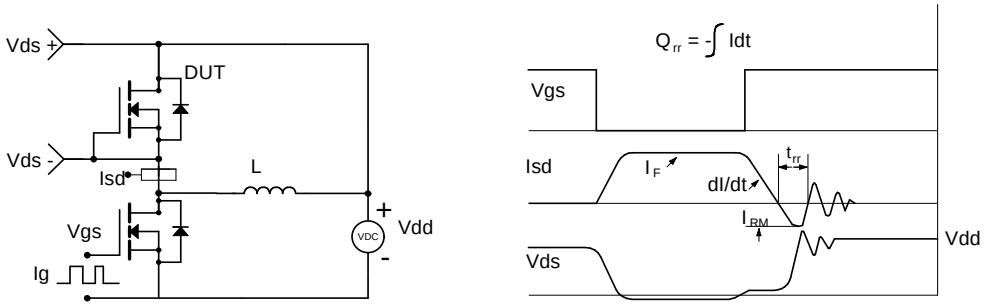
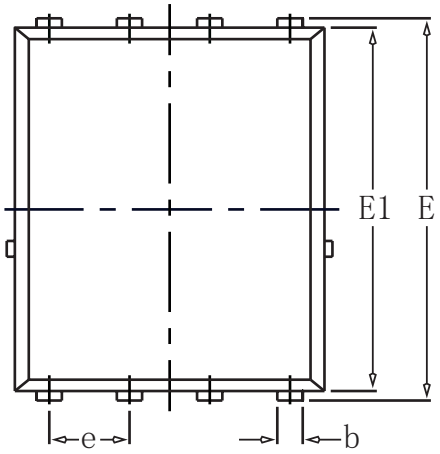
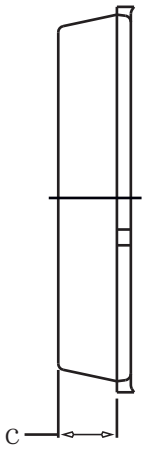


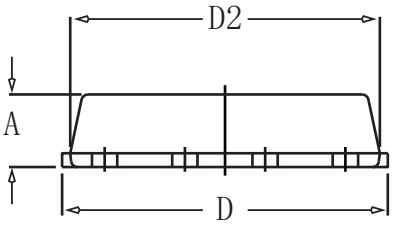
Figure D: Diode Recovery Test Circuit & Waveforms

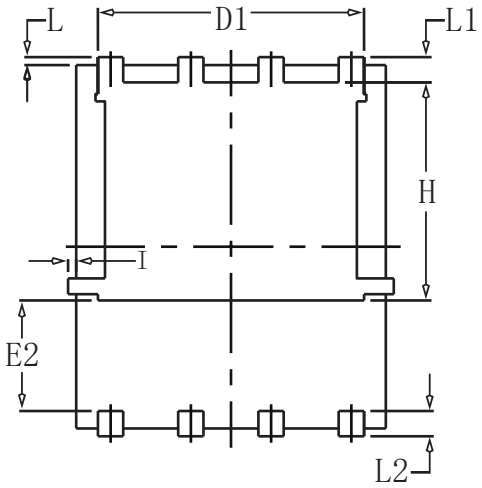


package information









SYMBOL	COMMON			
	MM		INCH	
	MIN	MAX	MIN	MAX
A	1.03	1.17	0.0406	0.0461
b	0.34	0.48	0.0134	0.0189
c	0.824	0.970	0.0324	0.0382
D	4.80	5.40	0.1890	0.2126
D1	4.11	4.31	0.1618	0.1697
D2	4.80	5.00	0.1890	0.1969
E	5.59	6.15	0.2343	0.2421
E1	5.65	5.85	0.2224	0.2303
E2	1.60	–	0.0630	–
e	1.27 BSC		0.05 BSC	
L	0.05	0.25	0.0020	0.0098
L1	0.38	0.50	0.0150	0.0197
L2	0.38	0.50	0.0150	0.0197
H	3.30	3.50	0.1299	0.1378
I	–	0.18	–	0.0070