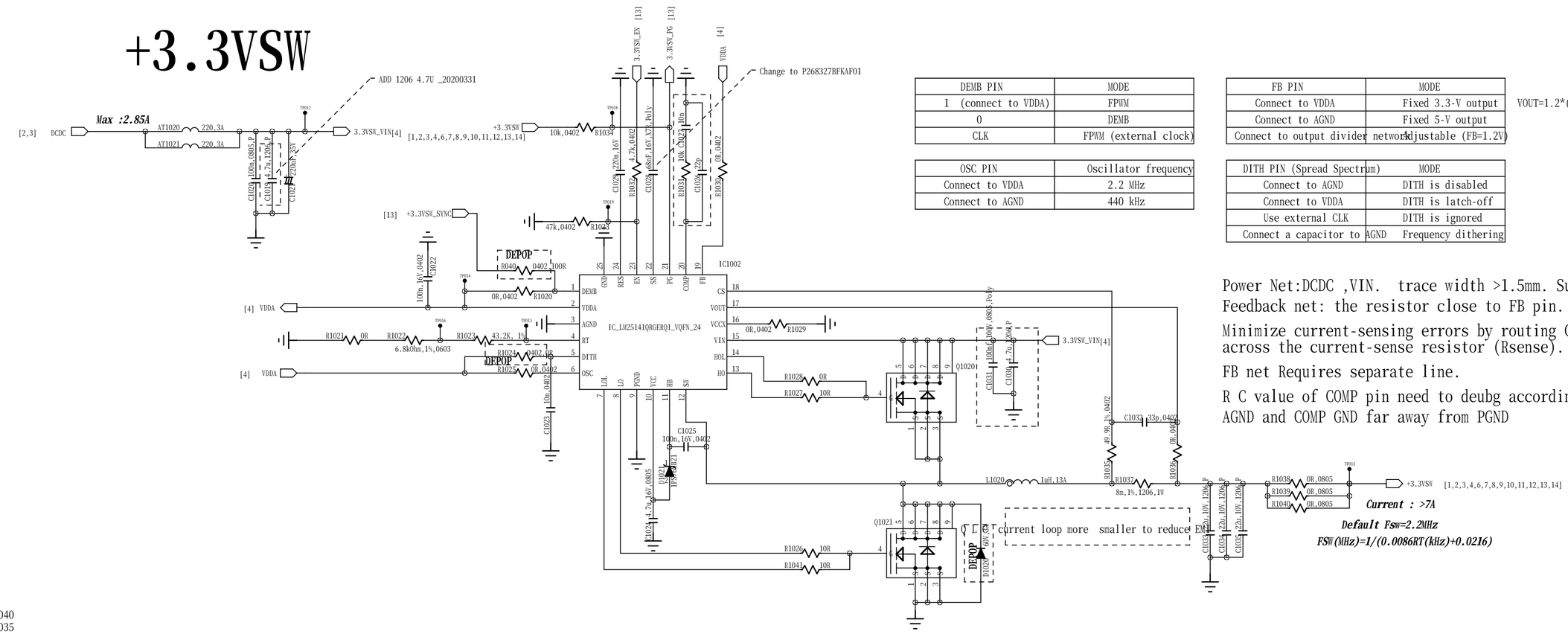
+3.3VSW



DEMB PIN	MODE
1 (connect to VDDA)	FPWM
0	DEMB
CLK	FPWM (external clock)

OSC PIN	Oscillator frequency
Connect to VDDA	2.2 MHz
Connect to AGND	440 kHz

FB PIN	MODE
Connect to VDDA	Fixed 3.3-V output
Connect to AGND	Fixed 5-V output
Connect to output divider network	Adjustable (FB=1.2V)

VOUT=1.2*(1+R2/R1)R2/R1=7/4

DITH PIN (Spread Spectrum)	MODE
Connect to AGND	DITH is disabled
Connect to VDDA	DITH is latch-off
Use external CLK	DITH is ignored
Connect a capacitor to AGND	Frequency dithering

Power Net:DCDC ,VIN. trace width >1.5mm. Suggest to use the copper panel
Feedback net: the resistor close to FB pin.

Minimize current-sensing errors by routing CS and VOUT using a kelvin ser
across the current-sense resistor (Rsense).

FB net Requires separate line.

R C value of COMP pin need to deubg according to the ripple of 3.3VSW.
AGND and COMP GND far away from PGND

R1020-1040
C1020-1035