WIDE V_{IN} DC/DC Power Solutions
Reliable Power for Demanding Systems

LM(2)5148/-Q1 Synchronous Buck Controller Design Tool

About | = Input Box | TERMS OF USE

LM5148

Step 1: Operating Specifications

Input Voltage – Min, $V_{IN(min)}$	**45**	**V**
Input Voltage – Nom, $V_{IN(nom)}$	**48**	**V**
Input Voltage – Max, $V_{IN(max)}$	**48**	**V**
Output Voltage, V_{OUT}	**36**	**V**
Full Load Output Current, I_{OUT}	**10**	**A**
Switching Frequency, F_{SW}	**253**	**kHz**
Frequency Set Resistor, R_T	86.6	kΩ
Ambient Temperature, T_A	**25**	**°C**

Step 2: Current Sense Resistor

Required I_{OCP} Setpoint at $V_{IN(nom)}$	**10**	**A**
Recommended Shunt Resistance	5.4	mΩ
Shunt Resistance, R_S	**2**	**mΩ**
Min Inductor Sat Current, $I_{LO(SAT)}$	30.0	A
Max Power Loss in Shunt	1.69	W
$I_{OUT(typ)}$ at OCP Inception: $V_{IN(min)}$	29.1	A
$V_{IN(nom)}$	28.8	A
$V_{IN(max)}$	28.8	A

Step 3: Buck Inductance

Inductance for Ideal Slope Comp	12.53	µH
Inductance, L_O	**15**	**µH**
Inductor DCR	**2.6**	**mΩ**
ΔI_L as a % at $V_{IN(nom)}$	24	%
Estimate Core Loss at $V_{IN(nom)}$	**0.2**	**W**

Step 4: Output Capacitors

Output Voltage Ripple Spec	**100**	**$mV_{PK=PK}$**
Minimum Output Capacitance	11.7	µF
Output Capacitance (derated), C_{OUT}	**34**	**µF**
Maximum Permitted ESR	40	mΩ
Output Capacitor ESR	**1**	**mΩ**
Resulting Output Voltage Ripple (max)	35	mV_{PK-PK}
Output Capacitor RMS Current (max)	0.69	A_{RMS}

Step 5: Input Capacitors

Input Voltage Ripple Spec	**100**	**mV_{PK-PK}**
Minimum Input Capacitance	99	µF
Input Capacitance (derated), C_{IN}	**200**	**µF**
Maximum Permitted ESR	4.5	mΩ
Input Capacitor ESR	**1**	**mΩ**
Resulting Input Voltage Ripple (max)	61	mV_{PK-PK}
Input Capacitor RMS Current (max)	5.0	A_{RMS}

Step 6: Precision Enable, DRSS, FPWM / PFM

UVLO Divider | DRSS Enabled | FPWM

Input Voltage UVLO Turn On	**45**	**V**
Input Voltage UVLO Turn Off	**43**	**V**
Upper Enable Resistor, R_{UV1}	200	kΩ
Lower Enable Resistor, R_{UV2}	4.5	kΩ
Configuration Resistor, R_{CNFG}	41.2	kΩ

*** Tie PFM to GND**

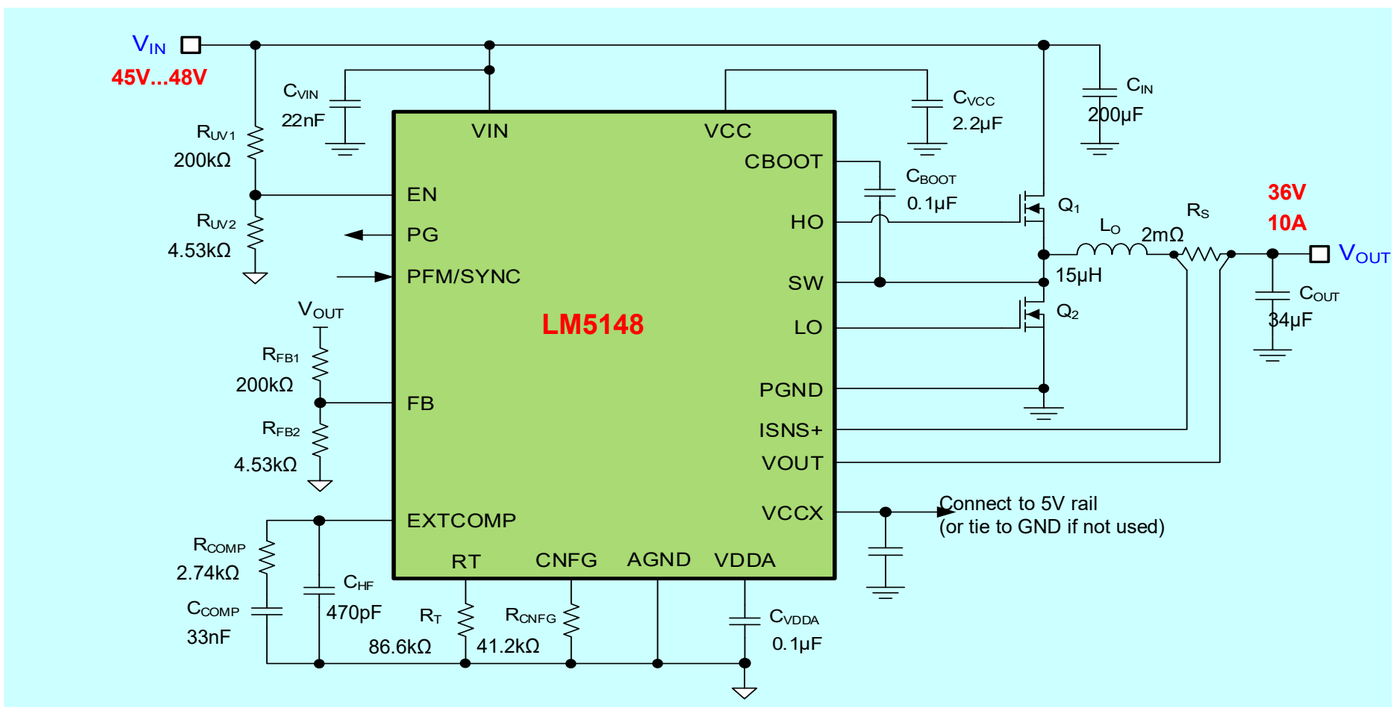
Step 7: Compensation Design

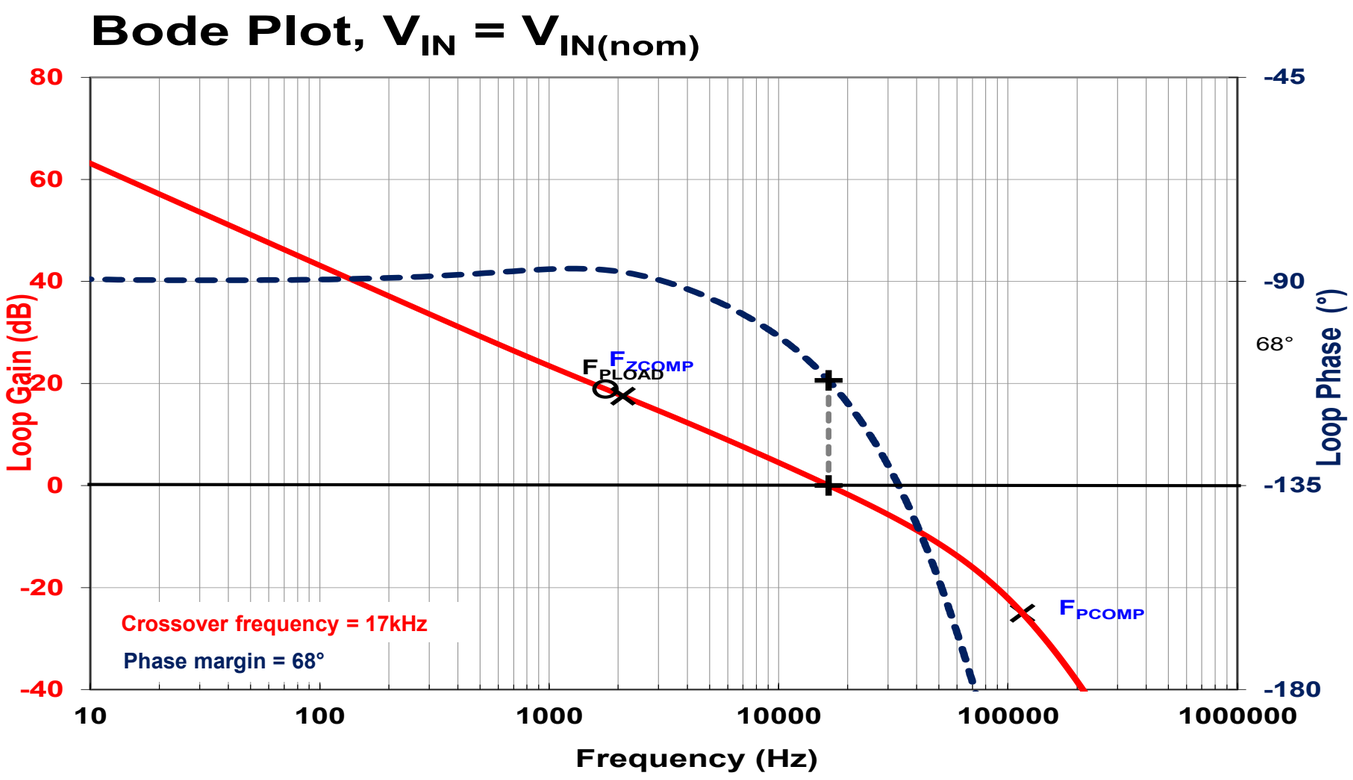
External Compensatic

Load Pole Frequency	2096	Hz
ESR Zero Frequency	4681	kHz
Desired Crossover Frequency	**17**	**kHz**
Error Amp Pole Frequency	0.08	Hz
Upper Feedback Resistor	**200**	**kΩ**
Lower Feedback Resistor	4.53	kΩ
Actual Output Voltage Setpoint	36.120	V

Compensation Components

	Calculated / Std Values	Std Values		Actual P/Z Frequencies
R_{C1}	2.7	2.74	**2.74** **kΩ**	0.1 Hz (F_{PEA})
C_{C1}	34.4	33	**33** **nF**	1.8 kHz (F_{ZCOMP})
C_{C2}	430	470	**470** **pF**	116 kHz (F_{PCOMP})





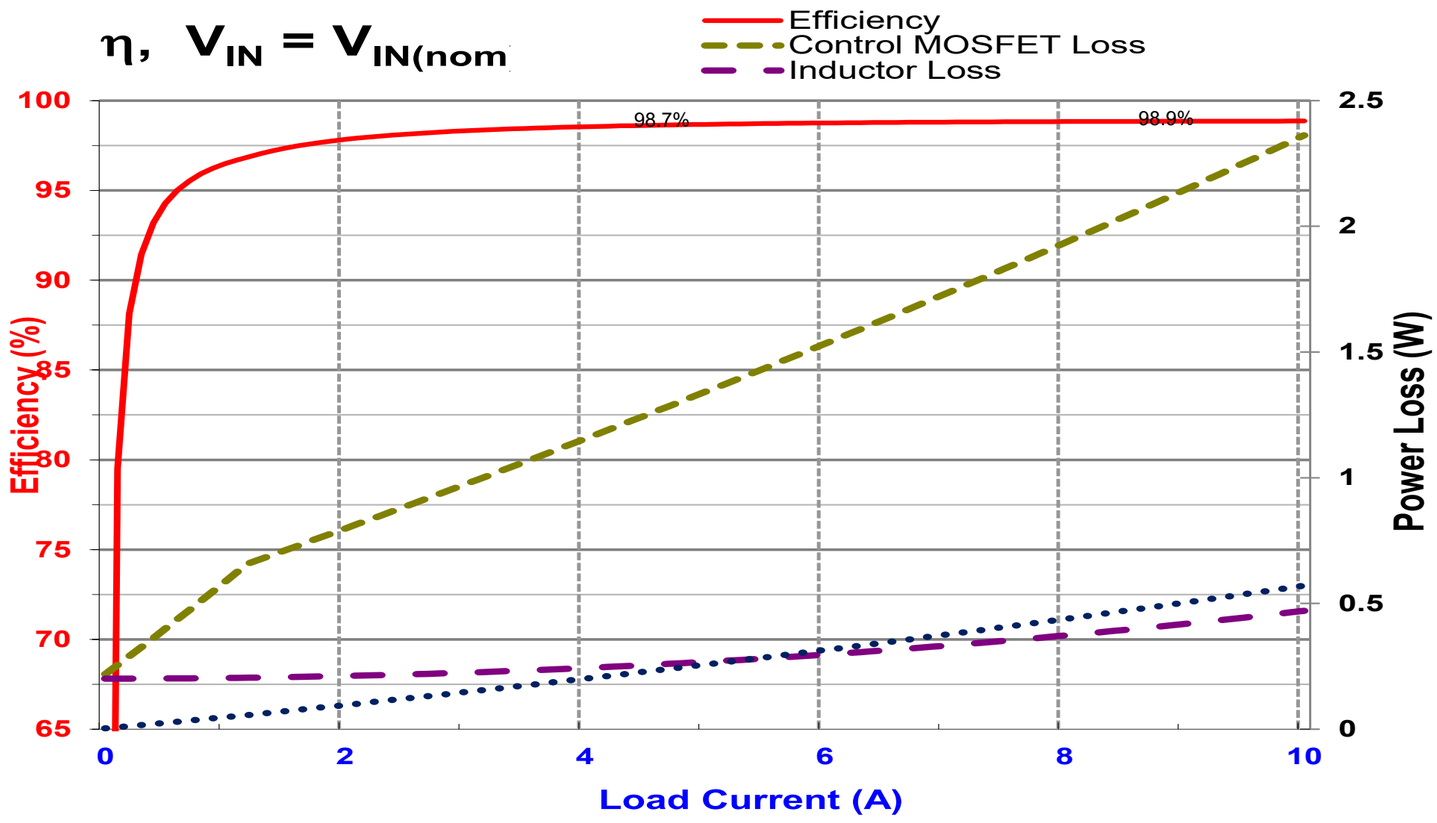
Efficiency / Power Loss Analyzer

Step 8: Efficiency

	Power MOSFETs (Q_1, Q_2) '852, '824 High-side	Low-side	
On-State Resistance, $R_{DS(on)}$	**2.6**	**4.4**	mΩ
Total Gate Charge, Q_G	**20**	**18**	nC
Gate-Drain Charge, Q_{GD}	**6.7**	**5.9**	nC
Gate-Source Charge, Q_{GS}	**8.8**	**6.9**	nC
Output Charge, Q_{OSS}		**32**	nC
Output Capacitance, C_{OSS}	**622**	**380**	pF
Gate Resistance, R_G	**0.8**	**1.2**	Ω
Transconductance, g_{FS}	**116**	**128**	S
Gate-Source Threshold Voltage, V_{TH}	**1.9**	**1.8**	V
Body Diode Forward Voltage, V_{BD}	**0.8**	**0.8**	V
Body Diode Rev Recovery Charge, Q_{RR}		**100**	nC
Thermal Resistance, θ_{JA}	**50**	**50**	°C/W

External Schottky Diode (if applicable)

Schottky Fwd Voltage, V_{FWDsch}	**0**	V
Schottky Rev Recovery Charge, Q_{RRsch}	**0**	nC



Step 9: IC Power Loss

No External VCC

IC Power Dissipation	0.46 W
IC Junction Temperature (estimate)	40.7 °C

*** Tie VCCX to PGND**