WIDE V_{IN} DC/DC Power Solutions
Reliable Power for Demanding Systems

LM(2)5148/-Q1 Synchronous Buck Controller Design Tool

About | = Input Box | TERMS OF USE

LM5148

Step 1: Operating Specifications

Input Voltage – Min, $V_{IN(min)}$	**45**	**V**
Input Voltage – Nom, $V_{IN(nom)}$	**48**	**V**
Input Voltage – Max, $V_{IN(max)}$	**50**	**V**
Output Voltage, V_{OUT}	**24**	**V**
Full Load Output Current, I_{OUT}	**16**	**A**
Switching Frequency, F_{SW}	**400**	**kHz**
Frequency Set Resistor, R_T	54.9	kΩ
Ambient Temperature, T_A	**25**	**°C**

Step 2: Current Sense Resistor

Required I_{OCP} Setpoint at $V_{IN(nom)}$	**10**	**A**
Recommended Shunt Resistance	4.9	mΩ
Shunt Resistance, R_S	**2**	**mΩ**
Min Inductor Sat Current, $I_{LO(SAT)}$	30.0	A
Max Power Loss in Shunt	1.56	W
$I_{OUT(typ)}$ at OCP Inception: $V_{IN(min)}$	27.9	A
$V_{IN(nom)}$	27.8	A
$V_{IN(max)}$	27.7	A

Step 3: Buck Inductance

Inductance for Ideal Slope Comp	5.28	µH
Inductance, L_O	**6.8**	**µH**
Inductor DCR	**8.9**	**mΩ**
ΔI_L as a % at $V_{IN(nom)}$	28	%
Estimate Core Loss at $V_{IN(nom)}$	**0.2**	**W**

Step 4: Output Capacitors

Output Voltage Ripple Spec	**100**	**$mV_{PK=PK}$**
Minimum Output Capacitance	13.9	µF
Output Capacitance (derated), C_{OUT}	**43**	**µF**
Maximum Permitted ESR	21	mΩ
Output Capacitor ESR	**1**	**mΩ**
Resulting Output Voltage Ripple (max)	33	mV_{PK-PK}
Output Capacitor RMS Current (max)	1.33	A_{RMS}

Step 5: Input Capacitors

Input Voltage Ripple Spec	**400**	**mV_{PK-PK}**
Minimum Input Capacitance	25	µF
Input Capacitance (derated), C_{IN}	**430**	**µF**
Maximum Permitted ESR	20.6	mΩ
Input Capacitor ESR	**1**	**mΩ**
Resulting Input Voltage Ripple (max)	42	mV_{PK-PK}
Input Capacitor RMS Current (max)	8.0	A_{RMS}

Step 6: Precision Enable, DRSS, FPWM / PFM

UVLO Divider | DRSS Enabled | FPWM

Input Voltage UVLO Turn On	**45**	**V**
Input Voltage UVLO Turn Off	**43**	**V**
Upper Enable Resistor, R_{UV1}	200	kΩ
Lower Enable Resistor, R_{UV2}	4.5	kΩ
Configuration Resistor, R_{CNFG}	41.2	kΩ

*** Tie PFM to GND**

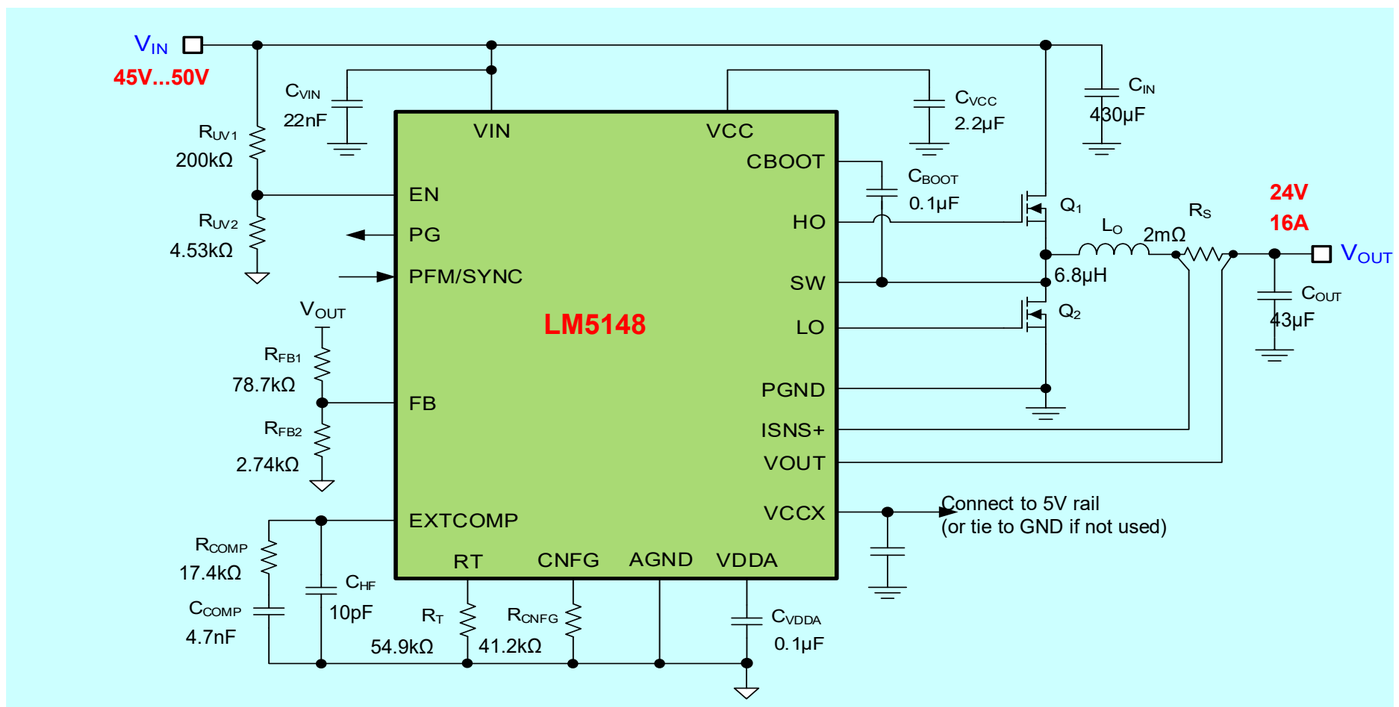
Step 7: Compensation Design

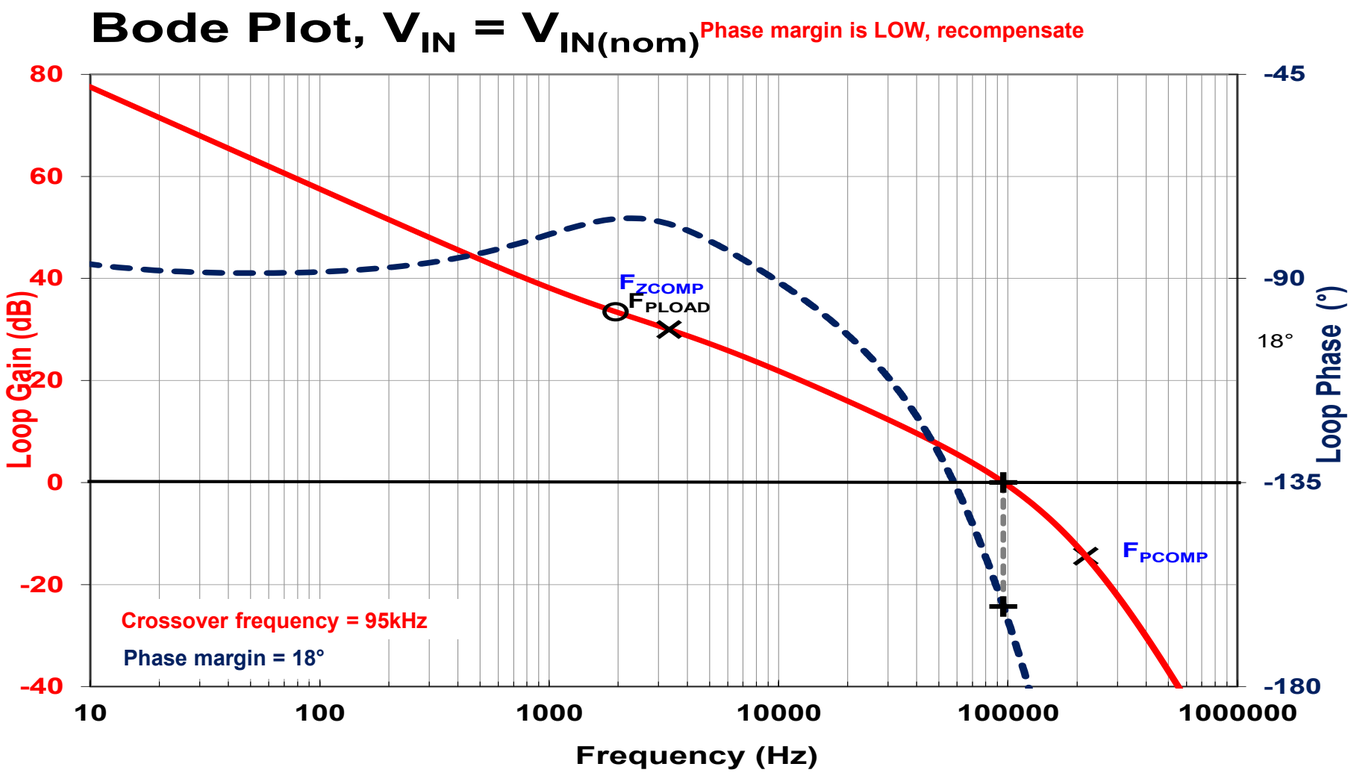
External Compensatic

Load Pole Frequency	3334	Hz
ESR Zero Frequency	3701	kHz
Desired Crossover Frequency	**40**	**kHz**
Error Amp Pole Frequency	0.53	Hz
Upper Feedback Resistor	**78.7**	**kΩ**
Lower Feedback Resistor	2.74	kΩ
Actual Output Voltage Setpoint	23.778	V

Compensation Components

	Calculated / Std Values	Std Values	Actual P/Z Frequencies
R_{C1}	5.4 / 5.36	**17.4 kΩ**	0.5 Hz (F_{PEA})
C_{C1}	7.4 / 6.8	**4.7 nF**	1.9 kHz (F_{ZCOMP})
C_{C2}	115 / 120	**10 pF**	219 kHz (F_{PCOMP})





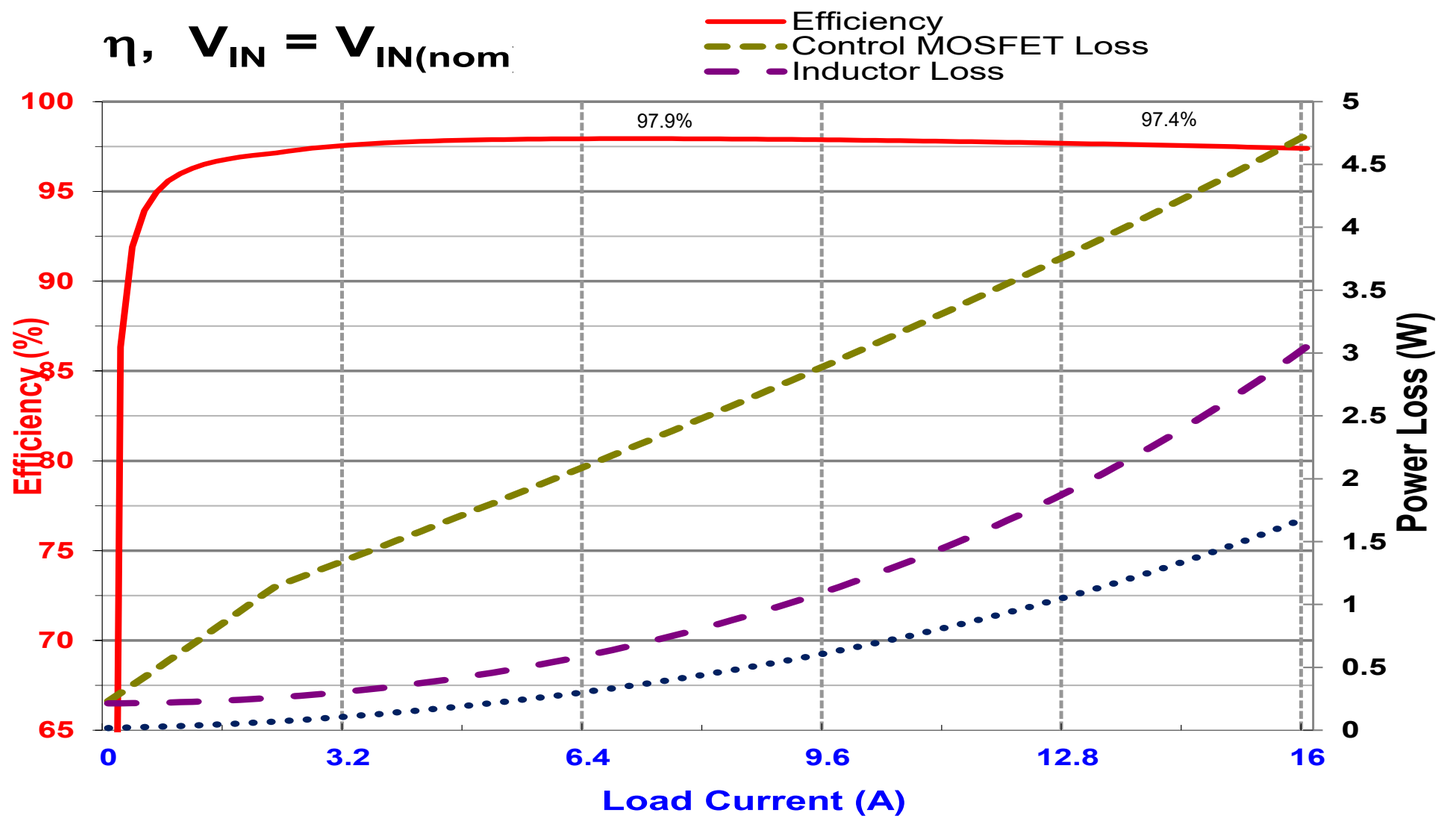
Efficiency / Power Loss Analyzer

Step 8: Efficiency

	Power MOSFETs (Q_1, Q_2) '852, '824 High-side	Low-side	
On-State Resistance, $R_{DS(on)}$	**2.6**	**8.8**	mΩ
Total Gate Charge, Q_G	**26**	**9**	nC
Gate-Drain Charge, Q_{GD}	**6.7**	**2**	nC
Gate-Source Charge, Q_{GS}	**8.8**	**4.5**	nC
Output Charge, Q_{OSS}		**30**	nC
Output Capacitance, C_{OSS}	**808**	**640**	pF
Gate Resistance, R_G	**1.6**	**1.2**	Ω
Transconductance, g_{FS}	**116**	**82**	S
Gate-Source Threshold Voltage, V_{TH}	**2.3**	**2**	V
Body Diode Forward Voltage, V_{BD}	**0.8**	**0.9**	V
Body Diode Rev Recovery Charge, Q_{RR}		**19**	nC
Thermal Resistance, θ_{JA}	**50**	**41**	°C/W

External Schottky Diode (if applicable)

Schottky Fwd Voltage, V_{FWDsch}	**0**	V
Schottky Rev Recovery Charge, Q_{RRsch}	**0**	nC



Step 9: IC Power Loss

VCCX Connectec

IC Power Dissipation	0.07 W
IC Junction Temperature (estimate)	27.4 °C