

10.2 Layout Example

A layout example is shown in 图 97. A four-layer board is used with 2-oz copper on the top and bottom layers and 1-oz copper on the inner two layers. 图 97 shows the relative scale of the LM73605-Q1/6-Q1 device with 0805 and 1210 input and output capacitors, 7-mm × 7-mm inductor and 0603 case size for all other passive components. The trace width of the signal connections are not to scale.

The components are placed on the top layer and the high current paths are routed on the top layer as well. The remaining space on the top layer can be filled with GND polygon. Thermal vias are used under the DAP and around the device. The GND copper was extended to the outside of the device, which serves as copper heat sink.

The mid-layer 1 is right underneath the top layer. It is a solid ground plane, which serves as noise shielding and heat dissipation path.

The V_{OUT} sense trace is routed on the 3rd layer, which is mid-layer 2. Ground plane provided noise shielding for the sense trace. The V_{OUT} to BIAS connection is routed by a separate trace.

The bottom layer is also a solid ground copper in this example. Solid copper provides best heat sinking for the device. If components and traces need to be on the bottom layer, leave the area around thermal vias as solid as possible. Try not to cut heat dissipation path by a trace. The board can be used for various frequencies and output voltages, with component variation. For more details, see the [LM73605/LM73606 EVM User's Guide](#).

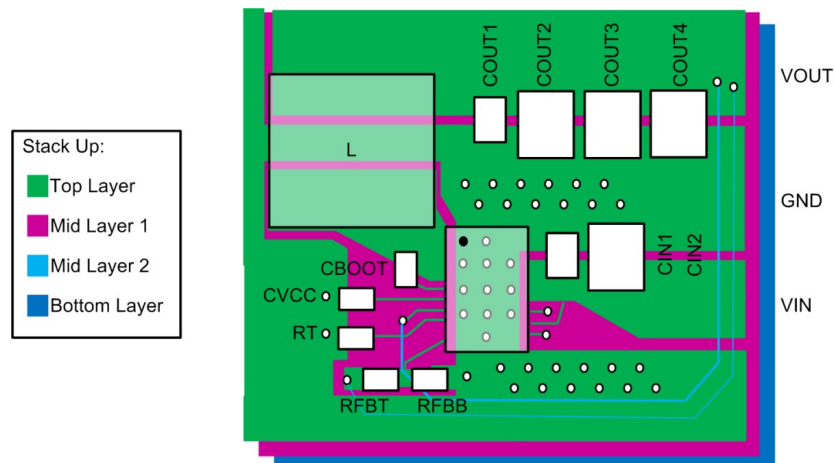


图 97. LM73605-Q1/6-Q1 Layout Example