Preliminary Datasheet
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LV2862

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LV2862
High Efficiency Wide Input Voltage Range Buck Regulator

Description

The LV2862 are PWM DC/DC buck (step-down) regulators. With a wide input range from 4V- 60V, they are suitable for a wide range of application from industrial to automotive for power conditioning from unregulated source. An ultra low 1uA current can further prolong battery life in shutdown mode. Operating frequency is fixed at 700kHz(X version) and 2.1MHz(Y version) allowing the use of small external components while still being able to have low output ripple voltage. Soft-start and compensation circuits are implemented internally, and these allow the device to be used with minimized external components.

The LV2862 is optimized for up to 600mA load currents, and it has a 0.765V nominal feedback voltage.

The device has built-in protection features such as pulse by pulse current limit, thermal sensing and shutdown due to excessive power dissipation. The LV2862 is available in a low profile TSOT-6L package.

Features

- **Input Range 4V to 60V**
- **1 µA Shutdown Current**
- **High Duty Cycle Operation Supported**
- **600mA Output Current Capability**
- **700kHz and 2.1 MHz Switching Frequency**
- **Internal Compensation**
- High Voltage Enable Input
- Internal Soft Start
- Over Current Protection
- Over Temperature Protection
- Small Overall Solution Size (TSOT-6L)

Applications

- **Power Meter**
- **Collector**
- **Concentrator**
- **Industrial Distributed Power Applications**

Typical Application Circuit
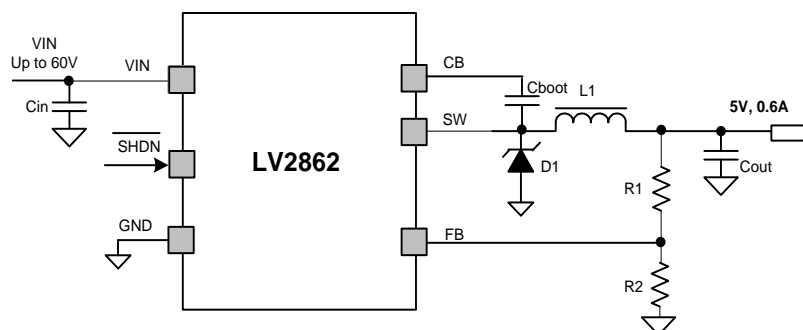
Typical application schematic

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Part Ordering Information

X=700kHz, Y=2.1MHz Switching frequency

Order Number	Package	Supplied As
LV2862XLVDDCT		250 Units on Tape and Reel
LV2862XLVDDCR	TSOT-6	3000 Units on Tape and Reel
LV2862YDDCT		250 Units on Tape and Reel
LV2862YDDCR		3000 Units on Tape and Reel

ABSOLUTE MAXIMUM RATINGS [(1)]

NO.		DESCRIPTION	VALUE	UNIT
1.1	VIN, /SHDN	Unregulated inputs	65	V
1.2	FB	Sense voltage for error amplifiers	5.5	V
1.3	SW	Switch point for buck converter	65 -2V for 30nS	V
1.4	CB	Bootstrap capacitor voltage	70	V
1.5	Top	Operating ambient temperature	-40 to 125	℃
1.6	T_S	Storage Temperature Range	-55 to 165	℃
1.7	T_J	Operating junction temperature range	-40 to 150	℃

Note (1):   Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Note (2):   The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin

THERMAL INFORMATION

	THERMAL METRIC	VALUE	UNIT
θ_{JA} [(3)]	Junction-to-ambient thermal resistance	102	
θ_{JCtop}	Junction-to-case (top) thermal resistance	36.9	
θ_{JB}	Junction-to-board characterization parameter	28.4	℃/W
Ψ_{JT}	Junction-to-top characterization parameter	3.2	
Ψ_{JB}	Junction-to-board characterization parameter	38.2	

RECOMMEDED OPERATING CONDITIONS

FUNCTION	TERMINAL	VALUE	UNIT
Buck Regulator	VIN	4 to 60	V
	CB	3.8 to 65	V
	SW	-1 to 60	V
	FB	0 to 5	V
Control	/SHDN	0 to 60	V

Note (3):   All numbers apply for packages soldered with 2 oz. copper on 4 layers in still air in accordance to JEDEC standards. Thermal resistance varies greatly with layout, copper thickness, number of layers in PCB, power distribution, number of thermal vias, board size, ambient temperature, and air flow.

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Electrical characteristics

VIN = 6V to 27V, /SHDN = VIN, T_A = 25 °C, unless otherwise noted.

PARAMETER	TEST CONDITIONS		Min	Typ	Max	Unit
VIN (Input Power Supply)						
Operating input voltage			4		60	V
Shutdown supply current	EN = 0 V, 25 °C			1	2	µA
Undervoltage lockout thresholds	On threshold			3.5		V
	Hysteresis			0.3		
Device on : not switching	V_{FB} = 0.765 V, VIN = 12 V, 25 °C			26		µA
Device on : not switching	Fixed 5V version, VIN = 12 V, 25 °C			31		µA
/SHDN AND UVLO						
Rising /SHDN Threshold Voltage			1.05	1.25	1.38	V
Input current	/SHDN = 2.3V			− 4.2		µA
	/SHDN = 0.9V			− 1		
Hysteresis current				− 3		µA
HIGH-SIDE MOSFET						
On-resistance	VIN = 12 V, CB to SW=5.8V			920		mΩ
t_{ON-min}	fsw = 2.1MHz			95		ns
D_{MAX} : Maximum duty cycle	LV2862 X			96		%
	LV2862 Y			97.5		
V_{FB} : Feedback voltage			0.747	0.765	0.782	V
CURRENT LIMIT						
Current limit threshold	VIN = 12 V, T_J = 25 °C	LV2862		1100	1600	mA
f_{SW} Switching frequency	LV2862 X		595	700	805	kHz
	LV2862 Y		1785	2100	2415	kHz
THERMAL PERFORMANCE						
$T_{SHUTDOWN}$ Thermal shutdown trip point				170		°C
T_{hys}	Hysteresis			10		°C

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Pin Configuration

DDC PACKAGE

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CB [1]   [6] SW

GND [2]   [5] V$_{IN}$

PIN 1 ID

FB [3]   [4] $\overline{SHDN}$
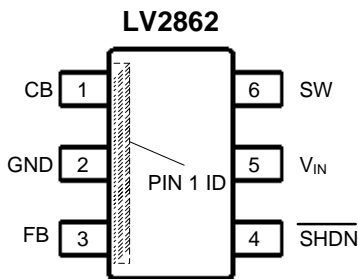
TSOT-6L (Top View)

PIN FUNCTIONS

Name	NO.	I/O	Description
CB	1	O	SW FET Gate Bias voltage. Connect Cboot cap between CB and SW
GND	2	-	Ground Connection
FB	3	I	Feedback Pin: Set feedback voltage divider ratio with $V_{OUT} = V_{FB}(1+(R1/R2))$
/SHDN	4	I	Enable and disable input pin(high voltage tolerant). Internal pull-up current source. Pull below 1.25V to disable. Float to enable. Adjust the input undervoltage lockout with two resistors.
VIN	5	I	Power input voltage pin: Input for internal supply and drain node input for internal high-side MOSFET
SW	6	I	Switch node, Connect to inductor, diode, and Cboot cap

TYPICAL CHARACTERISTICS

Unless otherwise specified the following conditions apply: Vin = 12V, Fsw=2.1MHz, T$_A$ = 25°C.

Efficiency vs. Load Current
(Fsw=2.1MHz, Vout=12V)

Efficiency vs. Load Current
(Fsw=2.1MHz, Vout=5V)

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Efficiency vs. Load Current
(Fsw=2.1MHz, Vin=18V/Vout=12V)

Line Regulation
(Vout=5V, Iout=200mA)

Load Regulation

Supply Current vs. Input Voltage

Switching Node and Output Voltage Waveform (500mA)

Load Transient Waveform (50mA to 500mA)

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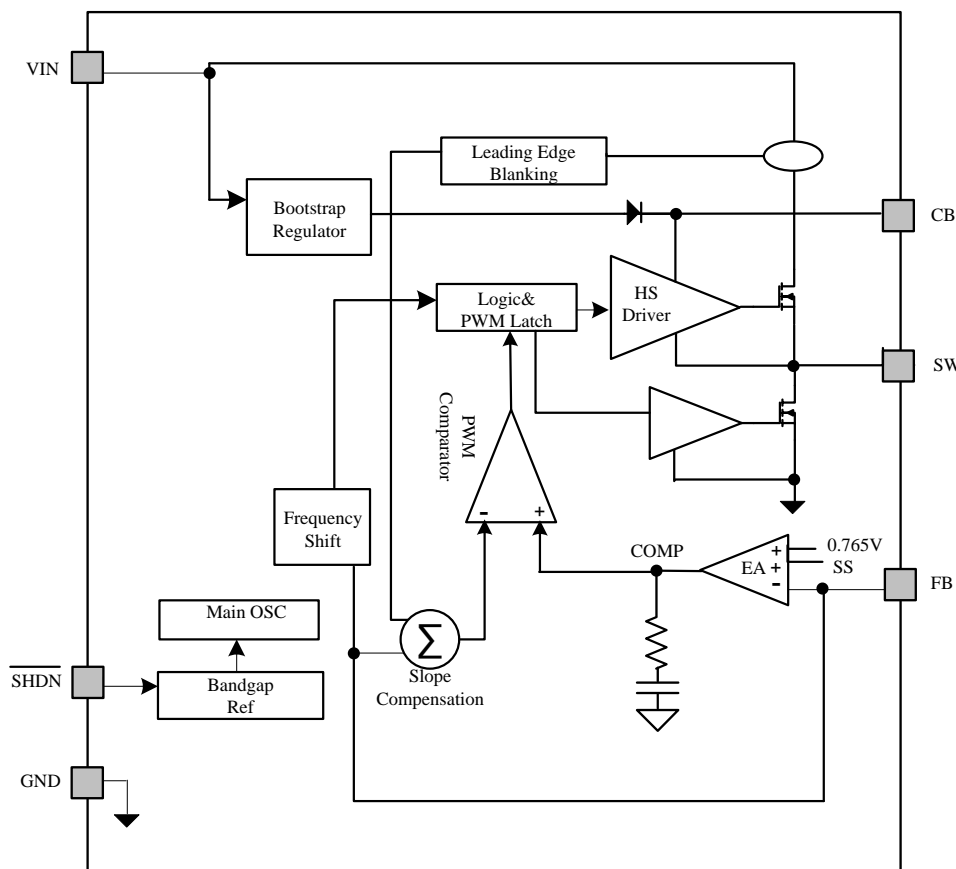**Rev 0.6**
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Start-up Waveform (12V/500mA)

Shutdown Waveform (12V/500mA)

Start-up Waveform (5V/500mA)

Shutdown Waveform (5V/500mA)

Short Circuit to Ground (5V)

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INTERNAL FUNCTIONAL BLOCKS

VIN

Leading Edge
Blanking

Bootstrap
Regulator

CB

Logic&
PWM Latch

HS
Driver

SW

PWM Comparator

Frequency
Shift

COMP

0.765V
SS

EA

FB

Main OSC

Slope
Compensation

SHDN

Bandgap
Ref

GND

DETAILED DESCRIPTION

The LV2862 device is a 60V, 600mA, step-down (buck) converter. The buck regulator has a very low quiescent current during the light load to prolong the battery life.

For LV2862, to improve performance during line and load transients it implements a constant frequency, current mode control which reduces output capacitance and simplifies frequency compensation design. Two switching frequency options, 700kHz and 2.1MHz, are available, thus smaller inductor and capacitor can be used. The LV2862 reduces the external component count by integrating the boot recharge diode. The bias voltage for the integrated high side MOSFET is supplied by a capacitor on the CB to SW pin. The boot capacitor voltage is monitored by an UVLO circuit and will turn the high side MOSFET off when the boot voltage falls below a preset threshold. The output voltage can be stepped down to as low as the 0.765V reference. Internal soft start is featured to minimize inrush currents.

Continuous Conduction Mode

The LV2862 steps the input voltage down to a lower output voltage. In continuous conduction mode (when the inductor current never reaches zero at steady state), the buck regulator operates in two cycles. The power switch is connected between VIN and SW. In the first cycle of operation the transistor is closed and the diode is reverse biased. Energy is collected in the inductor and the load current is supplied by Cout and the rising current through the inductor. During the second cycle the transistor is

open and the diode is forward biased due to the fact that the inductor current cannot instantaneously change direction. The energy stored in the inductor is transferred to the load and output capacitor. The ratio of these two cycles determines the output voltage. The output voltage is defined approximately as: D=VOUT/VIN and D' = (1-D) where D is the duty cycle of the switch, D and D' will be required for design calculations.

Fixed Frequency PWM Control

The LV2862 has two fixed frequency options, and it implements peak current mode control. The output voltage is compared through external resistors on the VFB pin to an internal voltage reference by an error amplifier which drives the internal COMP node. An internal oscillator initiates the turn on of the high side power switch. The error amplifier output is compared to the high side power switch current. When the power switch current reaches the level set by the internal COMP voltage, the power switch is turned off. The internal COMP node voltage will increase and decrease as the output current increases and decreases. The device implements a current limit by clamping the COMP node voltage to a maximum level.

Eco Mode

The LV2862 operates in eco mode at light load currents to improve efficiency by reducing switching and gate drive losses. For eco mode operation, the LV2862 senses peak current, not average or load current, so the load current where the device enters sleep mode is dependent on the output inductor value. When the load current is low and the output voltage is within regulation, the device enters eco mode and draws only 30uA input quiescent current.

Bootstrap Voltage (CB)

The LV2862 has an integrated boot regulator, and requires a small ceramic capacitor between the CB and SW pins to provide the gate drive voltage for the high side MOSFET. The CB capacitor is refreshed when the high side MOSFET is off and the low side diode conducts.

To improve drop out, the LV2862 is designed to operate at 100% duty cycle as long as the CB to SW pin voltage is greater than 2.1V. When the voltage from CB to SW drops below 2.1V, the high side MOSFET is turned off using an UVLO circuit which allows the low side diode to conduct and refresh the charge on the CB capacitor. Since the supply current sourced from the CB capacitor is low, the high side MOSFET can remain on for more switching cycles than are required to refresh the capacitor, thus the effective duty cycle of the switching regulator is high.

Attention must be taken in maximum duty cycle applications with light load. To ensure SW can be pulled to ground to refresh the CB capacitor, an internal circuit will charge the CB capacitor when the load is light or the device is working in dropout condition.

Set the output voltage

The output voltage is set using the feedback pin and a resistor divider connected to the output as shown on the front page schematic. The feedback pin voltage 0.765V, so the ratio of the feedback resistors sets the output voltage according to the following equation: Vout=0.765V (1+(R1/R2)) Typically R2 will be given as 100Ω - 10kΩ for a starting value. To solve for R1 given R2 and Vout uses R1=R2 ((Vout/0.765V)-1).

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Enable (/SHDN) and VIN Under Voltage Lockout

LV2862 /SHDN pin is a high voltage tolerant input with an internal pull up circuit. The device can be enabled even if the /SHDN pin is floating. The regulator can also be turned on using 1.23V or higher logic signals. If the use of a higher voltage is desired due to system or other constraints it may be used, a 100kΩ or larger resistor is recommended between the applied voltage and the /SHDN pin to protect the device. When /SHDN is pulled down to 0V, the chip is turned off and enters the lowest shutdown current mode. In shutdown mode the supply current will be decreased to approximately 1uA. If the shutdown function is not to be used the /SHDN pin may be tied to VIN. The maximum voltage to the SHDN pin should not exceed 60V.

LV2862 has an internal UVLO circuit to shutdown the output if the input voltage falls below an internally fixed UVLO threshold level. This ensures that the regulator is not latched into an unknown state during low input voltage conditions. The regulator will power up when the input voltage exceeds the voltage level. If there is a requirement for a higher UVLO voltage, the /SHDN can be used to adjust the input voltage UVLO by using external resistors.

Current Limit

The LV2862 implements current mode control which uses the internal COMP voltage to turn off the high side MOSFET on a cycle by cycle basis. Each cycle the switch current and internal COMP voltage are compared, when the peak switch current intersects the COMP voltage, the high side switch is turned off. During overcurrent conditions that pull the output voltage low, the error amplifier will respond by driving the COMP node high, increasing the switch current. The error amplifier output is clamped internally, which functions as a switch current limit.

Overvoltage Transient Protection

The LV2862 incorporates an overvoltage transient protection (OVTP) circuit to minimize voltage overshoot when recovering from output fault conditions or strong unload transients on power supply designs with low value output capacitance. For example, when the power supply output is overloaded the error amplifier compares the actual output voltage to the internal reference voltage. If the FB pin voltage is lower than the internal reference voltage for a considerable time, the output of the error amplifier will respond by clamping the error amplifier output to a high voltage. Thus, requesting the maximum output current. Once the condition is removed, the regulator output rises and the error amplifier output transitions to the steady state duty cycle. In some applications, the power supply output voltage can respond faster than the error amplifier output can respond, this actuality leads to the possibility of an output overshoot. The OVTP feature minimizes the output overshoot, when using a low value output capacitor, by implementing a circuit to compare the FB pin voltage to OVTP threshold which is 108% of the internal voltage reference. If the FB pin voltage is greater than the OVTP threshold, the high side MOSFET is disabled preventing current from flowing to the output and minimizing output overshoot. When the FB voltage drops lower than the OVTP threshold, the high side MOSFET is allowed to turn on at the next clock cycle.

Thermal Shutdown

The device implements an internal thermal shutdown to protect itself if the junction temperature exceeds 170 ℃(typ). The thermal shutdown forces the device to stop switching when the junction temperature exceeds the thermal trip threshold. Once the junction temperature decreases below 160 ℃(typ), the device reinitiates the power up sequence.

APPLICATION INFORMATION

Design Guide – Step By Step Design Procedure

This example details the design of a high frequency switching regulator using ceramic output capacitors. A few parameters must be known in order to start the design process. These parameters are typically determined at the system level:

Input Voltage, V_{IN}		9V to 16V, Typical 12V
Output Voltage, V_{OUT}		5.0V $\pm$ 3%
Maximum Output Current $I_{O\_max: Example}$		0.6A
Minimum Output Current $I_{O\_min: Example}$		0.03A
Transient Response 0.03A to 0.6A		5%
Output Voltage Ripple		1%
Switching Frequency f_{SW}		2.1MHz
Target during Load Transient	Over Voltage Peak Value	106% of Output Voltage
	Under Voltage Value	91% of Output Voltage

Selecting the Switching Frequency

The first step is to decide on a switching frequency for the regulator. Typically, the user will want to choose the highest switching frequency possible since this will produce the smallest solution size. The high switching frequency allows for lower valued inductors and smaller output capacitors compared to a power supply that switches at a lower frequency. The switching frequency that can be selected is limited by the minimum on-time of the internal power switch, the input voltage and the output voltage and the frequency shift limitation. For this example, the output voltage is 5 V and the maximum input voltage is 16 V, a switching frequency of 2100 kHz is used.
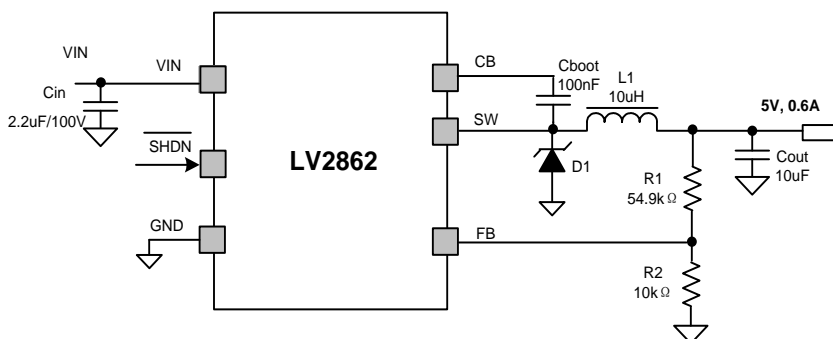
Application Circuit, 5V Output

Output Inductor Selection

The most critical parameters for the inductor are the inductance, peak current and the DC resistance. The inductance is related to the peak-to-peak inductor ripple current, the input and the output voltages. Since the ripple current increases with the input voltage, the maximum input voltage is always used to determine the inductance. To calculate the minimum value of the output inductor, use Equation 1. A reasonable value is setting the ripple current to be 30% of the DC output current. For this design example, the minimum inductor value is calculated to be 9.1 µH, and a nearest standard value was chosen: 10 µH. For the output filter inductor, it is important that the RMS current and saturation current ratings not be exceeded. The RMS and peak inductor current can be found from Equation 3 and Equation 4. The inductor ripple current is 0.16A, and the RMS current is 0.602A. As the equation set demonstrates, lower ripple currents will reduce the output voltage ripple of the regulator but will require a larger value of inductance. A good starting point for most applications is a 10µH with 1A current rating. Using a

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rating near 1A will enable the LV2862 to current limit without saturating the inductor. This is preferable to the LV2862 going into thermal shutdown mode and the possibility of damaging the inductor if the output is shorted to ground or other long-term overload.

$$L_{o\min} = \frac{V_{in\max} - V_{out}}{I_o \times K_{IND}} \times \frac{V_{out}}{V_{in\max} \times f_{sw}} \tag{1}$$

$$I_{ripple} = \frac{V_{out} \times (V_{in\max} - V_{out})}{V_{in\max} \times L_o \times f_{sw}} \tag{2}$$

$$I_{L-RMS} = \sqrt{I_o^2 + \frac{1}{12} I_{ripple}^2} \tag{3}$$

$$I_{L-peak} = I_o + \frac{I_{ripple}}{2} \tag{4}$$

Output Capacitor

The selection of Cout is mainly driven by three primary considerations. The output capacitor will determine the modulator pole, the output voltage ripple, and how the regulator responds to a large change in load current. The output capacitance needs to be selected based on the most stringent of these three criteria.

The desired response to a large change in the load current is the first criteria. The regulator usually needs two or more clock cycles for the control loop to see the change in load current and output voltage and adjust the duty cycle to react to the change. The output capacitance must be large enough to supply the difference in current for 2 clock cycles while only allowing a tolerable amount of droop in the output voltage. Equation 5 shows the minimum output capacitance necessary to accomplish this. For this example, the transient load response is specified as a 3% change in Vout for a load step from 0.03 A to 0.6 A (full load). For this example, ΔIout = 0.6 -0.03 = 0.57 A and ΔVout = 0.03 × 5 = 0.15 V. Using these numbers gives a minimum capacitance of 3.6 μF. For ceramic capacitors, the ESR is usually small enough to ignore in this calculation. Aluminum electrolytic and tantalum capacitors have higher ESR that should be taken into account.

The stored energy in the inductor will produce an output voltage overshoot when the load current rapidly decreases. The output capacitor must also be sized to absorb energy stored in the inductor when transitioning from a high load current to a lower load current. Equation 6 is used to calculate the minimum capacitance to keep the output voltage overshoot to a desired value. Where L is the value of the inductor, I_{OH} is the output current under heavy load, I_{OL} is the output under light load, V_f is the final peak output voltage, and V_i is the initial capacitor voltage. For this example, the worst case load step will be from 0.6 A to 0.03 A. The output voltage will increase during this load transition and the stated maximum in our specification is 3 % of the output voltage. This will make Vo_overshoot = 1.03 × 5 = 5.15V. V_i is the initial capacitor voltage which is the nominal output voltage of 5 V. Using these numbers in Equation 6 yields a minimum capacitance of 2.36 μF.

Equation 7 calculates the minimum output capacitance needed to meet the output voltage ripple specification. Where fsw is the switching frequency, Vo_ripple is the maximum allowable output voltage ripple, and I_{L_ripple} is the inductor ripple current. Equation 7 yields 0.21 μF.

Equation 8 calculates the maximum ESR an output capacitor can have to meet the output voltage ripple specification. Equation 8 indicates the ESR should be less than 277 mΩ.

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Additional capacitance de-ratings for aging, temperature and dc bias should be factored in which will increase this minimum value. For this example, 10 μF ceramic capacitors will be used. Capacitors in the range of 4.7 μF-100 μF are a good starting point with an ESR of 0.1Ω or less.

$$C_{out} > \frac{2 \times \Delta I_{out}}{fsw \times \Delta V_{out}} \tag{5}$$

$$C_{out} > L_O \times \frac{(Ioh^2 - Iol^2)}{(Vf^2 - Vi^2)} \tag{6}$$

$$C_{out} > \frac{1}{8 \times fsw} \times \frac{1}{\frac{V_{o\_ripple}}{I_{L-ripple}}} \tag{7}$$

$$R_{ESR} < \frac{V_{o\_ripple}}{I_{L-ripple}} \tag{8}$$

Schottky Diode

The breakdown voltage rating of the diode is preferred to be 25% higher than the maximum input voltage. The current rating for the diode should be equal to the maximum output current for best reliability in most applications. In cases where the input voltage is much greater than the output voltage the average diode current is lower. In this case it is possible to use a diode with a lower average current rating, approximately $(1-D) \times I_{OUT}$ however the peak current rating should be higher than the maximum load current. A 0.5 to 1A rated diode is a good starting point.

Input Capacitor

A low ESR ceramic capacitor is needed between the V_{IN} pin and ground pin. This capacitor prevents large voltage transients from appearing at the input. Use a 1 μF-10 μF value with X5R or X7R dielectric. Depending on construction, a ceramic capacitor's value can decrease up to 50% of its nominal value when rated voltage is applied. Consult with the capacitor manufactures data sheet for information on capacitor derating over voltage and temperature. The capacitor must also have a ripple current rating greater than the maximum input current ripple of the LV2862. The input ripple current can be calculated using below Equations.

For this example design, a ceramic capacitor with at least a 60V voltage rating is required to support the maximum input voltage. Common standard ceramic capacitor voltage ratings include 4V, 6.3V, 10V, 16V, 25V, 50V or 100V so a 100V capacitor should be selected. For this example design, one 2.2 μF, 100V capacitor is selected. The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using Equation 10. Using the design example values, Ioutmax = 0.6 A, Cin = 2.2 μF, $f$sw = 2100 kHz, yields an input voltage ripple of 32.5 mV and a rms input ripple current of 0.3 A.

$$I_{cirms} = I_{out} \times \sqrt{\frac{V_{out}}{V_{in\,min}} \times \frac{(V_{in\,min} - V_{out})}{V_{in\,min}}} \tag{9}$$

$$\Delta V_{in} = \frac{I_{out\,max} \times 0.25}{C_{in} \times f_{sw}} \tag{10}$$

Bootstrap Capacitor Selection

A 0.1 μF ceramic capacitor or larger is recommended for the bootstrap capacitor (C_{BOOT}). For applications where the input voltage is close to output voltage a larger capacitor is recommended, generally 0.1 μF to 1 μF to ensure plenty of gate drive for

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the internal switches and a consistently low R_{DSON}. A ceramic capacitor with an X7R or X5R grade dielectric with a voltage rating of 10V or higher is recommended because of the stable characteristics over temperature and voltage.

Other Typical Application Circuits
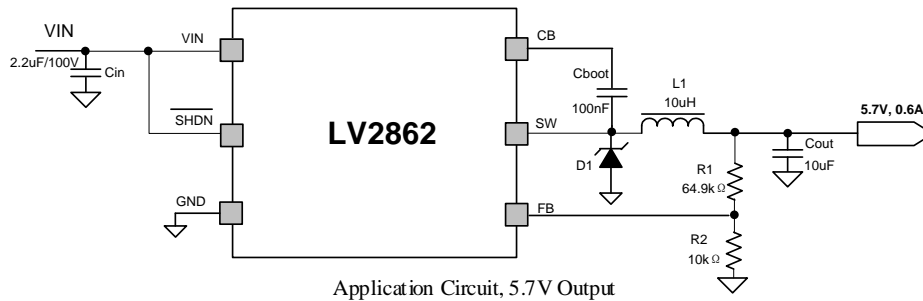

Application Circuit, 5.7V Output
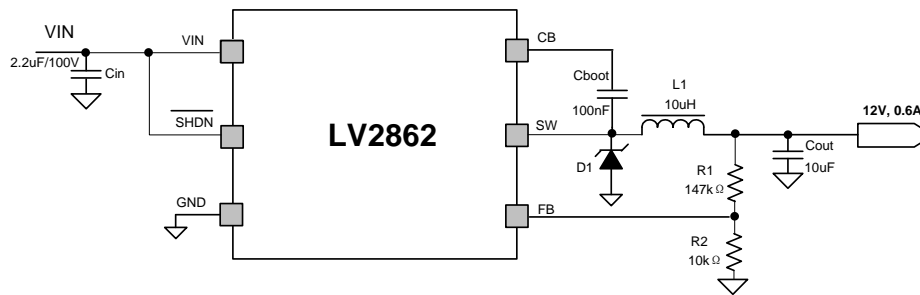
Application Circuit, 12V Output

Below are the recommended typical output voltage inductor/capacitor combinations for optimized total solution size.

P/N	Vout(V)	R1(kΩ)	R2(kΩ)	L(μH)	Cout(μF)
LV2862 Y	5	54.9(1%)	10(1%)	3.3	10
LV2862 Y	5.7	64.9(1%)	10(1%)	3.3	10
LV2862 Y	12	147(1%)	10(1%)	3.3	10

Layout Considerations

To reduce problems with conducted noise pick up the ground side of feedback network should be connected directly to the GND pin with its own connection. The feedback network, resistors R1 and R2, should be kept close to the FB pin, and away from the inductor to minimize coupling noise into the feedback pin. The input bypass capacitor C_{IN} must be placed close to the V_{IN} pin. This will reduce copper trace resistance which effects input voltage ripple of the IC. The inductor L1 should be placed close to the SW pin to reduce magnetic and electrostatic noise. The output capacitor, C_{OUT} should be placed close to the junction of L1 and the diode D1. The L1, D1, and C_{OUT} trace should be as short as possible to reduce conducted and radiated noise and increase overall efficiency. The ground connection for the diode, C_{IN}, and C_{OUT} should be as small as possible and tied to the system ground plane in only one spot (preferably at the C_{OUT} ground point) to minimize conducted noise in the system ground plane. For more detail on switching power supply layout considerations see Application Note AN-1149.

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Mechanical Package Outline for TSOT-23

Physical Dimensions inches (millimeters) unless otherwise noted
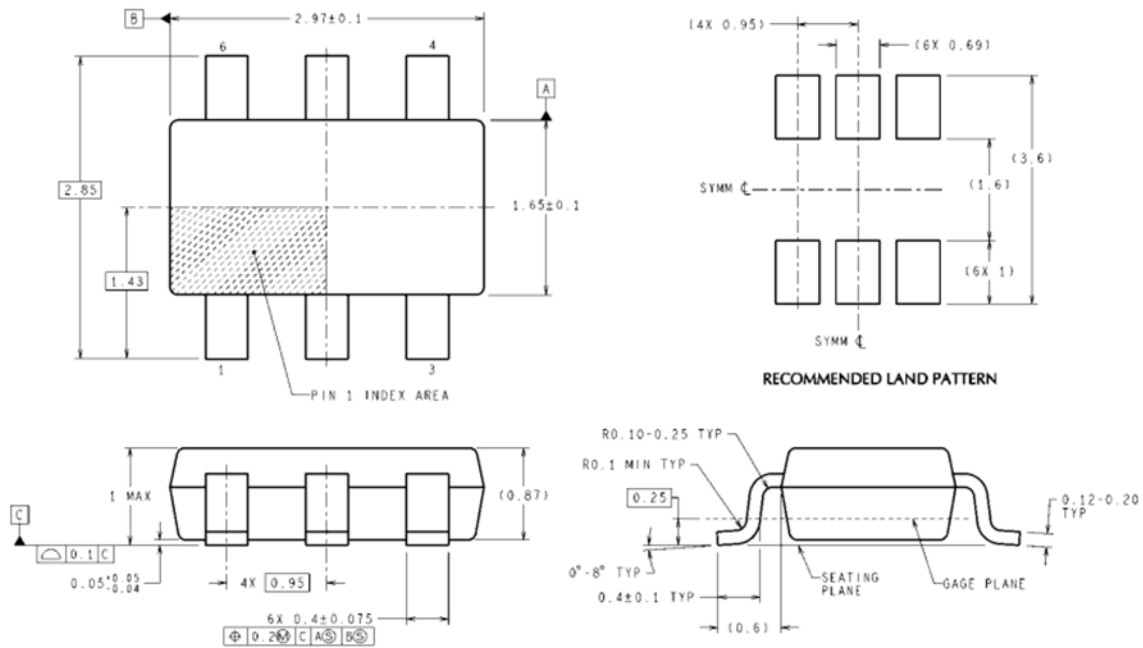
DIMENSIONS ARE IN MILLIMETERS

TSOT 6 Pin Package (MK)
For Ordering, Refer to Ordering Information Table
NS Package Number MK06A

MK06A (Rev E)