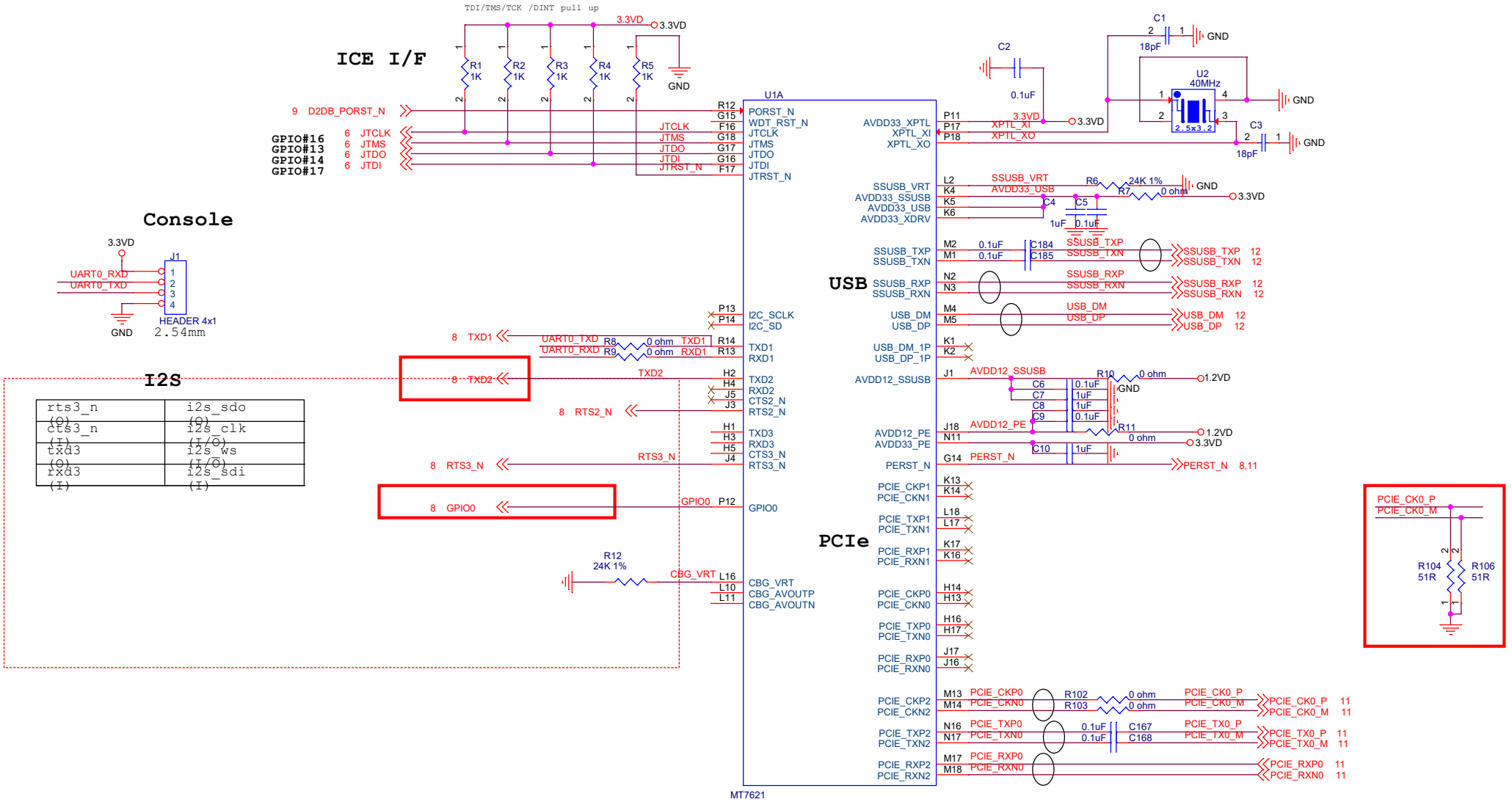
TDI/TMS/TCK /DINT pull up
ICE I/F
3.3VD
R1 1K
R2 1K
R3 1K
R4 1K
R5 1K
GND
9 D2DB_PORST_N
GPIO#16 6 JTCLK
GPIO#13 6 JTMS
GPIO#14 6 JTDO
GPIO#17 6 JTDI
U1A
R12 PORST_N
G15 WDT_RST_N
F16 JTCLK
G18 JTMS
G17 JTDO
G16 JTDI
F17 JTRST_N
C1 18pF
C2 0.1uF
U2 40MHz 2.5x3.2
C3 18pF
P11 AVDD33_XPTL
P17 XPTL_XI
P18 XPTL_XO
Console
J1
UART0_RXD
UART0_TXD
HEADER 4x1
2.54mm
L2 SSUSB_VRT
K4 AVDD33_USB
K5 AVDD33_SSUSB
K6 AVDD33_USB
AVDD33_XDRV
R6 24K 1%
R7 0 ohm
C4
C5 1uF
0.1uF
USB
M2 SSUSB_TXP
M1 SSUSB_TXN
C184 0.1uF
C185 0.1uF
N2 SSUSB_RXP
N3 SSUSB_RXN
M4 USB_DM
M5 USB_DP
K1 USB_DM_1P
K2 USB_DP_1P
J1 AVDD12_SSUSB
C6 0.1uF
C7 1uF
C8 1uF
C9 0.1uF
R10 0 ohm
1.2VD
J18 AVDD12_PE
N11 AVDD12_PE
R11 0 ohm
C10 1uF
G14 PERST_N
PERST_N 8,11
P13 I2C_SCLK
P14 I2C_SD
8 TXD1
UART0_TXD R8 0 ohm TXD1 R14
UART0_RXD R9 0 ohm RXD1 R13
TXD1
RXD1
8 TXD2
TXD2 H2
H4 RXD2
J5 CTS2_N
J3 RTS2_N
8 RTS2_N
H1 TXD3
H3 RXD3
H5 CTS3_N
J4 RTS3_N
8 RTS3_N
I2S
rts3_n (O)
cts3_n (I)
txd3 (O)
rxd3 (I)
i2s_sdo (O)
i2s_clk (I/O)
i2s_ws (I/O)
i2s_sdi (I)
8 GPIO0
GPIO0_P12
GPIO0
R12 24K 1%
CBG_VRT L16
L10 CBG_AVOUTP
L11 CBG_AVOUTN
PCIe
K13 PCIE_CKP1
K14 PCIE_CKN1
L18 PCIE_TXP1
L17 PCIE_TXN1
K17 PCIE_RXP1
K16 PCIE_RXN1
H14 PCIE_CKP0
H13 PCIE_CKN0
H16 PCIE_TXP0
H17 PCIE_TXN0
J17 PCIE_RXP0
J16 PCIE_RXN0
M13 PCIE_CKP0
M14 PCIE_CKN0
R102 0 ohm
R103 0 ohm
PCIE_CK0_P
PCIE_CK0_M
PCIE_CKP2
PCIE_CKN2
N16 PCIE_TXP0
N17 PCIE_TXN0
C167 0.1uF
C168 0.1uF
PCIE_TX0_P
PCIE_TX0_M
PCIE_TXP2
PCIE_TXN2
M17 PCIE_RXP0
M18 PCIE_RXN0
PCIE_RXP2
PCIE_RXN2
PCIE_RXP0 11
PCIE_RXN0 11
MT7621
PCIE_CK0_P
PCIE_CK0_M
R104 51R
R106 51R
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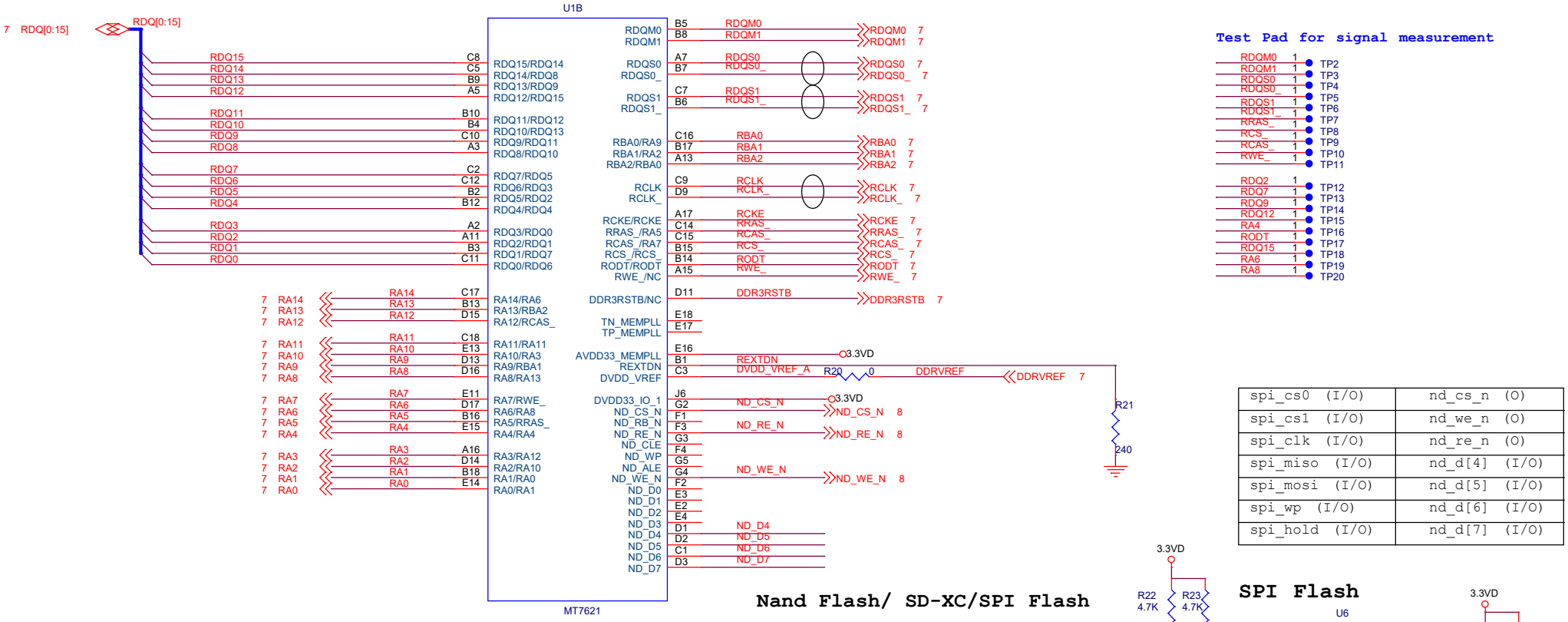
DDR3/DDR2 Interface
The pinout is differenet
when use DDR3 and DDR2

diff pair



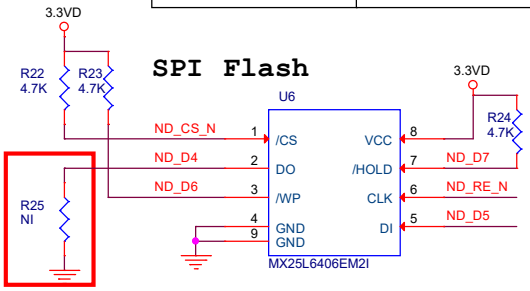
Test Pad for signal measurement

spi_cs0 (I/O)	nd_cs_n (O)
spi_cs1 (I/O)	nd_we_n (O)
spi_clk (I/O)	nd_re_n (O)
spi_miso (I/O)	nd_d[4] (I/O)
spi_mosi (I/O)	nd_d[5] (I/O)
spi_wp (I/O)	nd_d[6] (I/O)
spi_hold (I/O)	nd_d[7] (I/O)

Nand Flash/ SD-XC/SPI Flash

sd_wp (I)	nd_wp (O)
sd_clk (I/O)	nd_rb_n (I)
sd_cd (I)	nd_cle (O)
sd_cmd (I/O)	nd_ale (O)
sd_data[0] (I/O)	nd_d[0] (I/O)
sd_data[1] (I/O)	nd_d[1] (I/O)
sd_data[2] (I/O)	nd_d[2] (I/O)
sd_data[3] (I/O)	nd_d[3] (I/O)

SPI Flash



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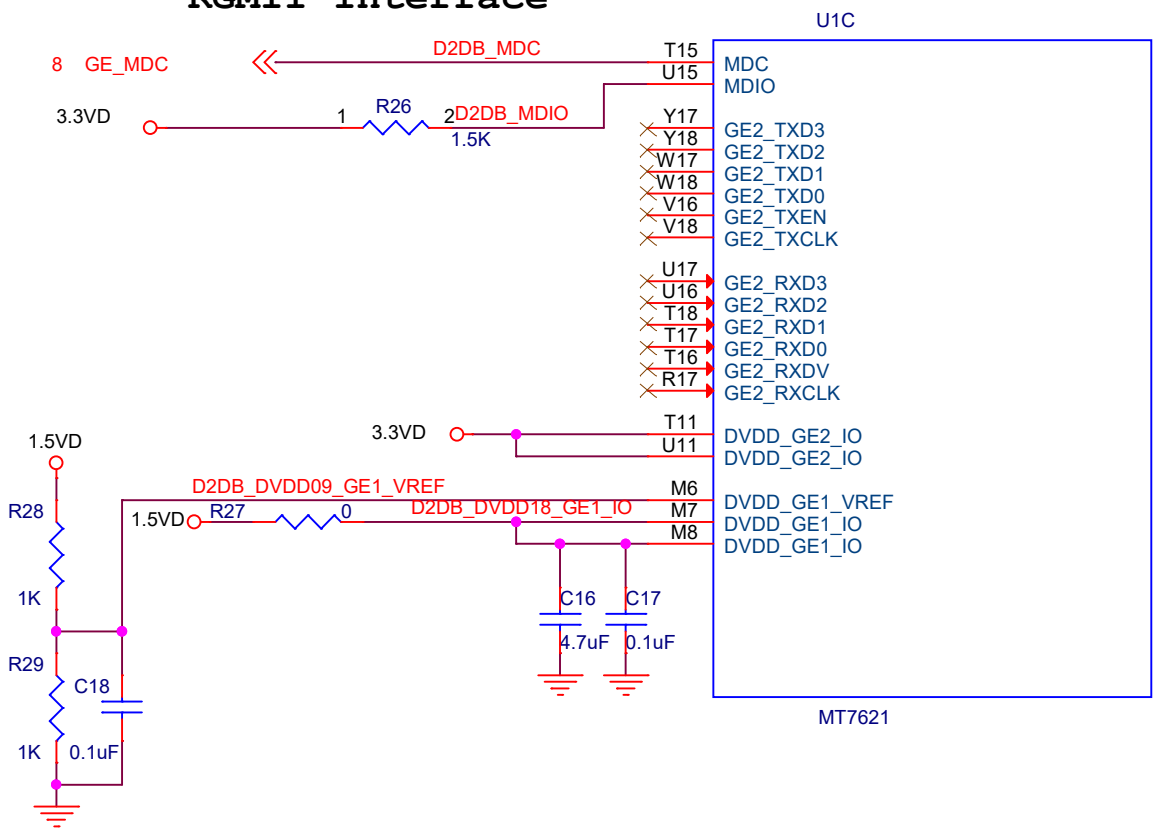
RGMII Interface



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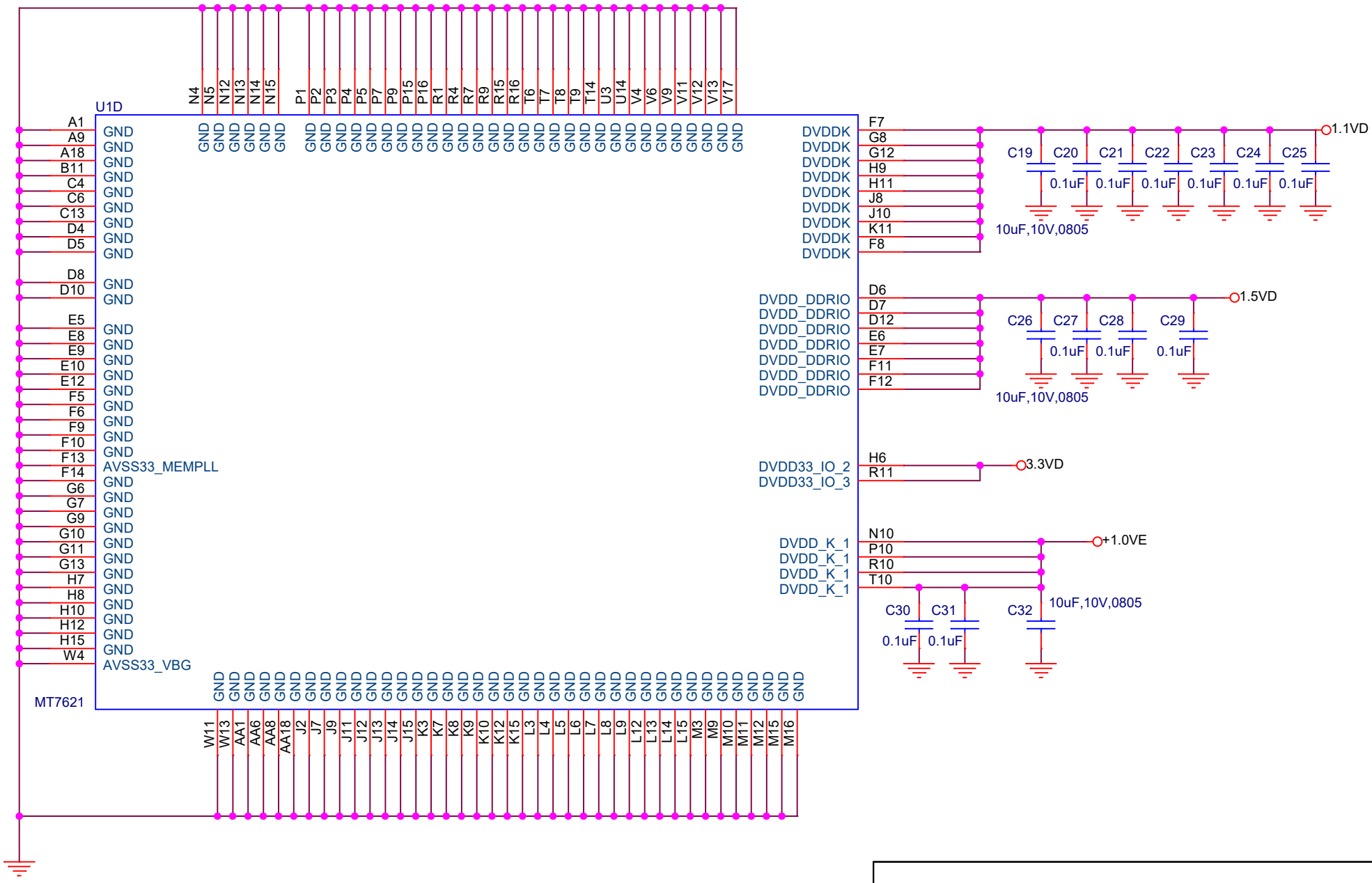
MT7621 Power



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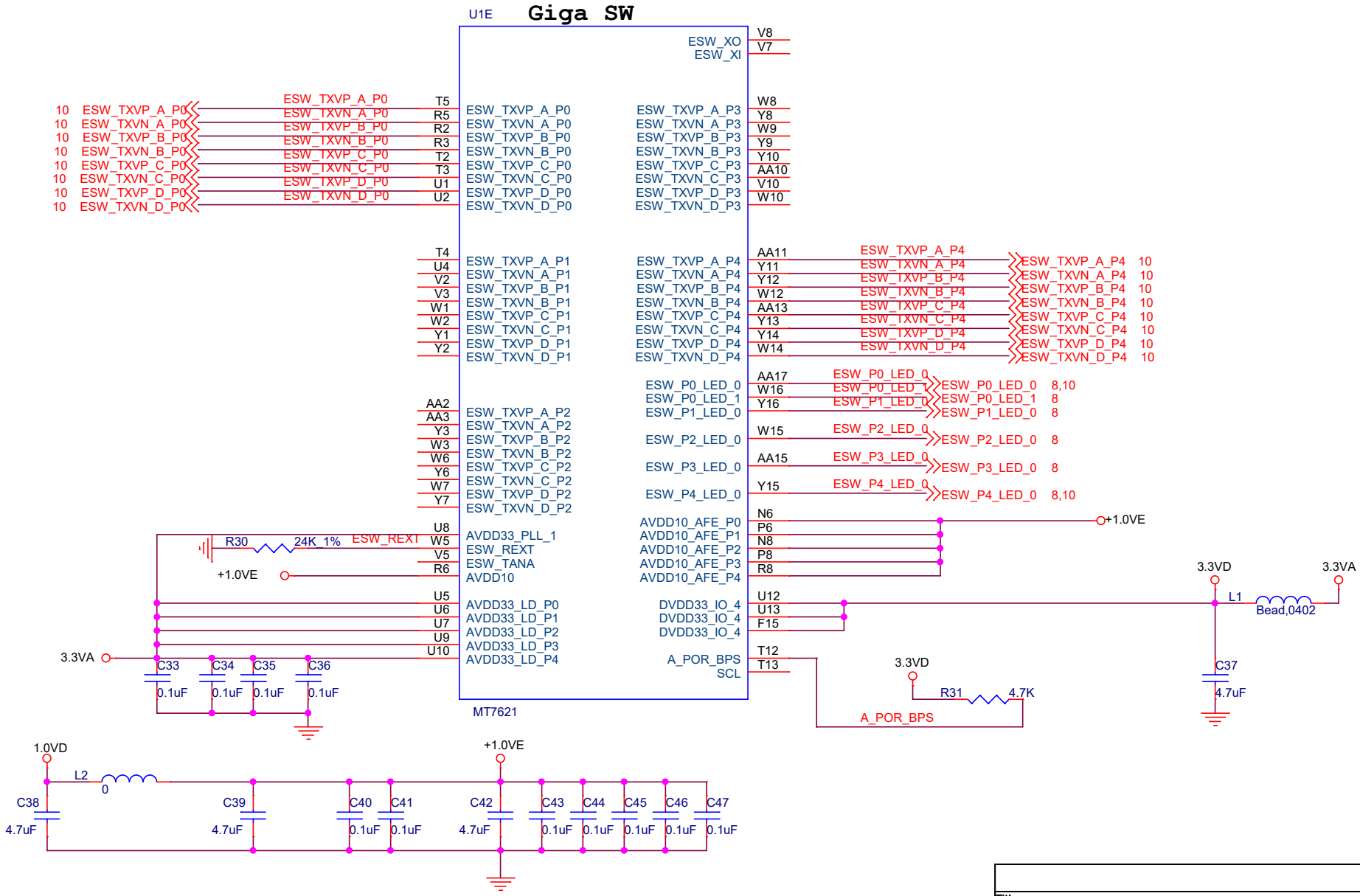

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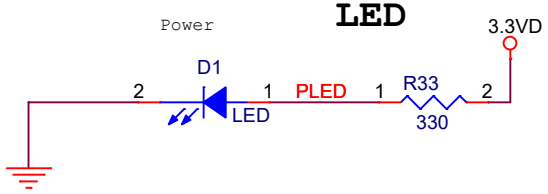
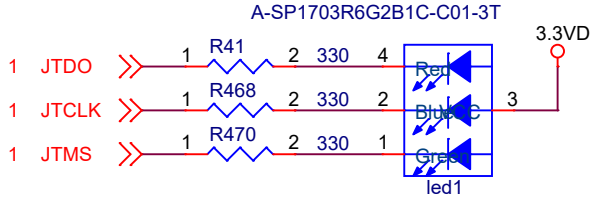
LED





RESET switch

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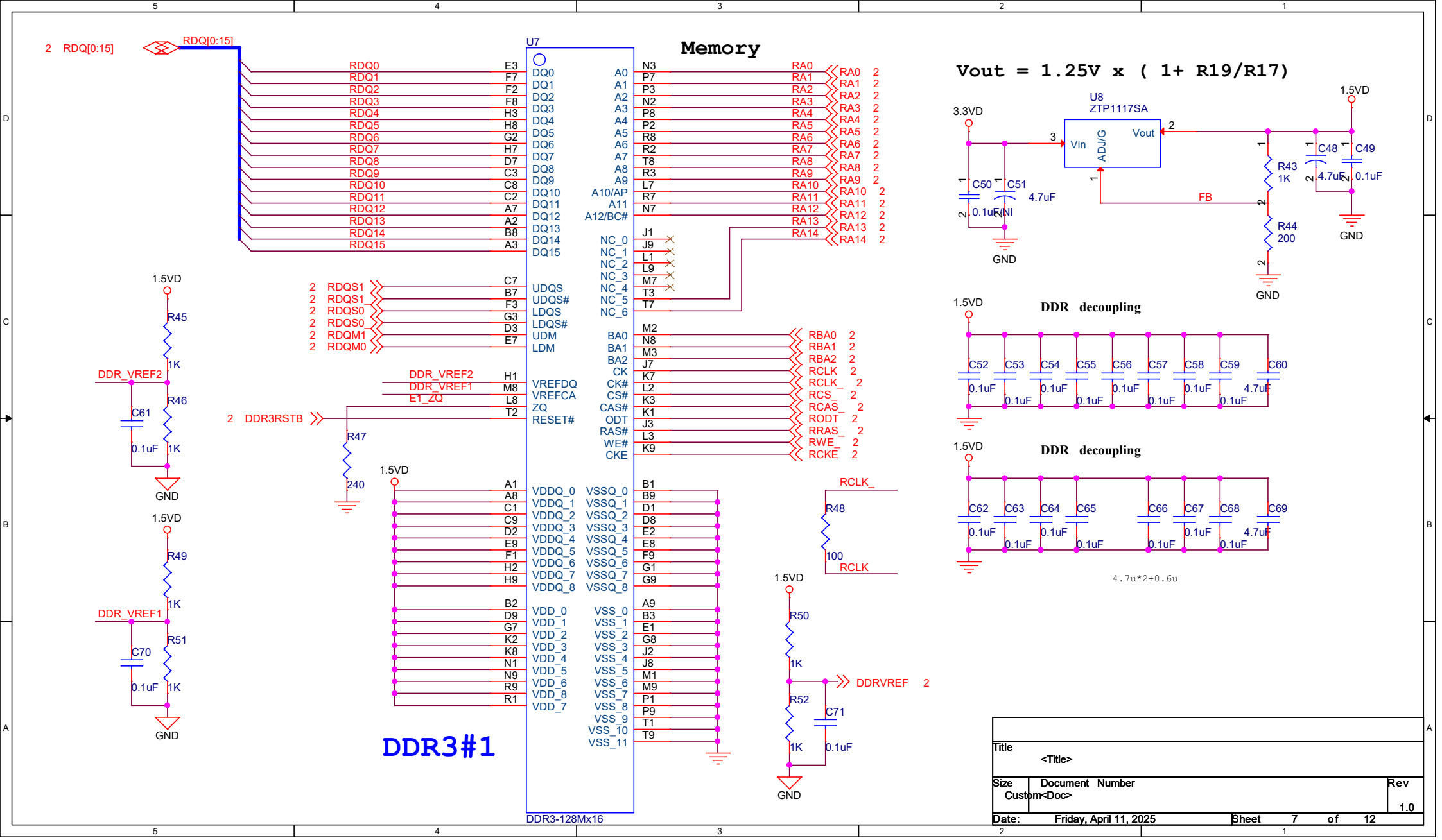

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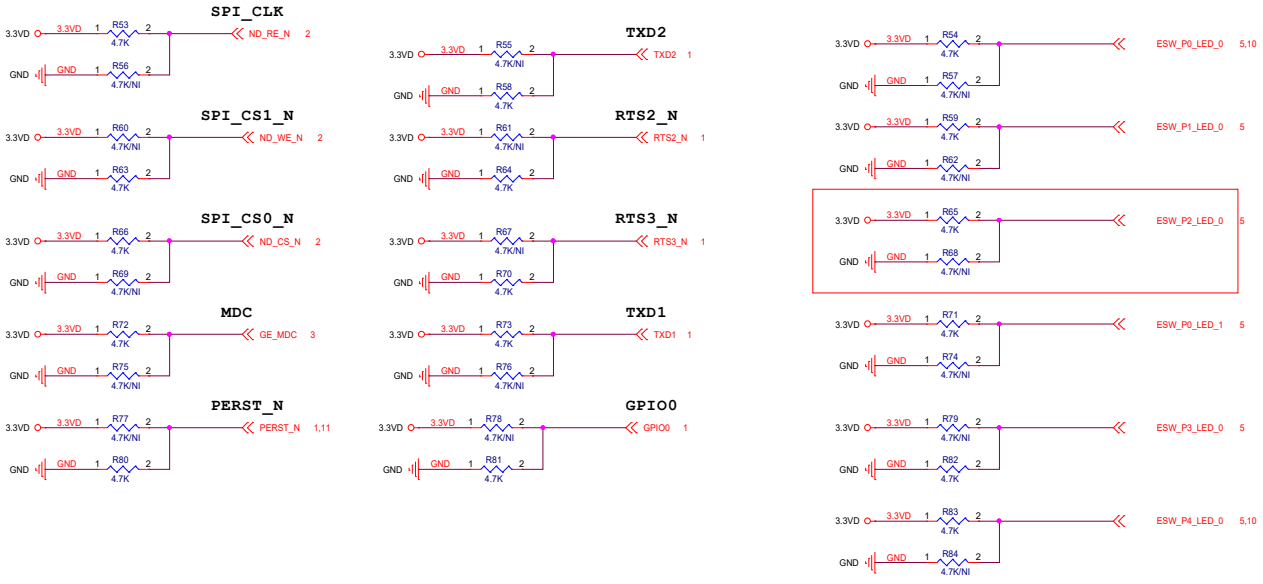
Boot Strapping

Pin Name	Description	Value	
SPI_CLK	DRAM_FROM_EE	For non scan mode: 0: DRAM/PLL configuration from EEPROM **1: DRAM configuration from Auto Detect**	For FT mode: 0: SUTIF 1: 3-wire SPI
{SPI_CS1_N, SPI_CS0_N, MDC }	XTAL_MODE	000: 20 MHz, Self Oscillation mode 001: 20 MHz, Single end input 010: 20 MHz, differential input **011: 40 MHz, Self Oscillation mode**	100: 40 MHz, Single end input 101: 40 MHz, differential input 110: 25 MHz, Self Oscillation mode 111: 25 MHz, Single end input
PERST_N	OCP_RATIO	**0: 1:3** 1: 1:4	
TXD2	DRAM_TYPE	**0: DDR3** 1: DDR2	
{RTS2_N, RTS3_N, TXD1, GPIO0}	CHIP_MODE[3:0]	0000: Normal / Boot from SPI 4-byte address and XTAL clock 0001: Normal / Boot from ROM (NAND page 2k+64 bytes) **0010: Normal / Boot from SPI 3-byte address** 0011: Normal / Boot from SPI 4-byte address 0100: iNIC RGMI / Boot from ROM 0101: iNIC MII / Boot from ROM 0110: iNIC RVMII / Boot from ROM 0111: iNIC PHY / Boot from ROM 1000: iNIC RGMII / Boot from ROM and XTAL clock 1001: Normal / Boot from internal SRAM 1010: Normal / Boot from ROM (NAND page 2k+128 bytes) 1011: Normal / Boot from ROM (NAND page 4k+128 bytes) 1100: Normal / Boot from ROM (NAND page 4k+224 bytes) 1101: Debug mode 1110: Scan mode 1111: Final Test	

Giga Switch Hardware Trap

Pin Name	Trap	Fuction	Description	Default
P0_LED_0	HWTRAP[0]	HT_CHIP_MODE[0]	chip_mode[3:0] 4'b0000: IDDQ mode 4'b0001: IOTEST mode 4'b0010: NANDTREE mode 4'b0011: RING mode (both IO and std-cell) 4'b0100: MBIST 4'b0101: SCAN mode (internal) 4'b0110: SCAN-COMP mode (compression) 4'b0111: SCAN-MBIST-OLT mode 4'b1000: AFE-OLT mode 4'b1001: GPHY ATE mode 4'b1010: GPHY ADUMP mode 4'b1011: GPHY ADUMP probe mode 4'b1100: Reserved 4'b1101: Reserved 4'b1110: bootup probe mode 4'b1111: normal mode	4'b1111
P1_LED_0	HWTRAP[1]	HT_CHIP_MODE[1]		
P2_LED_0	HWTRAP[2]	HT_CHIP_MODE[2]		
P0_LED_1	HWTRAP[3]	HT_CHIP_MODE[3]		
P3_LED_0	HWTRAP[9]	HT_XTAL_FSEL[0]	External Crystal Frequency Selection xtal_freq_sel[1:0] 2'b01: 20MHz 2'b10: 40MHz 2'b11: 25MHz	2'b10
P4_LED_0	HWTRAP[10]	HT_XTAL_FSEL[1]		



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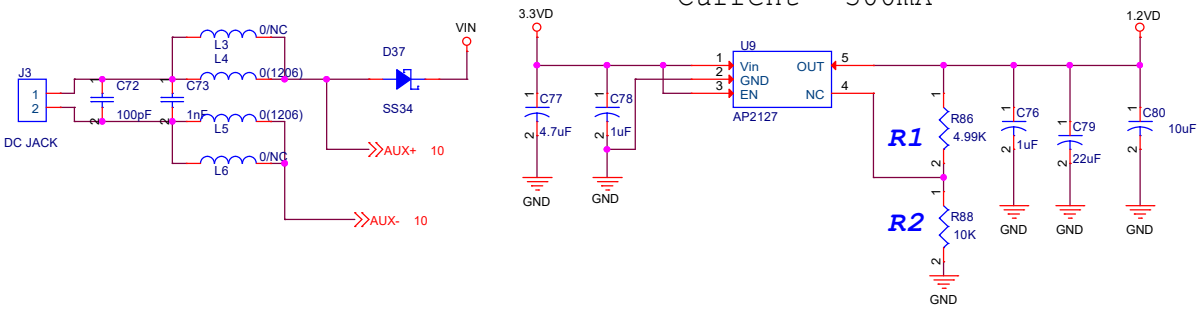
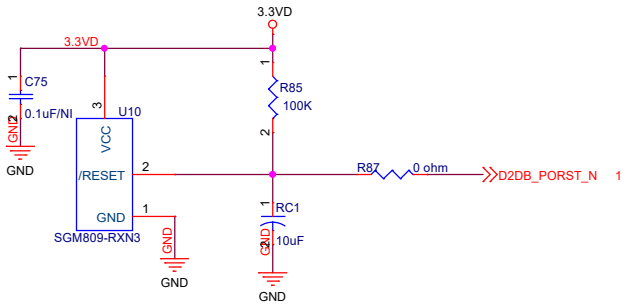
System Power

For USB/PCIe PHY Power (1.2V)

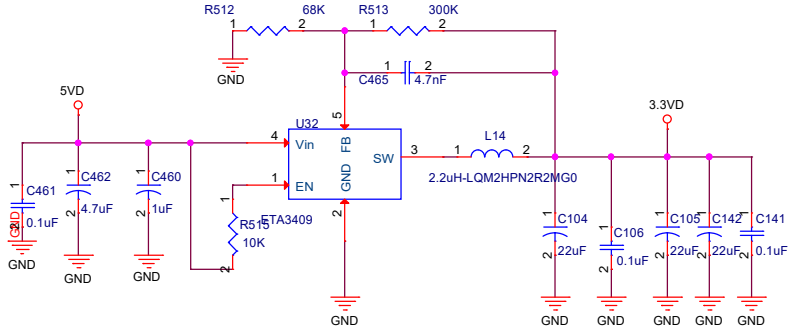
Current= 300mA

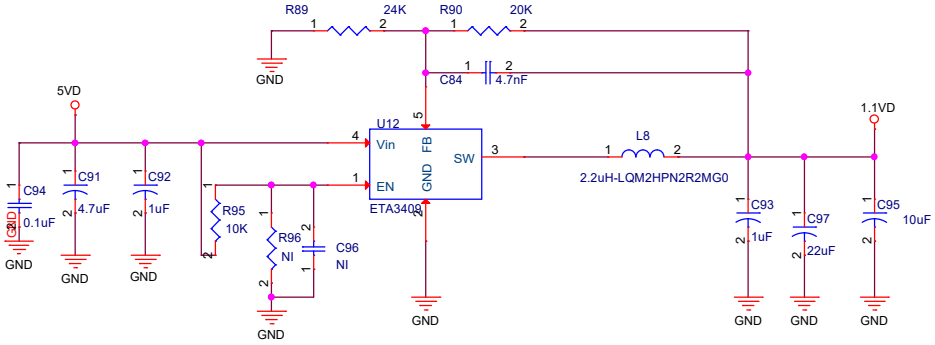


Reset Circuit

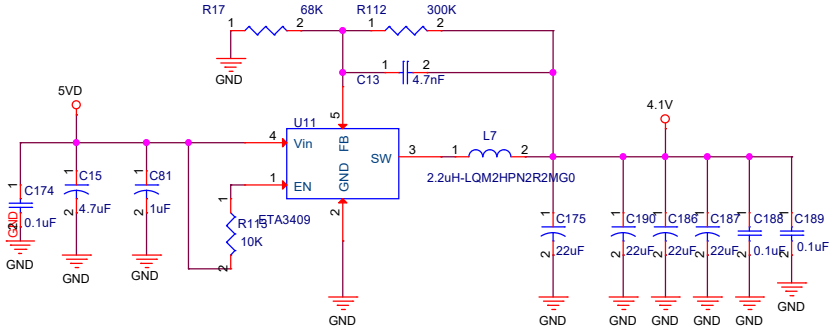


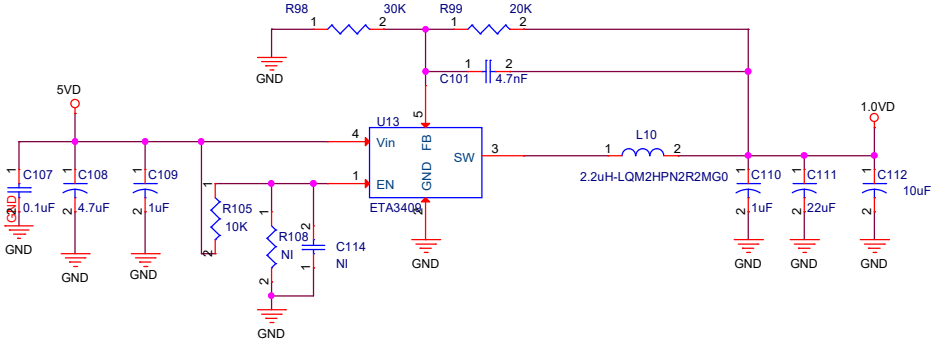
1.1V/1.5A

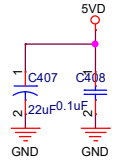




1.0V/1.5A







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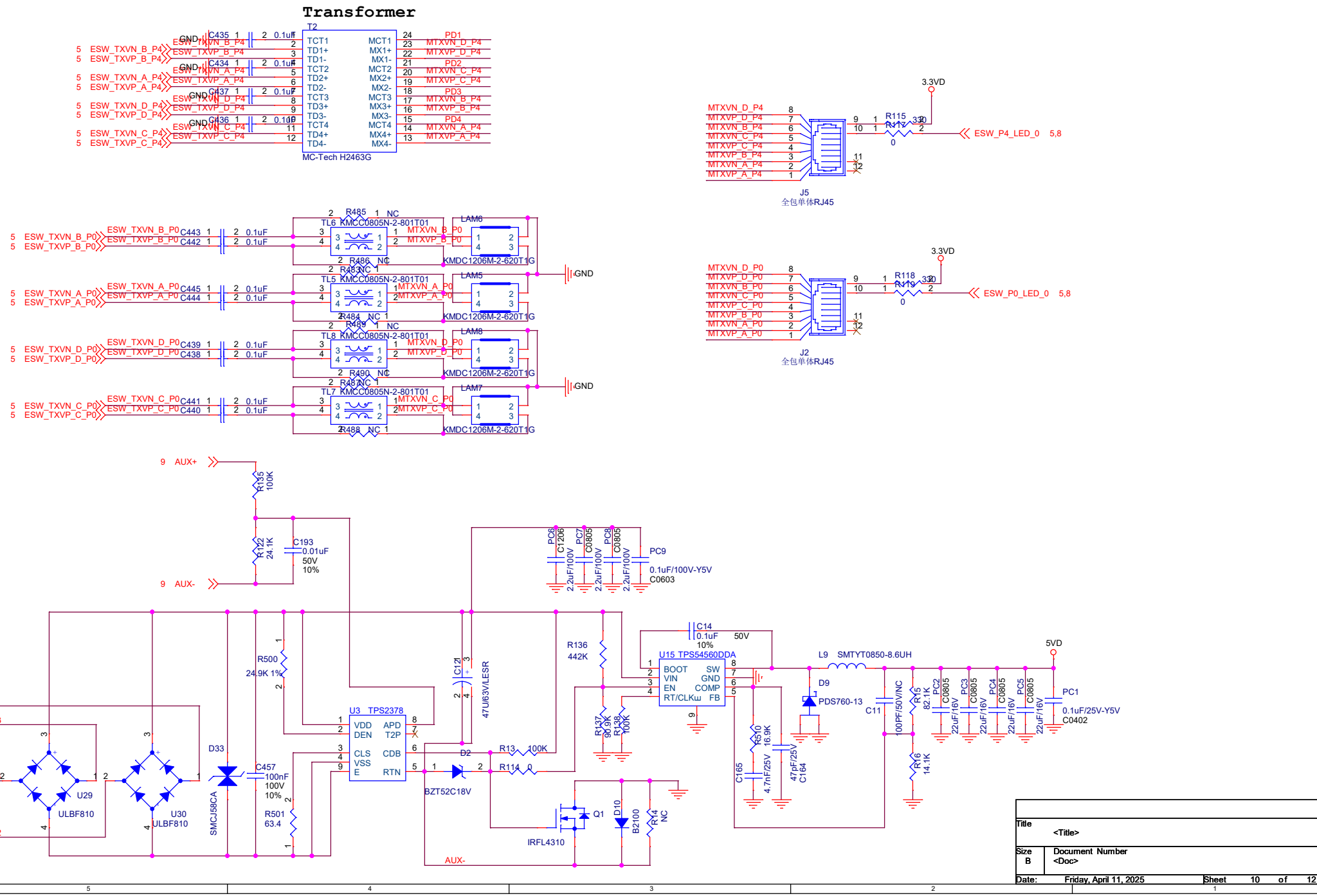
Transformer
T2
MC-Tech H2463G
J5
全包单体RJ45
J2
全包单体RJ45
TL6 KMCC0805N-2-801T01
TL5 KMCC0805N-2-801T01
TL8 KMCC0805N-2-801T01
TL7 KMCC0805N-2-801T01
KMDC1206M-2-620T1G
U3 TPS2378
U15 TPS54560DDA
U29 ULBF810
U30 ULBF810
SMCJ58CA
BZT52C18V
IRFL4310
B2100
PDS760-13
SMTYT0850-8.6UH
47U63VLESR
3.3VD
5VD
AUX+
AUX-
GND
ESW_P4_LED_0 5,8
ESW_P0_LED_0 5,8
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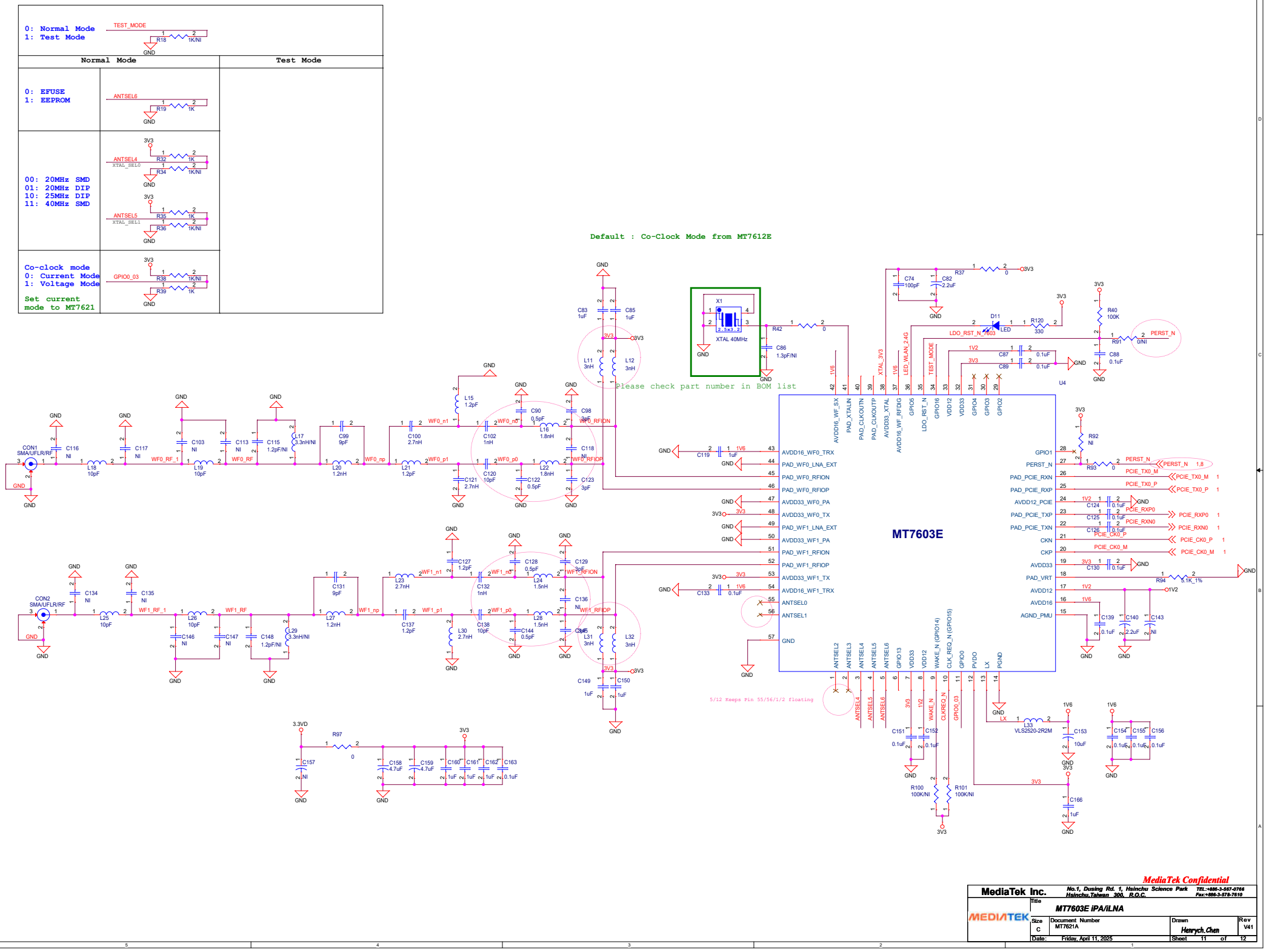
0: Normal Mode
1: Test Mode
TEST_MODE
R18 1K/NI
Normal Mode
Test Mode
0: EFUSE
1: EEPROM
ANTSEL6
R19 1K
00: 20MHz SMD
01: 20MHz DIP
10: 25MHz DIP
11: 40MHz SMD
ANTSEL4
XTAL_SEL0
R32 1K
R34 1K/NI
ANTSEL5
XTAL_SEL1
R35 1K
R36 1K/NI
Co-clock mode
0: Current Mode
1: Voltage Mode
Set current mode to MT7621
GPIO0_03
R38 1K/NI
R39 1K
Default : Co-Clock Mode from MT7612E
Please check part number in BOM list
X1
XTAL 40MHz
R42
C86 1.3pF/NI
MT7603E
AVDD16_WF0_TRX
PAD_WF0_LNA_EXT
PAD_WF0_RFION
PAD_WF0_RFIOP
AVDD33_WF0_PA
AVDD33_WF0_TX
PAD_WF1_LNA_EXT
AVDD33_WF1_PA
PAD_WF1_RFION
PAD_WF1_RFIOP
AVDD33_WF1_TX
AVDD16_WF1_TRX
ANTSEL0
ANTSEL1
5/12 Keeps Pin 55/56/1/2 floating
GPIO1
PERST_N
PAD_PCIE_RXN
PAD_PCIE_RXP
AVDD12_PCIE
PAD_PCIE_TXP
PAD_PCIE_TXN
CKN
CKP
AVDD33
PAD_VRT
AVDD12
AVDD16
AGND_PMU
PCIE_TX0_M
PCIE_TX0_P
PCIE_RXP0
PCIE_RXN0
PCIE_CK0_P
PCIE_CK0_M
R94 5.1K_1%
LDO_RST_N_1603
LED_WLAN_2.4G
TEST_MODE
R40 100K
R91 0/NI
D11 LED
R120 330
U4
R92 NI
R93 0
C74 100pF
C82 2.2uF
R37 0
C87 0.1uF
C88 0.1uF
C89 0.1uF
C124 0.1uF
C125 0.1uF
C126 0.1uF
C130 0.1uF
C139 0.1uF
C140 2.2uF
C143 NI
C151 0.1uF
C152 0.1uF
C153 10uF
C154 0.1uF
C155 0.1uF
C156 0.1uF
C166 1uF
R100 100K/NI
R101 100K/NI
L33 VLS2520-2R2M
CON1 SMA/UFLR/RF
CON2 SMA/UFLR/RF
WF0_RF_1
WF0_RF
WF0_np
WF0_n1
WF0_n0
WF0_p1
WF0_p0
WF0_RFION
WF0_RFIOP
WF1_RF_1
WF1_RF
WF1_np
WF1_n1
WF1_n0
WF1_p1
WF1_p0
WF1_RFION
WF1_RFIOP
C116 NI
C117 NI
C103 NI
C113 NI
C115 1.2pF/NI
C134 NI
C135 NI
C146 NI
C147 NI
C148 1.2pF/NI
C118 NI
C136 NI
C145 NI
L18 10pF
L19 10pF
L20 1.2nH
L21 1.2pF
L25 10pF
L26 10pF
L27 1.2nH
L29 3.3nH/NI
L17 3.3nH/NI
C99 9pF
C100 2.7nH
C102 1nH
C120 10pF
C121 2.7nH
C122 0.5pF
C123 3pF
C131 9pF
C132 1nH
C137 1.2pF
C138 10pF
C144 0.5pF
C149 1uF
C150 1uF
L15 1.2pF
L16 1.8nH
L22 1.8nH
L23 2.7nH
L24 1.5nH
L28 1.5nH
L30 2.7nH
L31 3nH
L32 3nH
L11 3nH
L12 3nH
C83 1uF
C85 1uF
C90 0.5pF
C98 3pF
C127 1.2pF
C128 0.5pF
C129 3pF
C119 1uF
C133 0.1uF
R97 0
C157 NI
C158 4.7uF
C159 4.7uF
C160 1uF
C161 1uF
C162 1uF
C163 0.1uF
3.3VD
3V3
1V6
1V2
GND
MediaTek Confidential
MediaTek Inc.
No.1, Dusing Rd. 1, Hsinchu Science Park, Hsinchu, Taiwan 300, R.O.C.
TEL:+886-3-567-0766
Fax:+886-3-578-7610
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Size C
Document Number MT7621A
Drawn Henrych.Chen
Rev V41
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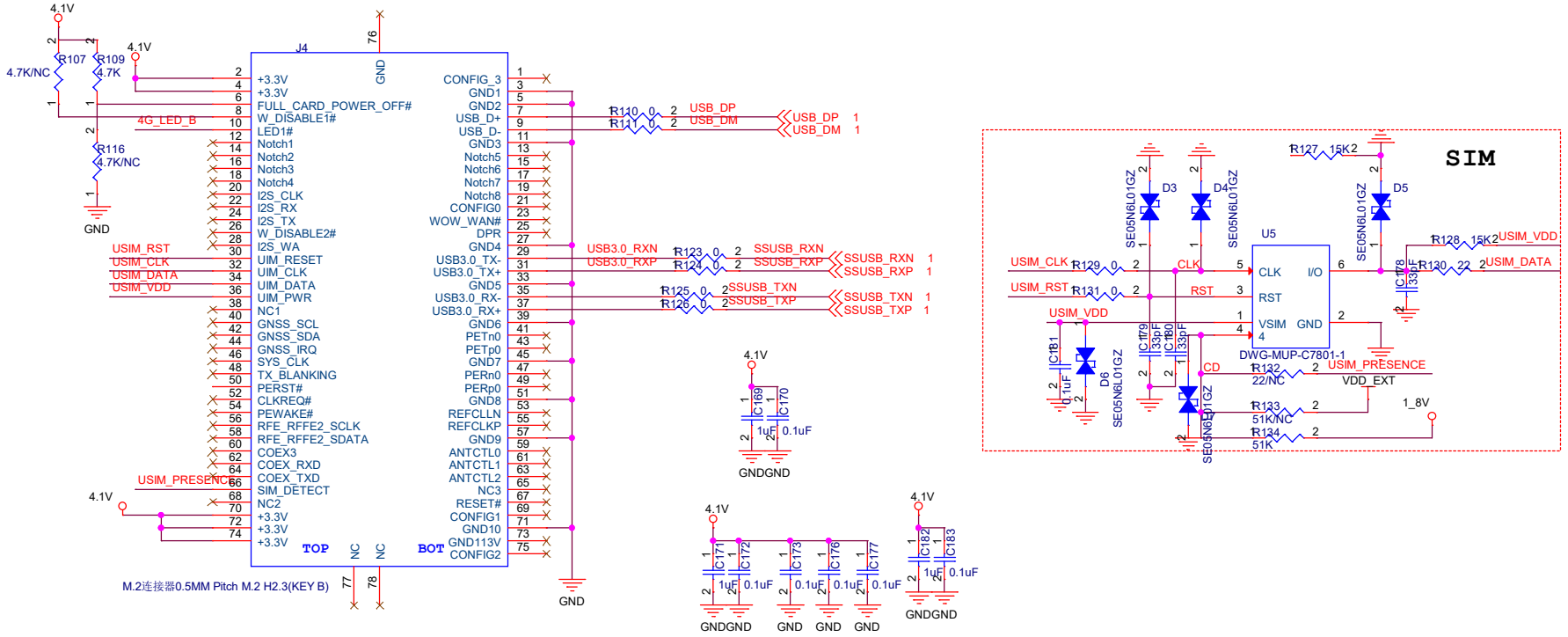

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