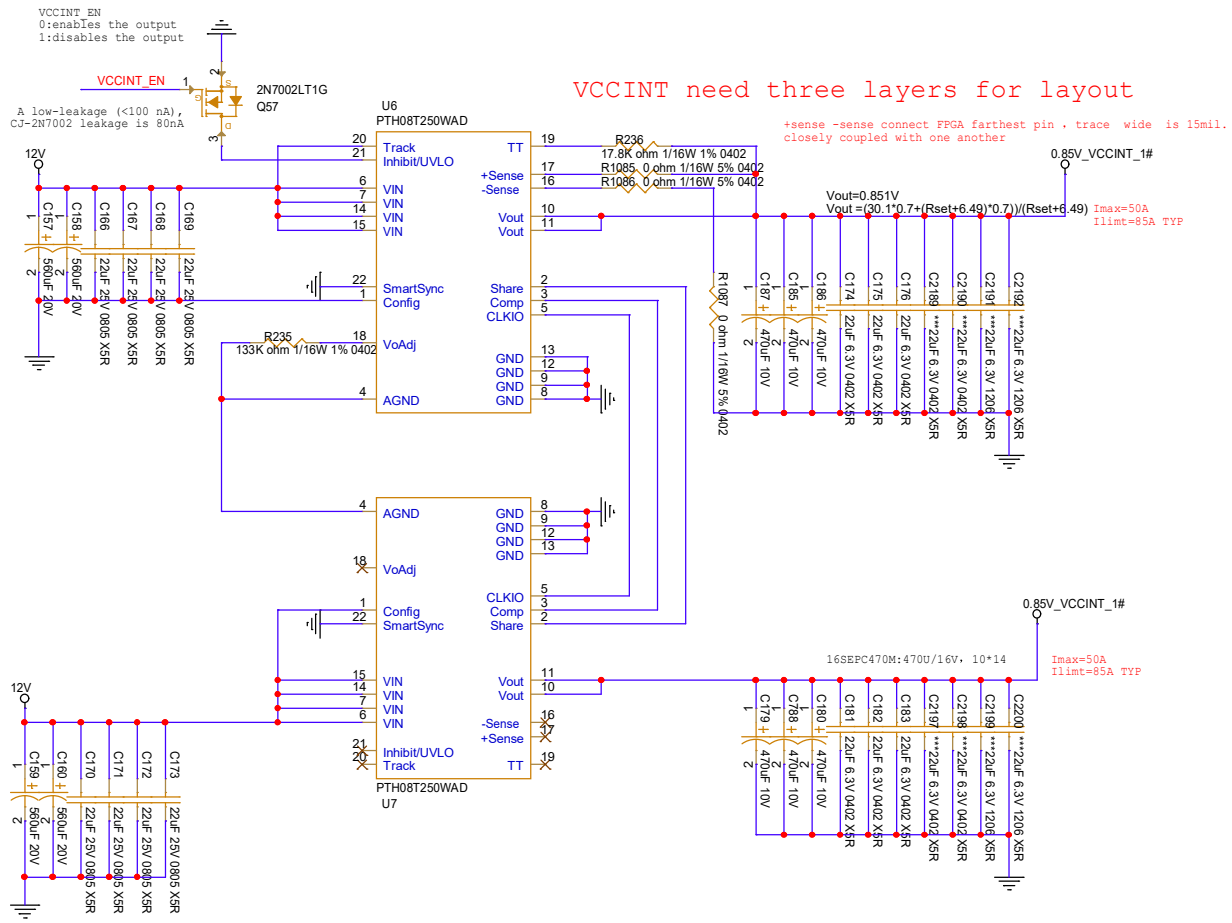
VCCINT_EN
0:enabIes the output
1:disables the output
VCCINT_EN
2N7002LT1G
Q57
A low-leakage (<100 nA),
CJ-2N7002 leakage is 80nA
VCCINT need three layers for layout
+sense -sense connect FPGA farthest pin , trace wide is 15mil.
closely coupled with one another
U6
PTH08T250WAD
12V
Track
Inhibit/UVLO
VIN
VIN
VIN
VIN
SmartSync
Config
VoAdj
AGND
TT
+Sense
-Sense
Vout
Vout
Share
Comp
CLKIO
GND
GND
GND
GND
R236
17.8K ohm 1/16W 1% 0402
R1085 0 ohm 1/16W 5% 0402
R1086 0 ohm 1/16W 5% 0402
R235
133K ohm 1/16W 1% 0402
R1087 0 ohm 1/16W 5% 0402
Vout=0.851V
Vout =(30.1*0.7+(Rset+6.49)*0.7)/(Rset+6.49)
0.85V_VCCINT_1#
Imax=50A
Ilimt=85A TYP
C157 560uF 20V
C158 560uF 20V
C166 22uF 25V 0805 X5R
C167 22uF 25V 0805 X5R
C168 22uF 25V 0805 X5R
C169 22uF 25V 0805 X5R
C187 470uF 10V
C185 470uF 10V
C186 470uF 10V
C174 22uF 6.3V 0402 X5R
C175 22uF 6.3V 0402 X5R
C176 22uF 6.3V 0402 X5R
C2189 **22uF 6.3V 0402 X5R
C2190 **22uF 6.3V 0402 X5R
C2191 **22uF 6.3V 1206 X5R
C2192 **22uF 6.3V 1206 X5R
AGND
VoAdj
Config
SmartSync
CLKIO
Comp
Share
-Sense
+Sense
Inhibit/UVLO
Track
PTH08T250WAD
U7
16SEPC470M:470U/16V, 10*14
C159 560uF 20V
C160 560uF 20V
C170 22uF 25V 0805 X5R
C171 22uF 25V 0805 X5R
C172 22uF 25V 0805 X5R
C173 22uF 25V 0805 X5R
C179 470uF 10V
C788 470uF 10V
C180 470uF 10V
C181 22uF 6.3V 0402 X5R
C182 22uF 6.3V 0402 X5R
C183 22uF 6.3V 0402 X5R
C2197 **22uF 6.3V 0402 X5R
C2198 **22uF 6.3V 0402 X5R
C2199 **22uF 6.3V 1206 X5R
C2200 **22uF 6.3V 1206 X5R