Single Cell Battery Fuel Gauge with Integrated Protector

FEATURES

- Highly Integrated Battery Fuel Gauge and Protector for 1-Series Li-Ion Applications
- Fully Integrated 262.144 kHz Low frequency Oscillator
- Fully Integrated 50.33 MHz High Frequency Oscillator
- Integrated High Side NMOS Protection FET Drive
  - Integrated Charge Pump
  - CHG/DSG FET drivers
  - Linear Charge Control
  - Minimum System Voltage Regulation
- 32-bit RISC ARM Cortex-M0+ CPU
  - Single-cycle 32-bit multiplier
  - 24-bit SysTick timer
  - Nested Vector Interrupt Controller (NVIC)
  - 2-wire serial debug (SWD)
  - 192Kbytes of Flash memory with ECC
  - 24Kbytes of RAM
  - 32Kbytes of ROM
- Host Communication Support
  - I2C (100 and 400kHz)
- High Accuracy Analog Front End with Three Independent ADC's
  - 18 bit High Resolution Delta-Sigma ADC for continuous current measurement
  - 16 bit High Resolution Delta-Sigma ADC for voltage/temperature measurement
  - 16 (including sign) bit High Resolution Delta-Sigma ADC for high frequency current sample measurement
  - Synchronous Measurement of Voltage/Current
- Programmable Current Protection
  - Overcurrent in Discharge
  - Overcurrent in Charge
- Supports up to Two External Thermistor measurements and an internal temperature sensor
- Peripherals
  - Two 24-bit General Purpose Timers
  - General Purpose I/O's
  - CRC generator
  - True Random Number Generator

DESCRIPTION

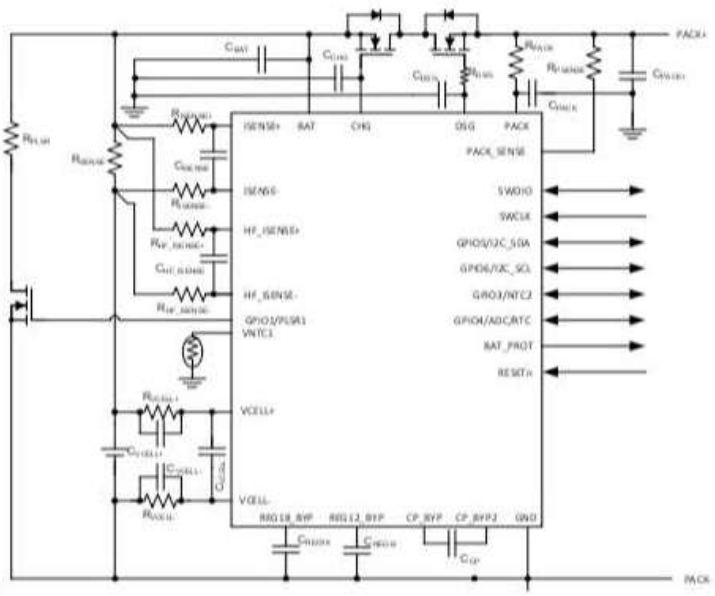
The bq7037 is a highly integrated system on chip for battery management and gas-gauge applications.

In a single CMOS Integrated Circuit, the bq7037 combines high-accuracy analog measurement capabilities with a low-power high-speed ARM Cortex M0+ processor, integrated flash memory, integrated LDO for core voltage operation and an array of peripheral features and communication ports. The program flash allows fast development of custom implementations, and the low-power analog peripherals improve accuracy beyond discrete implementations. The integrated battery charge and discharge protection feature eliminates the need for an external protection device.

Device Information

Part Number	Package	Body Size (Nom)
SN7037B0YFDR	YFD-32	1610µm x 3410µm
SN7037B0YFDT		

Simplified Schematic



1 Pin Configurations and Functions

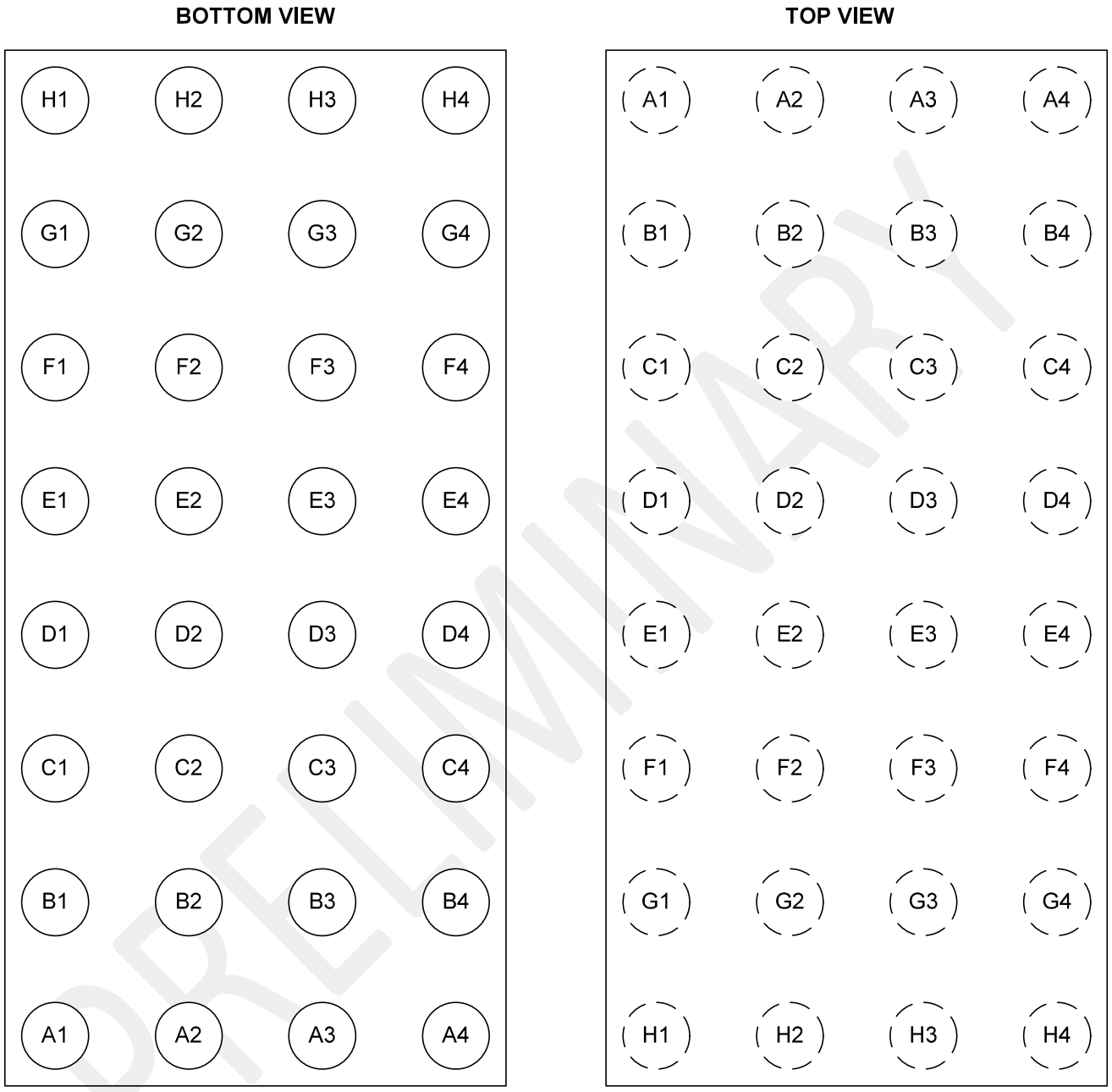


Figure 1 Pin Configuration

Table 1-1 Pin Functions

TERMINAL		I/O	DESCRIPTION
NAME	PIN		
PACK	E2	P	Device power from system when charger connected
PACK_SENSE	E1	I	Measurement of the PACK voltage used for linear control of the charge FET and A/D input
BAT	F3	P	Device power from cell
BAT_PROT	G1	O	High impedance output pin with the same voltage as the BAT pin
RESETn	B4	I	Active Low Reset input with internal pull up.
CHG	A3	O	External high side N-channel Charge FET driver
DSG	A2	O	External high side N-channel Discharge FET driver
ISENSE+	H2	I	Pack side of the current sense resistor for the continuous current A/D converter
ISENSE-	H1	I	Cell side of the current sense resistor for the continuous current A/D converter
SWCLK	B3	I	Serial Wire Debug Clock
SWDIO	C3	I/O	Serial Wire Debug Data In/Out
HF_ISENSE+	H4	I	Pack side of the current sense resistor for the High Frequency Current A/D
HF_ISENSE-	H3	I	Cell side of the current sense resistor for the High Frequency Current A/D
VCELL+	G3	I	Positive terminal of the cell
VCELL-	G2	I	Negative terminal of the cell
VNTC1	C4	I	A/D input designed to measure an external NTC thermistor
GPIO1/PLSR1	F1	I/O	Pin configurable as a general purpose input/output or as a pulser FET gate driver synchronized to the high frequency A/D sampling
GPIO2/PLSR2	F2	I/O	Pin configurable as a general purpose input/output, or as a driver for a second pulser FET
GPIO3/VNTC2	B2	I/O	Pin configurable as a general purpose input/output or as an A/D input designed to measure an external NTC thermistor
GPIO4/ADC/RTC	C2	I/O	Pin configurable as a general purpose input/output as an A/D input, or as a real time clock for an external precision clock input
GPIO5/I2C_SDA/HDQ	C1	I/O	Pin configurable as a general purpose input/output, the I2C bi-directional data line, or the bi-directional HDQ line
GPIO6/I2C_SCL	B1	I/O	General purpose input/output or the I2C clock line
REG18_BYP	G4	O	Internal linear regulator(1.8V) supply connection to an external bypass capacitor
	E3	O	Internal linear regulator(1.8V) supply connection to an external bypass capacitor
CP_BYP	A1	O	Internal charge pump connection to an external bypass capacitor
GND	F4	P	Device Ground
	D1	P	Device Ground
	D4	P	Device Ground
	A4	P	Device Ground
REG12_BYP	D2	O	Internal linear regualtor (1.2V) supply connection to an external bypass capacitor
	D3	O	Internal linear regualtor (1.2V) supply connection to an external bypass capacitor
	E4	O	Internal linear regualtor (1.2V) supply connection to an external bypass capacitor

*KEY: I =Input, O = Output, NC = No Connect, P = Power

Table 1-2 Pin Functions Ball Grids

Top View

A	CP_BYP	DSG	CHG	GND
B	GPIO6/I2C_SCL	GPIO3/VNTC2	SWCLK	RESETn
C	GPIO5/I2C_SDA/HDQ	GPIO4/ADC/RTC	SWDIO	VNTC1
D	GND	REG12_BYP	REG12_BYP	GND
E	PACK_SENSE	PACK	REG18_BYP	REG12_BYP
F	GPIO1/PLSR1	GPIO2/PLSR2	BAT	GND
G	BAT_PROT	VCELL-	VCELL+	REG18_BYP
H	ISENSE-	ISENSE+	HF_ISENSE-	HF_ISENSE+
	1	2	3	4

Bottom View

H	ISENSE-	ISENSE+	HF_ISENSE-	HF_ISENSE+
G	BAT_PROT	VCELL-	VCELL+	REG18_BYP
F	GPIO1/PLSR1	GPIO2/PLSR2	BAT	GND
E	PACK_SENSE	PACK	REG18_BYP	REG12_BYP
D	GND	REG12_BYP	REG12_BYP	GND
C	GPIO5/I2C_SDA/HDQ	GPIO4/ADC/RTC	SWDIO	VNTC1
B	GPIO6/I2C_SCL	GPIO3/VNTC2	SWCLK	RESETn
A	CP_BYP	DSG	CHG	GND
	1	2	3	4

2 Specifications

2.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	VALUE	UNITS
V_{PWR}	BAT, VCELL+, VCELL-, BAT_PROT	-0.3 to 6	V
V_{PACK}	PACK, PACK_SENSE	-0.3 to 6.5	V
V_{SR}	ISENSE+, ISENSE--, HF_ISENSE+, HF_ISENSE-	-0.3 to 6	V
V_{GPIOA}	RESETn, SWDIO, SWCLK, VNTC1, GPIO3/VNTC2, GPIO4/ADC/RTC, GPIO5/I2C_SDA/HDQ, GPIO6/I2C_SCL, GND, GND(TEST1)	-0.3 to 2.1	V
V_{GPIOB}	GPIO1/PLSR1, GPIO2/PLSR2	-0.3 to 6	V
V_{OUT}	CHG,DSG,CP_BYP	-0.3 to 8.5	V
V_{REG12_BYP}	REG12_BYP	-0.3 to 1.40	V
V_{REG18_BYP}	REG18_BYP	-0.3 to 2.1	V
T_A	Operating Ambient Temperature	-40 to 85	°C
$T_{STORAGE}$	Storage Temperature Range	-65 to 150	°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2.2 ESD Ratings

SYMBOL			VALUE	UNITS
V(ESD)	Electrostatic Discharge	Human Body Model (HBM), per JEDEC specification JESD22-A114	+/-1500	V
		Charged-device model (CDM),per JEDEC specification JESD22-C101F	+/-500	V

2.3 Recommended Operating Conditions

Typical values stated where T_A = 25 °C, Min/Max values stated where T_A = –40 °C to 85 °C unless otherwise noted.

SYMBOL	DESCRIPTION	CONDITIONS	MIN	TYP(1)	MAX	UNITS
V_{BAT}	Battery Input Voltage		2.0		5.0	V
V_{PACK}	Pack Input Voltage		2.0		5.0	V
V_{FWRITE}	VIN(2) Input Voltage	Flash Erase and Write allowed	2.4		5.0	V
C_{BAT}	Battery Input Capacitor		0.08	0.1	0.12	µF
C_{REG18}	1.8V LDO Bypass Capacitor		0.8	1	1.2	µF
C_{CP}	CP Bypass Capacitor		0.2	1	1.2	µF
C_{CHGIN}	CHG FET ripple Capacitor	Required if CHG FET C_{GS} < 10nF 3V < V_{CHG} < 8.1V	4.32	4.7	10	nF
C_{REG12}	1.2V LDO Bypass Capacitor		0.8	1	1.2	µF
C_{PACK}	PACK Capacitor		0.8	1	1.2	µF
R_{PACK}	PACK Series Resistor		180	200	220	Ω
R_{PSENSE}	PACK Sense Series Resistor		9	10	11	k Ω

(1) Production test uses typical values
(2) If (BAT > 2V), VIN = BAT, else VIN = PACK

2.4 Thermal Information

SYMBOL	PARAMETER (1)	VALUE	UNITS
Θ_{JA}	Junction-to-ambient thermal resistance(2)	78.1	°C/W
Θ_{JC}	Junction-to-case (top) thermal resistance(3)	0.3	
Θ_{JB}	Junction-to-board thermal resistance(4)	15.9	
Ψ_{JT}	Junction-to-top characterization parameter(5)	0.2	
Ψ_{JB}	Junction-to-board characterization parameter(6)	15.7	
Θ_{JCBOT}	Junction-to-case(bottom) thermal resistance(7)	NA	

1. For more information about traditional and new thermal metrics, see the device Package Thermal Metrics application report, SPRA953.
2. The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
3. The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
4. The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
5. The junction-to-top characterization parameter, Ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining Θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
6. The junction-to-board characterization parameter, Ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining Θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
7. The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

2.5 Supply Current

Typical values stated where T_A = 25 ºC, Min/Max values stated where T_A = –25 ºC to 65 ºC unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
AWAKE Mode	All Subsystems Enabled, Erasing Flash[1]		15		mA
	All Subsystems Enabled, No Flash Erase[1]		1.7		mA
Sleep Mode	SLEEP1 - See Table 4-1 for blocks enabled/disabled[1]		135		µA
	SLEEP2 - See Table 4-1 for blocks enabled/disabled[1]		134		µA
	SLEEP3 – See Table 4-1for blocks enabled/disabled		102		µA
	SLEEP4 – See Table 4-1 for blocks enabled/disabled		47		µA
Test_Mode	See Table 4-1 for blocks enabled/disabled		15		mA
Test_Init Mode	See Table 4-1 for blocks enabled/disabled		600		µA
Reset Mode	See Table 4-1 for blocks enabled/disabled		35		µA
Flash_Init Mode	See Table 4-1 for blocks enabled/disabled		53		µA
Power_Ready Mode	See Table 4-1 for blocks enabled/disabled		49		µA
Power_Off Mode	See Table 4-1 for blocks enabled/disabled		3.5		µA

1. Both HF_I_ADC/HF_VT_ADC are assumed to be running with a Output Sample Rate of 256 Hz

2.6 Voltage References

Typical values stated where T_A = 25 ºC, Min/Max values stated where T_A = –40 ºC to 85 ºC unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC_REF}	Coulomb Counter Reference Voltage	T_A = 25°C	1.00	1.16	1.34	V
V_{REF1p0}	Internal System Reference Voltage	T_A = 25°C	0.999	1.000	1.001	V
V_{CCREF_DRIFT}	CC_REF Reference Voltage Drift	T_A = -25°C to 65°C			±56	PPM/°C
$PSRR_{CC\_REF}$ (1)	Power Supply Rejection Ratio ($\Delta V_{BAT}/\Delta V_{CC\_REF}$)	I_{REG18} = 10mA, V_{BAT} > 2.5V, V_{BATAC} ±100mV f = 0 to 20kHz T_A = -25°C to 65°C	40	50	60	dB
I_{CC_REF}				10		µA
V_{HF_REF}	HF_ADC Reference Voltage	T_A = 25°C	1.00	1.21	1.36	V
$V_{HF\_REF\_DRIFT}$	HF_ADC Reference Voltage Drift	T_A = -25°C to 65°C			±56	PPM/°C
$PSRR_{HF\_REF}$ (1)	Power Supply Rejection Ratio ($\Delta V_{BAT}/\Delta V_{HF\_REF}$)	I_{REG18} = 10mA, V_{BAT} > 2.5V, V_{BATAC} ±100mV f = 0 to 20kHz T_A = -25°C to 65°C	40	50	60	dB
I_{HF_REF}	Current Consumption	HF_ADC Mod Fs = 512k		35		µA

(1) Specified by design. Not production tested

2.7 1.8V LDO Regulator (REG18)

Typical values stated where T_A = 25 ºC, Min/Max values stated where T_A = –40 ºC to 85 ºC unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{REG18}	Regulator output voltage	2 V < VIN[1] < 5 V, I_{REG18} = 0 to 12 mA 2.4 V < VIN[1] < 5 V, I_{REG18} = 0 to 22 mA	1.75	1.8	1.85	V
		After trim is loaded	-3		+3	%
$\Delta V_{REG18TEMP}$	Regulator output change with temperature (ΔV_{REG18}/ V_{REG18})	I_{REG18} = 1 mA	-1		1	%
$\Delta V_{REG18LINE}$	Line regulation ($\Delta V_{REG18}/\Delta V_{BAT}$)	I_{REG18} = 22 mA V_{BAT} = 2 to 5V	-2		2	%
$\Delta V_{REG18LOAD}$	Load regulation ($\Delta V_{REG18}/\Delta I_{REG18}$)	I_{REG18} = 0 to 22 mA	-2		2	%
$\Delta V_{TRANSIENT}$	Transient response load step	I_{REG18} = 0 to 10 mA	-55		45	mV
I_{REG18_EXT}	External load capability	V_{BAT} = 2 to 5V			1	mA
I_{REG18_SHORT}	Short Circuit Current Limit	V_{REG18} = 0 V	20	38	85	mA
		V_{REG18} = 0 V, After trim is loaded	26	38	72	mA
$PSRR_{REG18}$[(2)]	Power Supply Rejection Ratio ($\Delta V_{BAT}/\Delta V_{REG18}$)	I_{REG18} = 10 mA, V_{BAT} > 2.5 V, f = 1 Hz to 20 kHz, VIN[(1)] Ripple = ±100 mV	30	40	50	dB
$V_{REG18TH+}$	REG18 Good Threshold Rising	POR = $V_{REG18TH-}$ + $V_{REG18HYS}$		1.73		V
$V_{REG18TH-}$	REG18 Good Threshold Falling		1.63	1.7	1.77	V
$V_{REG18HYS}$	REG18 Good Hysteresis		10	30	50	mV
I_{REG18}	Current Consumption			6		µA

(1) If (BAT > 2V), VIN = BAT, else VIN = PACK
(2) Specified by design. Not production tested.

2.8 1.2V LDO Regulator (REG12)

Typical values stated where T_A = 25 ºC, Min/Max values stated where T_A = –40 ºC to 85 ºC unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{REG12}	Regulator output voltage	2 V < VIN[1] < 5 V, I_{REG12} = 0 to 10 mA	1.15	1.2	1.25	V
		After trim is loaded	-3		+3	%
$\Delta V_{REG12TEMP}$	Regulator output change with temperature (ΔV_{REG12}/ V_{REG12})	I_{REG12} = 1 mA	-1		1	%
$\Delta V_{REG12LINE}$	Line regulation ($\Delta V_{REG12}/\Delta V_{BAT}$)	I_{REG12} = 10 mA V_{BAT} = 2 to 5V	-1		1	%
$\Delta V_{REG12LOAD}$	Load regulation ($\Delta V_{REG12}/\Delta I_{REG12}$)	I_{REG12} = 0 to 10 mA	-1		1	%
$\Delta V_{TRANSIENT}$	Transient response load step	I_{REG12} = 0 to 10 mA	-55		45	mV
I_{REG12_SHORT}	Short Circuit Current Limit	V_{REG12} = 0 V	12	20	35	mA
$PSRR_{REG12}$ (2)	Power Supply Rejection Ratio ($\Delta V_{BAT}/\Delta V_{REG12}$)	I_{REG18} = 10 mA, V_{BAT} > 2.5 V, f = 1 Hz to 20 kHz, VIN Ripple = ±100 mV	30	50	130	dB
$V_{REG12TH+}$	REG12 Good Threshold Rising	POR = $V_{REG12TH-}$+ $V_{REG12HYS}$		1.03		V
$V_{REG12TH-}$	REG12 Good Threshold Falling		0.95	1	1.05	V
$V_{REG12HYS}$	REG12 Good Hysteresis		10	30	50	mV
I_{REG12}	Current Consumption	I_{REG12} = 0mA		3.5		µA

(1) If (BAT > 2V), VIN = BAT, else VIN = PACK
(2) Specified by design. Not production tested.

2.9 Under Voltage Lock Out (UVLO)

Typical values stated where T_A = 25 ºC, Min/Max values stated where T_A = –40 ºC to 85 ºC unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
$V_{UVLOTHR+}$	UVLO Detection Voltage Rising Threshold	V_{BAT} or V_{PACK}.	2.1	2.35	2.6	V
$V_{UVLOTHR-}$	UVLO Detection Voltage Falling Threshold, Post Trim	V_{BAT} or V_{PACK}. SCOMP_EN = 1	2.0	2.05	2.1	V
I_{UVLO}	Current Consumption			2		µA

2.10 Pack Overvoltage Protection (OVP)

Typical values stated where T_A = 25 ºC, Min/Max values stated where T_A = –40 ºC to 85 ºC unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{OVP_TH}	OVP Detection Voltage Rising Threshold	With respect to V_{PACK_SENSE}	4.95	5.0	5.05	V
t_{OVP}	OVP Detection Time	XYZ_FAST_EN = 3b100		180	250	µs
I_{OVP}	Current Consumption			3		µA

2.11 Fast Reaction Current Safety Discharge (DSG_SFTY)

Typical values stated where T_A = 25 ºC, Min/Max values stated where T_A = –40 ºC to 85 ºC unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{OCD_TH1}	DSG_SFTY 1 Detection Voltage Threshold	$V_{ISENSE+}$ - $V_{ISENSE-}$, DSG_SFTY_LVL1 = 1 to 127	-0.5		-62.5	mV
V_{OCD_TH1ST}	DSG_SFTY 1 Detection Voltage Threshold step size		250	500	750	µV
V_{OCD_TH2}	DSG_SFTY 2 Detection Voltage Threshold	$V_{ISENSE+}$ - $V_{ISENSE-}$, DSG_SFTY_LVL2 = 1 to 127	-0.5		-62.5	mV
V_{OCD_TH2ST}	DSG_SFTY 2 Detection Voltage Threshold step size		250	500	750	µV
V_{OCD_TH3}	DSG_SFTY 3 Detection Voltage Threshold	$V_{ISENSE+}$ - $V_{ISENSE-}$, DSG_SFTY_LVL3 = 1 to 127	-0.5		-62.5	mV
V_{OCD_TH3ST}	DSG_SFTY 3 Detection Voltage Threshold step size		250	500	750	µV
V_{OCD_TH4}	DSG_SFTY 4 Detection Voltage Threshold	$V_{ISENSE+}$ - $V_{ISENSE-}$, DSG_SFTY_LVL4 = 1 to 127	-0.5		-62.5	mV
V_{OCD_TH4ST}	DSG_SFTY 4 Detection Voltage Threshold step size		250	500	750	µV
$V_{OCD\_SCALEERR}$	DSG_SFTY Detection Scale Error			5		%
I_{OCD}	Current Consumption			1		µA
t_{OCD_DLY1}	DSG Safety Time1	DSG_SFTY_TIME1 = 0 to 255	61		15600	µs
$t_{OCD\_DLY1\_ACC}$	DSG Safety Time1 Accuracy	DSG_SFTY_TIME1 = 0 to 255	-15		15	µs
t_{OCD_DLY2}	DSG Safety Time2	DSG_SFTY_TIME2 = 0 to 255	0.98		250	ms
t_{OCD_DLY3}	DSG Safety Time3	DSG_SFTY_TIME3 = 0 to 255	15.6		4000	ms
t_{OCD_DLY4}	DSG Safety Time4	DSG_SFTY_TIME4 = 0 to 255	15.6		4000	ms
$t_{OCD\_DLY2,3,4\_ACC}$	DSG Safety Time2,3,4 Accuracy	DSG_SFTY_TIME2,3,4 = 0 to 255	-100		100	µs

2.12 Fast Reaction Current Safety Charge (CHG_SFTY)

Typical values stated where T_A = 25 ºC, Min/Max values stated where T_A = –40 ºC to 85 ºC unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{OCC_TH}	CHG_SFTY Detection Voltage Threshold	$V_{ISENSE-}$ - $V_{ISENSE+}$, CHG_SFTY_LVL = 1 to 127	62.5		0.5	mV
V_{OCC_THST}	CHG_SFTY Detection Voltage Threshold step size		250	500	750	µV
$V_{OCC\_SCALEERR}$	CHG_SFTY Detection Scale Error			5		%
I_{OCC}	Current Consumption			1		µA
t_{OCC_DLY}	CHG Safety Time	CHG_SFTY_TIME = 0 to 255	15.6		4000	ms
$t_{OCC\_DLY\_ACC}$	ChG Safety Time Accuracy	CHG_SFTY_TIME = 0 to 255	-100		100	µs

2.13 PTAT Good Comparator (PTATDET)

Typical values stated where T_A = 25 ºC, Min/Max values stated where T_A = –40 ºC to 85 ºC unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
T_{PTAT_TH}	PTAT Good Threshold		110	120	130	°C
T_{PTAT_HYS}	PTAT Good Hysteresis			10		°C
I_{PTAT}	Current Consumption			0.8		µA

2.14 Internal Temperature Sensor (INTTEMP)

Typical values stated where T_A = 25 ºC, Min/Max values stated where T_A = –40 ºC to 85 ºC unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
$V_{INTTEMP}$ (1)	Internal Temperature sensor voltage drift		-1.5	-1.9	-2.3	mV/°C
$V_{INTTEMP\_ERR}$	Internal Temperature sensor Accuracy		-3		+3	°C
$I_{INTTEMP}$	Current Consumption			50		µA

1) Data to calculate slope is stored in the device see section 7.1.4.14

2.15 Charger Detect (CD)

Typical values stated where T_A = 25 ºC, Min/Max values stated where T_A = –40 ºC to 85 ºC unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{CD}	Charger Detect Threshold	$V_{PACK\_SENSE} - V_{BAT}$ CHGR_DET_EN = 1	1		50	mV
$t_{debounce}$	Charger Debounce Times	CHGR_DET_DEBOUNCE = 0000	2	2	3	Clocks (1)
		CHGR_DET_DEBOUNCE = 0001	4	4	5	
		CHGR_DET_DEBOUNCE = 0010	8	8	9	
		CHGR_DET_DEBOUNCE = 0011	16	16	17	
		CHGR_DET_DEBOUNCE = 0100	32	32	33	
		CHGR_DET_DEBOUNCE = 0101	64	64	65	
		CHGR_DET_DEBOUNCE = 0110	128	128	129	
		CHGR_DET_DEBOUNCE = 0111	256	256	257	
		CHGR_DET_DEBOUNCE = 1000	512	512	513	
		CHGR_DET_DEBOUNCE = 1001	1024	1024	1025	
		CHGR_DET_DEBOUNCE = 1010	2048	2048	2049	
		CHGR_DET_DEBOUNCE = 1011	4096	4096	4097	
		CHGR_DET_DEBOUNCE = 1100	8192	8192	8193	
		CHGR_DET_DEBOUNCE = 1101	16384	16384	16385	
		CHGR_DET_DEBOUNCE = 1110	32768	32768	32769	
		CHGR_DET_DEBOUNCE = 1111	65536	65536	65537	
I_{CD}	Current Consumption	CHGR_DET_EN = 1		1		µA

(1) Clocks are those of the internal 32768 Hz clock derived from the Low Frequency Oscillator (LFO)

2.16 Protected Battery Output (BAT_PROT)

Typical values stated where T_A = 25 ºC, Min/Max values stated where T_A = –40 ºC to 85 ºC unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{PBOVIN}	Input Voltage Range	BAT_PROT_EN = 1	2.0		5	V
R_{PBORon}	Resistance On	BAT_PROT_EN = 1			5000	Ω
$I_{PBOIOUT}$	Output Current Drive Capability	BAT_PROT_EN = 1			100	µA
$I_{REVERSE}$	Reverse Current from BAT_PROT to BAT	BAT_PROT_EN = 1		-20		µA
		BAT_PROT_EN = 0		-1		µA
t_{FLT_DET}	Fault detection time	BAT_PROT_EN = 1, C_{BAT_PROT} ≤ 10nF			200	µs
I_{PBO}	Current Consumption	BAT_PROT_EN = 1		0.6		µA

2.17 Secondary Wakeup (SEC_WAKE)

Typical values stated where T_A = 25 ºC, Min/Max values stated where T_A = –40 ºC to 85 ºC unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
R_{SEC_WAKE}	Secondary Wake up Series Resistance	SCNDRY_WAKE_DATA = 1	400	550	800	Ω
t_{SEC_WAKE}	Secondary Wake up Connection Time		4.5	5	5.5	ms

2.18 Pack Clamp (PACK_CLAMP)

Typical values stated where T_A = 25 ºC, Min/Max values stated where T_A = –40 ºC to 85 ºC unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{PACK_CLAMP}	Rising voltage on Pack when clamp is active	I_{PACK_CLAMP} < 1mA	5.3			V
		I_{PACK_CLAMP} < 150mA	5.3			V
P_{PACK_CLAMP} (1) (2)	Pack Clamp Power Dissipation	$V_{PACK} = V_{PACK\_SENSE} \le V_{PACK\_CLAMP(MAX)}$			0.5	W
		$V_{PACK} = V_{PACK\_SENSE} \le V_{PACK\_CLAMP(MAX)}$, t = 10 ms			0.75	W
$I_{PACK\_CLAMP\_PEAK}$ (1)	Peak current consumption when clamp fully active	For a time < 1ms			150	mA
$I_{PACK\_CLAMP\_ON}$	Current consumption when clamp fully active				100	mA
t_{PACK_CLAMP} (1)	Clamp activation slew rate	$V_{PACK} = V_{PACK\_SENSE} \le V_{PACK\_CLAMP(MAX)}$, C_{PACK} = 1 µF	50	100		ns/V
$I_{PACK\_CLAMP\_OFF}$	Current Consumption	Not Clamping		0.1		µA

(1) Specified by design. Not production tested
(2) Simulated on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.

2.19 High Frequency Oscillator (HFO)

Typical values stated where T_A = 25 ºC, Min/Max values stated where T_A = –40 ºC to 85 ºC unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
F_{HOSC}	Operating Frequency	After system calibration	48	50.33	51.5	MHz
F_{HOSCD} (2)	Frequency Drift (1)	After system calibration -25°C to 65°C	-1.5%		2.5%	
		After system calibration -20°C to 55°C FLL_TIGHT_LOCK = 1	-1%		1%	
t_{HFO_START} (2)	HFO Start Up time	Oscillator frequency within ±3% of nominal			10	µs
I_{HOSC}	Current Consumption			24		µA

(1) The frequency drift is included and measured from the trimmed frequency at T_A = 25°C
(2) Specified by design. Not production tested

2.20 Low Frequency Oscillator (LFO)

Typical values stated where T_A = 25 ºC, Min/Max values stated where T_A = –40 ºC to 85 ºC unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
F_{LOSC}	Operating Frequency[1]		260.18	262.144	264.1	kHz
	Trim Accuracy	T_A = 25°C	-0.1%		0.1%	
F_{LOSCD}	Frequency Drift [2]	-25°C to 65°C (after system calibration)	-0.4%		0.4%	
t_{LFO_START} (3)	LFO Start Up time	Oscillator frequency within ±3% of nominal			80	µs
F_{LFO_WD} (3)	LFO Watchdog Fault Frequency		116	212	238	kHz
I_{LOSC}	Current Consumption			2.5		µA

(1) The raw LFO frequency will be will be divided to generate all the clocks for internal modules
(2) The frequency drift is included and measured from the trimmed frequency at T_A = 25°C
(3) Specified by design. Not production tested

2.21 Continuous Current ADC (CC_ADC)

Typical values stated where T_A = 25 ºC, Min/Max values stated where T_A = –25 ºC to 65 ºC unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
CC_{VIN}	Input Voltage Range	$V_{ISENSE+}$ - $V_{ISENSE-}$	-62.5		62.5	mV
CC_{CMODE} (3)	Input Common Mode Range	$V_{ISENSE-}$ - GND	0		5	V
CC_{ER}	Effective Resolution (1)(3)	Post system calibration, CC_CAL_MUX = 2b00	18			bits
		Pre system calibration, CC_CAL_MUX = 2b00	16			bits
		Post system calibration, CC_CAL_MUX = 2b01 or 2b10	16.5			bits
		Pre system calibratio, CC_CAL_MUX = 2b01 or 2b10	14.5			bits
CC_{INL}	Integral Non Linearity(2) (3)				±20	LSB
CC_{VOSER}	Offset Error	Post system calibration, CC_CAL _MUX= 2b00		±2		LSB
		Pre system calibration, CC_CAL _MUX= 2b00		±3		LSB
		Post system calibration. CC_CAL_MUX = 2b01 or 2b10		±3.5		LSB
		Pre system calibration, CC_CAL_MUX = 2b01 or 2b10		±4.5		LSB
CC_{VOS_DR}	Offset Error Drift(3)	T_A=-25 to 65°C, post system calibration		±5		LSB
		T_A=-25 to 65°C, Pre system calibration		±6		LSB
CC_{VOS}	Offset Error across full scale(3)	Post system calibration, CC_CAL_MUX = 2b00		0.0016		%FSR
		Pre system calibration, CC_CAL_MUX = 2b00		0.0023		%FSR
CC_{NOISE}	Noise Floor(2) (3)			700		nV/√Hz
CC_{GAINER}	Gain Error(5)	T_A= -25 to 65°C, 2 V ≤ VIN(6) ≤ 5 V, Post system calibration		±16		LSB
		T_A= -25 to 65°C, 2 V ≤VIN(6) ≤ 5 V, Pre system calibration		±18		LSB
CC_{GAINER_DR}	Gain Error Drift(3) (5)	T_A= -25 to 65°C, 2 V ≤VIN(6) ≤ 5 V, Post system calibration		5		LSB/°C
		T_A= -25 to 65°C, 2 V ≤VIN(6) ≤ 5 V, Pre system calibration		6		LSB/°C
CC_{GAIN}	Gain Error Across Full Scale(5)	Post system calibration		0.013		%FSR
		Pre system calibration		0.014		%FSR
CC_{DNL}	Differential Non Linearity(3) (4)	T_A=-25 to 65°C	-1		1	LSB
CC_{LKG}	Input Leakage				0.3	µA
I_{CC}	Current Consumption(3)			26.5		µA

1. Input signal Vcell+ = 4.35, DC = ±1mV, Harmonic Free Full Scale
2. First order curve fit from –FS to + FS
3. Specified by design. Not production tested
4. Monotonic performance
5. Does not include CC Reference Gain Error
6. If (BAT > 2V), VIN = BAT, else VIN = PACK

2.22 High Frequency Current ADC (HF_I_ADC)

Typical values stated where T_A = 25 °C, Min/Max values stated where T_A = –25 °C to 65 °C unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
$HFIADC_{IN}$	Input Voltage Range	$V_{HF\_ISENSE+}$ - $V_{HF\_ISENSE-}$	-62.5		62.5	mV
HFI_{CMODE} (5)	Input Common Mode Range	$V_{HF\_ISENSE-}$. GND	0		5	V
$HFIADC_{RES256}$	SNR and SFDR (1) (5) Sample Rate = 256 Hz	Modulator Clock = 524.288 kHz HF_FIR_SEL = 2b00	15			bits
$HFIADC_{RES1K}$	SNR and SFDR (1) (5) Sample Rate = 1.024 kHz	Modulator Clock = 2097.152 kHz HF_FIR_SEL = 2b00		15		bits
$HFIADC_{RES2K}$	SNR and SFDR (1) (5) Sample Rate = 2.048 kHz	Modulator Clock= 4194.304 kHz HF_FIR_SEL = 2b00		15		bits
$HFIADC_{RES4K}$	SNR and SFDR (1) (5) Sample Rate = 4.096 kHz	Modulator Clock= 8388.608 kHz HF_FIR_SEL = 2b11		14		bits
$HFIADC_{RES8K}$	SNR and SFDR (1) (5) Sample Rate = 8.192 kHz	Modulator Clock= 8388.608 kHz HF_FIR_SEL = 2b11		14		bits
$HFIADC_{RES16K}$	SNR and SFDR (1) (5) Sample Rate = 16.384 kHz	Modulator Clock= 8388.608 kHz HF_FIR_SEL = 2b11		13		bits
$HFIADC_{RES32K}$	SNR and SFDR (1) (5) Sample Rate = 32.768 kHz	Modulator Clock= 8388.608 kHz HF_FIR_SEL = 2b11		13		bits
$HFIADC_{RES64K}$	SNR and SFDR (1) (5) Sample Rate = 65.535 kHz	Modulator Clock= 8388.608 kHz HF_FIR_SEL = 2b11	12			bits
$t_{hfiadcconv256}$	Conversion Time (5) Sample Rate =256 Hz	HF_FREQ = 3b000 HF_FIR_SEL = 2b00		3.90		ms
$t_{hfiadcconv1K}$	Conversion Time (5) Sample Rate =1.024 kHz	HF_FREQ = 3b001 HF_FIR_SEL = 2b00		0.976		ms
$t_{hfiadcconv2K}$	Conversion Time (5) Sample Rate =2.048 kHz	HF_FREQ = 3b010 HF_FIR_SEL = 2b00		0.488		ms
$t_{hfiadcconv4K}$	Conversion Time (5) Sample Rate =4.096 kHz	HF_FREQ = 3b011 HF_FIR_SEL = 2b11		0.244		ms
$t_{hfiadcconv8K}$	Conversion Time (5) Sample Rate = 8.192 kHz	HF_FREQ = 3b100 HF_FIR_SEL = 2b11		122		µs
$t_{hfiadcconv16K}$	Conversion Time (5) Sample Rate = 16.384 kHz	HF_FREQ = 3b101 HF_FIR_SEL = 2b11		61		µs
$t_{hfiadcconv32K}$	Conversion Time (5) Sample Rate = 32.768 kHz	HF_FREQ = 3b110 HF_FIR_SEL = 2b11		31		µs
$t_{hfiadcconv64K}$	Conversion Time (5) Sample Rate = 65.535 kHz	HF_FREQ = 3b111 HF_FIR_SEL = 2b11		15		µs
$HFIADC_{INL256}$	Integral Non Linearity (2) (5) Sample Rate = 256 Hz	HF_FREQ = 3b000, Modulator Clock= 524.288 kHz HF_FIR_SEL = 2b00	-4		+4	LSB
$HFIADC_{INL1K}$	Integral Non Linearity (2) (5) Sample Rate = 1.024 kHz	HF_FREQ = 3b001 Modulator Clock= 2097.152 kHz HF_FIR_SEL = 2b00	-4		+4	LSB
$HFIADC_{INL2K}$	Integral Non Linearity (2) (5) Sample Rate = 2.048 kHz	HF_FREQ = 3b010 Modulator Clock= 4194.304 kHz HF_FIR_SEL = 2b00	-4		+4	LSB

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
$HFIADC_{INL4K}$	Integral Non Linearity[2] [5] Sample Rate = 4.096 kHz	HF_FREQ = 3b011 Modulator Clock= 8388.608 kHz HF_FIR_SEL = 2b11	-4		+4	LSB
$HFIADC_{INL8K}$	Integral Non Linearity[2] [5] Sample Rate = 8.192 kHz	HF_FREQ = 3b100 Modulator Clock= 8388.608 kHz HF_FIR_SEL = 2b11	-4		+4	LSB
$HFIADC_{INL16K}$	Integral Non Linearity[2] [5] Sample Rate = 16.384 kHz	HF_FREQ = 3b101 Modulator Clock= 8388.608 kHz HF_FIR_SEL = 2b11	-4		+4	LSB
$HFIADC_{INL32K}$	Integral Non Linearity[2] [5] Sample Rate = 32.768 kHz	HF_FREQ = 3b110 Modulator Clock= 8388.608 kHz HF_FIR_SEL = 2b11	-4		+4	LSB
$HFIADC_{INL64K}$	Integral Non Linearity[2] [5] Sample Rate = 65.535 kHz	HF_FREQ = 3b111 Modulator Clock= 8388.608 kHz HF_FIR_SEL = 2b11	-4		+4	LSB
$HFIADC_{VOSER}$	Offset Error[6]	Sample Rate =256 Hz, Modulator Clock= 524.288 kHz, T_A= -25 to 65°C, 2 V ≤VIN[8] ≤ 5 V, Post system calibration		±2		LSB
		Sample Rate =256 Hz, Modulator Clock= 524.288 kHz, T_A= -25 to 65°C, 2 V ≤VIN[8] ≤ 5 V, Pre system calibration		±3		LSB
$HFIADC_{VOSER\_DR}$	Offset Error Drift[5]	T_A= -25 to 65°C, 2 V ≤ VIN[7] ≤ 5 V, Post system calibration		±5		LSB
		T_A= -25 to 65°C, 2 V ≤ VIN[7] ≤ 5 V, Pre system calibration		±6		LSB
$HFIADC_{VOS}$	Offset Error across full scale[5]	T_A= -25 to 65°C, 2 V ≤ VIN[7] ≤ 5 V, Post system calibration		0.03		%FSR
		T_A= -25 to 65°C, 2 V ≤ VIN[7] ≤ 5 V, Pre system calibration		0.04		%FSR
$HFIADC_{NOISE}$	Noise Floor[5]	DC to Sample output rate /3		170		nV/√Hz
$HFIADC_{GAINER}$	Gain Error[4][5]	T_A= -25 to 65°C, 2 V ≤ VIN[7] ≤ 5 V, Post system calibration		±16		LSB
		T_A= -25 to 65°C, 2 V ≤ VIN[7] ≤ 5 V, Pre system calibration		±18		LSB
$HFIADC_{GAINER\_DR}$	Gain Error Drift[4] [5]	T_A= -25 to 65°C, 2 V ≤ VIN[7] ≤ 5 V ,Post system calibration		5		LSB/°C
		T_A= -25 to 65°C, 2 V ≤ VIN[7] ≤ 5 V, Pre system calibration		7		LSB/°C
$HFIADC_{GAIN}$	Gain Error across Full Scale Range[4] [5]	T_A= -25 to 65°C, 2 V ≤ VIN[7] ≤ 5 V, With in system calibration		0.25		%FSR
		T_A= -25 to 65°C, 2 V ≤ VIN[7] ≤ 5 V, Pre system calibration		0.5		%FSR
$HFIADC_{DNL}$	Differential Non Linearity[3] [5]	HF_FREQ = 3b000	-1		+1	LSB
$HFIADC_{ICC1}$	Current Consumption[5]	Sample Rate = 256 Hz, Modulator Clock= 524.288 kHz HF_FIR_SEL = 2b00		157		µA
$HFIADC_{ICC2}$		Sample Rate= 1024 Hz, Modulator Clock= 2097.152 kHz HF_FIR_SEL = 2b00		371		µA

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
$HFIADC_{ICC3}$		Sample Rate= 2048 Hz, Modulator Clock= 4194.304 kHz HF_FIR_SEL = 2b00		721		µA
$HFIADC_{ICC4}$		Sample Rate= 4096 Hz Modulator Clock= 8388.608 kHz HF_FIR_SEL = 2b11		1421		µA
$HFIADC_{ICC5}$		Sample Rate= 8192 Hz, Modulator Clock= 8388.608 kHz HF_FIR_SEL = 2b11		1421		µA
$HFIADC_{ICC6}$		Sample Rate= 16384 Hz, Modulator Clock= 8388.608 kHz HF_FIR_SEL = 2b11		1421		µA
$HFIADC_{ICC7}$		Sample Rate= 32768 Hz, Modulator Clock= 8388.608 kHz HF_FIR_SEL = 2b11		1421		µA
$HFIADC_{ICC8}$		Sample Rate= 65536 Hz, Modulator Clock= 8388.608 kHz HF_FIR_SEL = 2b11		1421		µA

1) Input signal Vcell+ = 4.35, AC =±1mV, f = Sample Rate /4, Harmonic Free Full Scale
2) First order curve fit from -FS to + FS
3) Monotonic Performance
4) Does not include HF Reference Gain Error
5) Specified by design. Not production tested
6) Offset error is the standard deviation of the measured offset
7) If (BAT > 2V), VIN = BAT, else VIN = PACK

2.23 High Frequency Voltage/Temp ADC (HF_VT_ADC)

Typical values stated where T_A = 25 °C, Min/Max values stated where T_A = –25 °C to 65 °C unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
$HFVTADC_{IN}$	V_{CELL} Range	SAMPn_SEL = 4b0001	0		5	V
	V_{PACK_SENSE} Range	SAMPn_SEL =4b0011	0		5	V
	$V_{INTTEMP}$ Range	SAMPn_SEL = 4b0100	0		1.2	V
	V_{GPIO4} Range	SAMPn_SEL = 4b0101	0		1.8	V
	V_{NTC} Range	SAMPn_SEL = 4b0110 or 4b0111	0		1.8	V
	V_{VDD_1P2} Range	SAMPn_SEL = 4b1000	0		1.8	V
	V_{VDD_1P8} Range	SAMPn_SEL = 4b1001	0		1.8	V
	V_{SCOMP} Range	SAMPn_SEL = 4b1010	0		1.8	V
	V_{HF_VREF} Range	SAMPn_SEL = 4b1011	0		1.8	V
	V_{CC_REF} Range	SAMPn_SEL = 4b1100	0		1.8	V
	V_{GND} Range	SAMPn_SEL = 4b1101	0		1.8	V
$HFVTADC_{RES256}$	SNR and SFDR[1] [5] [7] Sample Rate = 256Hz	Modulator Rate = 524.288 kHz, HF_FIR_SEL = 2b00	16			bits
$HFVTADC_{RES1K}$	SNR and SFDR[1] [5] [7] Sample Rate = 1.024 kHz	Modulator Clock= 2097.152 kHz, HF_FIR_SEL = 2b00		16		bits
$HFVTADC_{RES2K}$	SNR and SFDR[1] [5] [7] Sample Rate = 2.048 kHz	Modulator Clock= 4194.304 kHz, HF_FIR_SEL = 2b00		16		bits
$HFVTADC_{RES4K}$	SNR and SFDR[1] [5] [7] Sample Rate = 4.096 kHz	Modulator Clock= 8388.608 kHz, HF_FIR_SEL = 2b11		15		bits
$HFVTADC_{RES8K}$	SNR and SFDR[1] [5] [7] Sample Rate = 8.192 kHz	Modulator Clock= 8388.608 kHz, HF_FIR_SEL = 2b11		15		Bits
$HFVTADC_{RES16K}$	SNR and SFDR[1] [5] [7] Sample Rate = 16.384 kHz	Modulator Clock= 8388.608 kHz, HF_FIR_SEL = 2b11		14		bits
$HFVTADC_{RES32K}$	SNR and SFDR[1] [5] [7] Sample Rate = 32.768 kHz	Modulator Clock= 8388.608 kHz, HF_FIR_SEL = 2b11		14		bits
$HFVTADC_{RES64K}$	SNR and SFDR[1] [5] [7] Sample Rate = 65.535 kHz	Modulator Clock= 8388.608 kHz, HF_FIR_SEL = 2b11	13			bits
$t_{hfvtadcconv256}$	Conversion Time [5] Sample Rate = 256Hz	HF_FREQ = 3b000		3.90		ms
$t_{hfvtadcconv1K}$	Conversion Time [5] Sample Rate = 1.024 kHz	HF_FREQ = 3b001		0.976		ms
$t_{hfvtadcconv2K}$	Conversion Time [5] Sample Rate = 2.048 kHz	HF_FREQ = 3b010		0.488		ms
$t_{hfvtadcconv4K}$	Conversion Time [5] Sample Rate = 4.096 kHz	HF_FREQ = 3b011		0.244		ms
$t_{hfvtadcconv8K}$	Conversion Time [5] Sample Rate = 8.192 kHz	HF_FREQ = 3b100		0.122		ms
$t_{hfvtadcconv16K}$	Conversion Time [5] Sample Rate = 16.384 kHz	HF_FREQ = 3b101		0.061		ms
$t_{hfvtadcconv32K}$	Conversion Time [5] Sample Rate = 32.768 kHz	HF_FREQ = 3b110		0.031		ms

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
$t_{hfvtadcconv64K}$	Conversion Time [5] Sample Rate = 65.535 kHz	HF_FREQ = 3b111		0.016		ms
$HFVTADC_{INL256}$	Integral Non Linearity[2] [5] Sample Rate = 256 Hz	HF_FREQ = 3b000, Modulator Clock= 524.288 kHz HF_FIR_SEL = 2b00	-4		+4	LSB
$HFVTADC_{INL1K}$	Integral Non Linearity[2] [5] Sample Rate = 1.024 kHz	HF_FREQ = 3b001 Modulator Clock= 2097.152 kHz HF_FIR_SEL = 2b00	-4		+4	LSB
$HFVTADC_{INL2K}$	Integral Non Linearity[2] [5] Sample Rate = 2.048 kHz	HF_FREQ = 3b010 Modulator Clock= 4194.304 kHz HF_FIR_SEL = 2b00	-4		+4	LSB
$HFVTADC_{INL4K}$	Integral Non Linearity[2] [5] Sample Rate = 4.096 kHz	HF_FREQ = 3b011 Modulator Clock= 8388.608 kHz HF_FIR_SEL = 2b11	-4		+4	LSB
$HFVTADC_{INL8K}$	Integral Non Linearity[2] [5] Sample Rate = 8.192 kHz	HF_FREQ = 3b100 Modulator Clock= 8388.608 kHz HF_FIR_SEL = 2b11	-4		+4	LSB
$HFVTADC_{INL16K}$	Integral Non Linearity[2] [5] Sample Rate = 16.384 kHz	HF_FREQ = 3b101 Modulator Clock= 8388.608 kHz HF_FIR_SEL = 2b11	-4		+4	LSB
$HFVTADC_{INL32K}$	Integral Non Linearity[2] [5] Sample Rate = 32.768 kHz	HF_FREQ = 3b110 Modulator Clock= 8388.608 kHz HF_FIR_SEL = 2b11	-4		+4	LSB
$HFVTADC_{INL64K}$	Integral Non Linearity[2] [5] Sample Rate = 65.536 kHz	HF_FREQ = 3b111 Modulator Clock= 8388.60 8 kHz HF_FIR_SEL = 2b11	-4		+4	LSB
$HFVTADC_{VOSER}$	Offset Error[6]	Sample Rate =256 Hz, Modulator Clock= 524.288 kHz, T_A= -25 to 65°C, 2 V ≤VIN[6] ≤ 5 V, Post system calibration		±2		LSB
		Sample Rate =256 Hz, Modulator Clock= 524.288 kHz, T_A= -25 to 65°C, 2 V ≤VIN[6] ≤ 5 V, Pre system calibration		±3		LSB
$HFVTADC_{VOS\_DR}$	Offset Error Drift[5]	T_A= -25 to 65°C, 2 V ≤VIN[6] ≤ 5 V, Post system calibration	-5		5	LSB
		T_A= -25 to 65°C, 2 V ≤VIN[6] ≤ 5 V, Pre system calibration	-7		7	LSB
$HFVTADC_{VOS}$	Offset Error across Full Scale Range [4] [5]	T_A= -25 to 65°C, 2 V ≤VIN[6] ≤ 5 V, Post system calibration		0.03		%FSR
		T_A= -25 to 65°C, 2 V ≤VIN[6] ≤ 5 V, Pre system calibration		0.04		
$HFVTADC_{NOISE}$	Noise Floor [5]	DC to Sample output rate /3		7		µV/√Hz
$HFVTADC_{GAINER}$	Gain Error[4] [5]	T_A= -25 to 65°C, 2 V ≤VIN[6] ≤ 5 V, Post system calibration		±16		LSB
		T_A= -25 to 65°C, 2 V ≤VIN[6] ≤ 5 V, Pre system calibration		±18		
$HFVTADC_{GAINER\_DR}$	Gain Error Drift[4] [5]	T_A= -25 to 65°C, 2 V ≤VIN[6] ≤ 5 V, Post system calibration		5		LSB/°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
		T_A= -25 to 65°C, 2 V ≤VIN[6] ≤ 5 V, Pre system calibration		7		
$HFVTADC_{GAIN}$	Gain Error across Full Scale Range[4] [5]	T_A= -25 to 65°C, 2 V ≤VIN[6] ≤ 5 V, Post system calibration		0.25		%FSR
		T_A= -25 to 65°C, 2 V ≤VIN[6] ≤ 5 V, Pre system calibration		0.5		
$HFVTADC_{DNL}$	Differential Non Linearity [3] [5]	HF_FREQ = 3b000	-1		+1	LSB
$HFVTADC_{ICC1}$	Current Consumption[5]	Sample Rate= 256 Hz, Modulator Clock= 524.288 kHz HF_FIR_SEL = 2b00		157		µA
$HFVTADC_{ICC2}$		Sample Rate= 1024 Hz, Modulator Clock= 2097.152 kHz HF_FIR_SEL = 2b01		371		µA
$HFVTADC_{ICC3}$		Sample Rate= 2048 Hz Modulator Clock= 4194.304 kHz HF_FIR_SEL = 2b01		721		µA
$HFVTADC_{ICC3}$		Sample Rate= 4096 Hz Modulator Clock= 8388.608 kHz HF_FIR_SEL = 2b01		1421		µA
$HFVTADC_{ICC4}$		Sample Rate= 8192 Hz, Modulator Clock= 8388.608 kHz HF_FIR_SEL = 2b01		1421		µA
$HFVTADC_{ICC5}$		Sample Rate= 16384 Hz, Modulator Clock= 8388.608 kHz HF_FIR_SEL = 2b01		1421		µA
$HFVTADC_{ICC6}$		Sample Rate= 32768 Hz, Modulator Clock= 8388.608 kHz HF_FIR_SEL = 2b01		1421		µA
$HFVTADC_{ICC7}$		Sample Rate= 65536 Hz, Modulator Clock= 8388.608 kHz HF_FIR_SEL = 2b01		1421		µA

1) Input signal VCELL+ = 4.35 V, AC = ±100 mV, f = Sample Rate /4, Harmonic Free Full Scale
2) First order curve fit from -FS to + FS
3) Monotonic Performance
4) Specified by design. Not production tested
5) Does not include HF Reference Gain Error
6) If (BAT > 2V), VIN = BAT, else VIN = PACK
7) Applicable to VCELL+ - VCELL- input channel

2.24 Charge Pump (CP)

Typical values stated where T_A = 25 ºC, Min/Max values stated where T_A = –40 ºC to 85 ºC unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{CPIN}	Charge Pump Input Voltage Highest of V_{BAT} or V_{PACK}		2.0		5.0	V
V_{CP}	Charge Pump Voltage	VIN(1) < 3.5V, ((DSG_CTRL = 1 OR CHG_CTRL = 01,10,11) OR (DSG__CTRL= 1 AND CHG_CTRL = 01,10,11))	V_{IN}+4.5	V_{IN}+4.6	V_{IN}+4.7	V
		VIN(1) ≥ 3.5 ((DSG_CTRL = 1 OR CHG_CTRL = 01,10,11) OR (DSG__CTRL= 1 AND CHG_CTRL = 01,10,11))	8.0	8.1	8.2	V
V_{CP_HYS}	Charge Pump Voltage Hysteresis	Hysteresis between the two CP modes		50		mV
V_{CP_RIPPLE}	Charge pump ripple			±50		mV
$I_{CPDRIVE\_CHG}$	Charge Pump Output Drive Charge	CHG_CTRL = 01,10,11	6			µA
$I_{CPDRIVE\_DSG}$	Charge Pump Output Drive Discharge	DSG_CTRL = 1	6			µA
F_{CP}	Charge Pump Switching Frequency(2)	During turn On		16		MHz
		When On and including linear mode		4		
I_{CP}	Current Consumption per Output	(DSG_CTRL = 1 OR CHG_CTRL = 01,10,11)		6		µA

(1) V_{IN} = Maximum of V_{BAT} and V_{PACK}.
(2) Specified by design, not production tested

2.25 Charge Pump Good (CPGOOD)

Typical values stated where T_A = 25 °C, Min/Max values stated where T_A = –40 °C to 85 °C unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{CPTH}	Charge Pump Good Threshold for CHG and DSG	VIN[1] < 3.5V, (DSG_CTRL = 1 OR CHG_CTRL = 01,11) OR (DSG_CTRL = 1 AND CHG_CTRL = 01,11)	VIN+4.4	VIN+4.5	VIN+4.6	V
		VIN[1] ≥ 3.5 (DSG_CTRL = 1 OR CHG_CTRL = 01,11) OR (DSG_CTRL = 1 AND CHG_CTRL = 01,11)	7.9	8.0	8.1	V
V_{CPHYS}[2]	Charge Pump Good Hysteresis		25	50	75	mV
I_{CPGOOD}	Current Consumption	(DSG_CTRL = 1 OR CHG_CTRL = 01,11) OR (DSG_CTRL = 1 AND CHG_CTRL = 01,11)		1		µA

(1) If (BAT > 2V), VIN = BAT, else VIN = PACK
(2) Specified by design, not production tested

2.26 CHG and DSG FET Drive

Typical values stated where T_A = 25 °C, Min/Max values stated where T_A = –40 °C to 85 °C unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{FETON}	CHG Gate Drive Voltage On	C_L = 10nF, VIN[2] < 3.5V	VIN+4.5	VIN+4.6	VIN+4.7	V
		C_L = 10nF, VIN[2] ≥ 3.5V	8.0	8.1	8.2	V
	DSG Gate Drive Voltage On	C_L = 10nF, VIN[2] < 3.5V	VIN+ 4.5	VIN+4.6	VIN+ 4.7	V
		C_L = 10nF, VIN[2] ≥ 3.5V	8.0	8.1	8.2	V
V_{FETOFF}	CHG Gate Drive Voltage Off	(V_{CHG} – GND), C_L = 10nF		0.0	0.1	V
	DSG Gate Drive Voltage Off	(V_{DSG} – GND), C_L = 10nF		0.0	0.1	V
t_{FETON}	FET Gate Rise Time	C_L = 10nF , 10% to 90% of Gate Drive			500	µs
$t_{FETFULLON}$	FET Gate Rise Time when using CP_BYP	C_L = 10nF,C_{CP} = 1µF, 10% to 90% of Gate Drive			15	µs
$I_{LNRSFETOUT}$[1]	CHG Output Turn ON Current in Linear Mode	C_L = 10nF,C_{CP} = 1µF, VIN[2] = 3.5 V, V_{CHG} = 5V	33	44	55	µA
	CHG Output Turn OFF Current in Linear Mode	C_L = 10nF,C_{CP} = 1µF, V_{CHG} = 2 V	0.35	0.7	1.2	mA
R_{CPBYP_CHG}	Resistance between CP_BYP and CHG when path enabled			700	1000	Ω
$I_{FETTURNOFF}$	FET Drive current when turning off the FET	CHG: CHG_CTRL = 2b00 DSG: DSG_CTRL = 0 2V < V_{OL} ≤ 5 V	6.5	12.5	18.5	mA
I_{FETOFF}	FET Drive current when in 'OFF' State	CHG: CHG_CTRL = 2b00 DSG: DSG_CTRL = 0 V_{OL} = 0.1 V	160	200		µA
	Linear Regulation Transconductance[1]	Measured at 1 kHz	4.5	16.5	25	mA/V
	Open Loop Gain[1]		51		70	dB

(1) Specified by design. Not production tested
(2) VIN is the greatest of BAT or PACK

2.27 Ideal Diode Detector (ID)

Typical values stated where T_A = 25 °C, Min/Max values stated where T_A = –40 °C to 85 °C unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{IDCD}	Ideal Diode Charge Detection used to turn FET OFF	CHG_CTRL = 2b11, $V_{HF\_ISENSE+}$ - V_{HI_SENSE-}	250	500	750	µV
V_{CHG_RMVD}	Charger Removal Detection	CHG_CTRL = 2b11, $V_{PACK} < V_{BAT}$	-10	-20	-30	mV
t_{CHG_RMVD}	Charger Removal Detection Time	$V_{PACK\_SENSE} < V_{BAT} - V_{CHG\_RMVD}$ when CHG_STS = 3b010 or 3b100	7	11	15	µs
t_{CHG_DET}	Charger Detection Time	$V_{PACK\_SENSE} > V_{BAT}$ When CHG_STS = 3b100	30	45	60	µs
$t_{CHG\_CUR\_DET}$	Charger Current Detection Time		30	45	60	µs
I_{ID}	Current Consumption(1)	CHG_CTRL = 2b11		6		µA

1) Specified by design. Not production tested

2.28 DACs

Typical values stated where T_A = 25 °C, Min/Max values stated where T_A = –40 °C to 85 °C unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{LNR_TGT}	LNR_TGT Output Range	LNRTGT = 0x594 to 0x1BE6	1.0		5	V
V_{LNR_DAC}	LNR_TGT DAC Output Range	LNRTGT = 0x594 to 0x1BE6	0.16		0.8	V
V_{LNR_RES}	LNR_TGT DAC Resolution(2)		80	112	150	µV
V_{LNR_GAIN}	LNR_TGT DAC Output Gain			6.25		
V_{LNR_DNL}	LNR_TGT DAC DNL(2)		-1		1	LSB
I_{LNR_DAC}	Current Consumption	CHG_CTRL = 2b10		50		µA
V_{PACK_MIN}	PACK_MIN Output Range	PACKMIN = 0x00 to 0x3F	2.0		5	V
V_{PACK_DAC}	PACK_MIN DAC Output Range	PACKMIN = 0x00 to 0x3F	0.32		0.8	V
V_{PACK_RES}	PACK_MIN DAC Resolution		6	7.5	9	mV
V_{PACK_GAIN}	PACK_MIN DAC Output Gain			6.25		
V_{PACK_INL}	PACK_MIN DAC IN(2)		-2		2	bits
I_{PACK_MIN}	Current Consumption	CHG_CTRL = 2b10		1		µA
V_{CP_REF}	CP REF Output Range	2.0V ≤ VIN(1) < 3.5 V, PUMPREFDAC_TRIM_LOW = 0x00 to 0x31	3.9		5.7	V
		3.5 V ≤ VIN(1) ≤ 5 V, PUMPREFDAC_TRIM_HIGH = 0x00 to 0x31	5.9		8.5	V
V_{CP_REFDAC}	CP REF DAC Output Range	PUMPREFDAC_HIGH or PUMPREFDAC_LOW = 0x00 to 0x31	0.55		0.8	V
$V_{CP\_REF\_RES}$	CP REF DAC Resolution(2)		3.75	5	6.25	mV
$V_{CP\_REF\_GAIN}$	CP REF DAC Output Gain	2.0 V ≤ VIN(1) < 3.5 V		7.2		
		3.5 V ≤ VIN(1) ≤ 5 V		10.8		
$V_{CP\_REF\_INL}$	CP REF DAC INL(2)		-2		2	bits
I_{CP_REFDAC}	Current Consumption(1)	CHG_CTRL = 2b01,2b10, 2b11		5		µA

(1) The greater of V_{PACK} or V_{BAT}

2) Specified by design. Not production tested

2.29 General Purpose Input Characteristics

Typical values stated where T_A = 25 °C, Min/Max values stated where T_A = –40 °C to 85 °C unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High-level input voltage	PAD Voltage = REG18(1) GPIO1…4, SWDIO, SWCLK, RESETn		1.1			V
		PAD Voltage = REG18(1) GPIO5 , GPIO6		0.7* V_{DDS}(4)			
		PAD Voltage = BAT(2), V_{BAT} ≥ 3 V, GPIO1/PLSR1, GPIO2/PLSR2		2.4			V
V_{IL}	Low-level input voltage low	PAD Voltage = REG18(1) , GPIO1…6, SWDIO, SWCLK, RESETn				0.5	V
		PAD Voltage = REG18(1) , GPIO5 , GPIO6				0.3* V_{DDS}(4)	
		PAD Voltage = BAT(2) , V_{BAT} ≥ 3 V, GPIO1/PLSR1, GPIO2/PLSR2				0.9	V
V_{IOHYS}	Hysteresis of Input(3)	PAD Voltage = REG18(1) GPIO1…6, SWDIO, SWCLK, RESETn		75			mV
		PAD Voltage = BAT(2) , V_{BAT} ≥ 3 V, GPIO1/PLSR1, GPIO2/PLSR2		120			mV
R_{PD}	Internal pull down resistance	Pin pulled to GND, GPIO3…6, SWDIO, SWCLK. PXWKPU[i] = 1 AND PXPDR[n] = 0		18		50	kΩ
		Pin pulled to GND, GPIO1/PLSR1, GPIO2/PLSR2, PXWKPU[i] = 1 AND PXPDR[n] = 0	PAD Voltage = REG18(1)	10		100	kΩ
			PAD Voltage = BAT(2) V_{BAT} ≥ 3 V	7		50	kΩ
R_{PU}	Internal pull up resistance	Pin pulled to REG18, GPIO3…4, SWDIO, SWCLK, RESETn, PXWKPU[i] = 1 AND PXPDR[n] = 1		18		50	kΩ
		Pin pulled to PAD Voltage, GPIO1/PLSR1, GPIO2/PLSR2, PXWKPU[i] = 1 AND PXPDR[n] = 1	PAD Voltage = REG18(1)	10		100	kΩ
			PAD Voltage = BAT(2) V_{BAT} ≥ 3 V	7		50	kΩ
I_{I2CPD}	Internal I^2C pull down current	SCL and SDA, PXALT[5:4] = 2b11		50	100	150	nA
R_{NTCA}(5)	Internal NTC Support Resistance	VNTC1 and GPIO3/VNTC2 Only RNTC_EN = 1, RNTC_SEL_100K = 0		9.3	12	15	kΩ
R_{NTCB}(5)		VNTC1 and GPIO3/VNTC2 Only RNTC_EN = 1, RNTC_SEL _100K = 1		105	130	160	kΩ
R_{NTC_TC}	Internal NTC Support Resistor Temperature coefficient (3)	VNTC1 and GPIO3/VNTC2 Only RNTC_EN = 1, RNTC_SEL_100K = 0 or 1			0		ppm/°C
C_I	Input capacitance				5		pF
I_{lkg}	Input leakage current					1.0	µA

(1) PXHDRV[1:0] = 2b00
(2) PXHDRV[1:0] = 2b11
(3) Specified by design. Not production tested
(4) V_{DDS} is the pullup voltage
(5) This value is measured and stored in the device see section 7.1.6.2

2.30 General Purpose Output Characteristics

Typical values stated where T_A = 25 ºC, Min/Max values stated where T_A = –40 ºC to 85 ºC unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNITS
V_{OH}	Output voltage high	PAD Voltage = REG18(1) I_{out} = 450µA, GPIO1…4, SWDIO, SWCLK		0.85* V_{REG18}			V
		GPIO1/PLSR1, GPIO2/PLSR2, PAD Voltage = BAT(2) , C_L = 110pF	V_{BAT} ≥ 3.3 V, I_{out} = -2 mA,	0.85* V_{BAT}			V
			2.0 V ≤ V_{BAT} < 3.3 V, I_{out} = -100 µA,				
V_{OL}	Output voltage low	PAD Voltage = REG18(1) I_{out} = 450µA, GPIO1…6, SWDIO, SWCLK				0.1* V_{REG18}	V
		GPIO1/PLSR1, GPIO2/PLSR2 PAD Voltage = BAT(2)	V_{BAT} ≥ 3.3 V, I_{IN} = -2 mA,			0.1* V_{BAT}	V
			2.0 V ≤ V_{BAT} < 3.3 V, I_{IN} = -100 µA,			100	mV
I_{OH}	High-level output current	PAD Voltage = REG18(1) GPIO3…6, SWDIO, SWCLK, RESETn		-450			µA
		PAD Voltage = BAT(2) , V_{BAT} ≥ 3 V, GPIO1/PLSR1, GPIO2/PLSR2		-2			mA
I_{OL}	Low-level output current	PAD Voltage = REG18(1) GPIO1…6, SWDIO, SWCLK, RESETn		450			µA
		PAD Voltage = BAT(2) GPIO1/PLSR1, GPIO2/PLSR2		2			mA
$t_{PULSERRISE}$	Pulser FET Gate Rise Time	GPIO1/PLSR1, GPIO2/PLSR2, PAD Voltage = BAT(2), C_L = 110pF, Q_{tot} = 1nC, 0% to 90% of Gate Drive				6	µs
$t_{PULSERFALL}$	Pulser FET Gate Fall Time	GPIO1/PLSR1, GPIO2/PLSR2, PAD Voltage = BAT(2),C_L = 110pF, Q_{tot} = 1nC, 100% to 10% of Gate Drive				6	µs

(1) PXHDRV[1:0] = 2b00
(2) PXHDRV[1:0] = 2b11

2.31 Flash Memory

Typical values stated where T_A = 25 °C, Min/Max values stated where T_A = –40 °C to 85 °C unless otherwise noted.

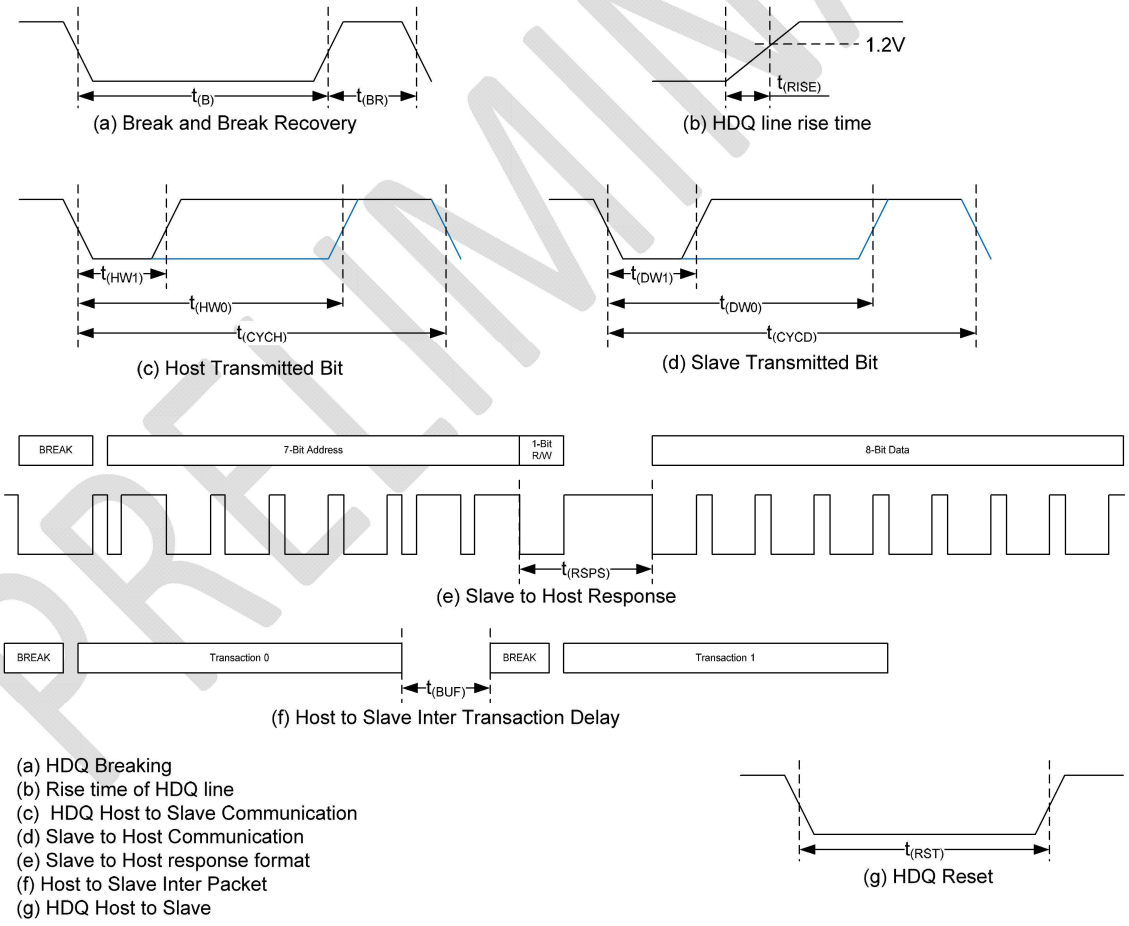
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
t_{DR}	Data retention(1)		10	100		Years
	Flash programming write-cycles(1)		20000			Cycles
$t_{ROWPROG}$	Word (64 bits) programming time(1)			40		µs
$t_{MASSERASE}$	Mass-erase time(1)			14	500	ms
$t_{PGERASE}$	Sector-erase time(1)			14	500	ms
I_{READ}	Flash Read Current(1)			1600		µA
I_{ERASE}	Flash Erase Current(1)			14700		µA
I_{WRITE}	Flash Write Current(1)			13900		µA

1. Specified by design. Not production tested.

2.32 HDQ Timing

Typical values stated where T_A = 25 °C, Min/Max values stated where T_A = –40 °C to 85 °C unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
$t_{(CYCH)}$	Cycle time, host to bq7037		190			µs
$t_{(CYCD)}$	Cycle time, bq7037 to host		190	205	250	µs
$t_{(HW1)}$	Host sends 1 to bq7037		0.5		50	µs
$t_{(DW1)}$	bq7037 sends 1 to host		32		50	µs
$t_{(HW0)}$	Host sends 0 to bq7037		86		145	µs
$t_{(DW0)}$	bq7037 sends 0 to host		80		145	µs
$t_{(RSPS)}$	Response time, bq7037 to host		190		950	µs
$t_{(B)}$	Break time		190			µs
$t_{(BR)}$	Break recovery time		40			µs
$t_{(RST)}$	HDQ reset		1.8		2.2	s
$t_{(RISE)}$	HDQ line rising time to logic 1 (1.2V)				1.8	µs
$t_{(BUF)}$	Inter transaction time		210			µs



(a) HDQ Breaking
(b) Rise time of HDQ line
(c) HDQ Host to Slave Communication
(d) Slave to Host Communication
(e) Slave to Host response format
(f) Host to Slave Inter Packet
(g) HDQ Host to Slave

Figure 2 – HDQ Timing Diagram

2.33 I²C Timing – 100 kHz

Typical values stated where T_A = 25 °C, Min/Max values stated where T_A = –40 °C to 85 °C unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
F_{SCL}	Clock Frequency	I2C_MODE = 0			100	kHz
$t_{HD:STA}$	START Condition Hold Time		4.0			µs
t_{LOW}	Low Period of SCL Clock		4.7			µs
t_{HIGH}	High Period of SCL Clock		4.0			µs
$t_{SU:STA}$	Setup Time for repeated START		4.7			µs
$t_{HD:DAT}$	Data In Hold Time		0			µs
$t_{SU:DAT}$	Data in Setup Time		250			ns
$t_{VD:DAT}$	Data Valid Time (1) (2)				3.45	µs
			75			ns
$t_{VD:ACK}$	Data Valid Acknowledge Time(1) (2)				3.45	µs
			75			ns
t_r	SDA and SCL Rise Time	30% to 70%			1000	ns
t_F	SDA and SCL Fall Time	70% to 30%			300	ns
$t_{SU:STO}$	STOP Condition Setup Time		4.0			µs
t_{BUF}	Bus Free Time between STOP and START		4.7			µs
$t_{TIMEOUT}$	Error SCL Low Signal Detect Time		25		35	ms
C_D	Capacitive load for each bus line				400	pF

1. This maximum is only met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.
2. Specified by Design. Not production tested.

2.34 I²C Timing – 400 kHz

Typical values stated where T_A = 25 °C, Min/Max values stated where T_A = –40 °C to 85 °C unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
F_{SCL}	Clock Frequency	I2C_MODE = 1			400	kHz
$t_{HD:STA}$	START Condition Hold Time		0.6			µs
t_{LOW}	Low Period of SCL Clock		1.3			µs
t_{HIGH}	High Period of SCL Clock		0.6			µs
$t_{SU:STA}$	Setup Time for repeated START		0.6			µs
$t_{HD:DAT}$	Data In Hold Time		0			µs
$t_{SU:DAT}$	Data in Setup Time		100			ns
$t_{VD:DAT}$	Data Valid Time (1) (2)				0.9	µs
			75			ns
$t_{VD:ACK}$	Data Valid Acknowledge Time (1) (2)				0.9	µs
			75			ns
t_r	SDA and SCL Rise Time	30% to 70%	20		300	ns
t_F	SDA and SCL Fall Time	70% to 30%, V_{PULLUP} is external pullup voltage source	20 * (V_{PULLUP} /5.5)		300	ns
$t_{SU:STO}$	STOP Condition Setup Time		0.6			µs
t_{BUF}	Bus Free Time between STOP and START		1.3			µs
$t_{TIMEOUT}$	Error SCL Low Signal Detect Time		25		35	ms
C_D	Capacitive load for each bus line				400	pF

1. This maximum is only met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.
2. Specified by Design. Not production tested.

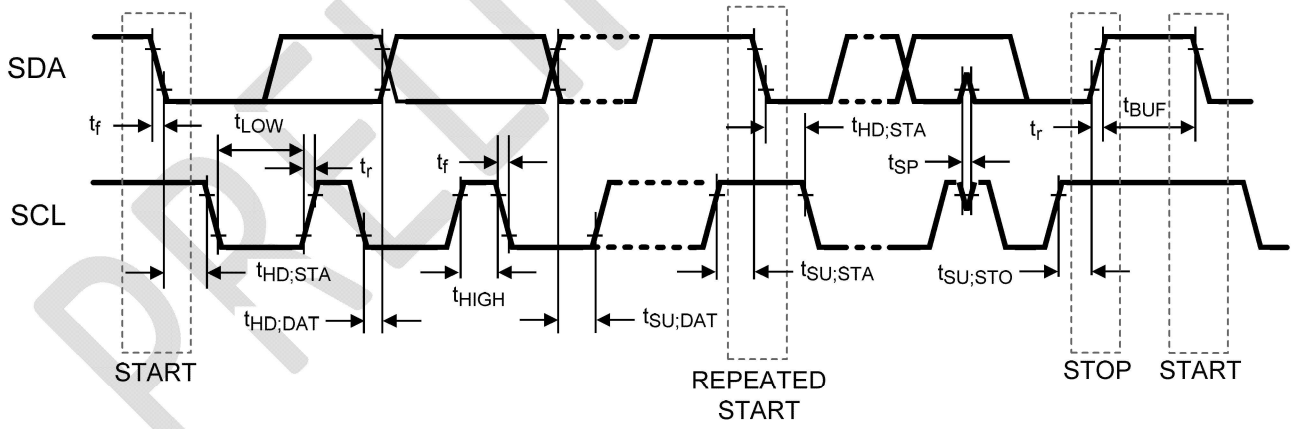


Figure 3 – I²C Timing Diagram

2.35 True Random Number Generator Timing

Typical values stated where T_A = 25 °C, Min/Max values stated where T_A = –40 °C to 85 °C unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
$t_{(TRNG)}$	TRNG creation time	TRNG_EN = 1 to TRNG_DRDY = 1 for 32-bits		50		ms

2.36 Power Control

Typical values stated where T_A = 25 °C, Min/Max values stated where T_A = –40 °C to 85 °C unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
I_{PWR_CTRL}	Current Consumption(1)			3.5		µA

1. Specified by design. Not production tested.