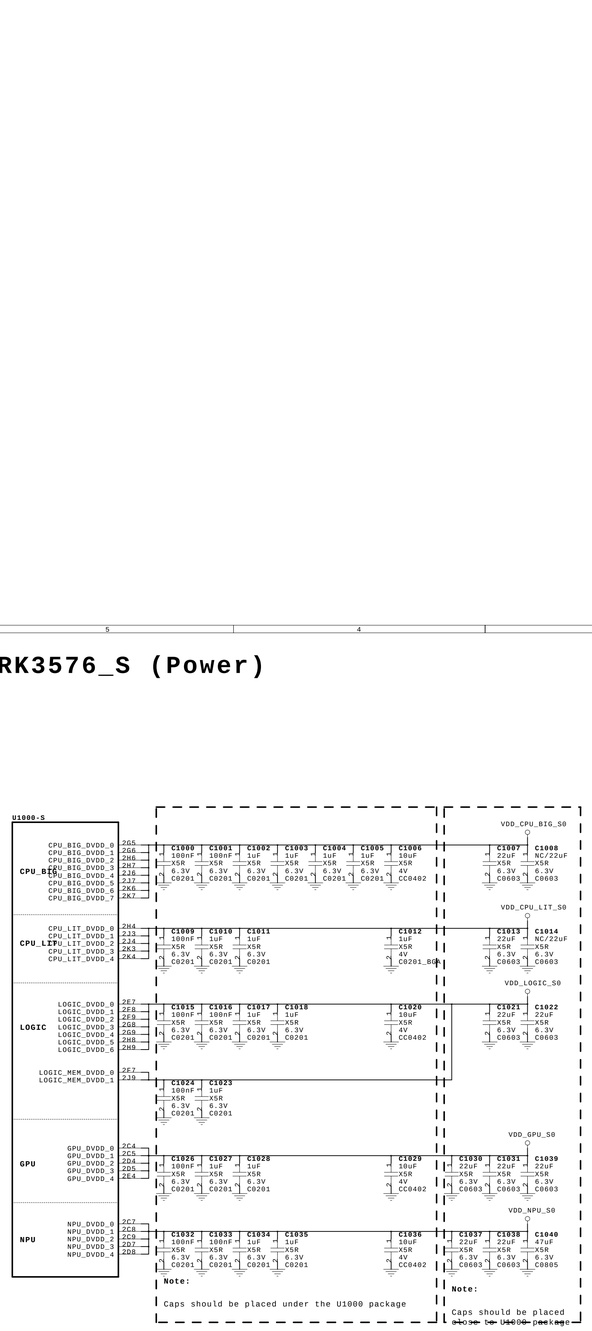
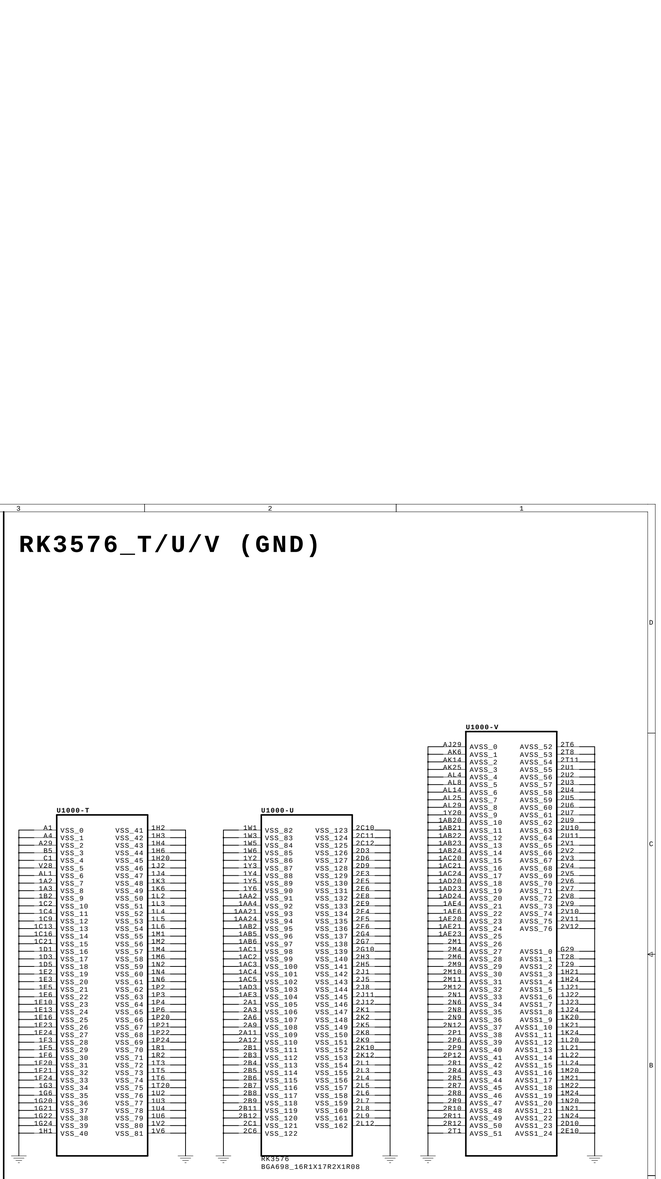
RK3576_S (Power)



RK3576_T/U/V (GND)



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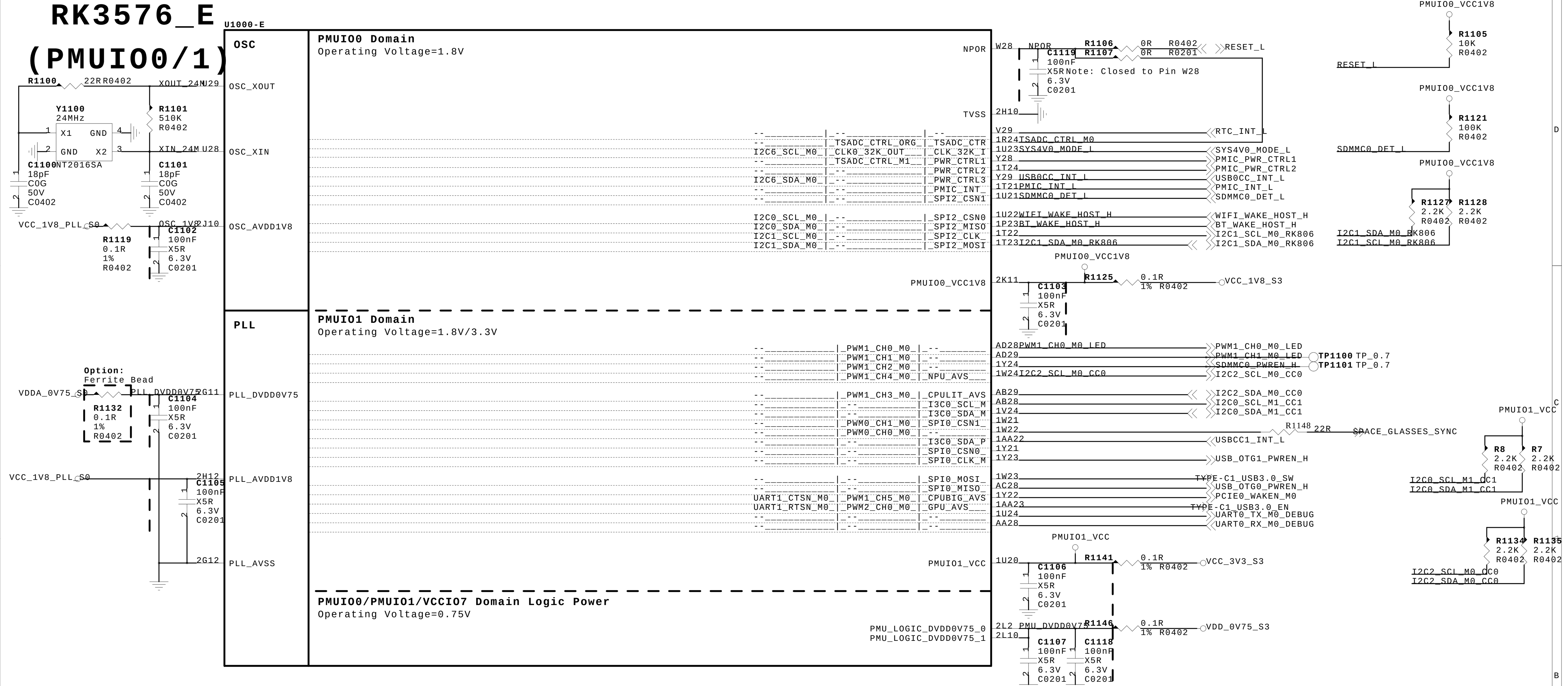
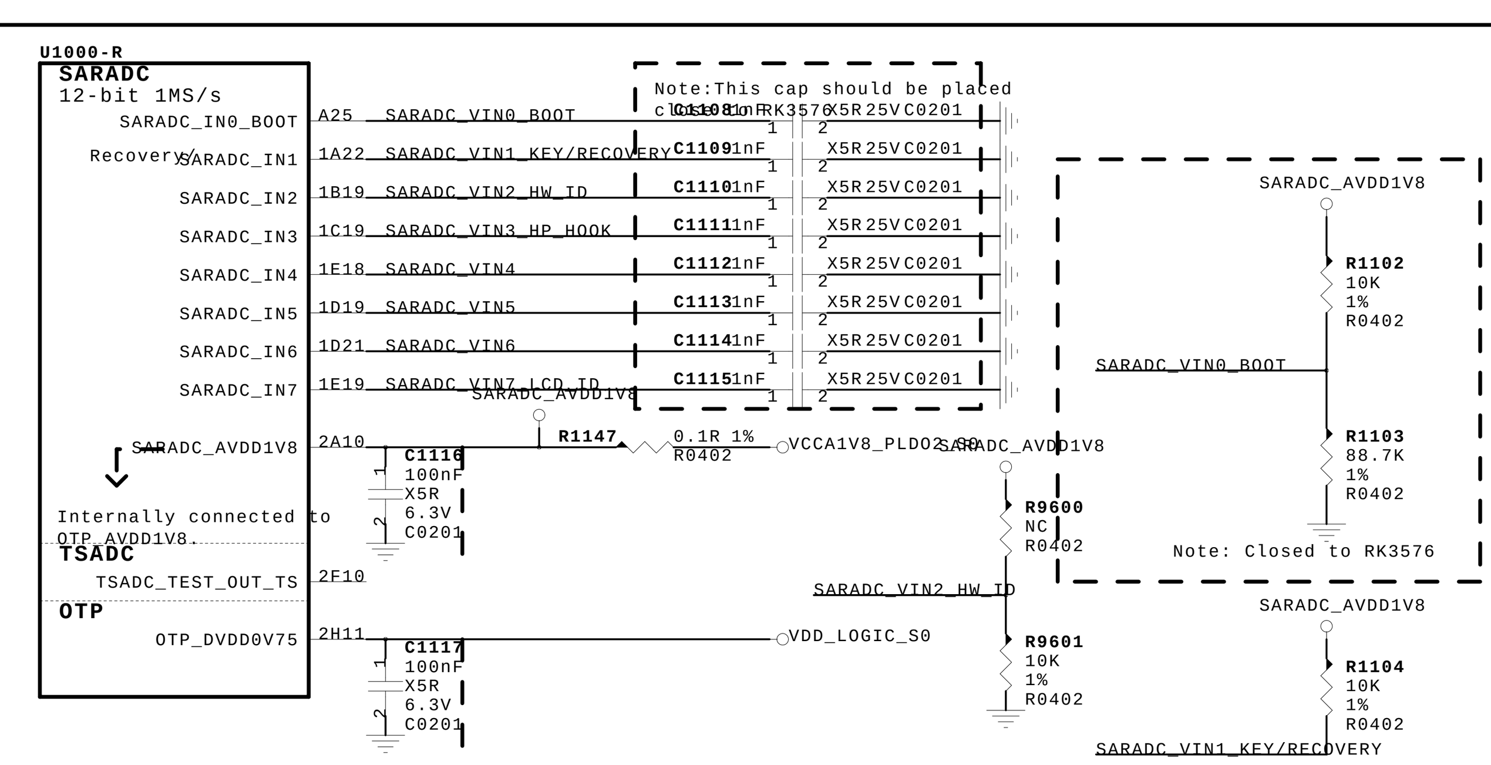
RK3576_E (PMUIO0/1)



RK3576_R (SARADC)



Note:

Caps of between dashed red lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

BOOT MODE CONFIG

Config Table for SARADC_VIN0_BOOT

Item	Rup	Rdown	ADC Value	Boot Mode
Config1	NC	10K	0	USB (Maskrom mode)
Config2	10K	1.13K	416	FSPI0->USB
Config3	10K	2.49K	816	FSPI1_M0->EMMC->USB
Config4	10K	4.3K	1231	FSPI1_M1->EMMC->USB
Config5	10K	6.8K	1658	FSPI0->UFS->USB
Config6	10K	10K	2048	FSPI1_M0->UFS->USB
Config7	10K	14.7K	2437	UFS->USB
Config8	10K	23.2K	2862	UFS->SDMMC0->USB
Config9	10K	40.2K	3279	RFU
Config10	10K	88.7K	3680	EMMC->SDMMC0->USB
Config11	10K	NC	4095	EMMC->USB

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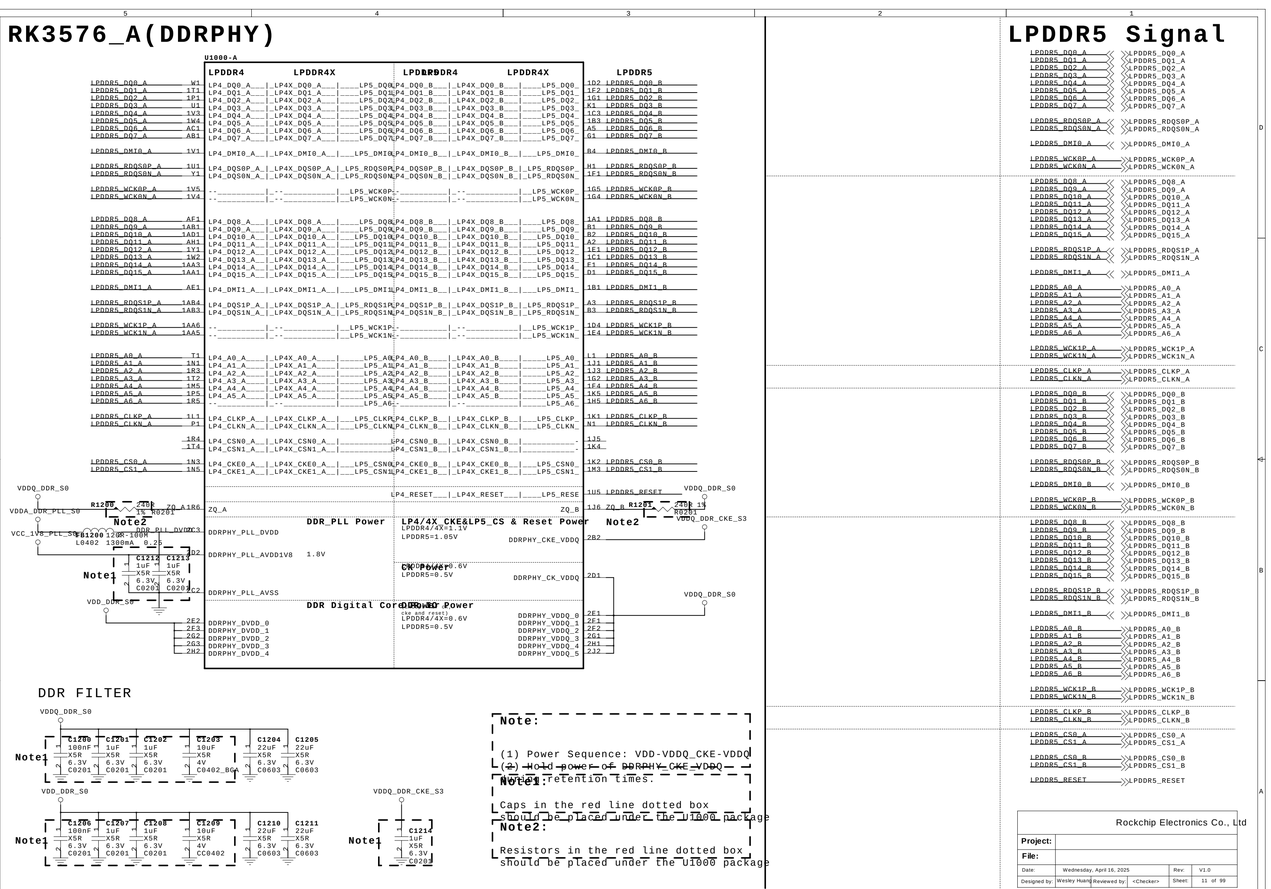
RK3576_A(DDRPHY)



DDR FILTER

Note:

(1) Power Sequence: VDD-VDDQ_CKE-VDDQ

(2) Hold power of DDRPHY_CKE_VDDQ during retention times.

Note1:

Caps in the red line dotted box should be placed under the U1000 package

Note2:

Resistors in the red line dotted box should be placed under the U1000 package

LPDDR5 Signal

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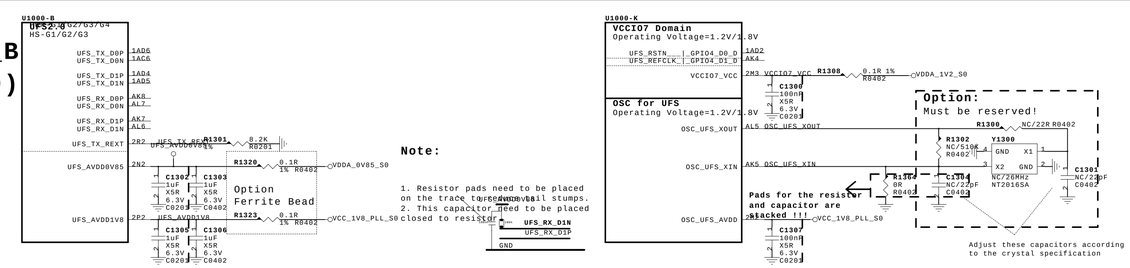
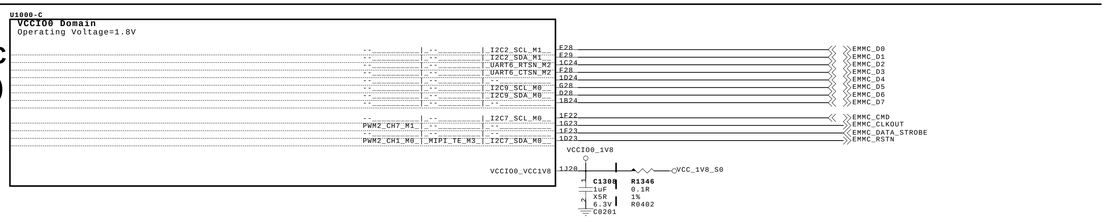
RK3576_B (UFS2.0)



RK3576_C (VCCIO0)



RK3576_D (VCCIO1)

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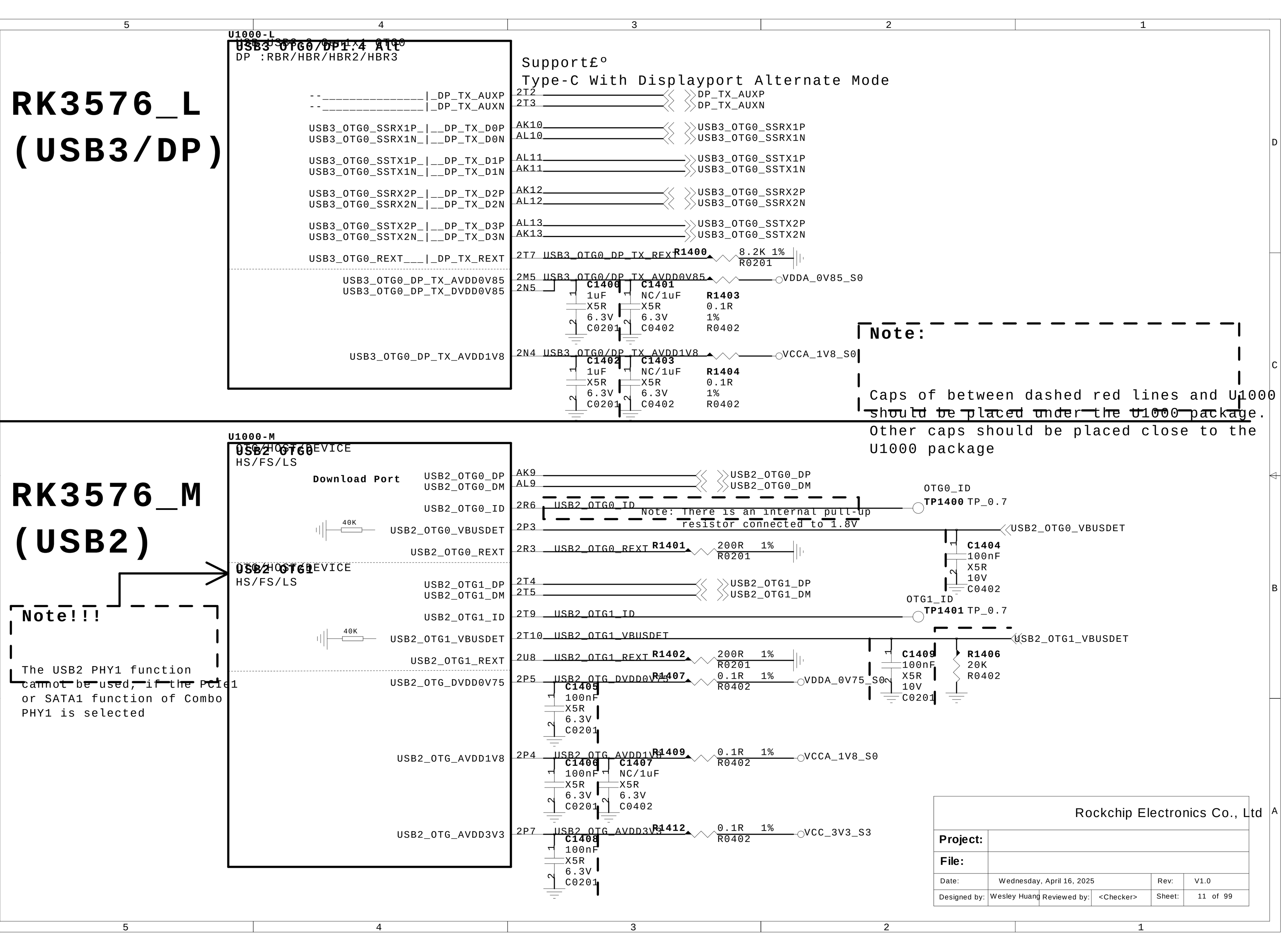
RK3576_L
(USB3/DP)
U1000-L
USB3 OTG0/DP1.4 Alt
DP :RBR/HBR/HBR2/HBR3
Support£º
Type-C With Displayport Alternate Mode
--________________|_DP_TX_AUXP
--________________|_DP_TX_AUXN
USB3_OTG0_SSRX1P_|__DP_TX_D0P
USB3_OTG0_SSRX1N_|__DP_TX_D0N
USB3_OTG0_SSTX1P_|__DP_TX_D1P
USB3_OTG0_SSTX1N_|__DP_TX_D1N
USB3_OTG0_SSRX2P_|__DP_TX_D2P
USB3_OTG0_SSRX2N_|__DP_TX_D2N
USB3_OTG0_SSTX2P_|__DP_TX_D3P
USB3_OTG0_SSTX2N_|__DP_TX_D3N
USB3_OTG0_REXT___|_DP_TX_REXT
USB3_OTG0_DP_TX_AVDD0V85
USB3_OTG0_DP_TX_DVDD0V85
USB3_OTG0_DP_TX_AVDD1V8
2T2
2T3
AK10
AL10
AL11
AK11
AK12
AL12
AL13
AK13
2T7
2M5
2N5
2N4
DP_TX_AUXP
DP_TX_AUXN
USB3_OTG0_SSRX1P
USB3_OTG0_SSRX1N
USB3_OTG0_SSTX1P
USB3_OTG0_SSTX1N
USB3_OTG0_SSRX2P
USB3_OTG0_SSRX2N
USB3_OTG0_SSTX2P
USB3_OTG0_SSTX2N
USB3_OTG0_DP_TX_REXT
R1400
8.2K 1%
R0201
USB3_OTG0/DP_TX_AVDD0V85
VDDA_0V85_S0
C1400
1uF
X5R
6.3V
C0201
C1401
NC/1uF
X5R
6.3V
C0402
R1403
0.1R
1%
R0402
USB3_OTG0/DP_TX_AVDD1V8
VCCA_1V8_S0
C1402
1uF
X5R
6.3V
C0201
C1403
NC/1uF
X5R
6.3V
C0402
R1404
0.1R
1%
R0402
Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package
RK3576_M
(USB2)
U1000-M
USB2 OTG0
OTG/HOST/DEVICE
HS/FS/LS
Download Port
USB2_OTG0_DP
USB2_OTG0_DM
USB2_OTG0_ID
USB2_OTG0_VBUSDET
USB2_OTG0_REXT
40K
USB2 OTG1
OTG/HOST/DEVICE
HS/FS/LS
USB2_OTG1_DP
USB2_OTG1_DM
USB2_OTG1_ID
USB2_OTG1_VBUSDET
USB2_OTG1_REXT
USB2_OTG_DVDD0V75
USB2_OTG_AVDD1V8
USB2_OTG_AVDD3V3
AK9
AL9
2R6
2P3
2R3
2T4
2T5
2T9
2T10
2U8
2P5
2P4
2P7
OTG0_ID
TP1400 TP_0.7
Note: There is an internal pull-up resistor connected to 1.8V
USB2_OTG0_VBUSDET
C1404
100nF
X5R
10V
C0402
R1401
200R 1%
R0201
USB2_OTG1_DP
USB2_OTG1_DM
OTG1_ID
TP1401 TP_0.7
USB2_OTG1_VBUSDET
R1402
200R 1%
R0201
C1409
100nF
X5R
10V
C0201
R1406
20K
R0402
R1407
0.1R 1%
R0402
VDDA_0V75_S0
C1405
100nF
X5R
6.3V
C0201
R1409
0.1R 1%
R0402
VCCA_1V8_S0
C1406
100nF
X5R
6.3V
C0201
C1407
NC/1uF
X5R
6.3V
C0402
R1412
0.1R 1%
R0402
VCC_3V3_S3
C1408
100nF
X5R
6.3V
C0201
Note!!!
The USB2 PHY1 function cannot be used, if the PCIe1 or SATA1 function of Combo PHY1 is selected
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RK3576_O(MIPI DCPHY)

U1000-O

MIPI DCPHY 2.5Gbps/Lane
C-PHY:V1.1 1.7Gsps/Trio

MIPI_DPHY_DSI_TX_D0N	AK15
MIPI_DPHY_DSI_TX_D0P	AL15
MIPI_DPHY_DSI_TX_D1N	AK16
MIPI_DPHY_DSI_TX_D1P	AL16
MIPI_DPHY_DSI_TX_CLKN	AK17
MIPI_DPHY_DSI_TX_CLKP	AL17
MIPI_DPHY_DSI_TX_D2N	AK18
MIPI_DPHY_DSI_TX_D2P	AL18
MIPI_DPHY_DSI_TX_D3N	AK19
MIPI_DPHY_DSI_TX_D3P	AL19

MIPI DCPHY 2.5Gbps/Lane
C-PHY:V1.1 2.5Gsps/Trio

MIPI_DPHY_CSI0_RX_D0N	AL20
MIPI_DPHY_CSI0_RX_D0P	AK20
MIPI_DPHY_CSI0_RX_D1N	AL21
MIPI_DPHY_CSI0_RX_D1P	AK21
MIPI_DPHY_CSI0_RX_CLKN	AL22
MIPI_DPHY_CSI0_RX_CLKP	AK22
MIPI_DPHY_CSI0_RX_D2N	AL23
MIPI_DPHY_CSI0_RX_D2P	AK23
MIPI_DPHY_CSI0_RX_D3N	AL24
MIPI_DPHY_CSI0_RX_D3P	AK24

MIPI_DCPHY_VREG — 2N7 MIPI_DCPHY_VREG — C1503 1uF X5R 6.3V C0201

MIPI_DCPHY_AVDD — 2M7 VDDA_0V75_S0 — C1504 1uF X5R 6.3V C0201; C1505 1uF X5R 6.3V C0402 — VDDA_0V75_S0

D-PHY 4.5Gbps & C-PHY 2.5Gsps 0.85V
D-PHY 2.5Gbps & C-PHY 1.5Gsps 0.75V

MIPI_DCPHY_AVDD1V2 — 2M8 VDDA_1V2_S0 — C1506 1uF X5R 6.3V C0201 — VDDA_1V2_S0

MIPI_DCPHY_AVDD1V8 — 2P8 VCCA_1V8_S0 — C1507 1uF X5R 6.3V C0201 — VCCA_1V8_S0

Note:

Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

RK3576_P(MIPI DPHY CSI RX)

U1000-P

MIPI DPHY CSI1/2 RX
MIPI V1.2/2.5Gbps

MIPI_DPHY_CSI1_RX_D0N	AE28
MIPI_DPHY_CSI1_RX_D0P	AE29
MIPI_DPHY_CSI1_RX_D1N	AF28
MIPI_DPHY_CSI1_RX_D1P	AF29
MIPI_DPHY_CSI1_RX_CLKN	1AC23
MIPI_DPHY_CSI1_RX_CLKP	1AC22
MIPI_DPHY_CSI1_RX_D2N	AG28
MIPI_DPHY_CSI1_RX_D2P	AG29
MIPI_DPHY_CSI1_RX_D3N	AH28
MIPI_DPHY_CSI1_RX_D3P	AH29
--	1AD22
--	1AD21

MIPI_DPHY_CSI1/2_RX_AVDD0V75 — 2L11VDDA_0V75_S0 — C1509 100nF X5R 6.3V C0201; C1501 1uF X5R 6.3V C0402 — VDDA_0V75_S0

MIPI_DPHY_CSI1/2_RX_AVDD1V8 — 1W28VCCA_1V8_S0 — C1502 1uF X5R 6.3V C0201 — VCCA_1V8_S0

MIPI DPHY CSI3/4 RX
MIPI V1.2/2.5Gbps

MIPI_DPHY_CSI3_RX_D0N	H29
MIPI_DPHY_CSI3_RX_D0P	H28
MIPI_DPHY_CSI3_RX_D1N	J29
MIPI_DPHY_CSI3_RX_D1P	J28
MIPI_DPHY_CSI3_RX_CLKN	1H23
MIPI_DPHY_CSI3_RX_CLKP	1H22
MIPI_DPHY_CSI3_RX_D2N	K29
MIPI_DPHY_CSI3_RX_D2P	K28
MIPI_DPHY_CSI3_RX_D3N	L29
MIPI_DPHY_CSI3_RX_D3P	L28
--	1K23
--	1K22

MIPI_DPHY_CSI3/4_RX_AVDD0V75 — 2D11VDDA_0V75_S0 — C1503 100nF X5R 6.3V C0201; C1508 1uF X5R 6.3V C0402 — VDDA_0V75_S0

MIPI_DPHY_CSI3/4_RX_AVDD1V8 — 2D12VCCA_1V8_S0 — C1511 1uF X5R 6.3V C0201 — VCCA_1V8_S0

Note:

Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

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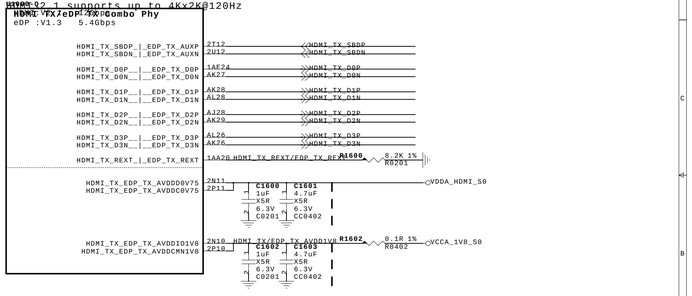
RK3576_Q(HDMI/eDP)

Note:
RK3576_Q_1 supports up to 4Kx2K@120Hz
HDMI VFx1eDP 7x4 Combo Phy
eDP :V1.3 5.4Gbps



Note:

Caps of between dashed red lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

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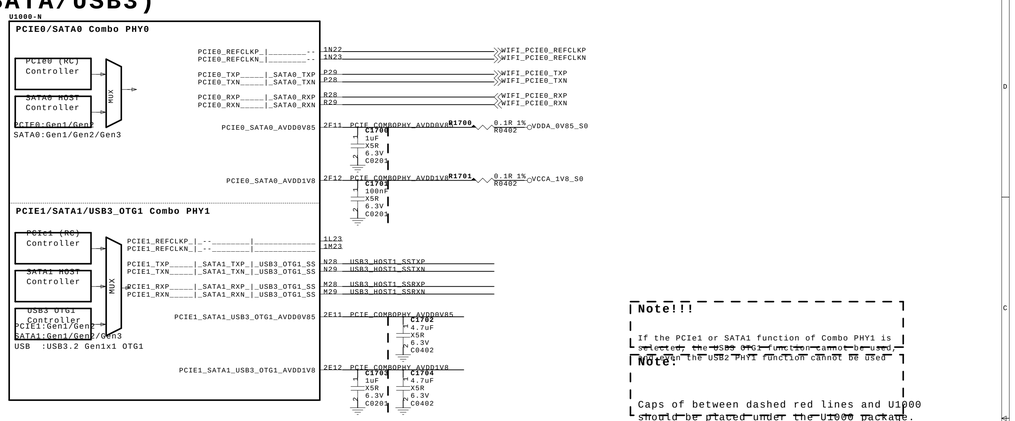
RK3576_N(PCIe/SATA/USB3)



Note!!!

If the PCIe1 or SATA1 function of Combo PHY1 is selected, the USB3 OTG function cannot be used. Meanwhile, the USB2 PHY1 function cannot be used.

Note:

Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

PCIe Port1

L: PCIe Slot;

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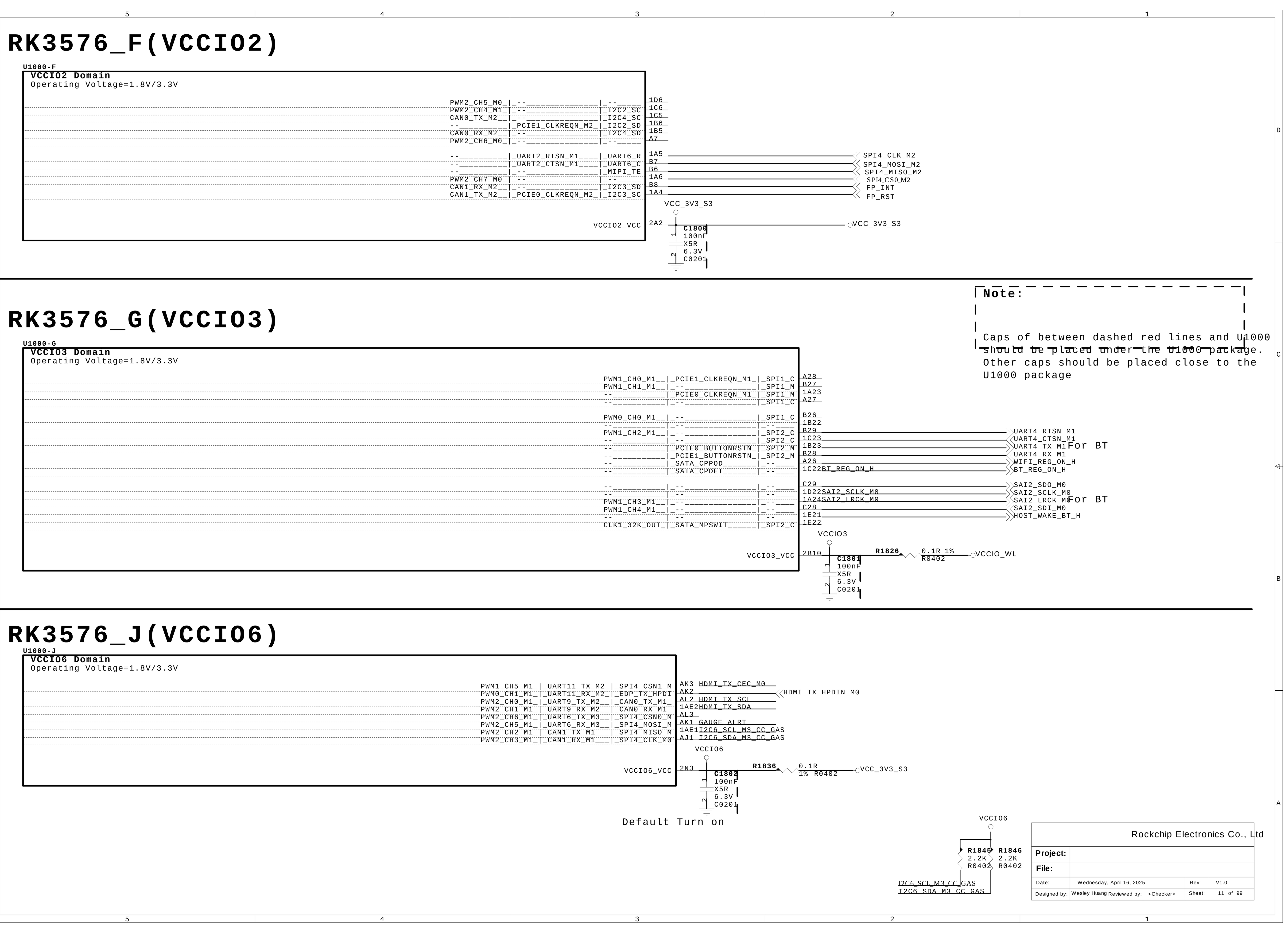
RK3576_F(VCCIO2)
U1000-F
VCCIO2 Domain
Operating Voltage=1.8V/3.3V
PWM2_CH5_M0_|_--_______________|_--_____ 1D6
PWM2_CH4_M1_|_--_______________|_I2C2_SC 1C6
CAN0_TX_M2__|_--_______________|_I2C4_SC 1C5
--__________|_PCIE1_CLKREQN_M2_|_I2C2_SD 1B6
CAN0_RX_M2__|_--_______________|_I2C4_SD 1B5
PWM2_CH6_M0_|_--_______________|_--_____ A7
--__________|_UART2_RTSN_M1____|_UART6_R 1A5 SPI4_CLK_M2
--__________|_UART2_CTSN_M1____|_UART6_C B7 SPI4_MOSI_M2
--__________|_--_______________|_MIPI_TE B6 SPI4_MISO_M2
PWM2_CH7_M0_|_--_______________|_--_____ 1A6 SPI4_CS0_M2
CAN1_RX_M2__|_--_______________|_I2C3_SD B8 FP_INT
CAN1_TX_M2__|_PCIE0_CLKREQN_M2_|_I2C3_SC 1A4 FP_RST
VCC_3V3_S3
VCCIO2_VCC 2A2 VCC_3V3_S3
C1800 100nF X5R 6.3V C0201
RK3576_G(VCCIO3)
U1000-G
VCCIO3 Domain
Operating Voltage=1.8V/3.3V
PWM1_CH0_M1__|_PCIE1_CLKREQN_M1_|_SPI1_C A28
PWM1_CH1_M1__|_--_______________|_SPI1_M B27
--___________|_PCIE0_CLKREQN_M1_|_SPI1_M 1A23
--___________|_--_______________|_SPI1_C A27
PWM0_CH0_M1__|_--_______________|_SPI1_C B26
--___________|_--_______________|_--____ 1B22
PWM1_CH2_M1__|_--_______________|_SPI2_C B29 UART4_RTSN_M1
--___________|_--_______________|_SPI2_C 1C23 UART4_CTSN_M1
--___________|_PCIE0_BUTTONRSTN_|_SPI2_M 1B23 UART4_TX_M1 For BT
--___________|_PCIE1_BUTTONRSTN_|_SPI2_M B28 UART4_RX_M1
--___________|_SATA_CPPOD_______|_--____ A26 WIFI_REG_ON_H
--___________|_SATA_CPDET_______|_--____ 1C22 BT_REG_ON_H BT_REG_ON_H
--___________|_--_______________|_--____ C29 SAI2_SDO_M0
--___________|_--_______________|_--____ 1D22 SAI2_SCLK_M0 SAI2_SCLK_M0
PWM1_CH3_M1__|_--_______________|_--____ 1A24 SAI2_LRCK_M0 SAI2_LRCK_M0 For BT
PWM1_CH4_M1__|_--_______________|_--____ C28 SAI2_SDI_M0
--___________|_--_______________|_--____ 1E21 HOST_WAKE_BT_H
CLK1_32K_OUT_|_SATA_MPSWIT______|_SPI2_C 1E22
VCCIO3
VCCIO3_VCC 2B10 R1826 0.1R 1% R0402 VCCIO_WL
C1801 100nF X5R 6.3V C0201
Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package
RK3576_J(VCCIO6)
U1000-J
VCCIO6 Domain
Operating Voltage=1.8V/3.3V
PWM1_CH5_M1_|_UART11_TX_M2_|_SPI4_CSN1_M AK3 HDMI_TX_CEC_M0
PWM0_CH1_M1_|_UART11_RX_M2_|_EDP_TX_HPDI AK2 HDMI_TX_HPDIN_M0
PWM2_CH0_M1_|_UART9_TX_M2__|_CAN0_TX_M1_ AL2 HDMI_TX_SCL
PWM2_CH1_M1_|_UART9_RX_M2__|_CAN0_RX_M1_ 1AE2 HDMI_TX_SDA
PWM2_CH6_M1_|_UART6_TX_M3__|_SPI4_CSN0_M AL3
PWM2_CH5_M1_|_UART6_RX_M3__|_SPI4_MOSI_M AK1 GAUGE_ALRT
PWM2_CH2_M1_|_CAN1_TX_M1___|_SPI4_MISO_M 1AE1 I2C6_SCL_M3_CC_GAS
PWM2_CH3_M1_|_CAN1_RX_M1___|_SPI4_CLK_M0 AJ1 I2C6_SDA_M3_CC_GAS
VCCIO6
VCCIO6_VCC 2N3 R1836 0.1R 1% R0402 VCC_3V3_S3
C1802 100nF X5R 6.3V C0201
Default Turn on
VCCIO6
R1845 2.2K R0402
R1846 2.2K R0402
I2C6_SCL_M3_CC_GAS
I2C6_SDA_M3_CC_GAS
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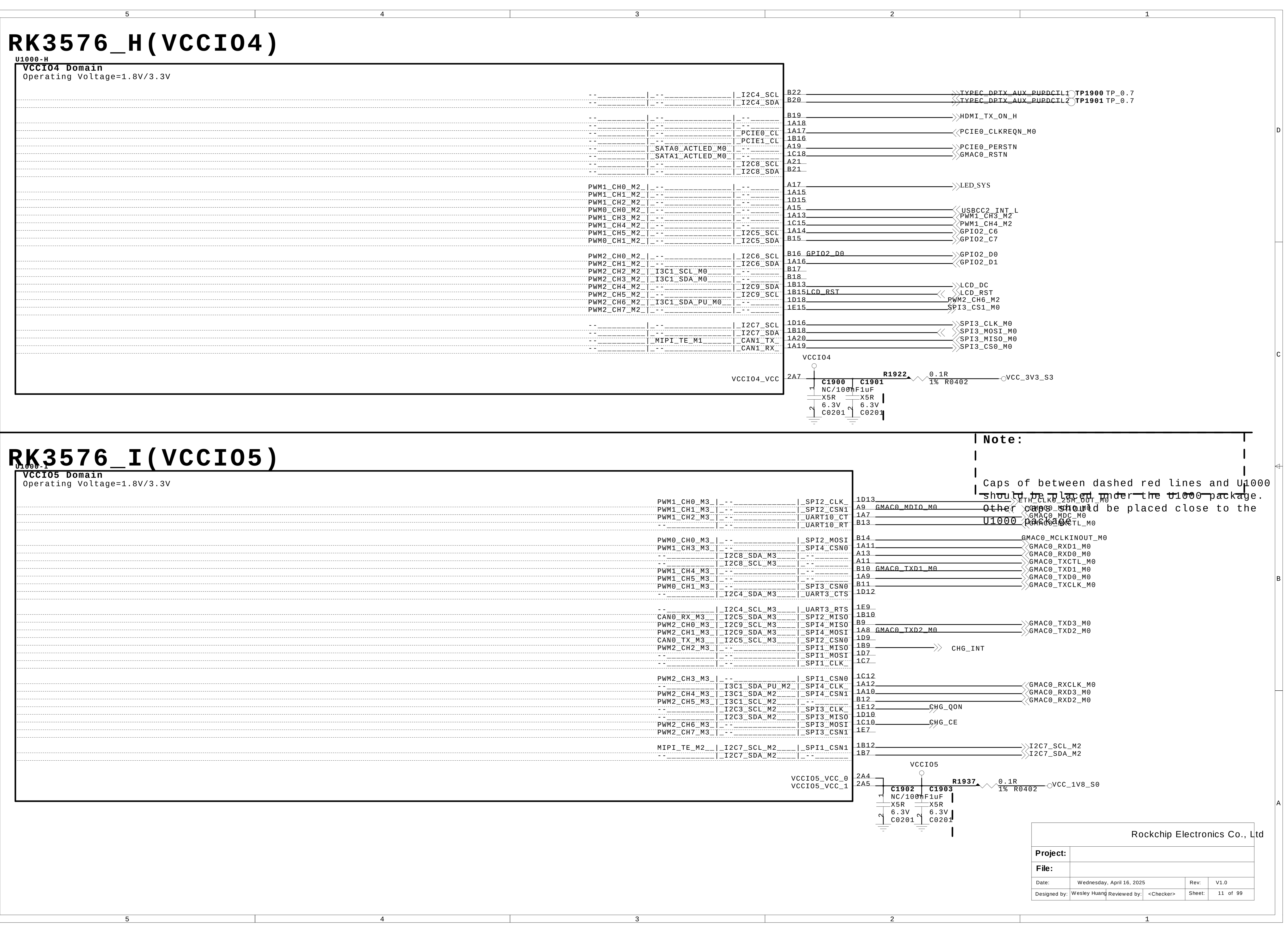

RK3576_H(VCCIO4)
U1000-H
VCCIO4 Domain
Operating Voltage=1.8V/3.3V
TYPEC_DPTX_AUX_PUPDCTL1
TYPEC_DPTX_AUX_PUPDCTL2
TP1900 TP_0.7
TP1901 TP_0.7
HDMI_TX_ON_H
PCIE0_CLKREQN_M0
PCIE0_PERSTN
GMAC0_RSTN
LED_SYS
USBCC2_INT_L
PWM1_CH3_M2
PWM1_CH4_M2
GPIO2_C6
GPIO2_C7
GPIO2_D0
GPIO2_D1
LCD_DC
LCD_RST
PWM2_CH6_M2
SPI3_CS1_M0
SPI3_CLK_M0
SPI3_MOSI_M0
SPI3_MISO_M0
SPI3_CS0_M0
VCCIO4
VCCIO4_VCC
R1922 0.1R 1% R0402
VCC_3V3_S3
C1900 NC/100nF X5R 6.3V C0201
C1901 1uF X5R 6.3V C0201
RK3576_I(VCCIO5)
U1000-I
VCCIO5 Domain
Operating Voltage=1.8V/3.3V
Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package.
GMAC0_MDIO_M0
GMAC0_MDC_M0
GMAC0_MCLKINOUT_M0
GMAC0_RXD1_M0
GMAC0_RXD0_M0
GMAC0_TXCTL_M0
GMAC0_TXD1_M0
GMAC0_TXD0_M0
GMAC0_TXCLK_M0
GMAC0_TXD3_M0
GMAC0_TXD2_M0
CHG_INT
GMAC0_RXCLK_M0
GMAC0_RXD3_M0
GMAC0_RXD2_M0
CHG_QON
CHG_CE
I2C7_SCL_M2
I2C7_SDA_M2
VCCIO5
VCCIO5_VCC_0
VCCIO5_VCC_1
R1937 0.1R 1% R0402
VCC_1V8_S0
C1902 NC/100nF X5R 6.3V C0201
C1903 1uF X5R 6.3V C0201
Rockchip Electronics Co., Ltd
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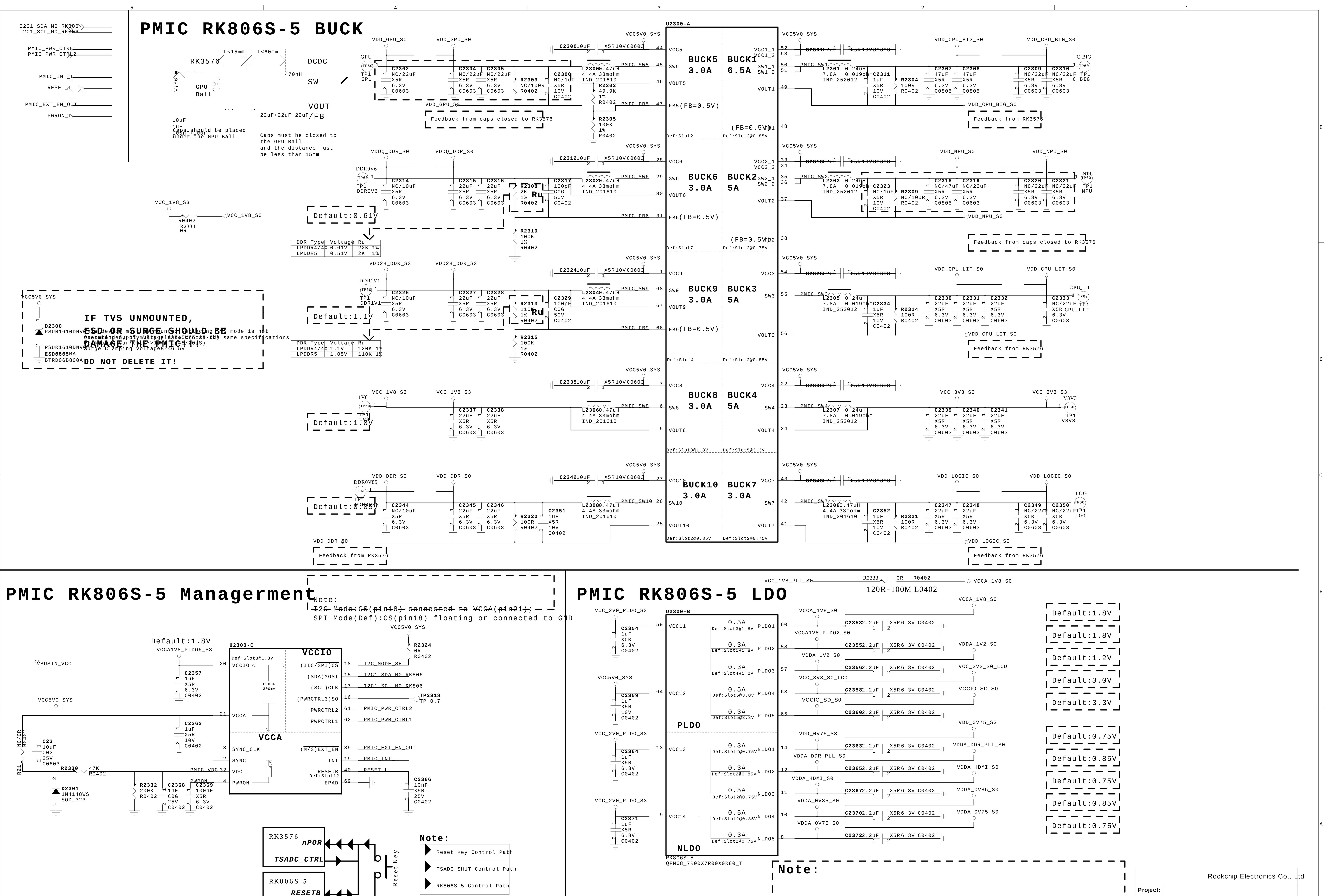

Note:

The RK806 LDO power distribution of the reference chematics is only suitable for the interface used in the reference schematics.
If other interface functions are to be added to the reference schematics, the RK806 LDO distribution needs to be re evaluated, otherwise the added functions may exceed the maximum current provided by the LDO

LPDDR5

U3900-A

CH A			CH B
LPDDR5_DQ0_A	D1	DQ0_A	DQ0_B	V15	LPDDR5_DQ0_B
LPDDR5_DQ1_A	C2	DQ1_A	DQ1_B	W14	LPDDR5_DQ1_B
LPDDR5_DQ2_A	F2	DQ2_A	DQ2_B	U14	LPDDR5_DQ2_B
LPDDR5_DQ3_A	D3	DQ3_A	DQ3_B	V13	LPDDR5_DQ3_B
LPDDR5_DQ4_A	B5	DQ4_A	DQ4_B	Y11	LPDDR5_DQ4_B
LPDDR5_DQ5_A	C6	DQ5_A	DQ5_B	W10	LPDDR5_DQ5_B
LPDDR5_DQ6_A	E6	DQ6_A	DQ6_B	U10	LPDDR5_DQ6_B
LPDDR5_DQ7_A	F5	DQ7_A	DQ7_B	T11	LPDDR5_DQ7_B
LPDDR5_RDQS0P_A	A3	RDQS0_T_A	RDQS0_T_B	Y13	LPDDR5_RDQS0P_B
LPDDR5_RDQS0N_A	C4	RDQS0_C_A	RDQS0_C_B	W12	LPDDR5_RDQS0N_B
LPDDR5_DMI0_A	A4	DMI0_A	DMI0_B	AA12	LPDDR5_DMI0_B
LPDDR5_WCK0P_A	E4	WCK0_T_A	WCK0_T_B	U12	LPDDR5_WCK0P_B
LPDDR5_WCK0N_A	D5	WCK0_C_A	WCK0_C_B	V11	LPDDR5_WCK0N_B
LPDDR5_DQ8_A	D15	DQ8_A	DQ8_B	V1	LPDDR5_DQ8_B
LPDDR5_DQ9_A	C14	DQ9_A	DQ9_B	W2	LPDDR5_DQ9_B
LPDDR5_DQ10_A	E14	DQ10_A	DQ10_B	U2	LPDDR5_DQ10_B
LPDDR5_DQ11_A	D13	DQ11_A	DQ11_B	V3	LPDDR5_DQ11_B
LPDDR5_DQ12_A	B13	DQ12_A	DQ12_B	Y5	LPDDR5_DQ12_B
LPDDR5_DQ13_A	C16	DQ13_A	DQ13_B	W6	LPDDR5_DQ13_B
LPDDR5_DQ14_A	E16	DQ14_A	DQ14_B	U6	LPDDR5_DQ14_B
LPDDR5_DQ15_A	F11	DQ15_A	DQ15_B	T5	LPDDR5_DQ15_B
LPDDR5_RDQS1P_A	B13	RDQS1_T_A	RDQS1_T_B	Y3	LPDDR5_RDQS1P_B
LPDDR5_RDQS1N_A	A12	RDQS1_C_A	RDQS1_C_B	W4	LPDDR5_RDQS1N_B
LPDDR5_DMI1_A	A12	DMI1_A	DMI1_B	AA4	LPDDR5_DMI1_B
LPDDR5_WCK1P_A	E11	WCK1_T_A	WCK1_T_B	U4	LPDDR5_WCK1P_B
LPDDR5_WCK1N_A	D11	WCK1_C_A	WCK1_C_B	V5	LPDDR5_WCK1N_B
LPDDR5_A0_A	G4	CA0_A	CA0_B	R12	LPDDR5_A0_B
LPDDR5_A1_A	H5	CA1_A	CA1_B	P11	LPDDR5_A1_B
LPDDR5_A2_A	G8	CA2_A	CA2_B	R8	LPDDR5_A2_B
LPDDR5_A3_A	H11	CA3_A	CA3_B	P5	LPDDR5_A3_B
LPDDR5_A4_A	G10	CA4_A	CA4_B	R6	LPDDR5_A4_B
LPDDR5_A5_A	H11	CA5_A	CA5_B	P3	LPDDR5_A5_B
LPDDR5_A6_A	G12	CA6_A	CA6_B	R4	LPDDR5_A6_B
LPDDR5_CLKP_A	H9	CK_T_A	CK_T_B	P7	LPDDR5_CLKP_B
LPDDR5_CLKN_A	J9	CK_C_A	CK_C_B	N7	LPDDR5_CLKN_B
LPDDR5_CS0_A	H7	CS0_A	CS0_B	P9	LPDDR5_CS0_B
LPDDR5_CS1_A	G6	CS1_A	CS1_B	R10	LPDDR5_CS1_B
ZQ_A	H15		RESET_N	H1	LPDDR5_RESET

LPDDR5_DQ0_A … LPDDR5_DQ7_A
LPDDR5_RDQS0P_A
LPDDR5_RDQS0N_A
LPDDR5_DMI0_A
LPDDR5_DQ8_A … LPDDR5_DQ15_A
LPDDR5_RDQS1P_A
LPDDR5_RDQS1N_A
LPDDR5_DMI1_A
LPDDR5_A0_A … LPDDR5_A6_A
LPDDR5_WCK1P_A
LPDDR5_WCK1N_A
LPDDR5_CLKP_A
LPDDR5_CLKN_A
LPDDR5_CS0_A
LPDDR5_CS1_A
LPDDR5_RESET

LPDDR5_DQ0_B … LPDDR5_DQ7_B
LPDDR5_RDQS0P_B
LPDDR5_RDQS0N_B
LPDDR5_DMI0_B
LPDDR5_WCK0P_B
LPDDR5_WCK0N_B
LPDDR5_DQ8_B … LPDDR5_DQ15_B
LPDDR5_RDQS1P_B
LPDDR5_RDQS1N_B
LPDDR5_DMI1_B
LPDDR5_A0_B … LPDDR5_A6_B
LPDDR5_WCK1P_B
LPDDR5_WCK1N_B
LPDDR5_CLKP_B
LPDDR5_CLKN_B
LPDDR5_CS0_B
LPDDR5_CS1_B

VDDQ_DDR_S0 — R3900 240R 1% R0201 — H15 ZQ_A

U3900-B

VDD2H_DDR_S3	A7	VDD2H_1	VDD2L_1	A6	VDD2L_0V9_DDR_S3
	A8	VDD2H_2	VDD2L_2	A10	
	A9	VDD2H_3	VDD2L_3	B6	
	B7	VDD2H_4	VDD2L_4	B10	
	B8	VDD2H_5	VDD2L_5	H14	
	C7	VDD2H_6	VDD2L_6	J12	
	C8	VDD2H_7	VDD2L_7	J14	
	D8	VDD2H_8	VDD2L_8	J16	
	E7	VDD2H_9	VDD2L_9	N2	
	E9	VDD2H_10	VDD2L_10	N14	
	F6	VDD2H_11	VDD2L_11	P2	
	F7	VDD2H_12	VDD2L_12	P14	
	F9	VDD2H_13	VDD2L_13	Y6	
	F10	VDD2H_14	VDD2L_14	Y10	
	J5	VDD2H_15	VDD2L_15	AA6	
	J11	VDD2H_16	VDD2L_16	AA10	
	K1	VDD2H_17	VDDQ		
	K2	VDD2H_18			
	K3	VDD2H_19			
	K4	VDD2H_20	VDDQ_1	A3	
	K5	VDD2H_21	VDDQ_2	A13	
	K6	VDD2H_22	VDDQ_3	B2	
	K10	VDD2H_23	VDDQ_4	B14	
	K11	VDD2H_24	VDDQ_5	C3	
	K12	VDD2H_25	VDDQ_6	C13	
	K13	VDD2H_26	VDDQ_7	D4	
	K14	VDD2H_27	VDDQ_8	D12	
	K15	VDD2H_28	VDDQ_9	E5	
	L6	VDD2H_29	VDDQ_10	E11	
	L7	VDD2H_30	VDDQ_11	F1	
	L8	VDD2H_31	VDDQ_12	F3	
	L9	VDD2H_32	VDDQ_13	F4	
	L10	VDD2H_33	VDDQ_14	F12	
	M1	VDD2H_34	VDDQ_15	F13	
	M2	VDD2H_35	VDDQ_16	F15	
	M3	VDD2H_36	VDDQ_17	G1	
	M4	VDD2H_37	VDDQ_18	G2	
	M5	VDD2H_38	VDDQ_19	G14	
	M6	VDD2H_39	VDDQ_20	G15	
	M10	VDD2H_40	VDDQ_21	R1	
	M11	VDD2H_41	VDDQ_22	R2	
	M12	VDD2H_42	VDDQ_23	R14	
	M13	VDD2H_43	VDDQ_24	R15	
	N14	VDD2H_44	VDDQ_25	T1	
	M15	VDD2H_45	VDDQ_26	T3	
	N5	VDD2H_46	VDDQ_27	T4	
	N11	VDD2H_47	VDDQ_28	T12	
	T6	VDD2H_48	VDDQ_29	T13	
	T7	VDD2H_49	VDDQ_30	T15	
	T9	VDD2H_50	VDDQ_31	U5	
	T10	VDD2H_51	VDDQ_32	U11	
	U7	VDD2H_52	VDDQ_33	V4	
	U9	VDD2H_53	VDDQ_34	V12	
	V8	VDD2H_54	VDDQ_35	W3	
	W7	VDD2H_55	VDDQ_36	W13	
	W9	VDD2H_56	VDDQ_37	Y2	
	Y7	VDD2H_57	VDDQ_38	Y14	
	Y9	VDD2H_58	VDDQ_39	AA3	
	AA7	VDD2H_59	VDDQ_40	AA13	
	AA8	VDD2H_60			
	AA9	VDD2H_61			
	J4	RFU_1	VDD1		
	J6	RFU_2	VDD1_1	C1	VDD1_1V8_DDR_S3
	P1	RFU_3	VDD1_2	C15	
	P15	RFU_4	VDD1_3	W1	
	B15	NC_6	VDD1_4	W15	
	B1	NC_5	NC_7	Y1	
	A15	NC_4	NC_8	Y15	
	A14	NC_3	NC_9	AA1	
	A2	NC_2	NC_10	AA2	
	A1	NC_1	NC_11	AA14	
			NC_12	AA15	

U3900-C

A5	VSS_1	VSS_102	AA11
A11	VSS_2	VSS_101	AA5
B4	VSS_3	VSS_100	V12
B8	VSS_4	VSS_99	V8
B12	VSS_5	VSS_98	V4
C5	VSS_6	VSS_97	W11
C6	VSS_7	VSS_96	W8
C11	VSS_8	VSS_95	W5
D2	VSS_9	VSS_94	W14
D6	VSS_10	VSS_93	V10
D7	VSS_11	VSS_92	V9
D9	VSS_12	VSS_91	V7
D10	VSS_13	VSS_90	V6
D14	VSS_14	VSS_89	V2
E1	VSS_15	VSS_88	U15
E3	VSS_16	VSS_87	U13
E8	VSS_17	VSS_86	U8
E13	VSS_18	VSS_85	U3
F15	VSS_19	VSS_84	U1
F2	VSS_20	VSS_83	T14
F8	VSS_21	VSS_82	T8
F14	VSS_22	VSS_81	T2
G3	VSS_23	VSS_80	R13
G5	VSS_24	VSS_79	R11
G7	VSS_25	VSS_78	R9
G9	VSS_26	VSS_77	R7
G11	VSS_27	VSS_76	R5
G13	VSS_28	VSS_75	R3
H3	VSS_29	VSS_74	P13
H4	VSS_30	VSS_73	P12
H6	VSS_31	VSS_72	P10
H8	VSS_32	VSS_71	P8
H10	VSS_33	VSS_70	P6
H12	VSS_34	VSS_69	P4
J1	VSS_35	VSS_68	N15
J3	VSS_36	VSS_67	N13
J7	VSS_37	VSS_66	N12
J8	VSS_38	VSS_65	N10
J10	VSS_39	VSS_64	N9
J12	VSS_40	VSS_63	N8
J13	VSS_41	VSS_62	N6
J15	VSS_42	VSS_61	N4
K7	VSS_43	VSS_60	N3
K8	VSS_44	VSS_59	N1
K9	VSS_45	VSS_58	M9
L1	VSS_46	VSS_57	M8
L2	VSS_47	VSS_56	M7
L3	VSS_48	VSS_55	L15
L4	VSS_49	VSS_54	L14
L5	VSS_50	VSS_53	L13
L11	VSS_51	VSS_52	L12

LPS_B315
BGA315_12R40X15R00X1R10

C3900 NC/1nF X5R 25V C0201

VDD2H_DDR_S3 — C3906 22uF X5R 6.3V C0603; C3907 10uF X5R 6.3V C0603; C3908 10uF X5R 6.3V C0603; C3909 100nF X5R 6.3V C0201; C3910 100nF X5R 6.3V C0201; C3911 NC/100nF X5R 6.3V C0201; C3912 100nF X5R 6.3V C0201; C3913 100nF X5R 6.3V C0201; C3914 100nF X5R 6.3V C0201; C3915 100nF X5R 6.3V C0201; C3916 100nF X5R 6.3V C0201; C3917 NC/100nF X5R 6.3V C0201; C3918 100nF X5R 6.3V C0201; C3919 100nF X5R 6.3V C0201; C3920 100nF X5R 6.3V C0201; C3921 100nF X5R 6.3V C0201; C3922 100nF X5R 6.3V C0201; C3923 100nF X5R 6.3V C0201; C3924 100nF X5R 6.3V C0201; C3925 100nF X5R 6.3V C0201

VDD2H_DDR_S3 — C3926 22uF X5R 6.3V C0603; C3927 10uF X5R 6.3V C0603; C3928 10uF X5R 6.3V C0603; C3929 1uF X5R 6.3V C0201; C3930 100nF X5R 6.3V C0201; C3931 NC/100nF X5R 6.3V C0201; C3932 100nF X5R 6.3V C0201; C3933 100nF X5R 6.3V C0201; C3934 100nF X5R 6.3V C0201; C3935 100nF X5R 6.3V C0201; C3936 NC/100nF X5R 6.3V C0201; C3937 NC/100nF X5R 6.3V C0201; C3938 100nF X5R 6.3V C0201; C3939 NC/100nF X5R 6.3V C0201; C3940 NC/100nF X5R 6.3V C0201; C3941 100nF X5R 6.3V C0201; C3942 100nF X5R 6.3V C0201; C3943 100nF X5R 6.3V C0201; C3944 100nF X5R 6.3V C0201; C3945 NC/100nF X5R 6.3V C0201; C3946 NC/100nF X5R 6.3V C0201; C3947 NC/100nF X5R 6.3V C0201; C3948 100nF X5R 6.3V C0201; C3949 100nF X5R 6.3V C0201; C3950 100nF X5R 6.3V C0201; C3951 100nF X5R 6.3V C0201; C3952 100nF X5R 6.3V C0201; C3953 100nF X5R 6.3V C0201; C3954 100nF X5R 6.3V C0201; C3955 100nF X5R 6.3V C0201; C3956 100nF X5R 6.3V C0201; C3957 100nF X5R 6.3V C0201; C3958 100nF X5R 6.3V C0201; C3959 100nF X5R 6.3V C0201; C3960 100nF X5R 6.3V C0201; C3961 100nF X5R 6.3V C0201; C3962 100nF X5R 6.3V C0201; C3963 NC/100nF X5R 6.3V C0201; C3964 100nF X5R 6.3V C0201; C3965 100nF X5R 6.3V C0201; C3966 100nF X5R 6.3V C0201; C3967 100nF X5R 6.3V C0201; C3968 100nF X5R 6.3V C0201

VDD1_1V8_DDR_S3 — C3970 10uF X5R 10V C0603; R3904 0R R0603; C3902 4.7uF X5R 6.3V C0402; C3903 1uF X5R 6.3V C0201; C3905 1uF X5R 6.3V C0201; C3904 100nF X5R 6.3V C0201

VDDQ_DDR_CKE_S3 — R3906 0R R0603; C3901 NC/1uF X5R6.3V C0201

VDDQ_DDR_S0 — C3906 22uF X5R 6.3V C0603; C3907 10uF X5R 6.3V C0603; C3908 10uF X5R 6.3V C0603; C3909 100nF X5R 6.3V C0201; C3910 100nF X5R 6.3V C0201; C3911 NC/100nF X5R 6.3V C0201; C3912 100nF X5R 6.3V C0201; C3913 100nF X5R 6.3V C0201; C3914 100nF X5R 6.3V C0201; C3915 100nF X5R 6.3V C0201; C3916 100nF X5R 6.3V C0201; C3917 NC/100nF X5R 6.3V C0201; C3918 100nF X5R 6.3V C0201; C3919 100nF X5R 6.3V C0201; C3920 100nF X5R 6.3V C0201; C3921 100nF X5R 6.3V C0201; C3922 100nF X5R 6.3V C0201; C3923 100nF X5R 6.3V C0201; C3924 100nF X5R 6.3V C0201; C3925 100nF X5R 6.3V C0201

VDD2H_DDR_S3 — C3926 22uF X5R 6.3V C0603; C3927 10uF X5R 6.3V C0603; C3928 10uF X5R 6.3V C0603; C3929 1uF X5R 6.3V C0201; C3930 100nF X5R 6.3V C0201; C3931 NC/100nF X5R 6.3V C0201; C3932 100nF X5R 6.3V C0201; C3933 100nF X5R 6.3V C0201; C3934 100nF X5R 6.3V C0201; C3935 100nF X5R 6.3V C0201; C3936 NC/100nF X5R 6.3V C0201; C3937 NC/100nF X5R 6.3V C0201; C3938 100nF X5R 6.3V C0201; C3939 NC/100nF X5R 6.3V C0201; C3940 NC/100nF X5R 6.3V C0201; C3941 100nF X5R 6.3V C0201; C3942 100nF X5R 6.3V C0201; C3943 100nF X5R 6.3V C0201; C3944 100nF X5R 6.3V C0201; C3945 NC/100nF X5R 6.3V C0201; C3946 NC/100nF X5R 6.3V C0201; C3947 NC/100nF X5R 6.3V C0201; C3948 100nF X5R 6.3V C0201; C3949 100nF X5R 6.3V C0201; C3950 100nF X5R 6.3V C0201; C3951 100nF X5R 6.3V C0201; C3952 100nF X5R 6.3V C0201; C3953 100nF X5R 6.3V C0201; C3954 100nF X5R 6.3V C0201; C3955 100nF X5R 6.3V C0201; C3956 100nF X5R 6.3V C0201; C3957 100nF X5R 6.3V C0201; C3958 100nF X5R 6.3V C0201; C3959 100nF X5R 6.3V C0201; C3960 100nF X5R 6.3V C0201; C3961 100nF X5R 6.3V C0201; C3962 100nF X5R 6.3V C0201; C3963 NC/100nF X5R 6.3V C0201; C3964 100nF X5R 6.3V C0201; C3965 100nF X5R 6.3V C0201; C3966 100nF X5R 6.3V C0201; C3967 100nF X5R 6.3V C0201; C3968 100nF X5R 6.3V C0201

VCC5V0_SYS — U3901 TPS3123Z2N-2A 3A peak; VIN, GND, EN, FB/OUT, LX; L3900 2.2uH IND_252010 2.10A 0.04ohm; C3957 100pF C0G 50V C0402; R3901 100K 1% R0402; R3902 56K R0402; R3903 200K 1% R0402; C3958 10uF X5R 6.3V C0603; C3959 NC/10nR0T_23.5 C0G25V C0402; C3956 10uF X5R 25V C0805; VCC_3V3_S3

RC for sequence: VDD2H>=VDD2L>=VDDQ

FB=0.6V
Default:0.9V

VDD2L_0V9_DDR_S3 — C3960 22uF X5R 6.3V C0603; C3961 1uF X5R 6.3V C0201; C3962 100nF X5R 6.3V C0201; C3963 NC/100nF X5R 6.3V C0201; C3964 100nF X5R 6.3V C0201; C3965 100nF X5R 6.3V C0201; C3966 100nF X5R 6.3V C0201; C3967 100nF X5R 6.3V C0201; C3968 100nF X5R 6.3V C0201

Note:

Power Sequence: VDD1>VDD2H>=VDD2L>VDDQ-200mV

VDD1: 1.70V--1.95V,Power for core1.

VDD2H: 1.01V--1.17V,Power for core2 and Input Buffer.

VDD2L: 0.87V--0.97V,Power for core2 and Input Buffer.

VDDQ: 0.47V--0.57V,Power for I/O Buffer.

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Project:	
File:	
Date: Wednesday, April 16, 2025	Rev: V1.0
Designed by: Wesley Huang	Reviewed by: <Checker>
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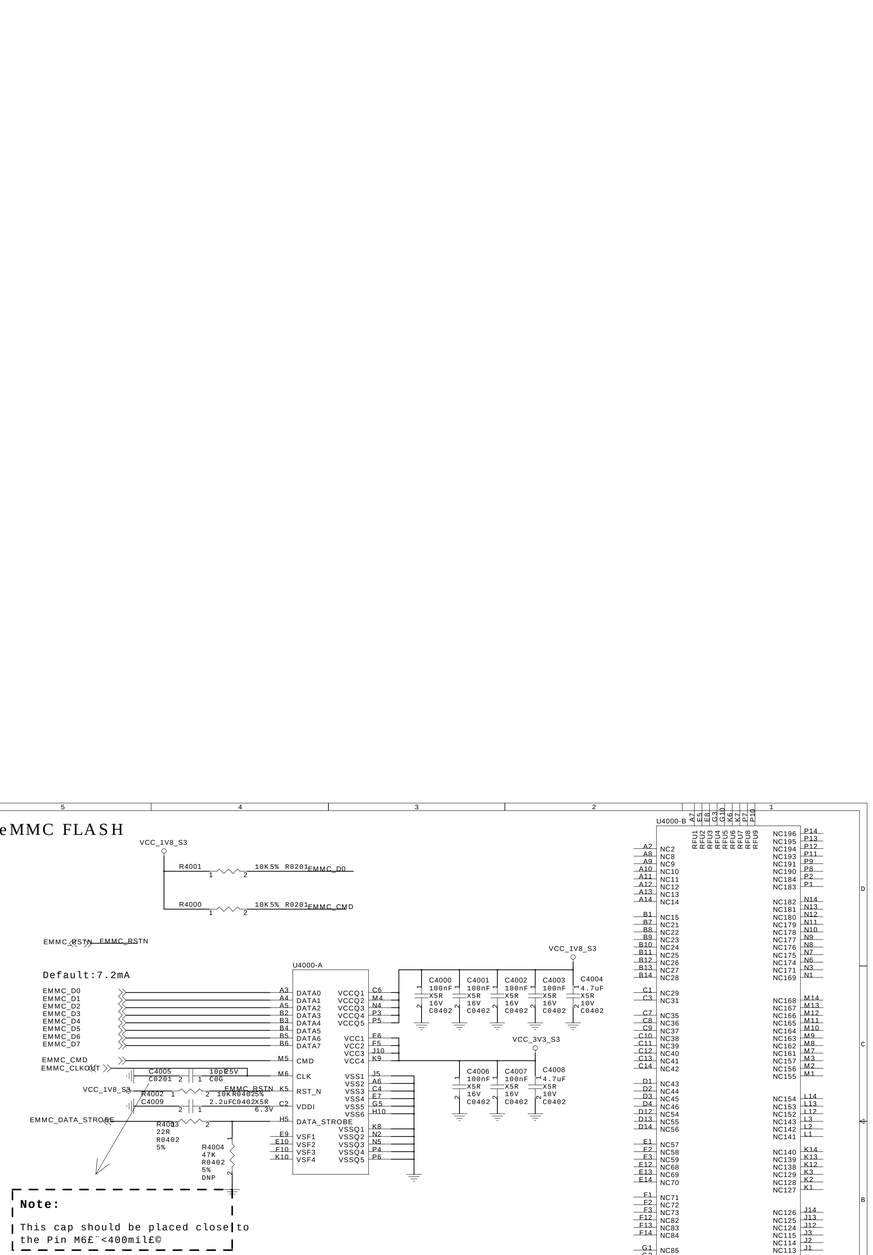
eMMC FLASH



Note:

This cap should be placed close to the Pin M6£¨<400mil£©

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Project:					
File:					
Date:	Monday, February 27, 2023			Rev.	V1.3
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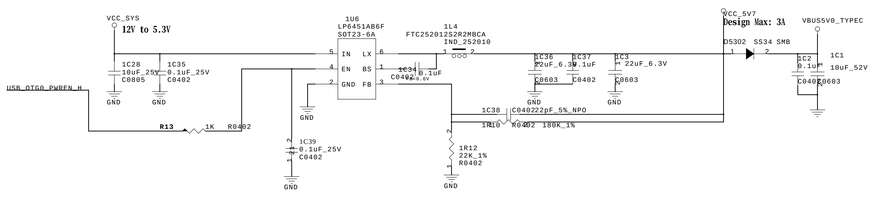
CC

Note:			
Different models of CC chips may require different driver software.		AW35615(Default)	HUSB311(Option)
	7bit address	0x22	0x4E
	VBUS	4V-21V,TYP=5V	4V-21V,TYP=5V
	VDD	2.7V~5.5V,TYP=3.3V	3V-5.5V,TYP=3.3V
	VCONN	2.7V~5.5V	3V-5.5V

TYPEC

With Displayport Alt Mode

This is also the firmware download interface



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Project:			
File:			
Date:	Friday, March 28, 2025	Rev.	V1.3
Designed by:	Westley Huang	Reviewed by:	<Checker>
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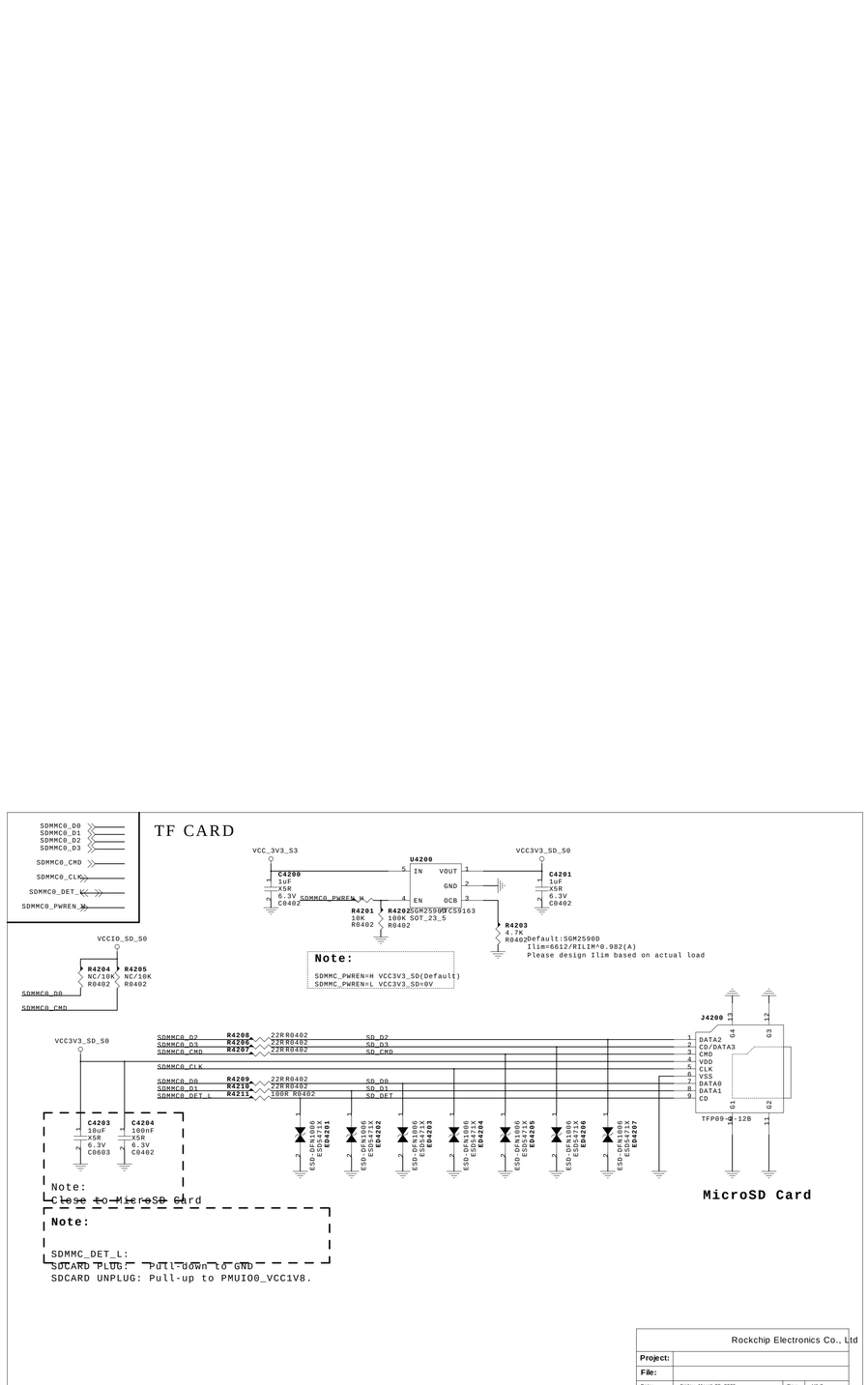
TF CARD



Rockchip Electronics Co., Ltd			
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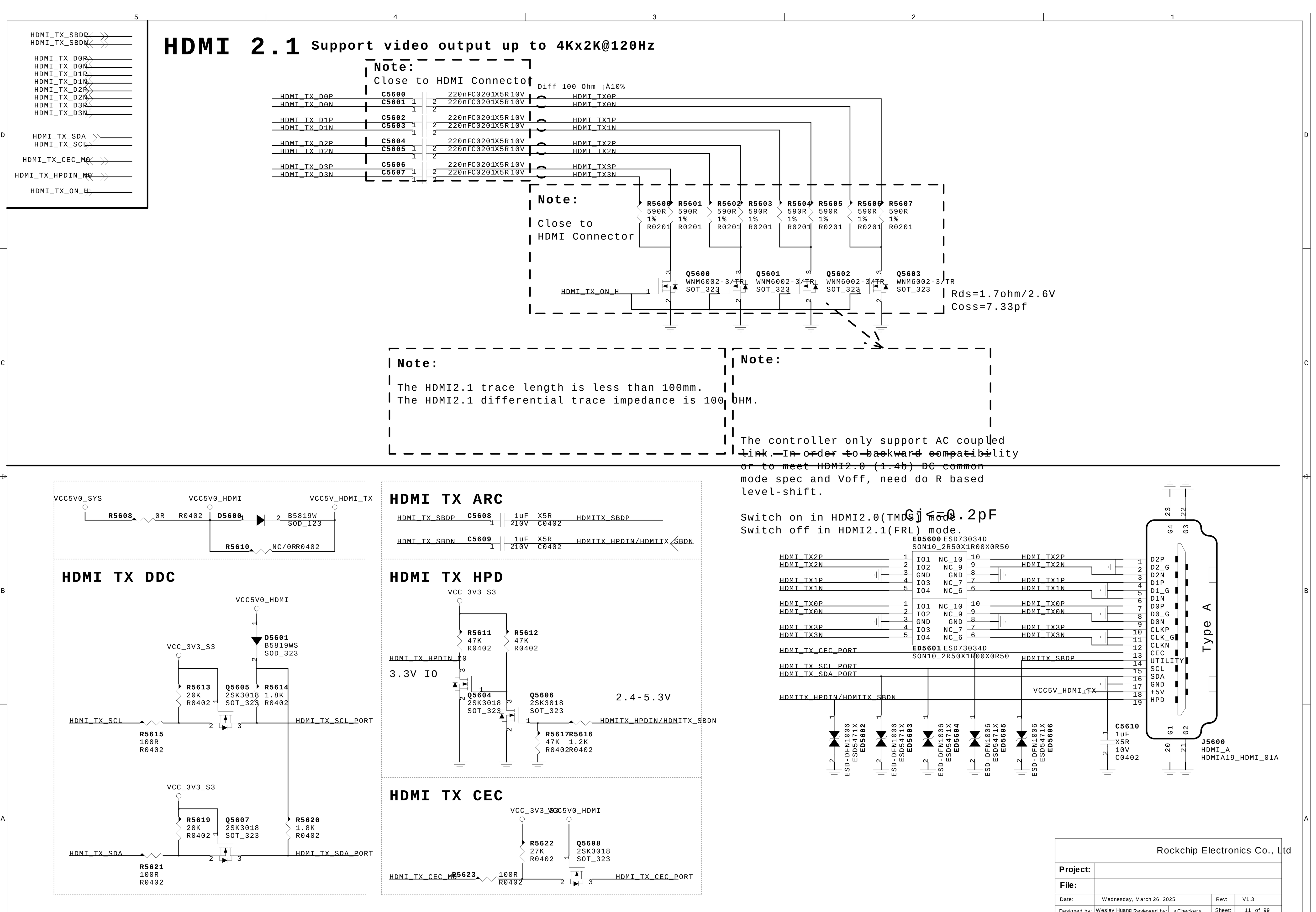
Designed by:	Wesley Huang	Reviewed by: <Checker>	Sheet: 11 of 99


HDMI 2.1
Support video output up to 4Kx2K@120Hz
Note:
Close to HDMI Connector
Diff 100 Ohm ¡À10%
HDMI_TX_SBDP
HDMI_TX_SBDN
HDMI_TX_D0P
HDMI_TX_D0N
HDMI_TX_D1P
HDMI_TX_D1N
HDMI_TX_D2P
HDMI_TX_D2N
HDMI_TX_D3P
HDMI_TX_D3N
HDMI_TX_SDA
HDMI_TX_SCL
HDMI_TX_CEC_M0
HDMI_TX_HPDIN_M0
HDMI_TX_ON_H
C5600 C5601 C5602 C5603 C5604 C5605 C5606 C5607 220nFC0201X5R10V
HDMI_TX0P HDMI_TX0N HDMI_TX1P HDMI_TX1N HDMI_TX2P HDMI_TX2N HDMI_TX3P HDMI_TX3N
Note:
Close to
HDMI Connector
R5600 R5601 R5602 R5603 R5604 R5605 R5606 R5607 590R 1% R0201
Q5600 Q5601 Q5602 Q5603 WNM6002-3/TR SOT_323
Rds=1.7ohm/2.6V
Coss=7.33pf
Note:
The HDMI2.1 trace length is less than 100mm.
The HDMI2.1 differential trace impedance is 100 OHM.
Note:
The controller only support AC coupled
link. In order to backward compatibility
or to meet HDMI2.0 (1.4b) DC common
mode spec and Voff, need do R based
level-shift.
Switch on in HDMI2.0(TMDS) mode.
Switch off in HDMI2.1(FRL) mode.
VCC5V0_SYS
VCC5V0_HDMI
VCC5V_HDMI_TX
R5608 0R R0402
D5600 B5819W SOD_123
R5610 NC/0RR0402
HDMI TX DDC
VCC5V0_HDMI
D5601 B5819WS SOD_323
VCC_3V3_S3
R5613 20K R0402
Q5605 2SK3018 SOT_323
R5614 1.8K R0402
HDMI_TX_SCL
HDMI_TX_SCL_PORT
R5615 100R R0402
R5619 20K R0402
Q5607 2SK3018 SOT_323
R5620 1.8K R0402
HDMI_TX_SDA
HDMI_TX_SDA_PORT
R5621 100R R0402
HDMI TX ARC
HDMI_TX_SBDP C5608 1uF X5R 10V C0402 HDMITX_SBDP
HDMI_TX_SBDN C5609 1uF X5R 10V C0402 HDMITX_HPDIN/HDMITX_SBDN
HDMI TX HPD
VCC_3V3_S3
R5611 47K R0402
R5612 47K R0402
HDMI_TX_HPDIN_M0
3.3V IO
Q5604 2SK3018 SOT_323
Q5606 2SK3018 SOT_323
2.4-5.3V
HDMITX_HPDIN/HDMITX_SBDN
R5617 47K R0402
R5616 1.2K R0402
HDMI TX CEC
VCC_3V3_S3
VCC5V0_HDMI
R5622 27K R0402
Q5608 2SK3018 SOT_323
HDMI_TX_CEC_M0
R5623 100R R0402
HDMI_TX_CEC_PORT
Cj<=0.2pF
ED5600 ESD73034D SON10_2R50X1R00X0R50
ED5601 ESD73034D SON10_2R50X1R00X0R50
IO1 IO2 GND IO3 IO4 NC_10 NC_9 GND NC_7 NC_6
ED5602 ED5603 ED5604 ED5605 ED5606 ESD5471X ESD-DFN1006
VCC5V_HDMI_TX
C5610 1uF X5R 10V C0402
D2P D2_G D2N D1P D1_G D1N D0P D0_G D0N CLKP CLK_G CLKN CEC UTILITY SCL SDA GND +5V HPD
Type A
J5600 HDMI_A HDMIA19_HDMI_01A
Rockchip Electronics Co., Ltd
Project:
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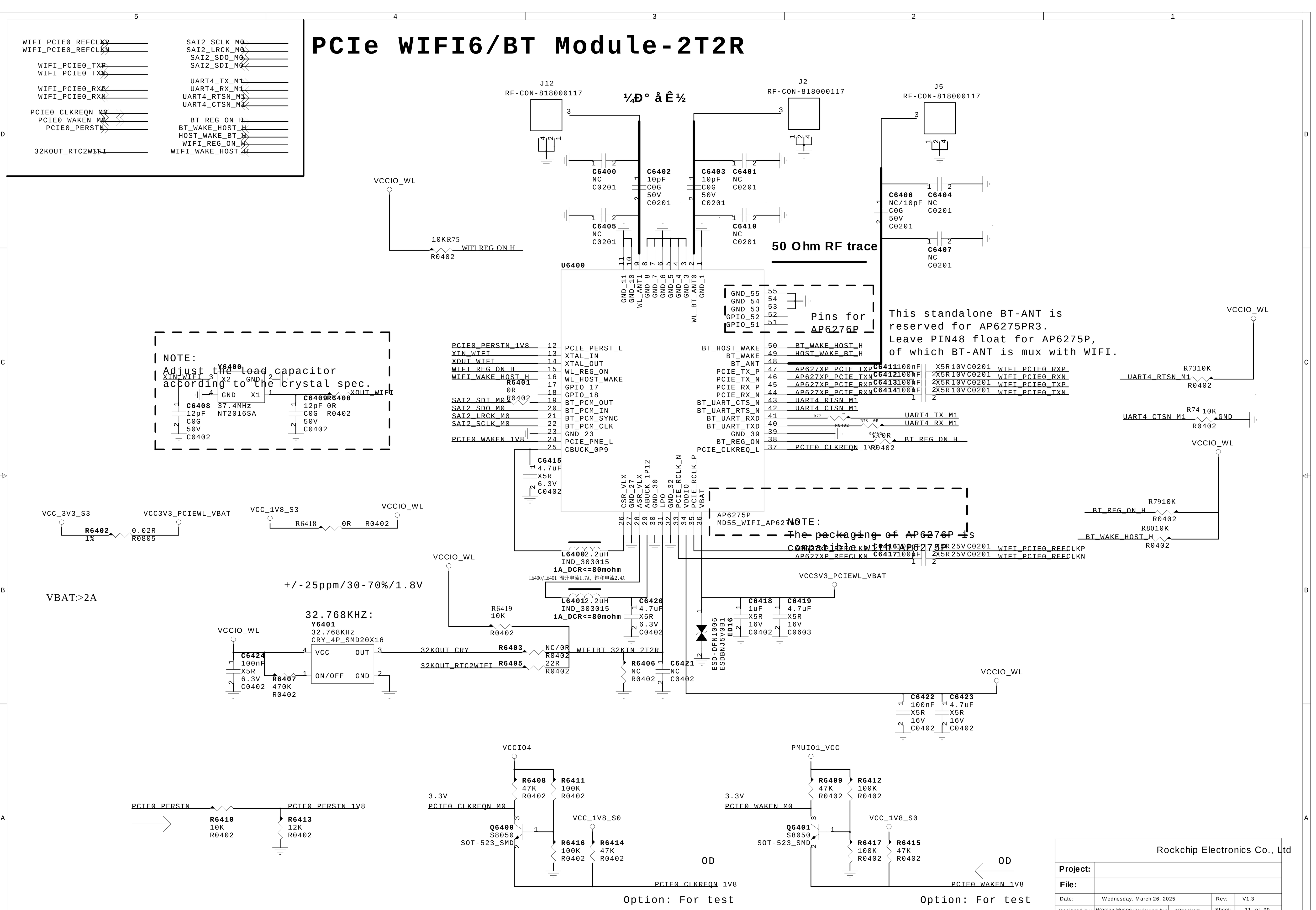

PCIe WIFI6/BT Module-2T2R
50 Ohm RF trace
This standalone BT-ANT is
reserved for AP6275PR3.
Leave PIN48 float for AP6275P,
of which BT-ANT is mux with WIFI.
Pins for
AP6276P
NOTE:
Adjust the load capacitor
according to the crystal spec.
NOTE:
The packaging of AP6276P is
compatible with AP6275P
+/-25ppm/30-70%/1.8V
32.768KHZ:
VBAT:>2A
1A_DCR<=80mohm
Option: For test
OD
U6400
AP6275P
J12
J2
J5
RF-CON-818000117
Y6400
37.4MHz
NT2016SA
Y6401
32.768KHz
Q6400
S8050
Q6401
S8050
SOT-523_SMD
Rockchip Electronics Co., Ltd
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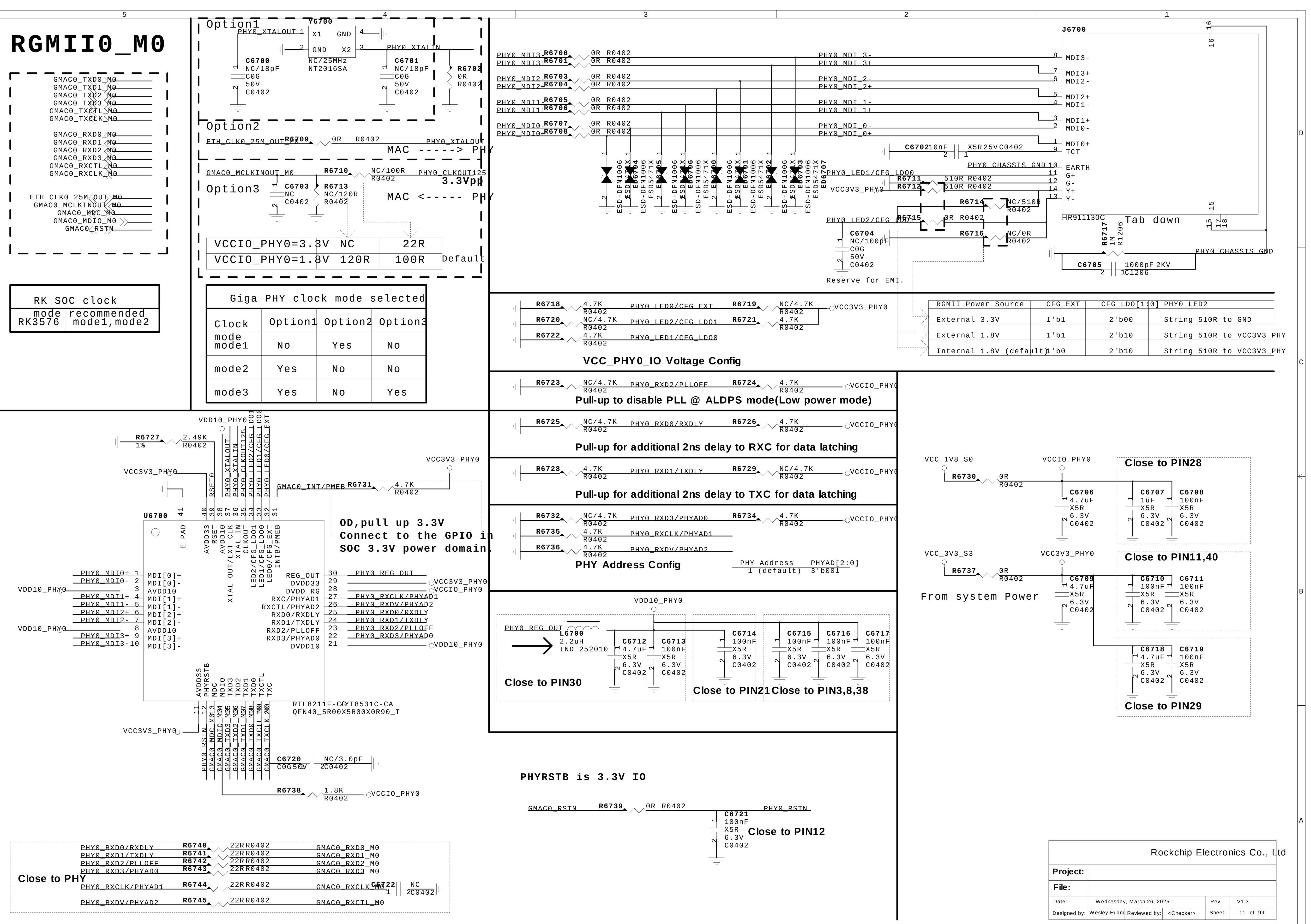
RGMII0_M0
Option1
Option2
Option3
MAC ------> PHY
MAC <------ PHY
3.3Vpp
VCCIO_PHY0=3.3V NC 22R
VCCIO_PHY0=1.8V 120R 100R Default
RK SOC clock
mode recommended
RK3576 mode1,mode2
Giga PHY clock mode selected
Clock mode | Option1 | Option2 | Option3
mode1 | No | Yes | No
mode2 | Yes | No | No
mode3 | Yes | No | Yes
Tab down
Reserve for EMI.
RGMII Power Source | CFG_EXT | CFG_LDO[1:0] | PHY0_LED2
External 3.3V | 1'b1 | 2'b00 | String 510R to GND
External 1.8V | 1'b1 | 2'b10 | String 510R to VCC3V3_PHY
Internal 1.8V (default) | 1'b0 | 2'b10 | String 510R to VCC3V3_PHY
VCC_PHY0_IO Voltage Config
Pull-up to disable PLL @ ALDPS mode(Low power mode)
Pull-up for additional 2ns delay to RXC for data latching
Pull-up for additional 2ns delay to TXC for data latching
PHY Address Config
PHY Address PHYAD[2:0]
1 (default) 3'b001
OD,pull up 3.3V
Connect to the GPIO in
SOC 3.3V power domain.
Close to PIN28
Close to PIN11,40
Close to PIN29
Close to PIN30
Close to PIN21
Close to PIN3,8,38
From system Power
PHYRSTB is 3.3V IO
Close to PIN12
Close to PHY
RTL8211F-CG
Rockchip Electronics Co., Ltd
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Reviewed by: <Checker>
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REVISION RECORD			
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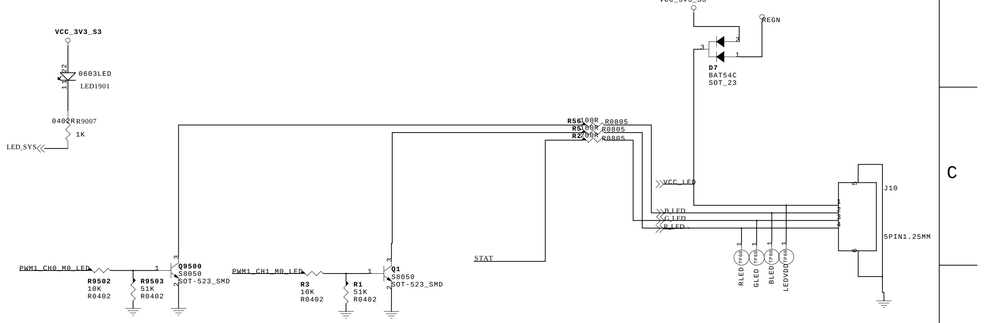

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TITLE:	<Title>

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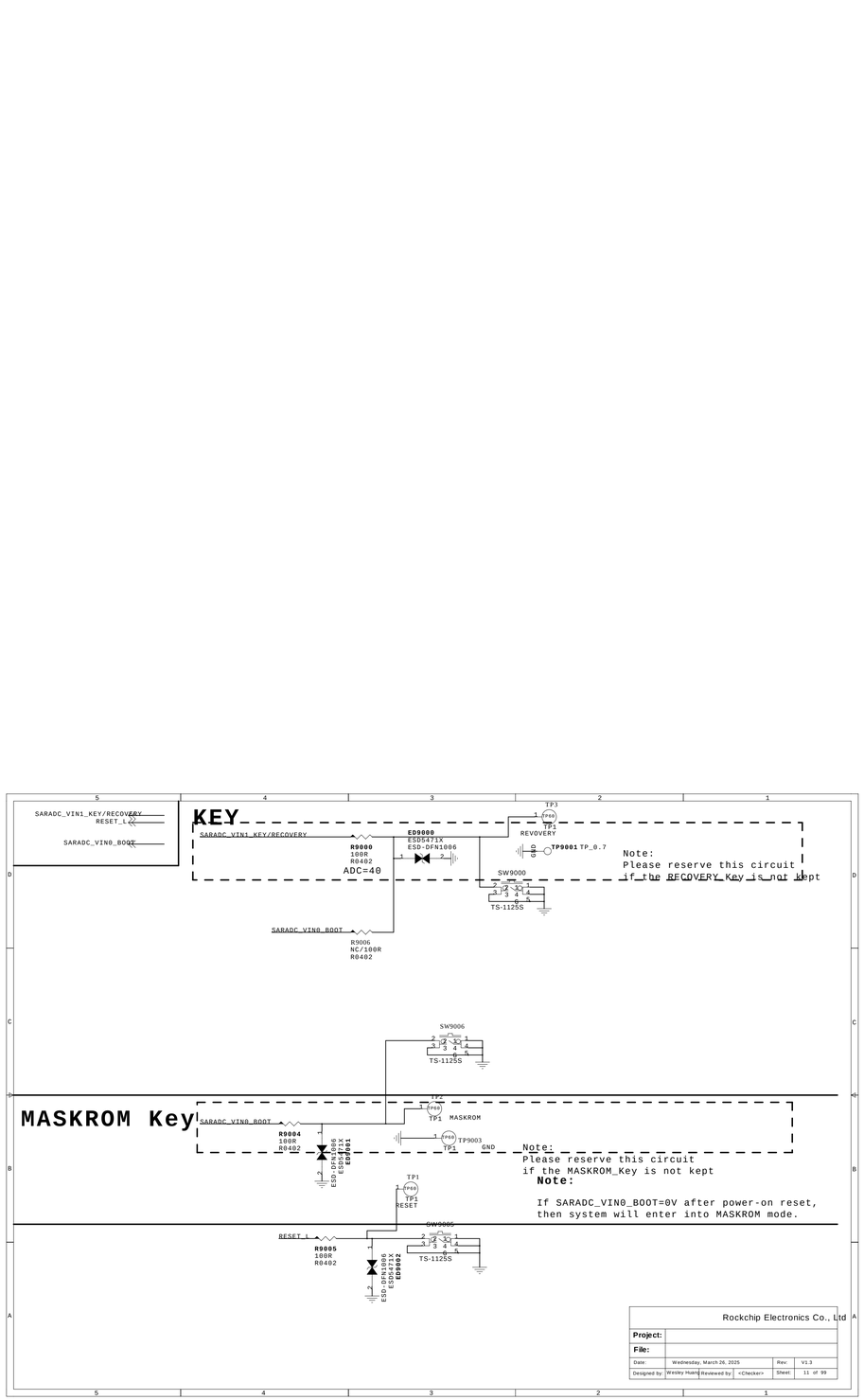
QUALITY CONTROL: <QC By>	DATED: <QC Date>	<Code>	D	<Drawing Number>
RELEASED: <Released By>	DATED: <Release Date>	SCALE: <Scale>		SHEET: 19 OF 27

REV: <Revision>



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Project:					
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Designed by:	Wesley Huang	Reviewed by:	<Checker>	Sheet:	11 of 99

CC

Note:

Different models of CC chips may require different driver software.

	AW35615(Default)	HUSB311(Option)
7bit address	0x22	0x4E
VBUS	4V~21V,TYP=5V	4V~21V,TYP=5V
VDD	2.7V~5.5V,TYP=3.3V	3V~5.5V,TYP=3.3V
VCONN	2.7V~5.5V	3V~5.5V

TYPEC

With Displayport Alt Mode

This is also the firmware download interface

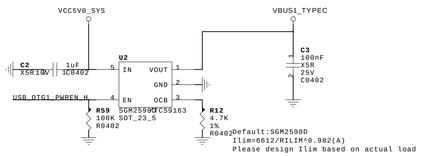
Cj<=0.2pF

Cj<=0.2pF

Note:

If common mode inductors are needed, it is recommended to keep 2.2ohm in series to improve the antistatic ability

USB POWER



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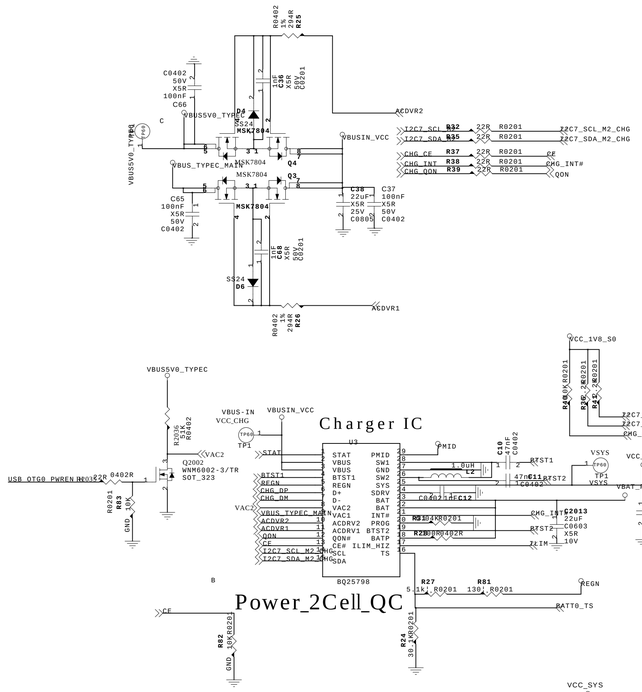
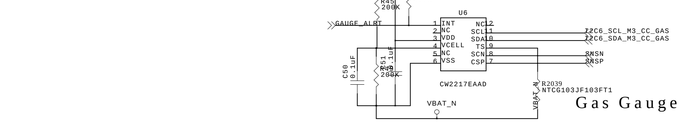
Power_2Cell_QC

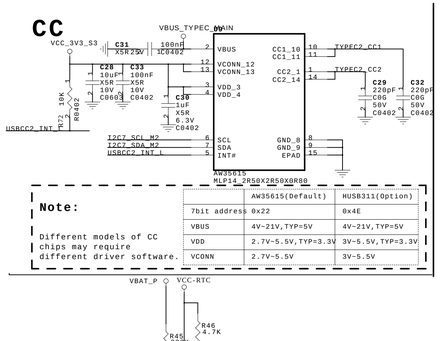


Charger IC

Gas Gauge



CC



Note:

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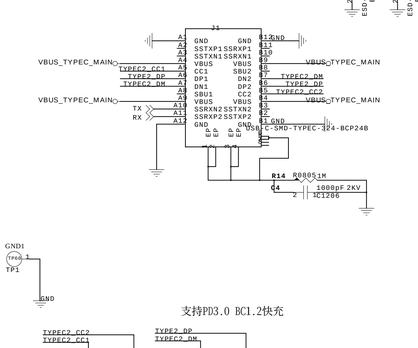
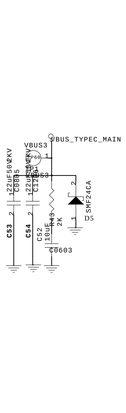
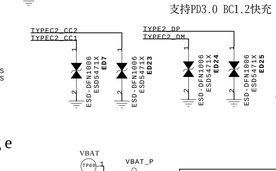
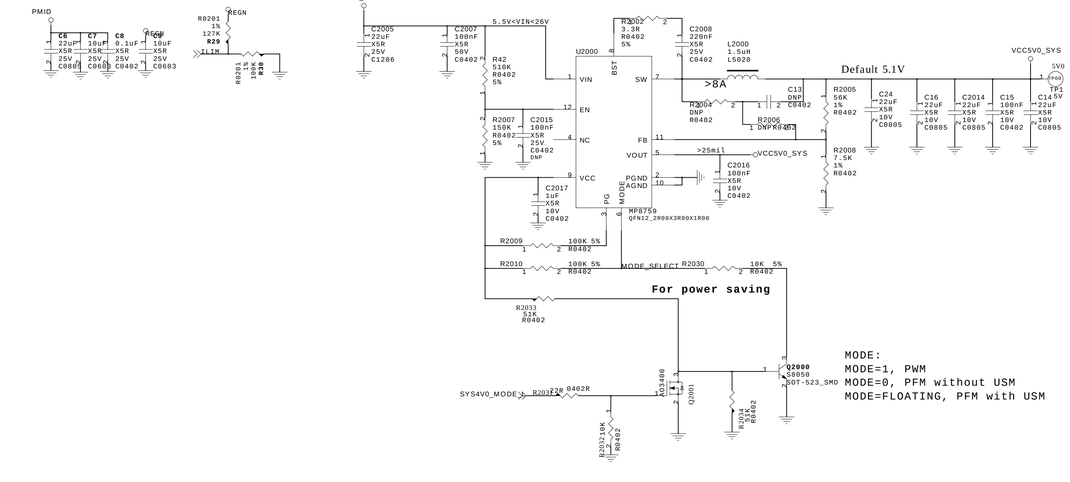
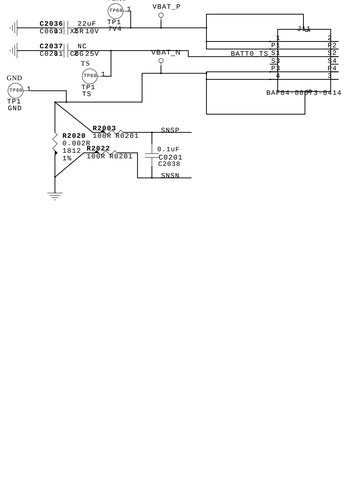
7bit address	0x22	0x4E
VBUS	4V~21V,TYP=5V	4V~21V,TYP=5V
VDD	2.7V~5.5V,TYP=3.3V	3V~5.5V,TYP=3.3V
VCONN	2.7V~5.5V	3V~5.5V

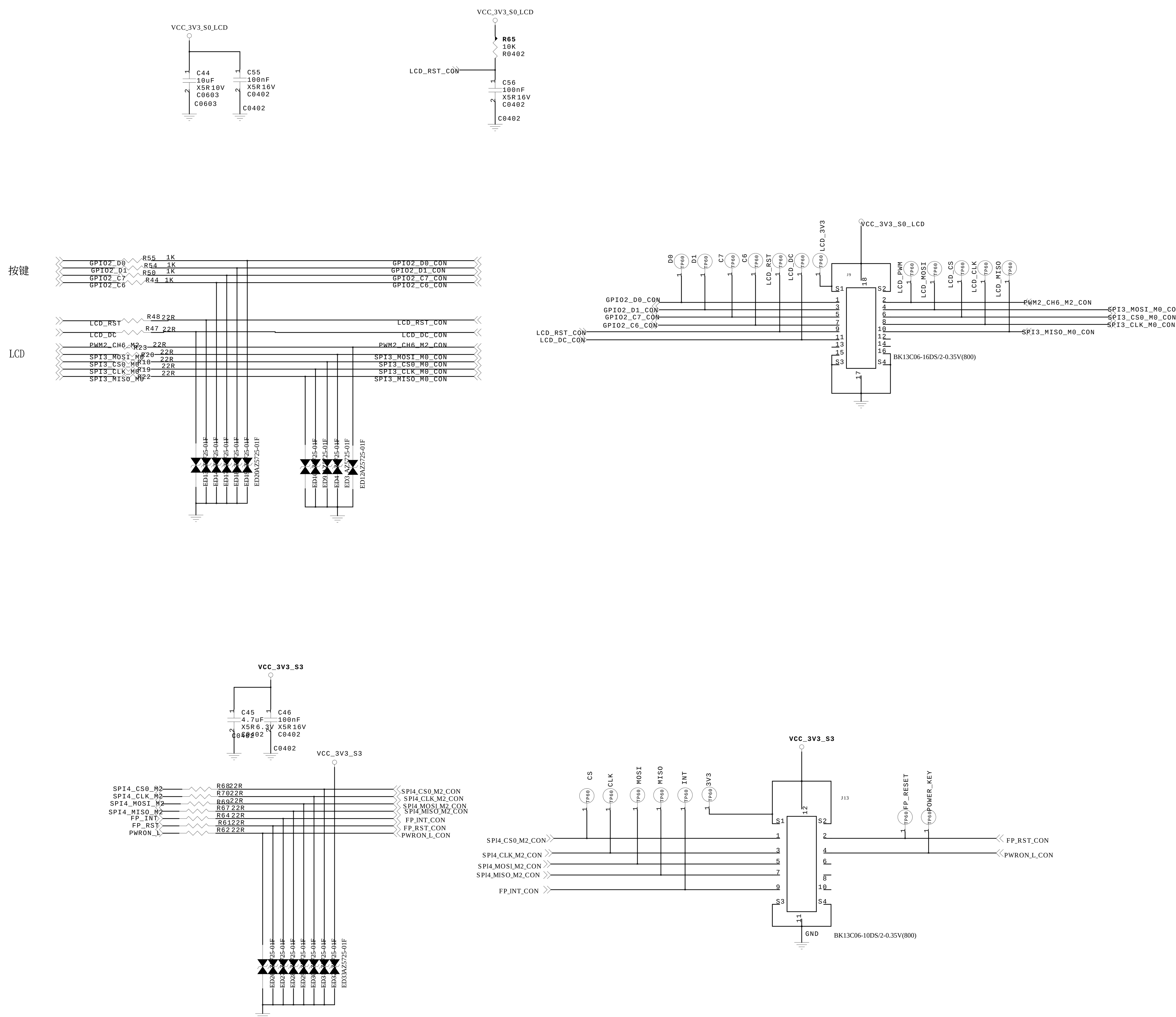












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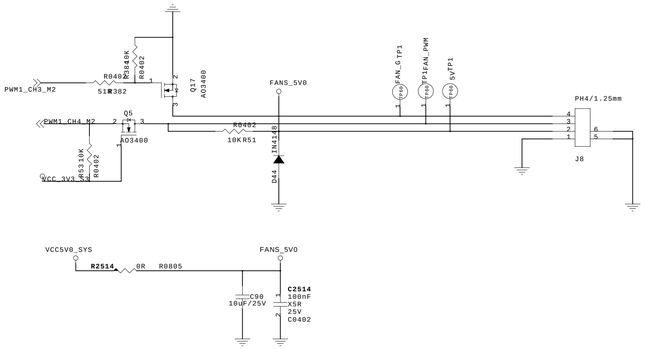

Default:SGM2590D
Ilim=6612/RILIM*0.982(A)
Please design Ilim based on actual load

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CHECKED: <Checked By>	DATED: <Checked Date>	TITLE: <Title>			
QUALITY CONTROL: <QC By>	DATED: <QC Date>	CODE: <Code>	SIZE: D	DRAWING NO: <Drawing Number>	REV: <Revision>
RELEASED: <Released By>	DATED: <Release Date>	SCALE: <Scale>		SHEET: 24 OF 27	

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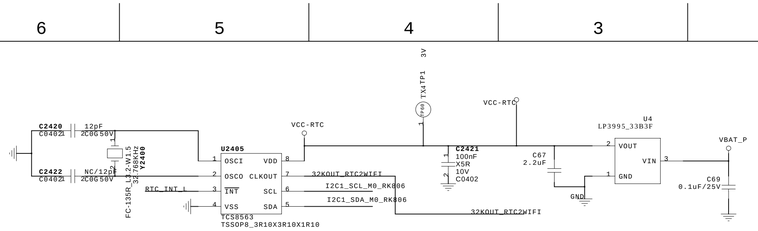

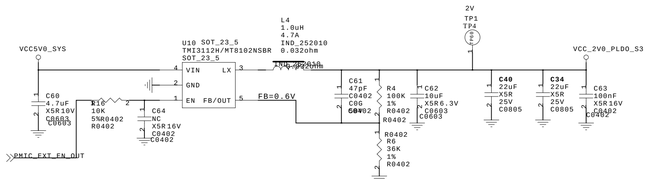

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REVISION RECORD			
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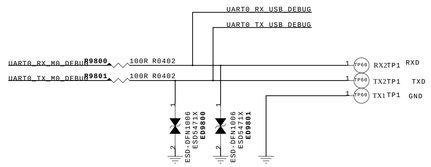

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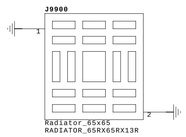
CHECKED: <Checked By>	DATED: <Checked Date>				
QUALITY CONTROL: <QC By>	DATED: <QC Date>				
RELEASED: <Released By>	DATED: <Release Date>	SCALE: <Scale>		SHEET: 26 OF 27	

Heatsink



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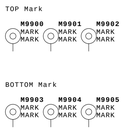
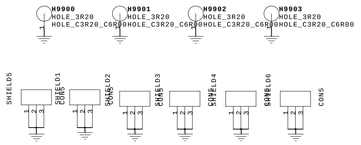


Hole



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Designed by:	Wesley Huang	Reviewed by: <Checker>	Sheet: 11 of 99