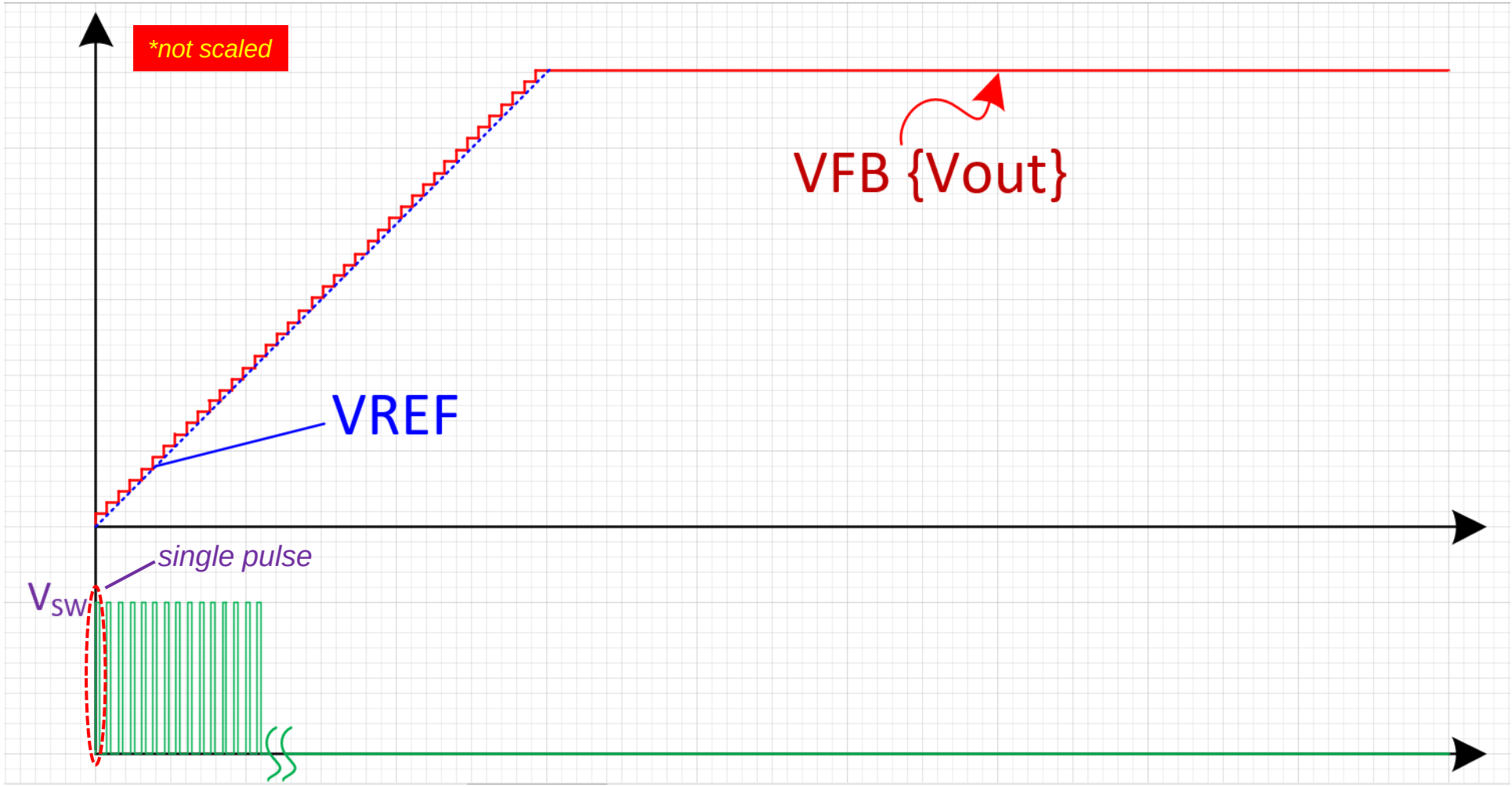
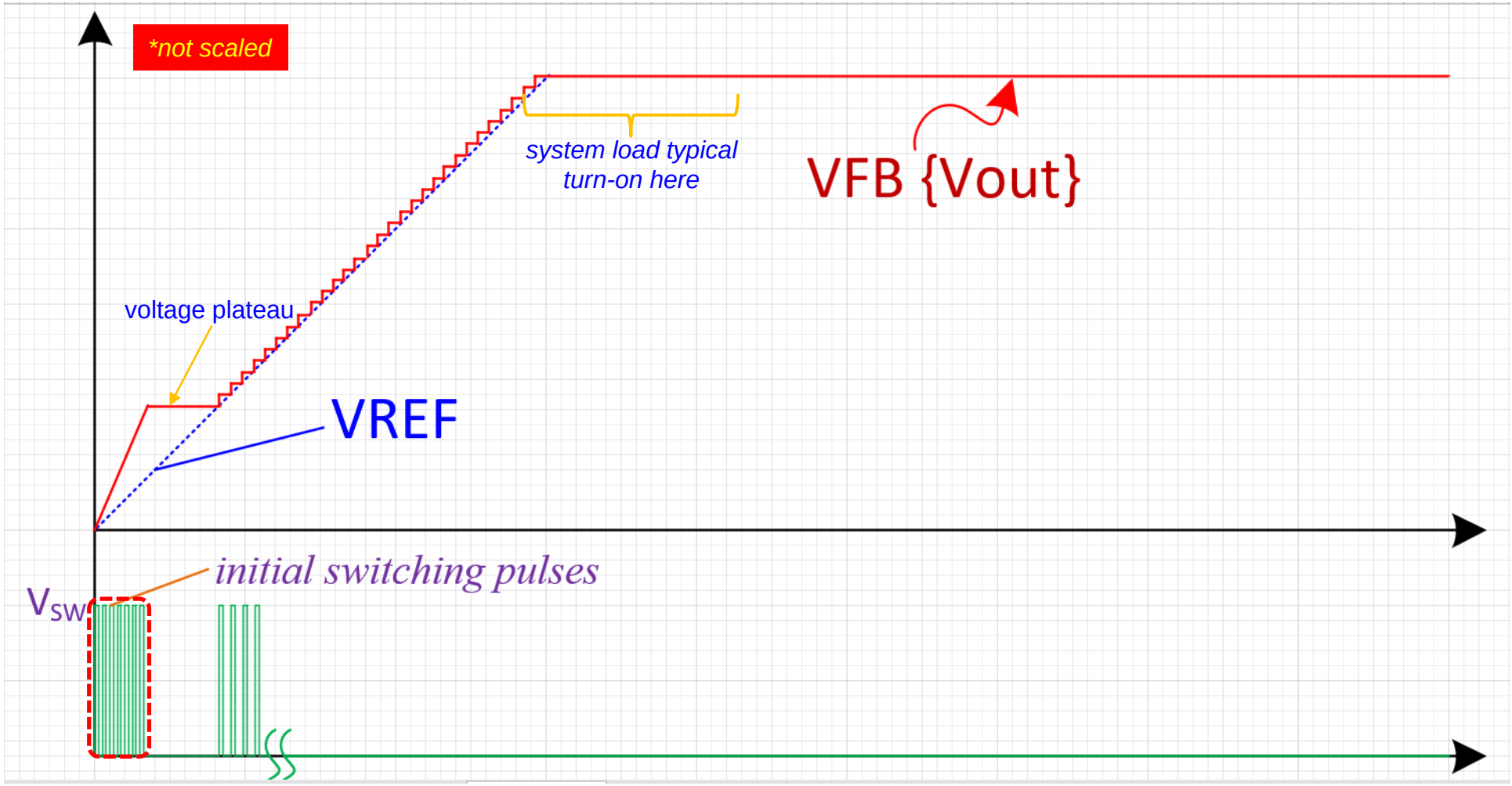
TLV62565: Startup voltage behavior

- After startup delay, Vref starts to rise, and the converter also start switching
- The high-side and low-side FETs turns for *one cycle* to charge the output, then it stops because Vfb is now greater than Vref
- Once Vref reached the same level of Vfb, the high-side, and low-side FETs will start switching again
- This event will continue until Vout reached the regulation level



TLV62568/69: Startup voltage behavior

- Similar to TLV62565, the Vref starts rise after startup delay
- Instead of a single pulse to charge the output, it generates multiple pulses causing the output voltage to rise significantly and way above the Vref
- It takes a while for the Vref to reach the same level of Vfb, which causes a plateau in the output voltage
- In the succeeding switching cycles, the no. of pulses are fewer that lead to linear rise output voltage until it reached the regulation level
- Because the high voltage step occurs at initial Vout ramp only, the system load will have a stable supply once it is ready to turn-on



TLV62568: Sample startup waveform

- Test condition
  - Vin = 3.3V
  - Vout = 0.6V; Iout = 0A