User's Guide
SLVU301–April 2009

TPS23754EVM-420 EVM: Evaluation Module for TPS23754

This User's Guide describes the TPS23754 EVM (TPS23754EVM-420). TPS23754EVM-420 contains evaluation and reference circuitry for the TPS23754. The TPS23754 is an IEEE 802.3at compliant powered device (PD) controller and power supply controller optimized for isolated converter topologies. TPS23754EVM-420 is targeted at 25W, synchronous flyback converter applications.

这份用户指南，介绍、评估TPS23754EVM参考电路。TPS23754符合IEEE802.3af标准；电路驱动控制器，电源授电控制器，优化器拓扑结构，

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1 Description

TPS23754EVM-420 will allow reference circuitry evaluation of the TPS23754. It contains input and output power connectors and an array of on board test points for circuit evaluation. An active clamp, 12V, 30W EVM is also available, see SLVU304.

1.1 Features

- Efficient, general market design
  - Self driven, synchronous rectified secondary
  - 25W output power from power over ethernet (PoE), 30W output power from a 48V adapter
  - Operates from either PoE or external adaptors (24 and 48V)
  - 5V output voltage

1.2 Applications

- Voice over Internet Protocol – IP telephones
- Wireless LAN – Wireless Access Points
- Security – Wired IP cameras

2 Electrical Specifications

Table 1. TPS23754EVM-420 Electrical and Performance Specifications

Parameter	Test Conditions		Min	Typ	Max	Unit
POWER INTERFACE						
Input Voltage	Applied to the power pins of connectors J1 or J3		0		57	V
Operating Voltage	After start up		30		57	V
Input UVLO	Rising input voltage				36	V
	Falling input voltage		30			
Detction voltage	At device terminals		1.6		10	V
Classification voltage 分级电压	At device terminals		10		23	V
Classification current 分级电路	Rclass = 63.5 Ω		36		44	mA
Inrush current-limit			100		180	mA
Operating current-limit			850		1100	mA
DC/DC CONVERTER						
Output voltage	21.6V ≤ Vin ≤ 57 V, ILOAD ≤ ILOAD (max)	5 V output	4.75	5.00	5.25	V
Output current	21.6V ≤ Vin ≤ 57 V	5 V output			5	A
Output ripple voltage, peak-to-peak	Vin = 44 V, ILOAD = 5 A	5 V output		50		mV
Efficency, end-to-end	Vin = 44 V, ILOAD = 5 A	5 V output		85%		
Switching frequency			225		275	kHz

3 Schematic

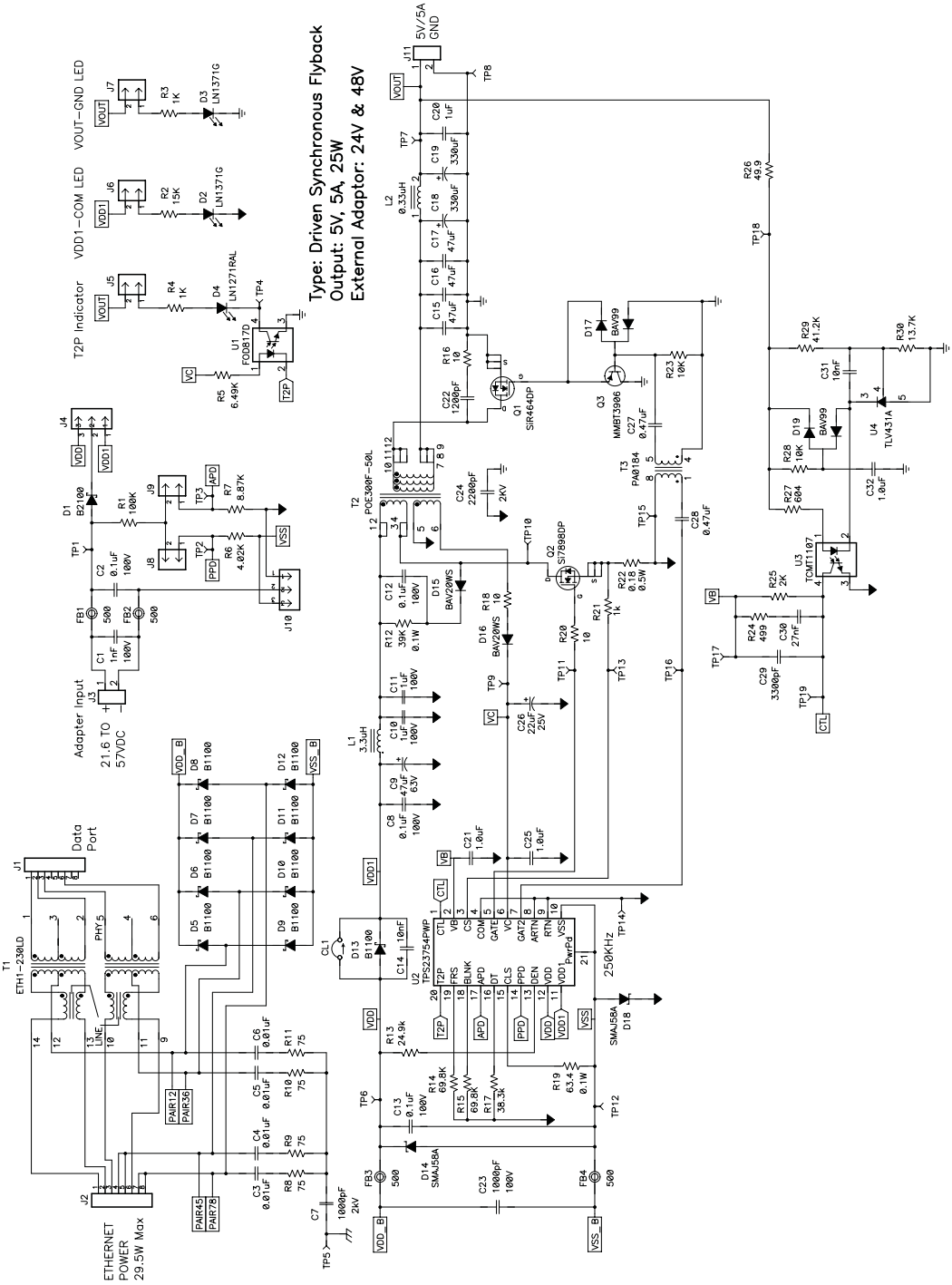

Figure 1. TPS23754EVM-420 Schematic

4 General Configuration and Description

4.1 Physical Access

Table 2 lists the TPS23754EVM-420 connector functionality and Table 3 describes the test point availability.

Table 2. Connector Functionality

Connector	Label	Description
J3	ADAPTER	External adapter input. J10 (low side) and J4 (high side) can select weather the adapter is at the PD controller input (VDD to VSS) or at the converter input (VDD1 to COM). J9 is installed to select APD function and J8 is installed to select the PPD function.
J11	VOUT	Output voltage connector
J2	Ethernet Power	Ethernet power input connector.
J1	Ethernet Data	Ethernet data port connector
TP5	Earth GND	Earth GND connection

Table 3. Test Points and Indicators

Test Point	Color	Label	Description
TP8	BLK	GND	Secondary side (output) grounds (GND)
TP9	RED	VC	DC/DC converter bias supply
TP10	ORG	DRAIN	Drain terminal of the primary side switching MOSFET
TP12	BLK	VSS	PoE input, low side
TP14, TP15	BLK	COM	DC/DC converter return
TP18	ORG	LOOP	Can be used with TP7 for overall feedback loop measurements.
TP7	RED	VOUT	DC/DC converter output voltage.
TP19	WHT	CTL	Control loop input to the pulse width modulator
TP13	WHT	CS	DC/DC converter primary side switching MOSFET current sense (device side).
TP17	RED	VB	Bias voltage regulator
TP11	WHT	GATE	Gate drive for the primary side switching MOSFET
TP16	WHT	GAT2	Gate drive for the secondary side MOSFET
TP6	RED	VDD	PD controller high side voltage.
TP1	RED	ADPV	Adapter input voltage
TP4	WHT	T2P	Type 2 PSE output from TPS23754
TP2	WHT	PPD	Connected to PPD pin of TPS23754
TP3	WHT	APD	Connected to APD pin of TPS23754
TP5	WHT	Earth GND	Earth GND common termination point for chassis terminators
D4	RED	T2P	Type 2 PSE indicator. Remove the shunt on J5 to inhibit the T2P indicator.
D2	GRN	COM	VDD1-COM voltage present. Remove the shunt on J6 to inhibit the COM indicator.
D3	GRN	OUT	Output power indicator. Remove the shunt on J7 to inhibit the output power indicator.
CL1	NA	CL1	CL1 provides a connection between VDD and VDD1 shorting out D13. Removing the short at CL1 allows certain power source priority schemes to be tested.

5 Test Setup

Figure 2 shows a typical test setup for TPS23754EVM-420. Input voltage can be applied as described in Table 2.

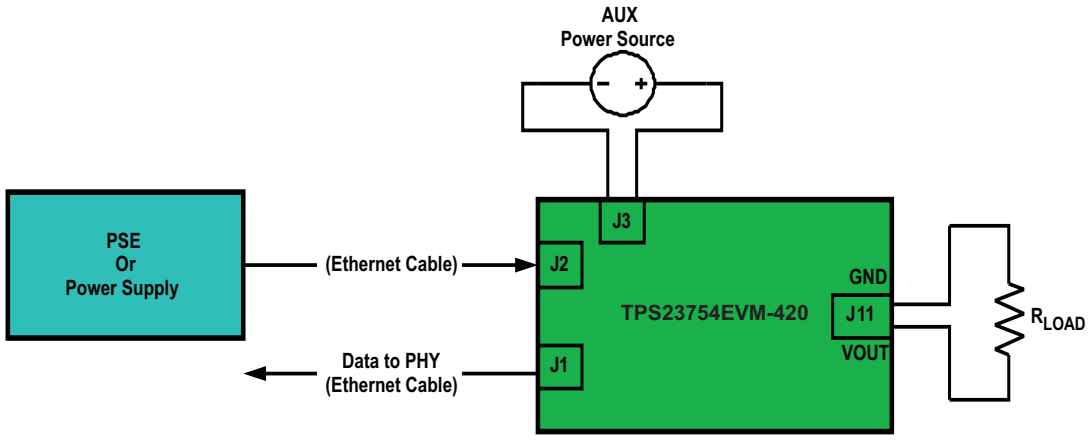

Figure 2. Typical TPS23754EVM-420 Test Setup

6 TPS23754EVM-420 Typical Performance Data

6.1 5V DC/DC Efficiency

Figure 3 illustrates three different 48VDC input efficiency plots:

1. PoE, 48V from J2
2. Converter only 48V
3. Adapter 48V from J3

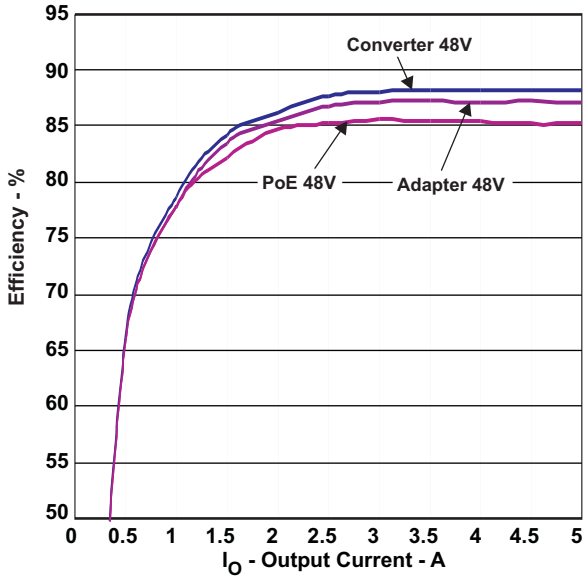

Figure 3. TPS23754EVM-420 Efficiency With 5V Output

7 EVM Assembly Drawings and Layout Guidelines

7.1 PCB Drawings

Figure 4 and Figure 5 shows component placement and layout.

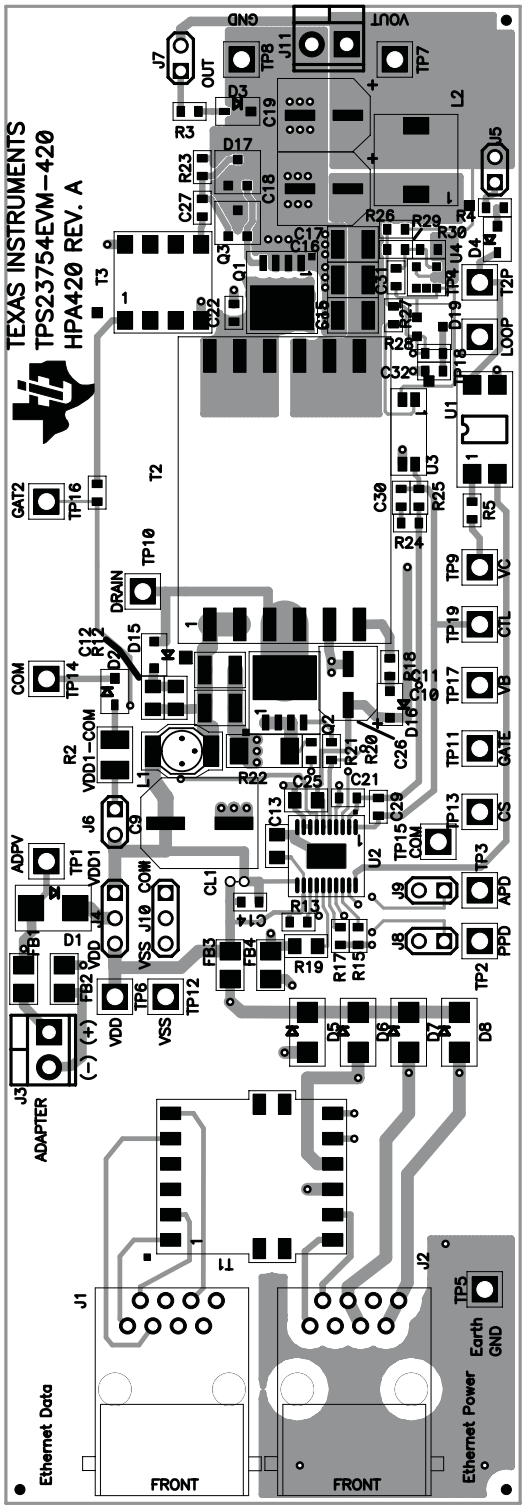

Figure 4. Top Side Layout

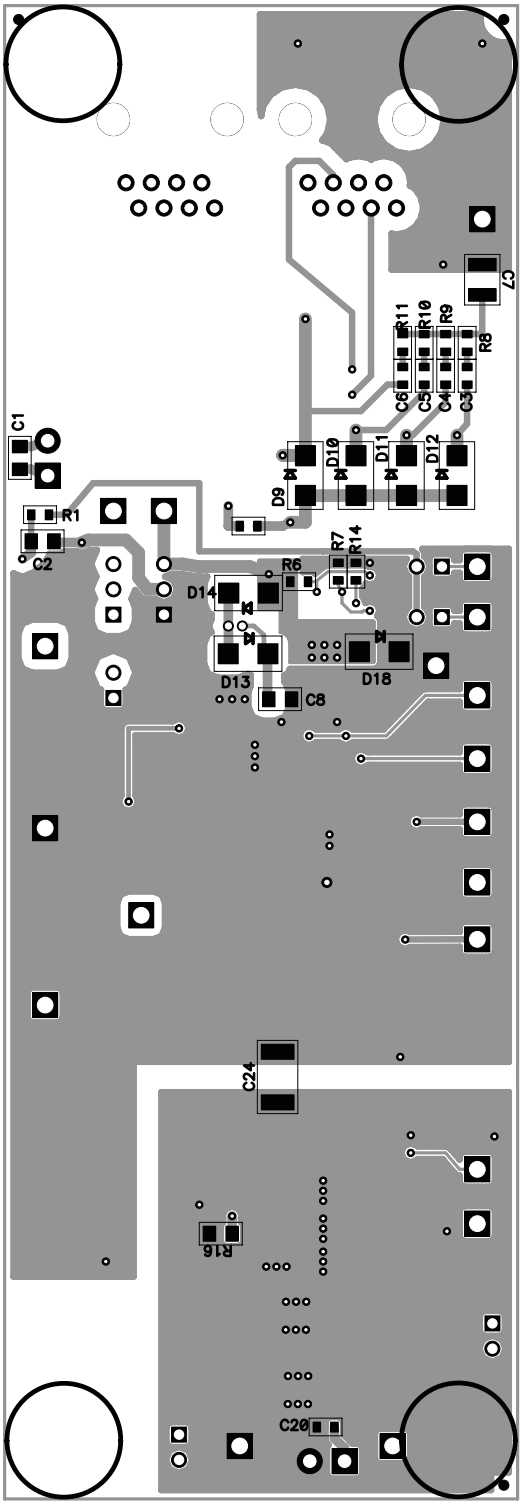

Figure 5. Bottom Side Layout

7.2 Layout Guidelines

POE前段布局应遵守，电源EMI/ESD最佳指导方针。

The layout of the PoE front end should follow power and EMI/ESD best practice guidelines. A basic set of recommendations include:

- Parts placement must be driven by power flow in a point-to-point manner; RJ-45, Ethernet transformer, diode bridges, TVS and 0.1-µF capacitor, and TPS23754 converter input bulk capacitor.
- All leads should be as short as possible with wide power traces and paired signal and return.
- There should not be any crossovers of signals from one part of the flow to another.
- Spacing consistent with safety standards like IEC60950 must be observed between the 48-V input voltage rails and between the input and an isolated converter output.
- The TPS23754 should be located over split, local ground planes referenced to VSS for the PoE input and to COM/RTN for the converter. Whereas the PoE side may operate without a ground plane, the converter side must have one. Logic ground and power layers should not be present under the Ethernet input or the converter primary side.
- Large copper fills and traces should be used on SMT power-dissipating devices, and wide traces or overlay copper fills should be used in the power path.

The DC/DC Converter layout can benefit from basic rules such as:

- Pair signals to reduce emissions and noise, especially the paths that carry high-current pulses which include the power semiconductors and magnetics.
- Minimize trace length of high current, power semiconductors, and magnetic components.
- Where possible, use vertical pairing.
- Use the ground plane for the switching currents carefully.
- Keep the high-current and high-voltage switching away from low-level sensing circuits including those outside the power supply.
- Proper spacing around the high-voltage sections of the converter.

7.3 EMI Containment

- Use compact loops for dv/dt and di/dt circuit paths (power loops and gate drives)
- Use minimal, yet thermally adequate, copper areas for heat sinking of components tied to switching nodes (minimize exposed radiating surface).
- Use copper ground planes (possible stitching) and top layer copper floods (surround circuitry with ground floods)
- Use 4 layer PCB if economically feasible (for better grounding)
- Minimize the amount of copper area associated with input traces (to minimize radiated pickup)
- Hide copper associated with switching nodes under shielded magnetics where possible
- Heat sink the “quiet side” of components instead of the “switching side” where possible (like the output side of inductor)
- Use Bob Smith terminations, Bob Smith EFT capacitor, and Bob Smith plane
- Use Bob Smith plane as ground shield on input side of PCB (creating a phantom or literal earth ground)
- Use LC filter at DC/DC input
- Dampen high frequency ringing on all switching nodes if present (allow for possible snubbers)
- Control rise times with gate drive resistors and possibly snubbers
- Switching frequency considerations
- Use of EMI bridge capacitor across isolation boundary (isolated topologies)
- Observe the polarity dot on inductors (embed noisy end)
- Use of ferrite beads on input (allow for possible use of beads or 0 ohm resistors)
- Maintain physical separation between input-related circuitry and power circuitry (use ferrite beads as boundary line)
- Balance efficiency vs. Acceptable noise margin
- Possible use of common-mode inductors
- Possible use of integrated RJ-45 jacks (shielded with internal transformer and Bob Smith terminations)

- End-product enclosure considerations (shielding)

8 Bill of Materials

Table 4. TPS23754EVM-420 Bill of Materials

Count	RefDes	Value	Description	Size	Part Number	MFR
1	C1	1 nF	Capacitor, Ceramic, 100V, X7R, 10%	0805	Std	Std
2	C10, C11	1 µF	Capacitor, Ceramic, 1 µF, 100V, X7R, 15%	1210	Std	Std
1	C14	10 nF	Capacitor, Ceramic, 100V, X7R, 10%	0603	Std	Std
3	C15–C17	47 µF	Capacitor, Ceramic, 10V, X5R, 15%	1210	Std	Std
2	C18, C19	330 µF	Capacitor, Aluminum, 6.3V, 20% inch	0.260 × 0.276	EEVFK0J331XP	Panasonic
1	C2	0.1 µF	Capacitor, Ceramic, 100V, X7R, 10%	0805	Std	Std
1	C20	1 µF	Capacitor, Ceramic, 16V, X7R, 15%	0603	Std	Std
2	C21, C32	1.0 µF	Capacitor, Ceramic, 16V, X7R, 10%	0603	Std	Std
1	C22	1200 pF	Capacitor, Ceramic, 50V, X7R, 15%	0603	Std	Std
1	C23	1000 pF	Capacitor, Ceramic, 100V, X7R, 15%	0603	Std	Std
1	C24	2200 pF	Capacitor, Ceramic, 2KV, X7R, 15%	1812	Std	Std
1	C25	1.0 µF	Capacitor, Ceramic, 25V, X7R, 10%	0805	Std	Std
1	C26	22 µF	Capacitor, Aluminum, 25V, 20%	5 × 5,8mm	EEVFK1E220R	Panasonic
2	C27, C28	0.47 µF	Capacitor, Ceramic, 16V, X7R, 15%	0603	Std	Std
1	C29	3300 pF	Capacitor, Ceramic, 50V, X7R, 15%	0603	Std	Std
4	C3–C6	0.01 µF	Capacitor, Ceramic, 100V, X7R, 15%	0603	Std	Std
1	C30	27 nF	Capacitor, Ceramic, 50V, X7R, 15%	0603	Std	Std
1	C31	10 nF	Capacitor, Ceramic, 50V, X7R, 15%	0603	Std	Std
1	C7	1000 pF	Capacitor, Ceramic, 2kV, X7R, 15%	1210	Std	Std
3	C8, C12, C13	0.1 µF	Capacitor, Ceramic, 100V, X7R, 15%	0805	Std	Std
1	C9	47 µF	Capacitor, Aluminum, 63V, ±20%	0.328 0 × 0.390 inch	EEVFK1J470P	Panasonic
1	CL1	NA	Current Loop, 0.025 holes	0.120 0 × 0.075 inch	NA	NA
1	D1	B2100	Diode, Schottky, 2-A, 100-V	SMB	B2100-13	Diodes Inc
2	D14, D18	SMAJ58A	Diode, TVS, 58-V, 1W	SMA	SMAJ58A	Diodes Inc.
2	D15, D16	BAV20WS	Diode, Small Signal, 250mA, 150V	SOD-323	BAV20WS	Micro Commercial Components
2	D17, D19	BAV99	Diode, Dual Ultra Fast, Series, 200-mA, 70-V	SOT23	BAV99	Fairchild
2	D2, D3	LN1371G	Diode, LED, Green, 10-mA, 2.6-mcd	0.114 0 × 0.049 inch	LN1371G	Panasonic
1	D4	LN1271RAL	Diode, LED, Ultra Bright Red, 10-mA, 5-mcd	0.114 0 × 0.049 inch	LN1271RAL	Panasonic
9	D5– D13	B1100	Diode, Schottky, 1A, 100V	SMA	B1100	Diodes, Inc
4	FB1–FB4	500	Bead, Ferrite, 2000mA, 60mΩ	1206	MI1206L501R-10	Steward
2	J1, J2	5520252-4	Connector, Jack, Modular, Rt. Angle,8 POS	0.705 0 × 0.820 inch	5520252-4	AMP
2	J3, J11	ED1514	Terminal Block, 2-pin, 6-A, 3,5mm	0.27 0 × 0.25	ED1514	
2	J4, J10	PTC36SAAN	Header, Male 3-pin, 100mil spacing, (36-pin strip)	0.100 inch 0 × 3	PTC36SAAN	Sullins
5	J5–J9	PTC36SAAN	Header, Male 2-pin, 100mil spacing, (36-pin strip)	0.100 inch 0 × 2	PTC36SAAN	Sullins
1	L1	3.3uH	Inductor, SMT, 2.0A, 80-mΩ	4.450 × 6.6mm	DO1608C-332	Coilcraft
1	L2	0.33uH	Inductor, SMT, 6.26A, 7.4-mΩ	0.300 sq"	DR74-R33	Cooper
1	Q1	SiR464DP	MOSFET, NChannel, 30V, 29A, 3mΩ	PWRPAK S0-8	SiR464DP	Vishay
1	Q2	Si7898DP	MOSFET, NChannel, 150V, 4.8A, 85-mΩ	PWRPAK S0-8	Si7898DP	Vishay
1	Q3	MMBT3906	Bipolar, PNP, 40V, 200mA, 225mW	SOT23	MMBT3906LT1	On Semi
1	R1	100K	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R12	39K	Resistor, Chip, 1/10W, 1%	0805	Std	Std
1	R13	24.9k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
2	R14, R15	69.8K	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R16	10	Resistor, Chip, 1/10W, 1%	0805	Std	Std
1	R17	38.3k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R18	10	Resistor, Chip, 1/16W, 5%	0603	Std	Std

Table 4. TPS23754EVM-420 Bill of Materials (continued)

Count	RefDes	Value	Description	Size	Part Number	MFR
1	R19	63.4	Resistor, Chip, 1/10W, 1%	0805	Std	Std
1	R2	15K	Resistor, Chip, 1/4W, 1%	1210	Std	Std
1	R20	10	Resistor, Chip, 1/16W, 1%	0603	Std	Std
3	R21	1k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R22	0.18	Resistor, Chip, 1/2W, 1%	2010	Std	Std
2	R23, R28	10K	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R24	499	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R25	2K	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R26	49.9	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R27	604	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R29	41.2K	Resistor, Chip, 1/16W, 1%	0603	Std	Std
2	R3, R4	1K	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R30	13.7K	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R5	6.49K	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R6	4.02K	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R7	8.87K	Resistor, Chip, 1/16W, 1%	0603	Std	Std
4	R8–R11	75	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	T1	ETH1-230LD	XFMR, Mid-Power PoE Magnetics	S0 14 Wide	ETH1-230LD	Coilcraft
1	T2	POE300F-50L	Transformer, SMT For PoE/PD, 25W, 2.8A	0.810 0 × 1.181 inch	POE300F-50L	Coilcraft
1	T3	PA0184	XFMR, SMT Gate Drive	0.355 0 × 0.340 inch	PA0184	Pulse
5	TP1, TP6, TP7, TP9, TP17	5010	Test Point, Red, Thru Hole	0.125 0 × 0.125 inch	5010	Keystone
3	TP10, TP13, TP18	5013	Test Point, Orange, Thru Hole	0.125 0 × 0.125 inch	5013	Keystone
7	TP2–TP5, TP11, TP16, TP19	5012	Test Point, White, Thru Hole	0.125 0 × 0.125 inch	5012	Keystone
4	TP8, TP12, TP14, TP15	5011	Test Point, Black, Thru Hole	0.125 0 × 0.125 inch	5011	Keystone
1	U1	FOD817D	IC, Optocoupler, 70-V, 300 - 600% CTR	SMT-4PDIP	FOD817DS	Fairchild
1	U2	TPS23754PWP	IC, IEEE 802.3at PoE Interface and Isolated Converter Controller	PWP20	TPS23754PWP	TI
1	U3	TCMT1107	IC, Photocoupler, 3750VRMS, 80-160% CTR	MF4	TCMT1107	Vishay
1	U4	TLV431A	IC, Shunt Regulator, 6V, 10mA, 1%	SOT23-5	TLV431ACDBVR	TI
6	—		Shunt, Black	100-mil	929950-00	3M
4		2566	Rubber Bumbers		2566	
1	—		PCB, 5.90 In × 2.03 In × 0.062 In		HPA420	Any

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 0 V to 57 V and the output voltage range of 4 V to 6 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 80°C. The EVM is designed to operate properly with certain components above 80°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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