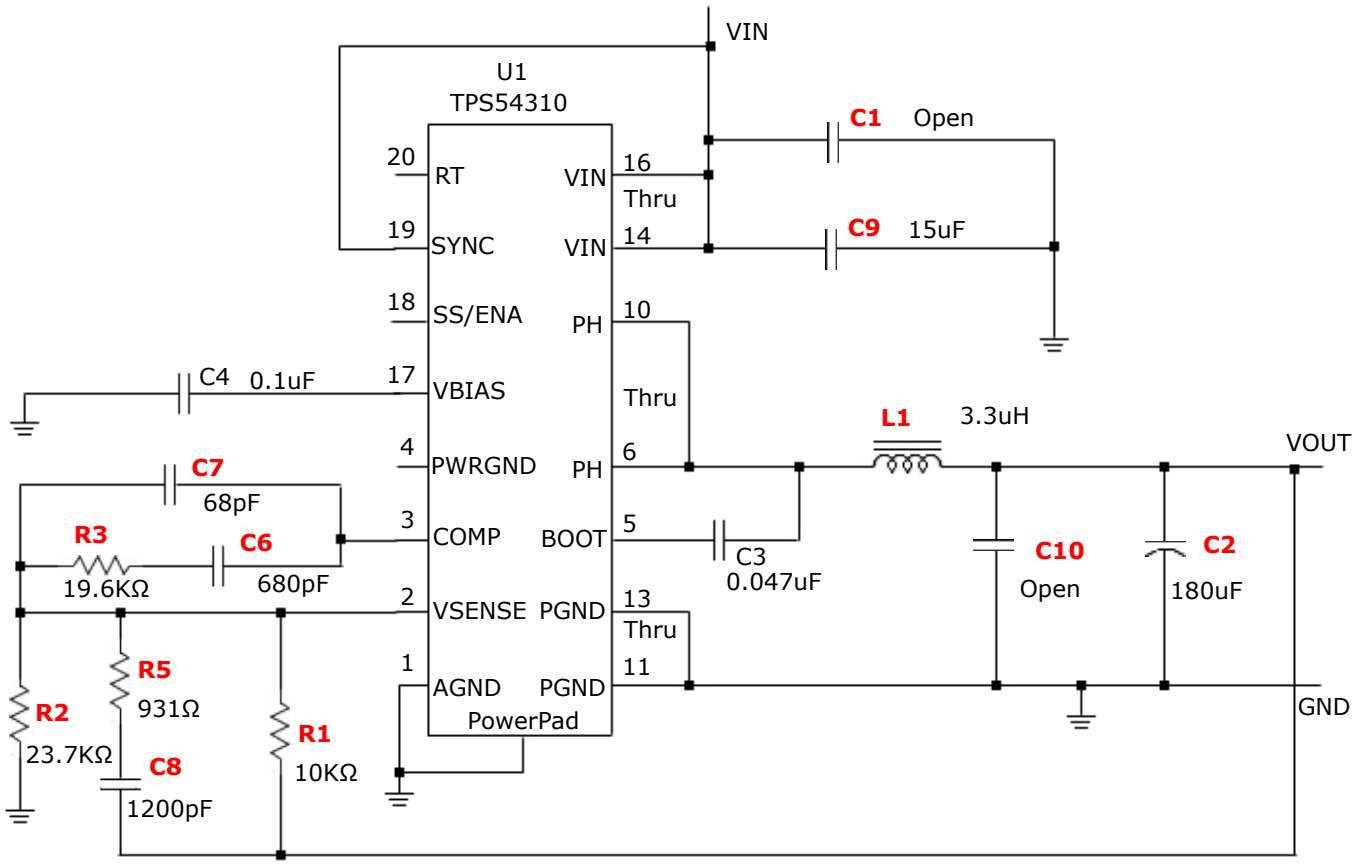
SwitcherPro Design Report
Schematic

Design Name: TPS54310 5.5V to 1.26V @ 3A **Part:** TPS54310

VinMin: 4.5V **VinMax:** 5.5V **Vout:** 1.26V **Iout:** 3A



SwitcherPro Design Report
Analysis - Main

Design Name: TPS54310 5.5V to 1.26V @ 3A **Part:** TPS54310

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Parameter Units-Symbol	User Input Minimum	User Input Nominal	User Input Maximum	Default Input Minimum	Default Input Nominal	Default Input Maximum	Calculated Minimum	Calculated Nominal	Calculated Maximum
Input Voltage Volts - V	4.50	-	5.50	-	-	-	-	-	-
Input Ripple mVp-p - mVp-p	-	-	-	-	-	110	-	-	105.6
UVLO(Start) Volts - V	-	-	-	-	-	-	-	2.95	-
UVLO(Stop) Volts - V	-	-	-	-	-	-	-	2.80	-
Switching Frequency KHz - KHz	-	-	-	-	550	-	-	-	-
Slow Start ms - ms	-	-	-	-	3.00	-	-	-	-
Estimated PCB Area mm² - mm²	-	-	-	-	-	-	-	398	-
Max Component Height mm - mm	-	-	-	-	-	25	-	-	4

SwitcherPro Design Report
Analysis - Output1

Design Name: TPS54310 5.5V to 1.26V @ 3A **Part:** TPS54310

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Parameter Units-Symbol	User Input Minimum	User Input Nominal	User Input Maximum	Default Input Minimum	Default Input Nominal	Default Input Maximum	Calculated Minimum	Calculated Nominal	Calculated Maximum
Output Voltage Volts - V	-	1.260	-	-	-	-	1.247	-	1.287
Output Ripple mVp-p - mVp-p	-	-	-	-	-	25	-	-	3.3
Output Current Amps - A	-	-	3.000	0.100	-	-	-	-	-
Inductor Peak to Peak Current Amps - A	-	-	-	-	-	-	0.617	-	0.667
Current Limit Threshold Amps - A	-	-	-	-	4.500	-	-	-	-
Gain Margin dB - dB	-	-	-	-10	-	-	-	-37	-
Phase Margin Deg. - Deg.	-	-	-	45	-	-	-	45	-
Upper FET RDSon mOhms - mΩ	-	-	-	-	-	-	64	-	73
Lower FET RDSon mOhms - mΩ	-	-	-	-	-	-	64	-	73
Duty Cycle % - %	-	-	-	-	-	-	27.2	-	33.9
On Time Min (switch) ns - ns	-	-	-	-	-	-	449.8	-	683.9
Cross Over Frequency KHz - KHz	-	-	-	-	-	-	-	37	-

SwitcherPro Design Report
Stress Results

Design Name: TPS54310 5.5V to 1.26V @ 3A **Part:** TPS54310

VinMin: 4.5V **VinMax:** 5.5V **Vout:** 1.26V **Iout:** 3A

Device	Rated Voltage	Calculated Voltage	Rated Current (RMS)	Calculated Current (RMS)	Error Message	Power	Calculated Max Temp
C9 (High Freq. Input Cap)	25V	5.53V	3.36A	1.38A	-	6mW	-
C2 (Bulk Output Cap)	6.3V	1.27V	4A	0.19A	-	185uW	-
L1 (Output Inductor)	-	-	4.6A	3.01A	-	136mW	-
U1 (Converter)	10V	5.53V	4A	3.01A	-	839mW	37°C

SwitcherPro Design Report

Efficiency

Design Name: TPS54310 5.5V to 1.26V @ 3A **Part:** TPS54310

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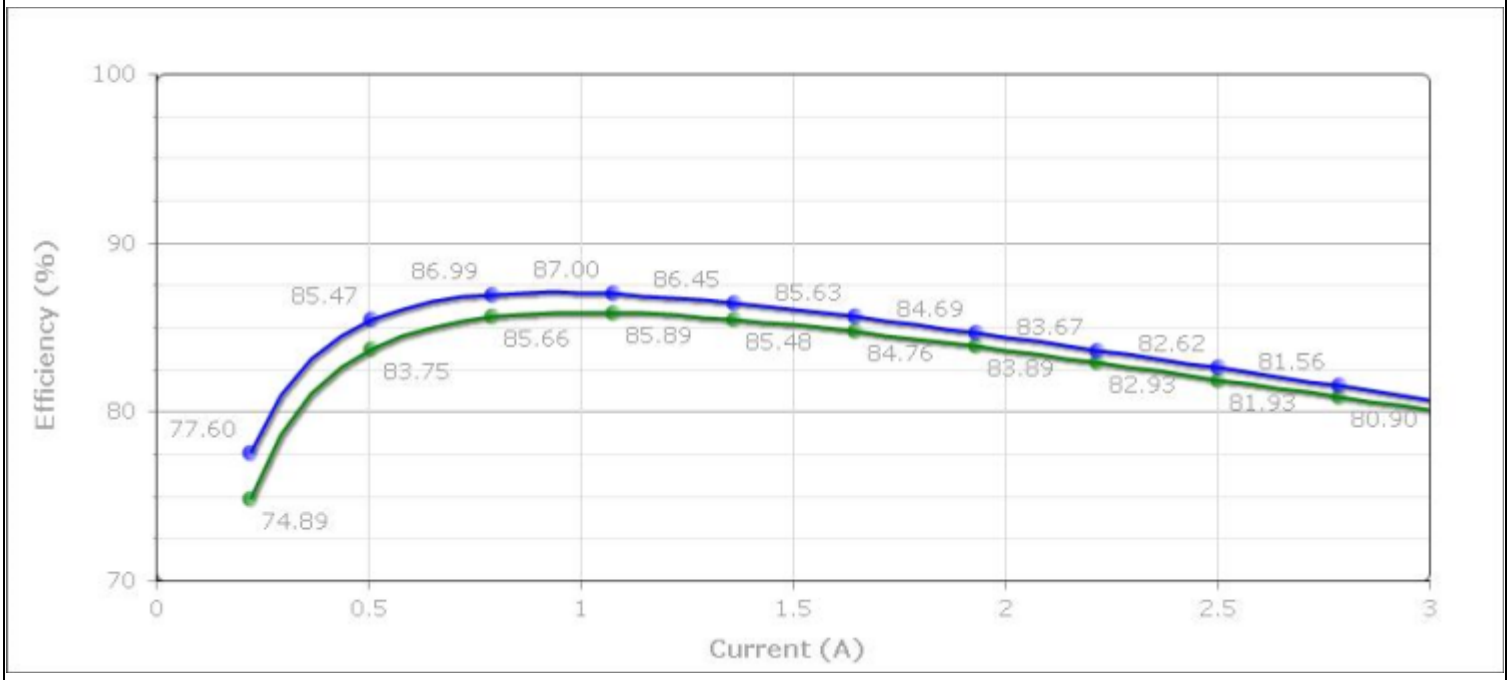
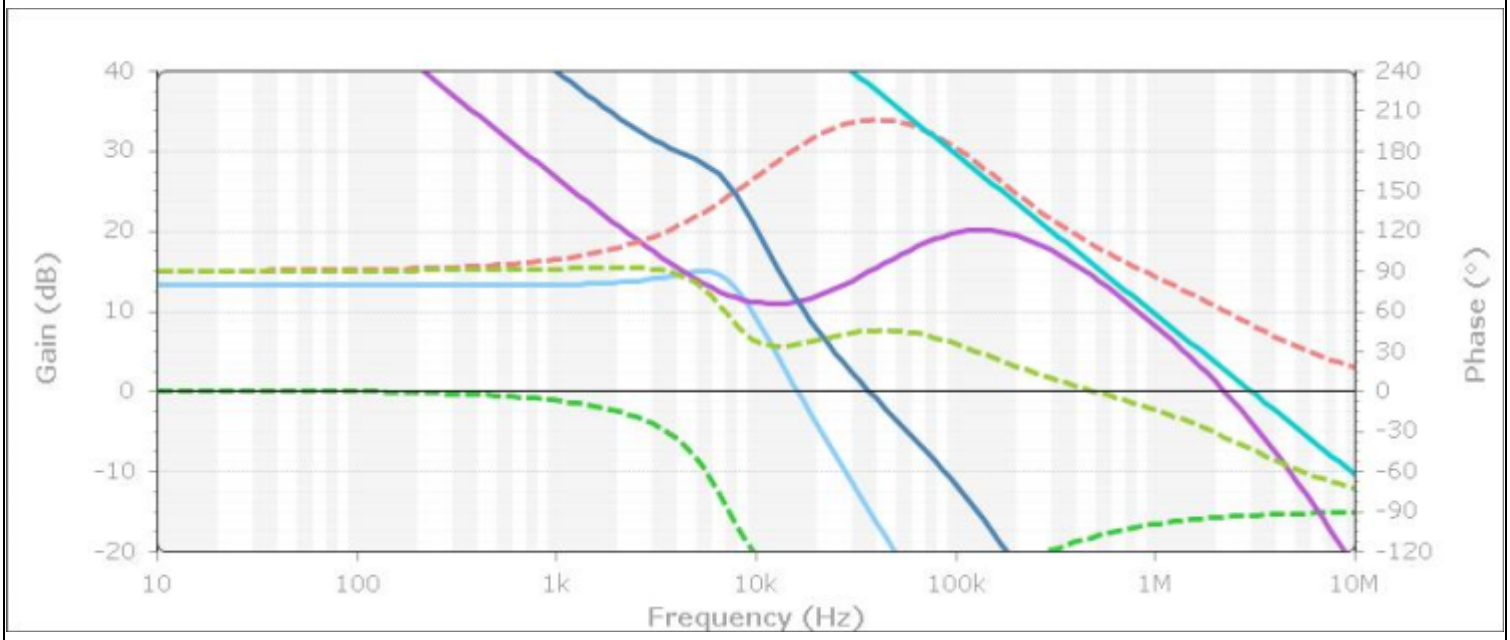


Efficiency For Vin Max
Efficiency For Vin Min

SwitcherPro Design Report
Loop Response

Design Name: TPS54310 5.5V to 1.26V @ 3A **Part:** TPS54310

VinMin: 4.5V **VinMax:** 5.5V **Vout:** 1.26V **Iout:** 3A



- Power Stage Gain
- Power Stage Phase
- Compensation Gain
- Compensation Phase
- Error Amp Gain
- Total Gain
- Total Phase

SwitcherPro Design Report
Bill of Materials

Design Name: TPS54310 5.5V to 1.26V @ 3A **Part:** TPS54310

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Name	Quantity	Part Number	Description	Manufacturer	Package	Area(mm²)	Height(mm)
C2	1	EEFSE0J181R	Capacitor, NA, 180uF, 6.3V, 20%	Panasonic	EEFSDE	32	4
C3	1	Standard	Capacitor, Ceramic, 0.047uF, 20V, 10%	Standard	0805	3	1
C4	1	Standard	Capacitor, Ceramic, 0.1uF, 20V, 10%	Standard	0603	2	1
C6	1	Standard	Capacitor, Ceramic, 680pF, 4V, 20%	Standard	0603	2	1
C7	1	Standard	Capacitor, Ceramic, 68pF, 4V, 20%	Standard	0603	2	1
C8	1	Standard	Capacitor, Ceramic, 1200pF, 4V, 20%	Standard	0603	2	1
C9	1	C4532X5R1E156M	Capacitor, Ceramic, 15uF, 25V, 20%	TDK	C4532 1812	16	2
L1	1	SRU1028-3R3Y	Inductor, 3.3uH, 4.6A, 15mΩ	Bourns	SRU1028	100	2
R1	1	Standard	Resistor, SurfaceMount, 10KΩ, 100mW, 1%	Standard	0603	2	1
R2	1	Standard	Resistor, SurfaceMount, 23.7KΩ, 100mW, 1%	Standard	0603	2	1
R3	1	Standard	Resistor, SurfaceMount, 19.6KΩ, 100mW, 1%	Standard	0603	2	1
R5	1	Standard	Resistor, SurfaceMount, 931Ω, 62mW, 1%	Standard	0603	2	1
U1	1	TPS54310	IC, Converter, 20 pins	Texas Instruments, Inc.	PWP	45	1

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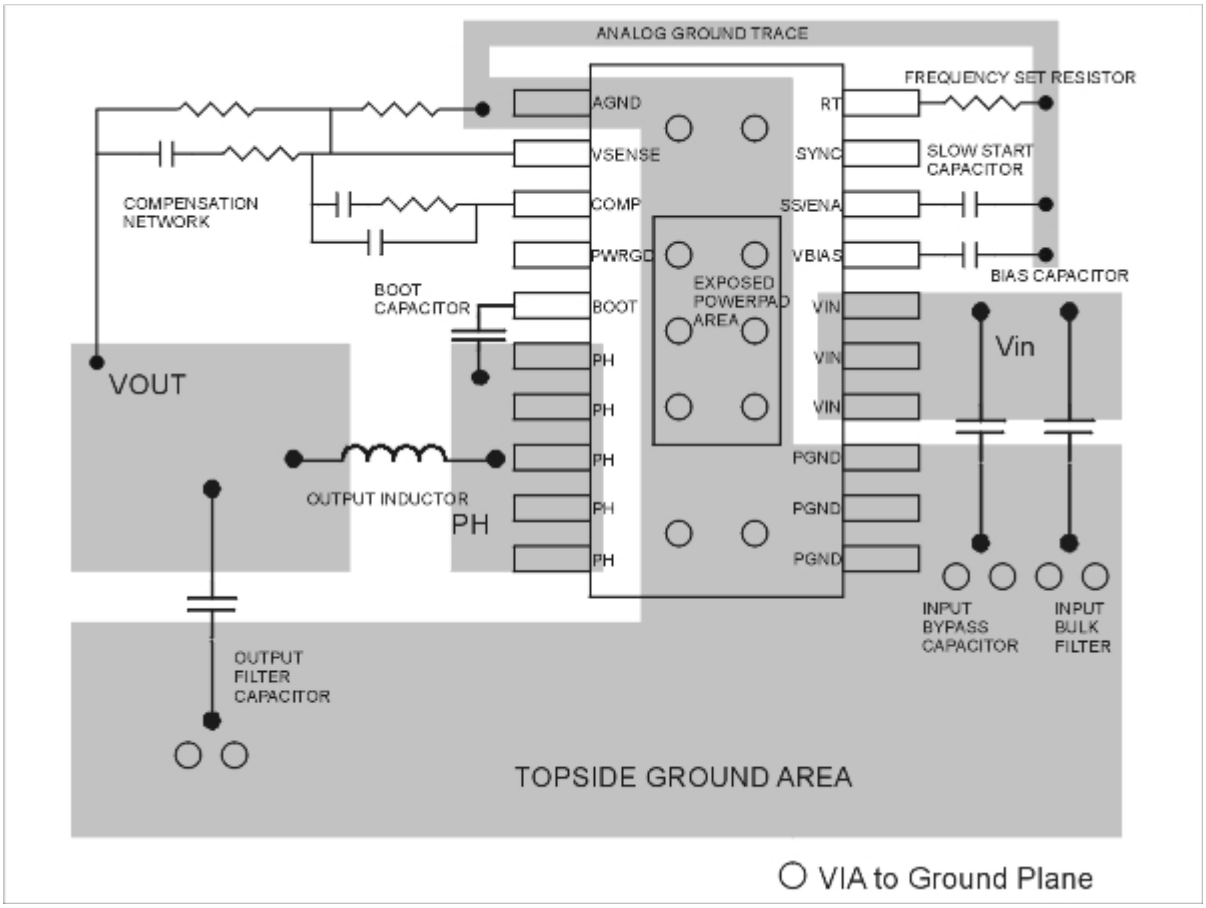

TPS54110, TPS54310, TPS54610, TPS54810, TPS54910

The VIN pins should be connected together on the printed circuit board (PCB) and bypassed with a low ESR ceramic bypass capacitor. Care should be taken to minimize the loop area formed by the bypass capacitor connections, the VIN pins, and the TPS54X10 ground pins. The minimum recommended bypass capacitance is 10 uF ceramic with a X5R or X7R dielectric and the optimum placement is closest to the VIN pins and the PGND pins.

There should be an area of ground on the top layer directly under the IC, with an exposed area for connection to the PowerPAD. Use vias to connect this ground area to any internal ground planes. Use additional vias at the ground side of the input and output filter capacitors as well. The AGND and PGND pins should be tied to the PCB ground by connecting them to the ground area under the device as shown. Use a separate wide trace for the analog ground signal path. This analog ground should be used for the voltage set point divider, timing resistor RT, slow start capacitor and bias capacitor grounds.

The PH pins should be tied together and routed to the output inductor. Since the PH connection is the switching node, inductor should be located very close to the PH pins and the area of the PCB conductor minimized to prevent excessive capacitive coupling.

Connect the boot capacitor between the phase node and the BOOT pin as shown. Keep the boot capacitor close to the IC and minimize the conductor trace lengths.

Connect the output filter capacitor(s) as shown between the VOUT trace and PGND. It is important to keep the loop formed by the PH pins, Lout, Cout and PGND as small as is practical.

Place the compensation components from the VOUT trace to the VSENSE and COMP pins. Do not place these components too close to the PH trace. Due to the size of the IC package and the device pin-out, they will have to be routed somewhat close, but maintain as much separation as possible while still keeping the layout compact.

Connect the bias capacitor from the VBIAS pin to analog ground using the isolated analog ground trace. If a slow-start capacitor or RT resistor is used, or if the SYNC pin is used to select 350 kHz operating frequency, connect them to this trace as well.