UCC28C4x Legacy IC Transition Guide – feedback loop

VOUT regulation via FB pin vs. COMP pin:

- 300mm ICs require components to tolerate I_{COMP} up to 5.5mA.

Use Case Summary:

- VOUT regulation via FB pin **is unaffected** (Figure 1)
- VOUT regulation via COMP pin may need a modification (Figure 2)

Solution:

- Update one resistor value (RF). No PCB layout change needed
- Solution will work for both legacy and 300m ICs

How to calculate new RF value?

RF = (VOUT – V_{TL431} – VF) / IF

Example	Parameters
I_{RD} = VF / RD = 1.15V / 1kΩ = 1.15mA	Requirement: • I_{COMP_MAX} = 5.5 mA Assumptions: • VOUT = 15V • U1, V_{TL431}, cathode V_{MIN} = 2.5V • U2 diode VF = 1.15V • RD = 1 kΩ • CTR = 1 (100%)
I_{FO} = I_{COMP} / CTR = 5.5 mA / 100% = 5.5 mA	
IF = I_{RD} + I_{FO} = VF/RD + I_{FO} = 1.15 mA + 5.5 mA = 6.65 mA	
RF = (**VOUT** – V_{TL431} – **VF**) / **IF** = (15V – 2.5V – 1.15V) / 6.65 mA = 1.71kΩ	

Figure 1 – VOUT regulation via **FB** pin

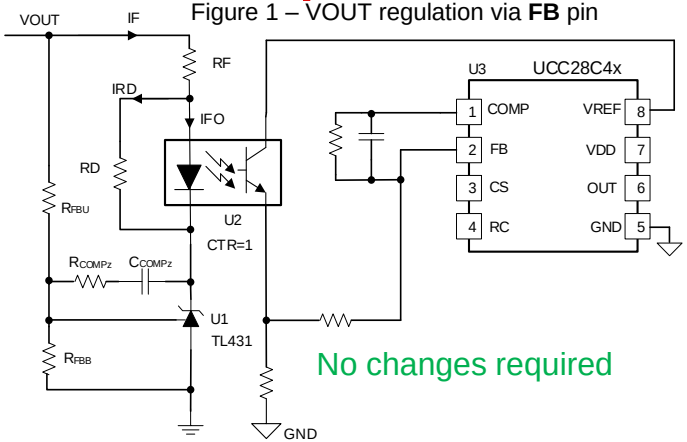
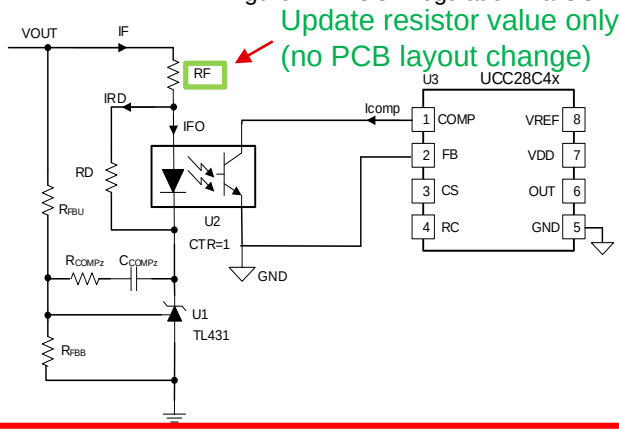


Figure 2 – VOUT regulation via **COMP** pin



UCC28C4x Legacy IC Transition Guide – Op-Amp comparison

Old Devices

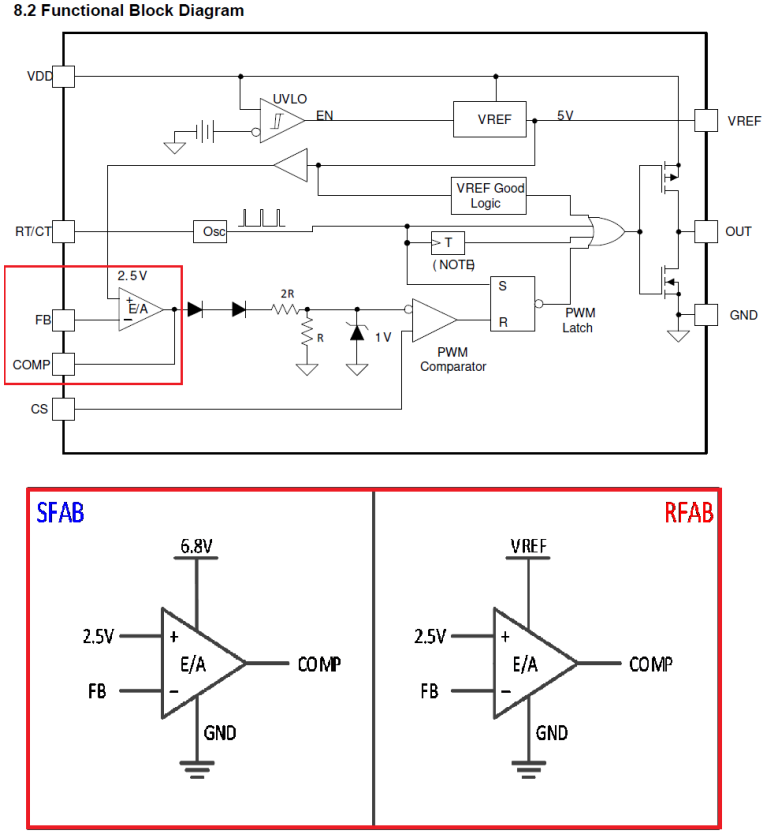
ERROR AMPLIFIER						
V_{FB}	Feedback input voltage, initial accuracy	V_{COMP} = 2.5 V, T_A = 25°C	2.475	2.5	2.525	V
	Feedback input voltage, total variation	V_{COMP} = 2.5 V	2.45	2.5	2.55	V
I_{FB}	Input bias current	V_{FB} = 5 V		–0.1	–2	µA
A_{VOL}	Open-loop voltage gain	2 V ≤ V_{OUT} ≤ 4 V	65	90		dB
	Unity gain bandwidth	See (2)	1	1.5		MHz
PSRR	Power supply rejection ratio	12 V ≤ V_{VDD} ≤ 18 V	60			dB
	Output sink current	V_{FB} = 2.7 V, V_{COMP} = 1.1 V	2	14		mA
	Output source current	V_{FB} = 2.3 V, V_{COMP} = 5 V	–0.5	–1		mA
No specs in history						
VOH	High-level COMP voltage	V_{FB} = 2.7 V, R_{COMP} = 15 kΩ COMP to GND	5	6.8		V
VOL	Low-level COMP voltage	V_{FB} = 2.7 V, R_{COMP} = 15 kΩ COMP to VREF		0.1	1.1	V

New Devices

ERROR AMPLIFIER						
V_{FB}	Feedback input voltage, initial accuracy	V_{COMP} = 2.5 V, T_J = 25°C	2.475	2.5	2.525	V
	Feedback input voltage, total variation	V_{COMP} = 2.5 V	2.45	2.5	2.55	V
I_{FB}	Input bias current (source current)	V_{FB} = 5 V		0.1	2	µA
A_{VOL}	Open-loop voltage gain	2 V ≤ V_{OUT} ≤ 4 V	65	90		dB
	Unity gain bandwidth	See (2)	1	1.5		MHz
PSRR	Power supply rejection ratio	12 V ≤ V_{VDD} ≤ 18 V	60			dB
	Output sink current	V_{FB} = 2.7 V, V_{COMP} = 1.1 V	2	14		mA
	Output source current	V_{FB} = 2.3 V, V_{COMP} = 5 V	0.5	1		mA
	Output source current(2)	V_{FB} ≤ 2.3V, V_{COMP} = 0V			5.5	mA
VOH	High-level COMP voltage	V_{FB} = 2.7 V, R_{COMP} = 15 kΩ COMP to GND	V_{REF} - 0.2			V
VOL	Low-level COMP voltage	V_{FB} = 2.7 V, R_{COMP} = 15 kΩ COMP to VREF		0.1	1.1	V

UCC28C4x Legacy IC Transition Guide – why COMP current increased

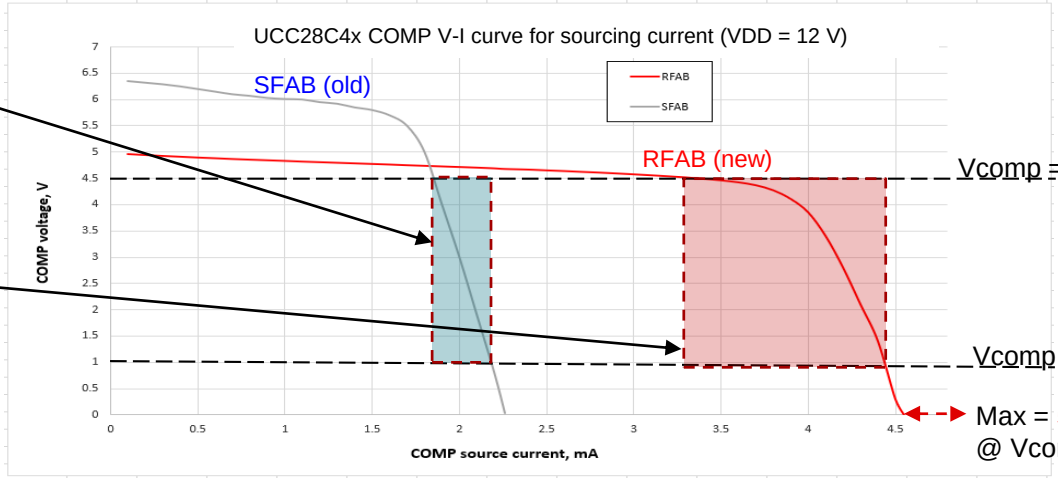
- Refer to the block diagram – notice the red blocked portion.
- The internal bias voltage for RFAB silicon was generated in a different way compared to SFAB silicon due to process technology differences.
- This led to the change in COMP pin source current to 5.5-mA max in order to achieve the same silicon performance(previously no datasheet maximum/parameter specified)

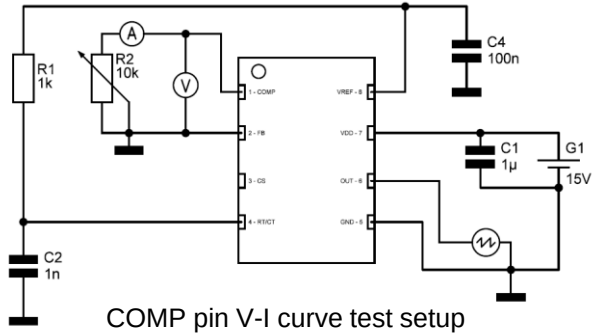


COMP Sourcing Current Voltage V-I Curve Comparison

➢ **COMP sourcing current V-I different between SFAB and RFAB (not a datasheet spec)**

- COMP effective range 1.0V to 4.5V
- "Old" (SFAB) works ok in the blue region as COMP voltage can be adjusted
- Same 0 to 2.5mA for "new" (RFAB) COMP voltage will keep above 4.5V, so not in the COMP effective region, then the regulation is not achieved
- Design check and / or adjustment is required when replace "old" with "new" to get COMP pin able to source max 5mA (5.5mA)
- Components associated need to tolerate 5mA. 10mA tolerance recommended to provide margin
- BOM changes only.
- Solution will work for both SFAB and RFAB devices





COMP pin V-I curve test setup