

UCD74120 Power Sequence Requirement

ABSTRACT

UCD74120 is a Synchronous Buck Power Stage, designed to work with UCD92xx Digital PWM System Controllers. If UCD74120 is powered before UCD92xx, a current limiting resistor is needed in the FLT pin path to avoid potential device damage.

1 UCD74120 UVLO Fault Assertion at Power-up

UCD74120 asserts undervoltage Lockout (UVLO) fault at power-up. The UVLO fault is asserted when BP3 voltage rises above 2.4 V, and is de-asserted when AVGG voltage rises above the UVLO-ON threshold (typically 4.4 V). The UVLO fault causes the FLT pin to be asserted for a short period at power-up. The sequence is illustrated in [Figure 1](#).

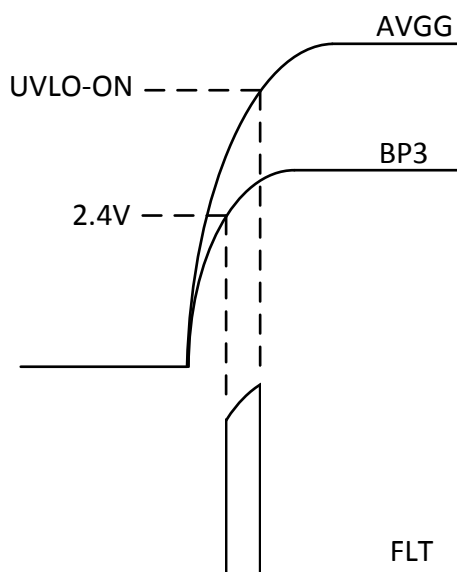


Figure 1. UCD74120 UVLO Fault Assertion at Power-up

2 FLT Pin Short-circuit Path at Power-up

The FLT pin of UCD74120 is connected to the FLT pin of digital controller (UCD92xx). If UCD74120 is powered before UCD92xx, the 3.3-V supply rail of UCD92xx is still at ground potential when UCD74120 asserts UVLO fault. The UCD74120 FLT output will forward-bias the ESD protection diode inside the UCD92xx FLT pin to its 3.3-V supply rail, causing a short-circuit path. The short-circuit current can potentially damage UCD74120. If such a failure occurs, UCD74120 will not operate. The short-circuit path is illustrated in [Figure 2](#). The diode's forward voltage drop is 0.6 V.

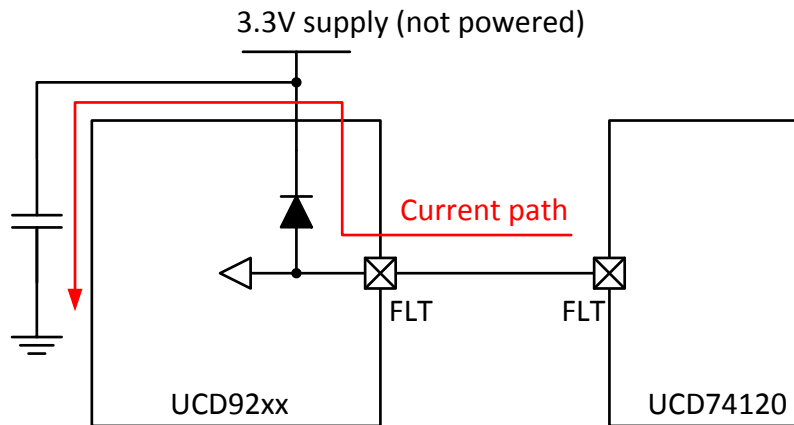


Figure 2. FLT Pin Short-circuit Current Path at Power-up

3 Power Sequence Requirement and Workaround

To avoid the FLT pin short-circuit condition at power-up, UCD92xx and UCD74120 should be powered at the same time. If UCD74120 must be powered prior UCD92xx, a current limiting resistor should be inserted in the FLT pin path to limit the FLT pin current at power-up. The suggested circuit is illustrated in Figure 3.

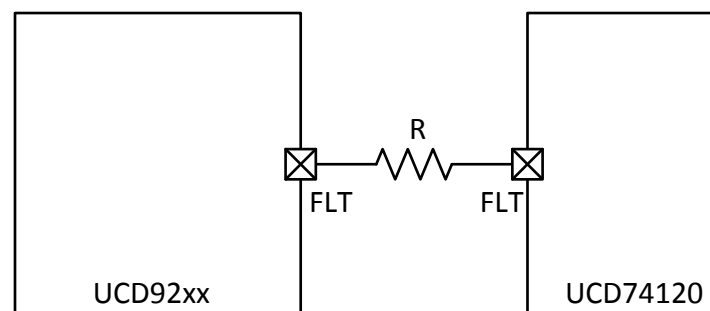


Figure 3. Insert Resistor to Limit FLT Path Current at Power-up

The maximum allowed current on the UCD74120 FLT pin is 15 mA. The internal resistance in the path of powering the FLT pin is 63 Ω – 85 Ω across the temperature range. With design margin considered, the suggested current limiting resistor value is:

$$R = \frac{3.3 \text{ V} - 0.6 \text{ V}}{10 \text{ mA}} - 63 \Omega = 207 \Omega \cong \text{at } 200 \Omega \quad (1)$$

Therefore, if UCD74120 is powered up prior UCD92xx, a 200- Ω resistor in the FLT path is recommended to limit the FLT pin current. Higher R value can better limit the current but unnecessarily reduces the current driving capacity of the FLT pin.

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