DVR RDK App Notes On AVS

DM8168 AVS PMBus Driver User Guide

Introduction

SmartReflex-AVS is a technology that uses adaptive power supply to achieve the goal of reducing active power consumption. DM816x device have Class 2B implementation of smart reflex and this allows dynamic AVS using software.

PMBus specific driver support is required for PMIC's such as TP40400 present in DM816x based device. PMBus is an open standard protocol that defines a means of communicating with power conversion and other devices. It is a communications protocol based on I2C. Hence it is just a specification or a wrapper over I2C.

TPS40400 is a buck controller and allows programming and monitoring via the PMBus interface. The TPS40400 supports a subset of the commands in the PMBus 1.1 specification.

Acronyms & definitions

AVS	Adaptive Voltage Scaling
SR	SmartReflex
HVT	High Voltage Threshold sensor
SVT	Standard Voltage Threshold sensor
GPIO	General Purpose Input Output
PMIC	Power Management Integrated Circuit
VR	Voltage regulator
PMBus	Power Management Bus

Driver Configuration

This section describes about the kernel configurations for PMBus driver & its dependencies

Voltage Regulator Driver configuration

The default kernel configuration enables support for TPS40400 PMBus voltage regulator Driver (built into the kernel).

To enable or disable TPS40400 PMBus based voltage regulator driver kernel build, follow these steps:

$ make CROSS_COMPILE=arm-none-linux-gnueabi- ARCH=arm menuconfig

Select Device Drivers from the main menu.

- Power management options --->
- [*] Networking support --->
- Device Drivers --->
- File systems --->
- ...

Select Voltage and Current Regulator Support from the menu.

- Sonics Silicon Backplane --->
- -*- Multifunction device drivers --->
- -*- Voltage and Current Regulator Support --->
- <*> Multimedia support --->
- ...

Select TI TPS40400 PMBus PMIC from the menu

- < > National Semiconductors LP3972 PMIC regulator driver
- <*> TI TPS40400 PMBus PMIC
- <*> GPIO voltage regulator
- < > TI TPS6507X Power regulators
- < > Intersil ISL6271A Power regulator
- ...

After doing driver selection, exit and save the kernel configuration when prompted.

Kernel Building

Once the configuration done according to your requirement then build the kernel by referring Compiling Linux Kernel part of PSP User Guide

Using this Driver

Type the below commands to enable/disable the driver at the Linux prompt manually:

$ mount -t debugfs debugfs /sys/kernel/debug

Enable

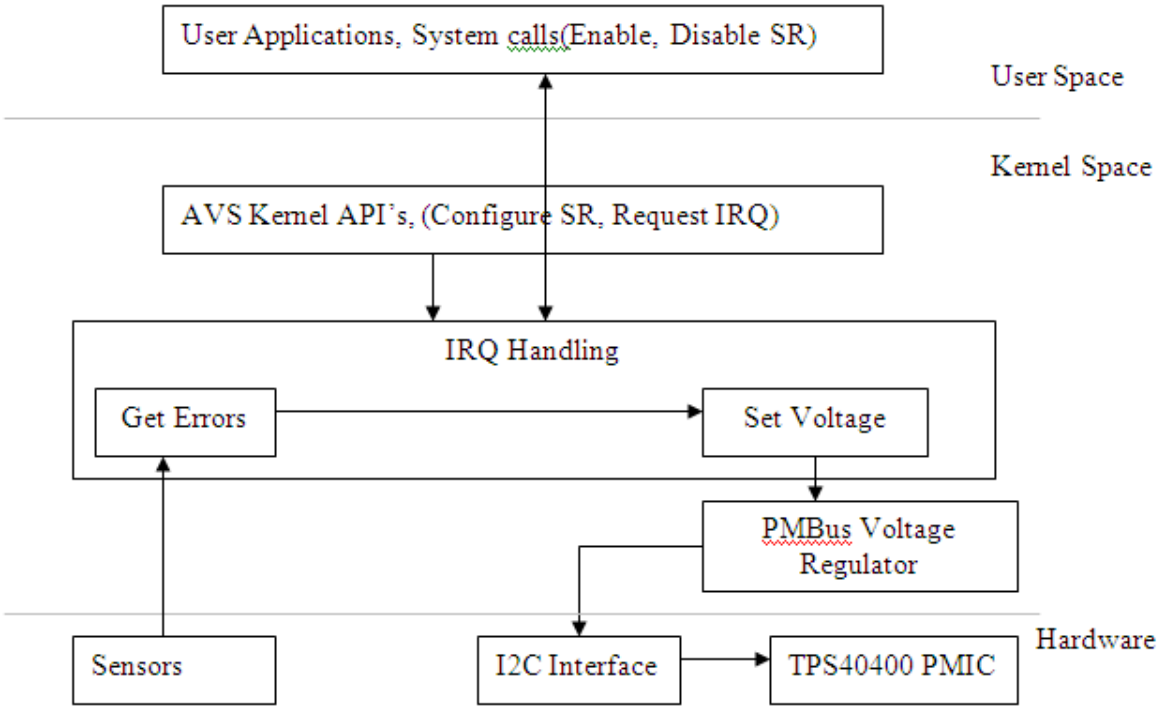
$ echo 1 > /sys/kernel/debug/smartreflex/autocomp

Note: This is enabled by default in the driver, hence the above steps may not be required

Disable

$ echo 0 > /sys/kernel/debug/smartreflex/autocomp

SmartReflex-PMBus Driver Architecture



Features

The AVS driver supports following features

- Supports the PMIC TPS40400
- Supports both HVT and SVT sensors
- Voltage control over PMBus-I2C lines

Implemented PMBus Commands

The voltage regulator driver which has been developed for AVS supports the following PMBus commands only required for the this purpose:

- **PMBUS_OPERATION**

The OPERATION command is used to turn the device output on or off. It is also used to set the output voltage to the upper or lower MARGIN voltages.

- **PMBUS_CLEAR_FAULTS**

The CLEAR_FAULTS command is used to clear any fault bits that have been set.

- **PMBUS_VOUT_MODE**

It is a byte that consists of a 3-bit Mode and 5-bit exponent parameter, as shown below. The 3-bit Mode sets whether the device uses the Linear or Direct modes for output voltage related commands. The 5-bit parameter sets the exponent value for the linear data mode. It is a read only based command.

- **PMBUS_VOUT_TRIM**

The VOUT_TRIM command is used to apply a fixed offset voltage to the output voltage command value.

- **PMBUS_VOUT_CAL_OFFSET**

This command applies an offset to the READ_VOUT command results to calibrate out offset errors in the on board measurement system.

- **PMBUS_VOUT_CAL_GAIN**

This command applies a gain correction to the READ_VOUT command results to calibrate out gain errors in the on board measurement system.

- **PMBUS_IOUT_CAL_GAIN**

The IOUT_CAL_GAIN is the ratio of the voltage at the current sense element to the sensed current

- **PMBUS_FREQUENCY_SWITCH**

The FREQUENCY_SWITCH command sets the switching frequency.

- **PMBUS_VOUT_SCALE_LOOP**

VOUT_SCALE_LOOP is equal to the feedback resistor ratio. The nominal output voltage is set by a resistor divider and the internal 600mV reference voltage.

- **PMBUS_READ_VOUT**

The READ_VOUT commands returns data that represents the output voltage of the controller.

- **PMBUS_REVISION**

The PMBUS_REVISION command returns data that indicates that the TPS40400 is compliant with the 1.1 revision of the PMBus specification.

Additions made to the Kernel to Support AVS with a PMBus based PMIC

Note: This section is only meant for modifications related to controlling the vdd_avs voltage from SmartReflex driver

1. Implement voltage regulator for chosen PMBus based PMIC and provide the generic calls to the SmartReflex driver
   Like, regulator_get(), regulator_get_voltage(), regulator_set_voltage(). If needed provide the enable and disable hook ups.
   For reference go through voltage regulator driver at "drivers/regulator/tps40400-regulator.c". Current implementation of SmartReflex driver uses this PMBus based voltage regulator
2. Add Voltage Regulator platform specific data to the board file at "arch/arm/mach-omap2/board-ti8168evm.c".
   Change the pmbus_pmic_init_data for the max and min voltage defaults specific to the PMIC.
   Change the PMBus-I2C address which is specific to the PMIC. Here
   “I2C_BOARD_INFO("pmbus", 0x38)”
3. Add SR platform specific data based on the chosen PMIC to the devices file at "arch/arm/mach-omap2/devices.c", so that SR driver request the same
   These fields must change according to the PMIC
   a. voltage domain name, which is registered as a supply name in voltage regulator driver
      .vd_name = "vdd_avs",
   b. Step size of the PMIC, which is used to calculate the voltage delta
      .vstep_size = 15000, Ex: 15mV, which is a default one for voltage regulator.
4. Based on voltage step size, modify err_minlimit & e2v_gain fields in ti816x_sr_sdata structure,
   <html />http://processors.wiki.ti.com/index.php/
   TI81XX_PSP_AVS_Driver_Guide#Supporting_AVS_with_a_different_PMIC

5. Based on the platform change the nominal voltage value & the exponent for PMIC here in this file "drivers/regulator/tps40400-regulator.c"

pmic->exponent = -10; /*Set this as per default value for PMIC(TPS40400)*/
pmic->nominal_uV = 1000000; /* For DM8168 - nominal voltage is 1V)*/

TPS40400 Configurations

AVS Control System

The AVS control system in context with the TPS40400 has been described in much details in the below sections

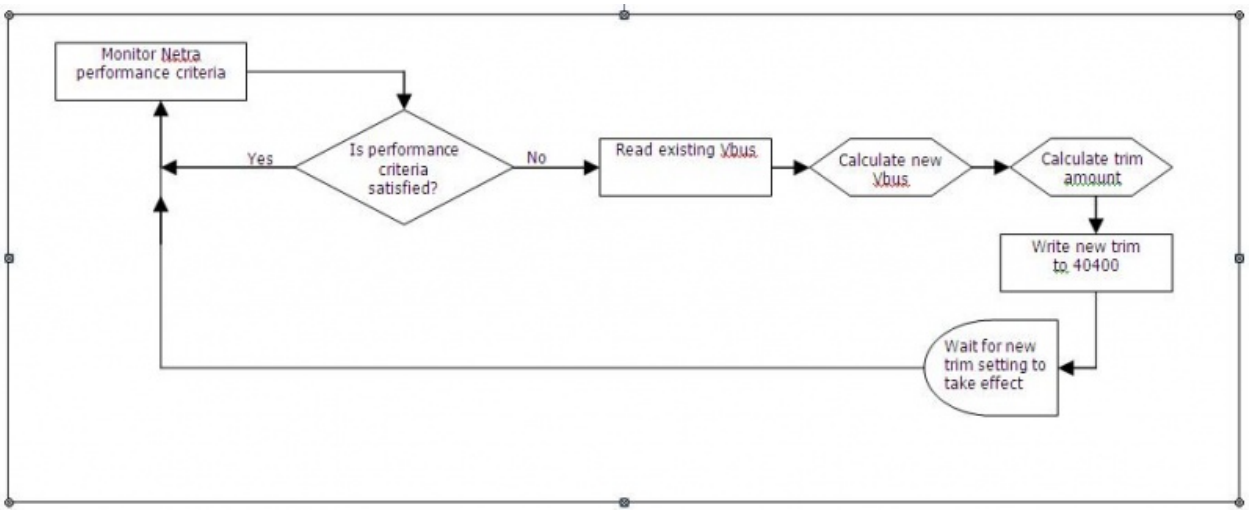
Description

The purpose of this section is to provide details behind the necessary steps required to successfully implement an AVS control algorithm for the TPS40400.

In an AVS control system, the output voltage bus that is produced and controlled by the TPS40400 (hereafter called “Vbus”) is monitored by another device (external to the TPS40400) and can be adjusted by that external device in order to meet some specified dynamic performance requirements. A typical application would be the Vbus for a device like the Netra TMS320DM8168 Digital Media Processor (hereafter called Netra). This device requires that the Vbus be adjusted during live operation so that performance speed and power consumption are maintained at optimal levels. This document will describe an AVS control system for such an application.

The TPS40400 is an analog controller (analog control loop, analog PWM) but it has an integrated PMBus interface. This interface can be used to retrieve real-time operating conditions such as output voltage and current, and it can also be used to trim the Vbus during operation.

For a typical AVS control system, the host, in this case the Netra, monitors its own performance parameters(SR) and based on those parameters it can determine if a new/different Vbus setting is required to maintain optimal performance. In simple terms, Netra might apply the following:



This simplified flow chart highlights a possible process that Netra could use to adjust the Vbus based on Netra’s own performance needs.

As stated, the 40400 is an analog controller which is capable of controlling its duty cycle to any required value, subject to the limitations of the 40400 controller specifications.

Output voltage trim logic

However, the PMBus interface is digital in nature and as such it imposes limitations on the trim settings as well as the voltage readback resolution. The manner in which trim is achieved in the 40400 is by changing the internal reference by a fixed number of steps over a fixed range. The nominal reference voltage is 600mV, and the adjustment range for the reference is +/- 25%, or from 450mV to 750mV. The trim resolution is based on a 7-bit architecture, which implies a total of (2^7), or 128 discrete steps. Each step is then defined by Equation 1:

$$\text{Vref trim step size} = \frac{(750\text{m} - 450\text{m})}{2^7} = 2.34375\text{mV}$$

The trim setting is controlled by this 7-bit word mantissa. This mantissa can be set anywhere from 0000000 to 1111111, or in hex from 0x00 to 0x7F.

This result in the following available reference voltages (not all steps are shown):

	Mantissa Bits								
Decimal	MSB **6**	**5**	**4**	**3**	**2**	**1**	LSB **0**	**Available Vref Steps**	**Comment**
0	0	0	0	0	0	0	0	450.000E-3	Min value
1	0	0	0	0	0	0	1	452.344E-3	Min + 1 step
2	0	0	0	0	0	1	0	454.688E-3	Min + 2 steps
:	:	:	:	:	:	:	:	:	:
63	0	1	1	1	1	1	1	597.656E-3	No trim -1 step
64	1	0	0	0	0	0	0	**600.000E-3**	**No trim**
65	1	0	0	0	0	0	1	602.344E-3	No trim +1 step
:	:	:	:	:	:	:	:	:	:
125	1	1	1	1	1	0	1	742.969E-3	Max - 2 steps
126	1	1	1	1	1	1	0	745.312E-3	Max - 1 step
127	1	1	1	1	1	1	1	747.656E-3	Max value

The table above shows the available voltage reference settings. The resulting available Vbus settings depend on the resistor divider values in the feedback circuit of the 40400.

As a representative example which abpplies to the DVR-RDK Netra board, if the nominal output voltage is designed to be 1.0V, this defines the ratio of the divider resistors. The upper resistor would be 0.4X, and the lower divider resistor would be 0.6X (X is the same for both values, and would be chosen to yield appropriate real resistor values). If we combine these divider values with the available Vref steps, then these reference voltage steps would then map to the following Vbus steps:

Decimal	Available Vref	*'Available Vbus Steps'*
0	450.000E-3	750.000E-3
1	452.344E-3	753.906E-3
2	454.688E-3	757.813E-3
:	:	:
63	597.656E-3	996.094E-3
64	**600.000E-3**	**1.000E+0**
65	602.344E-3	1.004E+0
:	:	:
125	742.969E-3	1.238E+0
126	745.312E-3	1.242E+0
127	747.656E-3	1.246E+0

This shows that while the step size of the reference is defined by the equation above, which yields a step size of 2.34375mV, the resulting Vbus steps depend on the voltage divider values and are given by Equation 2

$$\text{Vbus trim step size} = \text{Vref Step Size} * \frac{(R_{top} + R_{bottom})}{(R_{bottom})} = (2.34375\text{mV}) * \frac{(0.4 + 0.6)}{0}.6 = 3.90625\text{mV}$$

This implies that for a Vbus with a designed nominal voltage of 1.0V, this Vbus can be trimmed only in integer multiples of 3.90625mV, either up or down, from nominal. So for example, if the Netra desired to set the new Vbus to 1.002V, this Vbus setting would not be possible. The closest achievable Vbus setting would have to be either 1.0000V (no trim) or 1.0039V (1 LSB above no trim).

The preceding is a description of available Vref trim steps. There is another set of constraints to consider when using the 40400 in an AVS control system.

The 40400 can report its actual output voltage (which is Vbus), and this voltage is determined based on a 10-bit architecture. This implies a total of (2^10), or 1024 discrete steps. The range of Vbus measurement is fixed and is 0V to 16V. Each Vbus read step is then defined by Equation 3:

$$\text{Vbus read step size} = \frac{(16 - 0)}{2^{10}} = 15.625\text{mV}$$

This Vbus read step resolution is fixed, and it is not dependent on the Vref trim setting or the feedback resistor divider values. The Vbus read word is reported by a 10-bit word mantissa. This word can be anywhere from 0000000000 to 1111111111, or in a hex word from 0x000 to 0x3FF. In this case, the 10-bit mantissa is embedded in a 16-bit word, and the other 6 bits are not discussed here, but note that the 10-bit mantissa for Read_Vout is mapped to bits 13 through 4.

This results in the following available Vbus read voltages (not all steps are shown):

	Mantissa Bit											
Dec	MSB **13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	LSB **4**	**Available Read_Vout Steps**	**Comment**
0	0	0	0	0	0	0	0	0	0	0	0.000000	Min value
1	0	0	0	0	0	0	0	0	0	1	0.015625	Min + 1 step
2	0	0	0	0	0	0	0	0	1	0	0.031250	Min + 2 steps
:	:	:	:	:	:	:	:	:	:	:	:	:
63	0	0	0	0	1	1	1	1	1	1	0.984375	Nominal -1 step
64	0	0	0	1	0	0	0	0	0	0	1.000000	Nominal Vbus
65	0	0	0	1	0	0	0	0	0	1	1.015625	Nominal +1 step
:	:	:	:	:	:	:	:	:	:	:	:	:
1021	1	1	1	1	1	1	1	1	0	1	15.953125	Max - 2 steps
1022	1	1	1	1	1	1	1	1	1	0	15.968750	Max - 1 step
1023	1	1	1	1	1	1	1	1	1	1	15.984375	Max value

It is important to note that while the available Vbus trim settings have a step size of 3.91mV, the available Read_Vout steps have a step size of 15.625mV (when nominal is 1.0V). This means that there are 4 Vbus trim steps for every Read_Vout step, so it is possible to trim the output voltage by a few steps and not get an appreciable change in the Read_Vout data, even though the actual output voltage will have changed by that many steps. This will be discussed further in the measured data discussion.

As can be seen from the available Read_Vout steps, even though it is possible that the actual output voltage exist between available steps, the 40400 will only report in the available steps. So during an AVS exercise, it would not serve any purpose to expect a Read_Vout result at any voltage other than the available steps. If the Netra wanted a Vbus of 0.996V, the 40400 could only report a Vbus of either 0.984375 or 1.000000V, even though the desired Vbus of 0.996V is achievable from the available Vbus trim steps.

Wait time after a set voltage

The next point to be discussed is particular to the 40400. The 40400 has a configurable soft-start time, and that time can be set to any of several fixed numbers (see 40400 datasheet for details). But this soft start time sets the slew rate for any operation that changes the output voltage, including trim and margin. If for example the nominal Vbus is 1.0V and the soft start time of 2.7mSec was selected in configuration, that means that any trim event would slew at that same rate (in this case 1V in 2.7mSec). So after a trim command is written to the 40400, the host must allow the 40400 enough time to slew the output voltage to the new setting, given this fixed slew rate. This amounts to applying a wait time as shown in Equation 4.

$$\text{Wait time after Trim} \geq \frac{(\text{trim } \delta V) * (\text{TON}_{\text{RISE}}\text{ time})}{(\text{Vout Nominal})}\text{, in Sec, where:}$$

- Wait time is the amount of time between the Trim Vout write and the next Read Vout

- trim δV is the requested change in output voltage from where it is now (the delta V)

- TON_RISE time is the configured soft-start time for the 40400

- Vout Nominal is the un-trimmed nominal Vbus voltage

The reason for this required wait time is because if a Read_Vout is performed before the required wait time, the 40400 will not have completed the transition from old to new Vbus settings. So even if all else was correctly applied

(averaging, dead band), this would result in an unstable AVS algorithm because the Netra would potentially apply a second trim before the first one was completed. The second trim would in all likelihood apply an over-trim, and then a trim would be required in the other direction. Repeat. This would result in oscillations on the Vbus.

Summary

So in summary, these requirements should be included in the AVS algorithm:

- Wait a pre-determined amount of time after a Trim Vout command. The wait time must be at least (Trim delta V)/(Soft Start slew rate)

Voltage Control Logic and Calculations

Setting the VOUT_SCALE_LOOP

This setting is necessary for the correct calculation of the VOUT_TRIM, VOUT_MARGIN_HIGH and VOUT_MARGIN_LOW.
i.) The feedback resistors in the schematic of the DVR RDK are 15k and 10k. The nominal reference (VFB) is 600 mV. The expected output voltage is 10k*0.6/15k = 1.0V.
ii.) VOUT_SCALE_LOOP is defined as VFB/VOUT(nom) = 0.6
iii.) Converting 0.6 to the linear format (Mantissa * 2^ Exponent)
- the exponent is fixed by design at -9 decimal or 10111 binary.
- the mantissa is calculated as 0.6/(2^-9) = 0.6 *2^9 = 0.6 * 512 = 307.2 or 00100110011 as an unsigned binary integer
iv.) The resultant conjugation is 1011 1001 0011 0011 b or B933 h.

Understanding the IOUT_CAL_GAIN

The DCR of the output inductor must be entered into this register. The calculation is as follows:

DCR = (decimal entry)*2-15
The range of programmable DCR is 30.5uΩ to 15.6mΩ, so the range of hex entry is 1h to 200h, and the corresponding range in decimal is 1 to 512.
So for example,
1. If the DCR was 6.348mΩ, you would enter a value of 6.384 *10-3*215= 208 = D0h
2. If the DCR was 2mΩ, you would enter a hex value of 42h, which would give 2.01mΩ
Setting this is a Must. Otherwise reported current, OC Warn and OC Fault will be incorrect.

Checking and setting the offset for VOUT_CAL_OFFSET

READ_VOUT calibration example: On initial system startup, the output is precisely trimmed to be 1.0 volts. Issuing a PMBus read on the READ_VOUT command returns an average value of say the output voltage reading 916 mV so We set vout_cal_offset to be the difference of nominal voltage and the above value as offset required.
Therefore, This command applies an offset to the READ_VOUT command results to calibrate out offset errors in the on board measurement system

Understanding the READ_VOUT Command

The accuracy of this output is greatly influenced by the quality of the PCB layout and the precision of the calibration
i) For example, if issuing a READ_VOUT command returns 480h, this would indicate that the output voltage is 480h * 2^-10 = 1152/1024 = 1.125 volts
ii) Detailed understanding of mechanism to read voltages is mentioned in this section above 10.1.3.

Understanding the VOUT_TRIM Command

This command allows the PMBus host to adjust or trim the output voltage. If you use this command to correct for an offset within your system for absolute accuracy AND use this command to implement DVS, the host will need to account for the fixed offset.

The trimming of output voltage happens in certain steps as descibed in section above
i.) If Vout(nominal) is 1 volt, the range of acceptable values for VOUT_TRIM would be -250 mV to 250 mV.

ii.) Suppose that you choose to increase the output voltage by 100 mV:

1.) First you would calculate the difference between the nominal and the required absolute voltage(current+100mV).

2.) To get to the desired voltage, you would write the above difference to VOUT_TRIM.

Understanding PMBUS_IOUT_OC_FAULT_LIMIT/ PMBUS_IOUT_OC_WARN_LIMIT

The PMBUS_IOUT_OC_FAULT_LIMIT command sets the value of the output current, in amperes, that causes the over-current detector to indicate an over-current fault condition.
The PMBUS_IOUT_OC_WARN_LIMIT command sets the value of the output current, in amperes, that causes the over-current detector to indicate an over-current warning.

Enabling debug logs to check convergence of setting voltages

If you want to see the debug prints of the TPS40400 PMBus based driver and its voltage convergence, enable printing of logs in this file and rebuild the kernel.

"drivers/regulator/tps40400-regulator.c"

```
#if 1
#define dprintk(x...) printk(" [reg] " x)
#else
#define dprintk(x...)
#endif
```

References

http://ap-fpdsp-swapps.dal.design.ti.com/index.php/DVR_RDK_Main_Page

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