	00000000	Address :		0x
	00000000	Default Value		0000
bit	default	Definition	Description	Sett
6	7 0 6 0			(
5				
4	·	0d = Page 0	page页选择	
3			page0x00选择00	
2		 255d = Page 255	page0x01选择01	
1	1 0	2550 = Page 255		
	-			
	<u> </u>			
	00000001	Address	0x01	0x
	00000000	Default Value	0x00	0000
bit	default	Definition	Description	Set
7				
6	6 0			
5				-
4		Reserved		
3	3 0			
2	2 0			-
1	L 0			(
		Software reset. This bit is self-clearing.		
	0	0d = Do not reset	not reset	
`	1	1d = Reset		
		•		
	00000010	Address :	0x02	0x
	00000000	Default Value		0000
bit	default	Definition	Description	Set
7		Reserved		- 001
6				
5				
	†			
4	1 0	The duration of the quick-charge for the VREF external capacitor is set using		
	'l "	an internal series impedance of 200 Ω .		
		0d = VREF quick-charge duration of 3.5 ms (typical)	VREF decoupling 1uF对应延迟时间3.5ms	
		1d = VREF quick-charge duration of 10 ms (typical) 2d = VREF quick-charge duration of 50 ms (typical)	, , , , , , , , , , , , , , , , , , ,	
3	3 0	2d = VREF quick-charge duration of 50 ms (typical) 3d = VREF quick-charge duration of 100 ms (typical)		
		130 based and describe a setting of		
		I2C broadcast addressing setting. Od = I2C broadcast mode disabled; the I2C slave address is determined		
2	, n	based on the ADDR pins	I2C地址根据pin选择	
-	-	1d = I2C broadcast mode enabled; the I2C slave address is fixed at 1001	120-EST [KMpinte]+	
		100		
1	1 0	100		
1	L O	100 Reserved		
		100 Reserved Sleep mode setting.	不进 λ sleen棒式	
1		100 Reserved	不进入sleep模式	
		100 Reserved Sleep mode setting. 0d = Device is in sleep mode	不进入sleep模式	
	0	100 Reserved Sleep mode setting. 0d = Device is in sleep mode 1d = Device is not in sleep mode		
	00000101	100 Reserved Sleep mode setting. 0d = Device is in sleep mode 1d = Device is not in sleep mode Address:	0x05	02
С	00000101	100 Reserved Sleep mode setting. 0d = Device is in sleep mode 1d = Device is not in sleep mode	0x05 0x05	0000
	00000101 00000101 default	100 Reserved Sleep mode setting. 0d = Device is in sleep mode 1d = Device is not in sleep mode Address: Default Value:	0x05	0; 0000 Set
bit 7	0 0 00000101 00000101 default 7 0	100 Reserved Sleep mode setting. 0d = Device is in sleep mode 1d = Device is not in sleep mode Address: Default Value:	0x05 0x05	0x 0000 Set
bit 7	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	100 Reserved Sleep mode setting. 0d = Device is in sleep mode 1d = Device is not in sleep mode Address Default Value	0x05 0x05	0) 0000 Set
bit 7	00000101 00000101 00000101 default 7 0 6 0	100 Reserved Sleep mode setting. 0d = Device is in sleep mode 1d = Device is not in sleep mode Address: Default Value:	0x05 0x05	0) 0000 Set
bit 7	00000101 00000101 default 7 0 6 0	100 Reserved Sleep mode setting. 0d = Device is in sleep mode 1d = Device is not in sleep mode Address: Default Value:	0x05 0x05	0) 0000 Set
	00000101 00000101 default 7 0 6 0 6 0	100 Reserved Sleep mode setting. 0d = Device is in sleep mode 1d = Device is not in sleep mode Address: Default Value : Definition Reserved	0x05 0x05	0) 0000 Set
bit 7	00000101 00000101 default 7 0 6 0 6 0	100 Reserved Sleep mode setting. 0d = Device is in sleep mode 1d = Device is not in sleep mode Address: Default Value: Definition Reserved Shutdown configuration. 0d = DREG is powered down immediately after SHDNZ asserts	0x05 0x05	0) 0000 Set
	00000101 00000101 default 7 0 6 0 6 0	100 Reserved Sleep mode setting. 0d = Device is in sleep mode 1d = Device is not in sleep mode Address: Default Value: Definition Reserved Shutdown configuration. 0d = DREG is powered down immediately after SHDNZ asserts 1d = DREG remains active to enable a clean shut down until a time-out is	0x05 0x05 Description	0; 0000 Set
	00000101 00000101 default 7 0 6 0 6 0	100 Reserved Sleep mode setting. 0d = Device is in sleep mode 1d = Device is not in sleep mode Address: Default Value: Definition Reserved Shutdown configuration. 0d = DREG is powered down immediately after SHDNZ asserts 1d = DREG remains active to enable a clean shut down until a time-out is reached; after the time-out period, DREG is forced to power off	0x05 0x05	0) 0000 Set
	00000101 00000101 default 7 0 5 0 6 0 8 0	100 Reserved Sleep mode setting. 0d = Device is in sleep mode 1d = Device is not in sleep mode Address: Default Value: Definition Reserved Shutdown configuration. 0d = DREG is powered down immediately after SHDNZ asserts 1d = DREG remains active to enable a clean shut down until a time-out is reached; after the time-out period, DREG is forced to power off 2d = DREG remains active until the device cleanly shuts down	0x05 0x05 Description	0) 0000 Set
bit 76 6 5 4 4 3 3	00000101 00000101 default 7 0 5 0 6 0 8 0	Reserved Sleep mode setting. 0d = Device is in sleep mode 1d = Device is not in sleep mode Address: Default Value: Definition Reserved Shutdown configuration. 0d = DREG is powered down immediately after SHDNZ asserts 1d = DREG remains active to enable a clean shut down until a time-out is reached; after the transport period, DREG is forced to power off 2d = DREG remains active until the device cleanly shut down	0x05 0x05 Description	0) 0000 Set
bit 76 6 5 4 4 3 3	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Reserved Sleep mode setting. 0d = Device is in sleep mode 1d = Device is not in sleep mode Address: Default Value: Definition Reserved Shutdown configuration. 0d = DREG is powered down immediately after SHDNZ asserts 1d = DREG remains active to enable a clean shut down until a time-out is reached; after the time-out period, DREG is forced to power off 2d = DREG remains active until the device cleanly shuts down 3d = Reserved	0x05 0x05 Description	0) 0000 Set
bit 77 6 5 4 4 3 3	00000101 00000101 default 6 0 6 0 6 0 7 0 8 0 9 0 1 0	Reserved Sleep mode setting. 0d = Device is in sleep mode 1d = Device is not in sleep mode Address: Default Value: Definition Reserved Shutdown configuration. 0d = DREG is powered down immediately after SHDNZ asserts 1d = DREG remains active to enable a clean shut down until a time-out is reached; after the time-out period, DREG is forced to power off 2d = DREG remains active until the device cleanly shuts down 3d = Reserved These bits set how long DREG remains active after SHDNZ asserts.	0x05 0x05 Description	0) 0000 Set
bit 76 6 5 4 4 3 3	00000101 00000101 default 6 0 6 0 6 0 7 0 8 0 9 0 1 0	100 Reserved Sleep mode setting. 0d = Device is in sleep mode 1d = Device is not in sleep mode Address: Default Value: Definition Reserved Shutdown configuration. 0d = DREG is powered down immediately after SHDNZ asserts 1d = DREG remains active to enable a clean shut down until a time-out is reached; after the time-out period, DREG is forced to power off 2d = DREG remains active until the device cleanly shuts down 3d = Reserved These bits set how long DREG remains active after SHDNZ asserts. 0d = DREG remains active for 30 ms (typical)	0x05 0x05 Description 掉电设置(default)	0: 0000(Set
bit 77 6 5 4 4 3 3	00000101 00000101 default 6 0 6 0 6 0 7 0 8 0 9 0 1 0	Reserved Sleep mode setting. 0d = Device is in sleep mode 1d = Device is not in sleep mode Address: Default Value: Definition Reserved Shutdown configuration. 0d = DREG is powered down immediately after SHDNZ asserts 1d = DREG remains active to enable a clean shut down until a time-out is reached; after the time-out period, DREG is forced to power off 2d = DREG remains active until the device cleanly shuts down 3d = Reserved These bits set how long DREG remains active after SHDNZ asserts. 0d = DREG remains active for 30 ms (typical) 1d = DREG remains active for 25 ms (typical)	0x05 0x05 Description	0x 00000 Set
bit 77 6 5 4 4 3 3	0 00000101 00000101 default 7 0 5 0 6 0 8 0 8 0	Reserved Sleep mode setting. 0d = Device is in sleep mode 1d = Device is not in sleep mode Address: Default Value: Definition Reserved Shutdown configuration. 0d = DREG is powered down immediately after SHDNZ asserts 1d = DREG remains active to enable a clean shut down until a time-out is reached; after the time-out period, DREG is forced to power off 2d = DREG remains active until the device cleanly shuts down 3d = Reserved These bits set how long DREG remains active after SHDNZ asserts. 0d = DREG remains active for 30 ms (typical) 1d = DREG remains active for 25 ms (typical) 2d = DREG remains active for 10 ms (typical)	0x05 0x05 Description 掉电设置(default)	0000 Set
bit 77 66 5 4 4 3 3	0 00000101 00000101 default 7 0 5 0 6 0 8 0 8 0	Reserved Sleep mode setting. 0d = Device is in sleep mode 1d = Device is not in sleep mode Address: Default Value: Definition Reserved Shutdown configuration. 0d = DREG is powered down immediately after SHDNZ asserts 1d = DREG remains active to enable a clean shut down until a time-out is reached; after the time-out period, DREG is forced to power off 2d = DREG remains active until the device cleanly shuts down 3d = Reserved These bits set how long DREG remains active after SHDNZ asserts. 0d = DREG remains active for 30 ms (typical) 1d = DREG remains active for 25 ms (typical)	0x05 0x05 Description 掉电设置(default)	0) 0000 Set
bit 77 66 5 4 4 3 3	0 00000101 00000101 default 7 0 5 0 6 0 8 0 8 0	Reserved Sleep mode setting. 0d = Device is in sleep mode 1d = Device is not in sleep mode Address: Default Value: Definition Reserved Shutdown configuration. 0d = DREG is powered down immediately after SHDNZ asserts 1d = DREG remains active to enable a clean shut down until a time-out is reached; after the time-out period, DREG is forced to power off 2d = DREG remains active until the device cleanly shuts down 3d = Reserved These bits set how long DREG remains active after SHDNZ asserts. 0d = DREG remains active for 30 ms (typical) 1d = DREG remains active for 25 ms (typical) 2d = DREG remains active for 10 ms (typical)	0x05 0x05 Description 掉电设置(default)	0000 Set
bit 77 66 5 4 4 3 3	0 00000101 00000101 default 7 0 5 0 5 0 7 0 8 0 9 0 1	Reserved Sleep mode setting. 0d = Device is in sleep mode 1d = Device is not in sleep mode Address: Default Value: Definition Reserved Shutdown configuration. 0d = DREG is powered down immediately after SHDNZ asserts 1d = DREG remains active to enable a clean shut down until a time-out is reached; after the time-out period, DREG is forced to power off 2d = DREG remains active until the device cleanly shuts down 3d = Reserved These bits set how long DREG remains active after SHDNZ asserts. 0d = DREG remains active for 30 ms (typical) 1d = DREG remains active for 25 ms (typical) 2d = DREG remains active for 10 ms (typical) 3d = DREG remains active for 5 ms (typical) 3d = DREG remains active for 5 ms (typical)	0x05 0x05 Description 掉电设置(default) Remain active 25ms(default)	0) 0000 Set
bit 77 66 5 4 4 3 3	00000101 00000101 default 7 0 5 0 6 0 8 0 8 0 1 0 1 0 1 0	Reserved Sleep mode setting. 0d = Device is in sleep mode 1d = Device is not in sleep mode Address: Default Value: Definition Reserved Shutdown configuration. 0d = DREG is powered down immediately after SHDNZ asserts 1d = DREG remains active to enable a clean shut down until a time-out is reached; after the time-out period, DREG is forced to power off 2d = DREG remains active until the device cleanly shuts down 3d = Reserved These bits set how long DREG remains active after SHDNZ asserts. 0d = DREG remains active for 30 ms (typical) 1d = DREG remains active for 25 ms (typical) 2d = DREG remains active for 10 ms (typical) 3d = DREG remains active for 5 ms (typical) 3d = DREG remains active for 5 ms (typical) 3d = DREG remains active for 5 ms (typical)	0x05 0x05 Description 掉电设置(default) Remain active 25ms(default)	0) 0000 Set
bit 77 6 5 5 4 4 4 3 3 2 2	00000101 00000101 default 0 0 0 0 0 0 1 0 0 0 0	Reserved Sleep mode setting. 0d = Device is in sleep mode 1d = Device is not in sleep mode Address: Default Value: Definition Reserved Shutdown configuration. 0d = DREG is powered down immediately after SHDNZ asserts 1d = DREG remains active to enable a clean shut down until a time-out is reached; after the time-out period, DREG is forced to power off 2d = DREG remains active until the device cleanly shuts down 3d = Reserved These bits set how long DREG remains active after SHDNZ asserts. 0d = DREG remains active for 30 ms (typical) 1d = DREG remains active for 25 ms (typical) 2d = DREG remains active for 10 ms (typical) 3d = DREG remains active for 5 ms (typical) Address: Default Value:	0x05 0x05 Description 掉电设置 (default) Remain active 25ms (default) 0x07 0x30	0) 00000 Set
bit 77 66 5 4 4 3 3	00000101 00000101 default 7 0 6 0 6 0 7 0 8 0 1	100 Reserved Sleep mode setting. 0d = Device is in sleep mode 1d = Device is not in sleep mode Address: Default Value: Definition Reserved Shutdown configuration. 0d = DREG is powered down immediately after SHDNZ asserts 1d = DREG remains active to enable a clean shut down until a time-out is reached; after the time-out period, DREG is forced to power off 2d = DREG remains active until the device cleanly shuts down 3d = Reserved These bits set how long DREG remains active after SHDNZ asserts. 0d = DREG remains active for 30 ms (typical) 1d = DREG remains active for 25 ms (typical) 2d = DREG remains active for 10 ms (typical) 3d = DREG remains active for 5 ms (typical) Address: Default Value : Definition	0x05 0x05 Description 掉电设置(default) Remain active 25ms(default)	0x 00000 Set
bit 77 6 5 5 4 4 4 3 3 2 2	00000101 00000101 default 7 0 6 0 6 0 7 0 8 0 1	Reserved Sleep mode setting. 0d = Device is in sleep mode 1d = Device is not in sleep mode Address: Default Value: Definition Reserved Shutdown configuration. 0d = DREG is powered down immediately after SHDNZ asserts 1d = DREG remains active to enable a clean shut down until a time-out is reached; after the time-out period, DREG is forced to power off 2d = DREG remains active until the device cleanly shuts down 3d = Reserved These bits set how long DREG remains active after SHDNZ asserts. 0d = DREG remains active for 30 ms (typical) 1d = DREG remains active for 25 ms (typical) 2d = DREG remains active for 10 ms (typical) 3d = DREG remains active for 5 ms (typical) Address: Default Value: Definition ASI protocol format.	0x05 0x05 Description 掉电设置 (default) Remain active 25ms (default) 0x07 0x30	0x 00000 Set (((((((((((((((((((
bit 7 6 5 4 4 3 3 2 1	00000101 00000101 default 7 0 6 0 6 0 7 0 8 0 1	Reserved Sleep mode setting. 0d = Device is in sleep mode 1d = Device is not in sleep mode Address: Default Value: Definition Reserved Shutdown configuration. 0d = DREG is powered down immediately after SHDNZ asserts 1d = DREG remains active to enable a clean shut down until a time-out is reached; after the time-out period, DREG is forced to power off 2d = DREG remains active until the device cleanly shuts down 3d = Reserved These bits set how long DREG remains active after SHDNZ asserts. 0d = DREG remains active for 30 ms (typical) 1d = DREG remains active for 25 ms (typical) 2d = DREG remains active for 10 ms (typical) 3d = DREG remains active for 5 ms (typical) Address: Default Value: Definition Address: Default Value: Definition	0x05 0x05 Description 掉电设置(default) Remain active 25ms(default) 0x07 0x30 Description	0x 00000 Set
bit 7 6 5 4 4 3 3 2 1	00000101 00000101 default 7 0 6 0 6 0 7 0 8 0 1	Reserved Sleep mode setting. 0d = Device is in sleep mode 1d = Device is not in sleep mode Address: Default Value: Definition Reserved Shutdown configuration. 0d = DREG is powered down immediately after SHDNZ asserts 1d = DREG remains active to enable a clean shut down until a time-out is reached; after the time-out period, DREG is forced to power off 2d = DREG remains active until the device cleanly shuts down 3d = Reserved These bits set how long DREG remains active after SHDNZ asserts. 0d = DREG remains active for 30 ms (typical) 1d = DREG remains active for 25 ms (typical) 2d = DREG remains active for 10 ms (typical) 3d = DREG remains active for 5 ms (typical) Address: Default Value: Definition ASI protocol format. 0d = TDM mode 1d = 12S mode	0x05 0x05 Description 掉电设置 (default) Remain active 25ms (default) 0x07 0x30	0x 00000 Set
bit 7 6 5 4 4 3 3 2 1	00000101 00000101 default 7 0 6 0 6 0 7 0 8 0 9 1 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1	Reserved Sleep mode setting. 0d = Device is in sleep mode 1d = Device is not in sleep mode Address: Default Value: Definition Reserved Shutdown configuration. 0d = DREG is powered down immediately after SHDNZ asserts 1d = DREG remains active to enable a clean shut down until a time-out is reached; after the time-out period, DREG is forced to power off 2d = DREG remains active until the device cleanly shuts down 3d = Reserved These bits set how long DREG remains active after SHDNZ asserts. 0d = DREG remains active for 30 ms (typical) 1d = DREG remains active for 25 ms (typical) 2d = DREG remains active for 10 ms (typical) 3d = DREG remains active for 5 ms (typical) Address: Default Value : Definition ASI protocol format. 0d = TDM mode 1d = I2S mode 2d = LJ (left-justified) mode	0x05 0x05 Description 掉电设置(default) Remain active 25ms(default) 0x07 0x30 Description	0x 00000 Set 0x 000000 Set
bit 7 6 5 4 4 3 3 2 1 1 5 1 1	00000101 00000101 default 7 0 6 0 6 0 7 0 8 0 9 1 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1	Reserved Sleep mode setting. 0d = Device is in sleep mode 1d = Device is not in sleep mode Address: Default Value: Definition Reserved Shutdown configuration. 0d = DREG is powered down immediately after SHDNZ asserts 1d = DREG remains active to enable a clean shut down until a time-out is reached; after the time-out period, DREG is forced to power off 2d = DREG remains active until the device cleanly shuts down 3d = Reserved These bits set how long DREG remains active after SHDNZ asserts. 0d = DREG remains active for 30 ms (typical) 1d = DREG remains active for 25 ms (typical) 2d = DREG remains active for 10 ms (typical) 3d = DREG remains active for 5 ms (typical) Address: Default Value: Definition ASI protocol format. 0d = TDM mode 1d = 12S mode 2d = 11 (left-inistified) mode	0x05 0x05 Description 掉电设置(default) Remain active 25ms(default) 0x07 0x30 Description	0x 00000 Set 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
bit 7 6 5 4 4 3 3 2 1 1 5 1 1	00000101 00000101 00000101 default	Reserved Sleep mode setting. 0d = Device is in sleep mode 1d = Device is not in sleep mode Address: Default Value: Definition Reserved Shutdown configuration. 0d = DREG is powered down immediately after SHDNZ asserts 1d = DREG remains active to enable a clean shut down until a time-out is reached; after the time-out period, DREG is forced to power off 2d = DREG remains active until the device cleanly shuts down 3d = Reserved These bits set how long DREG remains active after SHDNZ asserts. 0d = DREG remains active for 30 ms (typical) 1d = DREG remains active for 25 ms (typical) 2d = DREG remains active for 10 ms (typical) 3d = DREG remains active for 5 ms (typical) Address: Default Value: Definition ASI protocol format. 0d = TDM mode 1d = 12S mode 2d = L1 (left-justified) mode 3d = Reserved ASI word or slot lenoth.	0x05 0x05 Description 掉电设置(default) Remain active 25ms(default) 0x07 0x30 Description	0x 00000 Set ((((((((((((((((((((
bit 7 6 5 4 4 3 3 2 1 1 5 1 1	00000101 00000101 00000101 default	Reserved Sleep mode setting. 0d = Device is in sleep mode 1d = Device is not in sleep mode Address: Default Value: Definition Reserved Shutdown configuration. 0d = DREG is powered down immediately after SHDNZ asserts 1d = DREG is powered down immediately after SHDNZ asserts 1d = DREG remains active to enable a clean shut down until a time-out is reached; after the time-out period, DREG is forced to power off 2d = DREG remains active until the device cleanly shuts down 3d = Reserved These bits set how long DREG remains active after SHDNZ asserts. 0d = DREG remains active for 30 ms (typical) 1d = DREG remains active for 30 ms (typical) 2d = DREG remains active for 10 ms (typical) 3d = DREG remains active for 5 ms (typical) Address: Default Value: Definition ASI protocol format. 0d = TDM mode 1d = 12S mode 2d = LJ (left-justified) mode 3d = Reserved ASI word or slot length. 0d = 16 bits	0x05 0x05 Description 掉电设置(default) Remain active 25ms(default) 0x07 0x30 Description	0x 00000 Set ((((((((((((((((((((
bit 7 6 5 4 4 3 3 2 1 1 5 1 1	00000101 00000101 00000101 default	Reserved Sleep mode setting. 0d = Device is in sleep mode 1d = Device is not in sleep mode Address: Default Value: Definition Reserved Shutdown configuration. 0d = DREG is powered down immediately after SHDNZ asserts 1d = DREG remains active to enable a clean shut down until a time-out is reached; after the time-out period, DREG is forced to power off 2d = DREG remains active until the device cleanly shuts down 3d = Reserved These bits set how long DREG remains active after SHDNZ asserts. 0d = DREG remains active for 30 ms (typical) 1d = DREG remains active for 25 ms (typical) 2d = DREG remains active for 10 ms (typical) 3d = DREG remains active for 5 ms (typical) 3d = DREG remains active for 5 ms (typical) Address: Default Value: Definition ASI protocol format. 0d = TDM mode 1d = 12S mode 2d = LJ (left-justified) mode 3d = Reserved ASI word or slot length. 0d = 16 bits 1d = 20 bits	0x05 0x05 Description 掉电设置(default) Remain active 25ms(default) 0x07 0x30 Description	0) 00000 Set
bit 7 6 5 4 4 3 3 2 1 1 5 1 5 1 5 5 5 5	00000101	Reserved Sleep mode setting. 0d = Device is in sleep mode 1d = Device is not in sleep mode Address: Default Value: Definition Reserved Shutdown configuration. 0d = DREG is powered down immediately after SHDNZ asserts 1d = DREG remains active to enable a clean shut down until a time-out is reached, after the time-out period, DREG is forced to power off 2d = DREG remains active until the device cleanly shuts down 3d = Reserved These bits set how long DREG remains active after SHDNZ asserts. 0d = DREG remains active for 30 ms (typical) 1d = DREG remains active for 25 ms (typical) 2d = DREG remains active for 10 ms (typical) 3d = DREG remains active for 5 ms (typical) Address: Default Value : Definition ASI protocol format. 0d = TDM mode 1d = I2S mode 2d = LJ (left-justified) mode 3d = Reserved ASI word or slot length. 0d = 16 bits 1d = 20 bits 2d = 24 bits	0x05 0x05 Description 掉电设置(default) Remain active 25ms(default) 0x07 0x30 Description TDM	0x 00000 Set
bit 7 6 5 4 4 3 3 2 1 1 5 1 1	00000101	Reserved Sleep mode setting. 0d = Device is in sleep mode 1d = Device is not in sleep mode Address: Default Value: Definition Reserved Shutdown configuration. 0d = DREG is powered down immediately after SHDNZ asserts 1d = DREG remains active to enable a clean shut down until a time-out is reached; after the time-out period, DREG is forced to power off 2d = DREG remains active until the device cleanly shuts down 3d = Reserved These bits set how long DREG remains active after SHDNZ asserts. 0d = DREG remains active for 30 ms (typical) 1d = DREG remains active for 25 ms (typical) 2d = DREG remains active for 10 ms (typical) 3d = DREG remains active for 5 ms (typical) Address: Default Value: Definition ASI protocol format. 0d = TDM mode 1d = I2S mode 2d = LJ (left-justified) mode 3d = Reserved ASI word or slot length. 0d = 16 bits 1d = 20 bits 2d = 24 bits	0x05 0x05 Description 掉电设置(default) Remain active 25ms(default) 0x07 0x30 Description TDM	0x 00000
bit 7 6 5 4 4 3 3 2 1 1 5 1 5 1 5 5 5 5	00000101	Reserved Sleep mode setting. 0d = Device is in sleep mode 1d = Device is not in sleep mode Address: Default Value: Definition Reserved Shutdown configuration. 0d = DREG is powered down immediately after SHDNZ asserts 1d = DREG remains active to enable a clean shut down until a time-out is reached, after the time-out period, DREG is forced to power off 2d = DREG remains active until the device cleanly shuts down 3d = Reserved These bits set how long DREG remains active after SHDNZ asserts. 0d = DREG remains active for 30 ms (typical) 1d = DREG remains active for 25 ms (typical) 2d = DREG remains active for 10 ms (typical) 3d = DREG remains active for 5 ms (typical) Address: Default Value : Definition ASI protocol format. 0d = TDM mode 1d = I2S mode 2d = LJ (left-justified) mode 3d = Reserved ASI word or slot length. 0d = 16 bits 1d = 20 bits 2d = 24 bits	0x05 0x05 Description 掉电设置(default) Remain active 25ms(default) 0x07 0x30 Description TDM	0x 00000 Settl (() (() () () () () () () () () () () (

2	0	ASI BCLK polarity. 0d = Default polarity as per standard protocol 1d = Inverted polarity with respect to standard protocol	Inverted polarity with respect to standard protocol	1
1	0	ASI data output (on the primary and secondary data pin) transmit edge. Od = Default edge as per the protocol configuration setting in bit 2 (BCLK_POL) 1d = Inverted following edge (half cycle delay) with respect to the default edge setting	used as default	0
0	0	ASI data output (on the primary and secondary data pin) for any unused cycles Od = Always transmit 0 for unused cycles 1d = Always use Hi-Z for unused cycles	used as default	0

	00001000	Address :	0x08	
	00000000	Default Value :	0x00	
bit	default	Definition	Description	
7	0	ASI data output (on the primary and secondary data pin) for LSB transmissions. 0d = Transmit the LSB for a full cycle 1d = Transmit the LSB for the first half cycle and Hi-Z for the second half cycle	used as default	
6	0	ASI data output (on the primary and secondary data pin) bus keeper. Od = Bus keeper is always disabled 1d = Bus keeper is always enabled	used as default	
5	0	2d = Bus keeper is enabled during LSB transmissions only for one cycle 3d = Bus keeper is enabled during LSB transmissions only for one and half cycles	document of the second of the	
4	0	ASI data MSB slot 0 offset (on the primary and secondary data pin).		
3	0	Od = ASI data MSB location has no offset and is as per standard protocol 1d = ASI data MSB location (TDM mode is slot 0 or I2S, LJ mode is the left and right slot 0) offset of one BCLK cycle with respect to standard protocol		
2	0	2d = ASI data MSB location (TDM mode is slot 0 or I2S, LJ mode is the left and right slot 0) offset of two BCLK cycles with respect to standard protocol	offset=1	
1	0	3d to 30d = ASI data MSB location (TDM mode is slot 0 or 12S, LJ mode is the left and right slot 0) offset assigned as per configuration 31d = ASI data MSB location (TDM mode is slot 0 or 12S, LJ mode is the left		
0	0	and right slot 0) offset of 31 BCLK cycles with respect to standard protocol		

	00001001	Address :	0x09
00000000		Default Value : 0x00	
bit	default	Definition	Description
7	0	ASI daisy chain connection. Od = All devices are connected in the common ASI bus 1d = All devices are daisy-chained for the ASI bus	不采用菊花链方式
6	0	Reserved	
5	0	ASI bus error detection. Od = Enable bus error detection 1d = Disable bus error detection	used as default
4	0	ASI bus error auto resume. Od = Enable auto resume after bus error recovery 1d = Disable auto resume after bus error recovery and remain powered down until the host configures the device	used as default
3	0		
2	0	Reserved	
1	0	reserved	
0	0		

	00001011	Address :	0x0B
	00000000	Default Value :	0x00
bit	default	Definition	Description
7	0	Reserved	
6		Channel 1 output line. 0d = Channel 1 output is on the ASI primary output pin (SDOUT) 1d = Channel 1 output is on the ASI secondary output pin (GPIO1 or GPOx)	通过SDOUT输出
5	0	Channel 1 slot assignment.	
4	0	0d = TDM is slot 0 or I2S, L) is left slot 0 1d = TDM is slot 1 or I2S, L) is left slot 1	
3		2d to 30d = Slot assigned as per configuration 31d = TDM is slot 31 or I2S. LJ is left slot 31	ch1=slot0
2	0	32d = TDM is slot 32 or I2S, LJ is right slot 0	CHIT-3IOLO
1	0	33d = TDM is slot 33 or I2S, LJ is right slot 1 34d to 62d = Slot assigned as per configuration	
0	0	63d = TDM is slot 63 or I2S, ∐ is right slot 31	

	00001100	Address :	0x0C
	00000001	Default Value:	0x01
bit	default	Definition	Description
7	0	Reserved	
6	0	Channel 2 output line. 0d = Channel 2 output is on the ASI primary output pin (SDOUT) 1d = Channel 2 output is on the ASI secondary output pin (GPIO1 or GPOx)	通过SDOUT输出
5	0	Channel 2 slot assignment.	
4	0	0d = TDM is slot 0 or I2S, LJ is left slot 0 1d = TDM is slot 1 or I2S, LJ is left slot 1	
3	0	2d to 30d = Slot assigned as per configuration 31d = TDM is slot 31 or I2S, LJ is left slot 31	ch2=slot2
2		32d = TDM is slot 32 or I2S, LJ is right slot 0 33d = TDM is slot 33 or I2S 11 is right slot 1	

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	1 .	วอง – เบเท เจ ลเบเ ออ บเ เรอ, ม เจ เเทูเเเ ลเบเ เ	1	
1 0		34d to 62d = Slot assigned as per configuration 63d = TDM is slot 63 or I2S, LJ is right slot 31		0
	1			U
	00001101	Address :		0x04
bit	00000010 default	Default Value :	0x02 Description	00000100 Setting
7		Reserved	Description	0
6	0	Channel 3 output line. Od = Channel 3 output is on the ASI primary output pin (SDOUT)	通过SDOUT输出	0
5	0	1d = Channel 3 output is on the ASI secondary output pin (GPIO1 or GPOx)		0
4		Channel 3 slot assignment. 0d = TDM is slot 0 or I2S, LJ is left slot 0		0
3		1d = TDM is slot 1 or I2S, LJ is left slot 1 2d to 30d = Slot assigned as per configuration		0
2		31d = TDM is slot 31 or I2S, LJ is left slot 31 32d = TDM is slot 32 or I2S, LJ is right slot 0	ch3=slot4	1
1	_	33d = TDM is slot 33 or I2S, LJ is right slot 1		0
0		34d to 62d = Slot assigned as per configuration 63d = TDM is slot 63 or I2S, LJ is right slot 31		0
	0			
	00001110	Address :		0x06
bit	00000011 default	Default Value :	0x03 Description	00000110 Setting
7		Reserved	Description	0
		Channel 4 output line.		
6	0	Od = Channel 4 output is on the ASI primary output pin (SDOUT) 1d = Channel 4 output is on the ASI secondary output pin (GPIO1 or GPOx)	通过SDOUT输出	0
5	0	Channel 4 slot assignment.		0
4	0	0d = TDM is slot 0 or I2S, LJ is left slot 0 1d = TDM is slot 1 or I2S, LJ is left slot 1		0
3	0	2d to 30d = Slot assigned as per configuration 31d = TDM is slot 31 or I2S, LJ is left slot 31	ch4=slot6	0
2	0	32d = TDM is slot 32 or I2S, LJ is right slot 0 33d = TDM is slot 33 or I2S, LJ is right slot 1	1114-31010	1
1	1	334d to 62d = Slot assigned as per configuration 163d = TDM is slot 63 or I2S, L) is right slot 31		1
0	1			0
	00001111	Address :	0x0F	0x08
	00000100	Default Value :	0x04	00001000
bit	default	Definition	Description	Setting
	1	Reserved Channel 5 output line.		0
6	0	0d = Channel 5 output is on the ASI primary output pin (SDOUT) 1d = Channel 5 output is on the ASI secondary output pin (GPIO1 or GPOx)	通过SDOUT输出	0
5	0			0
4	. 0	Channel 5 slot assignment. Od = TDM is slot 0 or I2S, L) is left slot 0		0
3	0	1d = TDM is slot 1 or I2S, U is left slot 1 2d to 30d = Slot assigned as per configuration		1
2	1	31d = TDM is slot 31 or I2S, LJ is left slot 31 32d = TDM is slot 32 or I2S, LJ is right slot 0	ch5=slot8	
1	0			0
		33d = TDM is slot 33 or I2S, LJ is right slot 1 34d to 62d = Slot assigned as per configuration		0
0		34d to 62d = Slot assigned as per configuration 63d = TDM is slot 63 or I2S, LJ is right slot 31		
0	0	34d to 62d = Slot assigned as per configuration 63d = TDM is slot 63 or I2S, IJ is right slot 31		0
0	00010000	34d to 62d = Slot assigned as per configuration 63d = TDM is slot 63 or I2S, LJ is right slot 31 Address:	0x10	0 0
	00010000	34d to 62d = Slot assigned as per configuration 63d = TDM is slot 63 or I2S, IJ is right slot 31	0x05	0 0 0 0 0x0A 00001010
bit 7	00010000 0000101 default	34d to 62d = Slot assigned as per configuration 63d = TDM is slot 63 or I2S, LJ is right slot 31 Address: Definition Reserved		0 0
bit	00010000 00000101 default	34d to 62d = Slot assigned as per configuration 63d = TDM is slot 63 or I2S, LJ is right slot 31 Address: Default Value: Definition Reserved Channel 6 output line. 0d = Channel 6 output is on the ASI primary output pin (SDOUT)	0x05	0 0 0 0x0A 00001010 Setting
bit 7	00010000 0000101 default 0	34d to 62d = Slot assigned as per configuration 63d = TDM is slot 63 or I2S, LJ is right slot 31 Address: Default Value: Definition Reserved Channel 6 output line. 0d = Channel 6 output is on the ASI primary output pin (SDOUT) 1d = Channel 6 output is on the ASI secondary output pin (GPIO1 or GPOx)	0x05 Description	0 0 0 0x0A 00001010 Setting 0
bit 7	00010000 0000101 default 0	34d to 62d = Slot assigned as per configuration 63d = TDM is slot 63 or I2S, LJ is right slot 31 Address: Default Value: Definition Reserved Channel 6 output line. 0d = Channel 6 output is on the ASI primary output pin (SDOUT) 1d = Channel 6 output is on the ASI secondary output pin (GPIO1 or GPOx) Channel 6 slot assignment. 0d = TDM is slot 0 or I2S, LJ is left slot 0	0x05 Description	0 0 0 0 00001010 Setting 0
bit 7 6	00010000 0000101 default 0	34d to 62d = Slot assigned as per configuration 63d = TDM is slot 63 or I2S, LJ is right slot 31 Address: Default Value: Definition Reserved Channel 6 output line. 0d = Channel 6 output is on the ASI primary output pin (SDOUT) 1d = Channel 6 output is on the ASI secondary output pin (GPIO1 or GPOx) Channel 6 slot assignment. 0d = TDM is slot 0 or I2S, LJ is left slot 0 1d = TDM is slot 1 or I2S, LJ is left slot 1 2d to 30d = Slot assigned as per configuration	0x05 Description 通过SDOUT输出	0 0 0 00001010 Setting 0 0
bit 7 6 5	00010000 00000101 default 0	34d to 62d = Slot assigned as per configuration 63d = TDM is slot 63 or I2S, LJ is right slot 31 Address: Default Value: Definition Reserved Channel 6 output line. 0d = Channel 6 output is on the ASI primary output pin (SDOUT) 1d = Channel 6 output is on the ASI secondary output pin (GPIO1 or GPOX) Channel 6 slot assignment. 0d = TDM is slot 1 or I2S, LJ is left slot 0 1d = TDM is slot 1 or I2S, LJ is left slot 1 2d to 30d = Slot assigned as per configuration 31d = TDM is slot 31 or I2S, LJ is left slot 31 32d = TDM is slot 32 or I2S, LJ is right slot 0	0x05 Description	0 0 0 0 00001010 Setting 0 0
bit 7 6 5 4	00010000 00000101 default 0 0 0 0	34d to 62d = Slot assigned as per configuration 63d = TDM is slot 63 or I2S, LJ is right slot 31 Address: Default Value: Definition Reserved Channel 6 output line. Od = Channel 6 output is on the ASI primary output pin (SDOUT) Id = Channel 6 output is on the ASI secondary output pin (GPIO1 or GPOX) Channel 6 slot assignment. Od = TDM is slot 0 or I2S, LJ is left slot 0 Id = TDM is slot 1 or I2S, LJ is left slot 1 2d to 30d = Slot assigned as per configuration 3Id = TDM is slot 31 or I2S, LJ is left slot 31 32d = TDM is slot 32 or I2S, LJ is right slot 0	0x05 Description 通过SDOUT输出	0 0 0 0 00001010 Setting 0 0 0
bit 7 6 5 4 3 2	00010000 00001011 default 0 0 0 0 1	34d to 62d = Slot assigned as per configuration 63d = TDM is slot 63 or I2S, LJ is right slot 31 Address: Default Value: Definition Reserved Channel 6 output line. 0d = Channel 6 output is on the ASI primary output pin (SDOUT) 1d = Channel 6 output is on the ASI secondary output pin (GPIO1 or GPOX) Channel 6 slot assignment. 0d = TDM is slot 1 or I2S, LJ is left slot 0 1d = TDM is slot 1 or I2S, LJ is left slot 1 2d to 30d = Slot assigned as per configuration 31d = TDM is slot 31 or I2S, LJ is left slot 31 32d = TDM is slot 32 or I2S, LJ is right slot 0	0x05 Description 通过SDOUT输出	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1
bit 7 6 5 4 3 2	00010000 00001011 default 0 0 0 0 1	34d to 62d = Slot assigned as per configuration 63d = TDM is slot 63 or I2S, LJ is right slot 31 Address: Default Value: Definition Reserved Channel 6 output line. Od = Channel 6 output is on the ASI primary output pin (SDOUT) Id = Channel 6 output is on the ASI secondary output pin (GPIO1 or GPOx) Channel 6 slot assignment. Od = TDM is slot 0 or I2S, LJ is left slot 0 Id = TDM is slot 1 or I2S, LJ is left slot 1 2d to 30d = Slot assigned as per configuration 31d = TDM is slot 31 or I2S, LJ is right slot 0 33d = TDM is slot 32 or I2S, LJ is right slot 0 33d = TDM is slot 33 or I2S, LJ is right slot 1 34d to 62d = Slot assigned as per configuration	0x05 Description 通过SDOUT输出	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 1
bit 7 6 5 4 3 2 1	00010000 0000101 default 0 0 0 0 0 0 1 1 00010011 00000010	34d to 62d = Slot assigned as per configuration 63d = TDM is slot 63 or I2S, LJ is right slot 31 Address: Default Value: Definition Reserved Channel 6 output line. 0d = Channel 6 output is on the ASI primary output pin (SDOUT) 1d = Channel 6 output is on the ASI secondary output pin (GPIO1 or GPOx) Channel 6 slot assignment. 0d = TDM is slot 0 or I2S, LJ is left slot 0 1d = TDM is slot 1 or I2S, LJ is left slot 1 2d to 30d = Slot assigned as per configuration 31d = TDM is slot 32 or I2S, LJ is right slot 0 33d = TDM is slot 32 or I2S, LJ is right slot 0 33d = TDM is slot 33 or I2S, LJ is right slot 1 34d to 62d = Slot assigned as per configuration 63d = TDM is slot 63 or I2S, LJ is right slot 1 Address: Default Value:	Ox05 Description 通过SDOUT输出 ch6=slot10 Ox13 Ox02	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 1 0
bit 7 6 5 4 3 2	00010000 00000101 default 0 0 0 0 1 0 1	34d to 62d = Slot assigned as per configuration 63d = TDM is slot 63 or I2S, LJ is right slot 31 Address: Default Value: Definition Reserved Channel 6 output line. 0d = Channel 6 output is on the ASI primary output pin (SDOUT) 1d = Channel 6 output is on the ASI secondary output pin (GPIO1 or GPOx) Channel 6 slot assignment. 0d = TDM is slot 0 or I2S, LJ is left slot 0 1d = TDM is slot 1 or I2S, LJ is left slot 1 2d to 30d = Slot assigned as per configuration 31d = TDM is slot 31 or I2S, LJ is right slot 0 33d = TDM is slot 32 or I2S, LJ is right slot 0 33d = TDM is slot 33 or I2S, LJ is right slot 1 34d to 62d = Slot assigned as per configuration 63d = TDM is slot 63 or I2S, LJ is right slot 1 Address: Default Value:	0x05 Description 通过SDOUT输出 ch6=slot10	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 1 0
bit 7 6 5 4 3 2 1 0	00010010 0001011 00010011 00010011 00000101 0000010 001 001 001001	34d to 62d = Slot assigned as per configuration 63d = TDM is slot 63 or I2S, LJ is right slot 31 Address: Default Value: Definition Reserved Channel 6 output line. Od = Channel 6 output is on the ASI primary output pin (SDOUT) Id = Channel 6 output is on the ASI secondary output pin (GPIO1 or GPOx) Channel 6 slot assignment. Od = TDM is slot 0 or I2S, LJ is left slot 0 Id = TDM is slot 1 or I2S, LJ is left slot 1 2d to 30d = Slot assigned as per configuration 3Id = TDM is slot 31 or I2S, LJ is left slot 31 32d = TDM is slot 32 or I2S, LJ is right slot 1 34d to 62d = Slot assigned as per configuration 63d = TDM is slot 30 rI2S, LJ is right slot 1 34d to 62d = Slot assigned as per configuration 63d = TDM is slot 63 or I2S, LJ is right slot 31 Address: Default Value: Definition ASI master or slave configuration register setting. Od = Device is in slave mode (both BCLK and FSYNC are inputs to the	Ox05 Description 通过SDOUT输出 Ox13 Ox02 Description slave mode	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 1 0 0 0 2 0 0 0 5etting 0 0 5etting
bit 7 6 5 4 3 2 1 0	00010010 0001011 00010011 00010011 00000101 0000010 001 001 001001	34d to 62d = Slot assigned as per configuration 63d = TDM is slot 63 or I2S, LJ is right slot 31 Address: Default Value: Definition Reserved Channel 6 output line. 0d = Channel 6 output is on the ASI primary output pin (SDOUT) 1d = Channel 6 output is on the ASI secondary output pin (GPIO1 or GPOX) Channel 6 slot assignment. 0d = TDM is slot 10 or I2S, LJ is left slot 0 1d = TDM is slot 1 or I2S, LJ is left slot 1 2d to 30d = Slot assigned as per configuration 31d = TDM is slot 31 or I2S, LJ is left slot 31 32d = TDM is slot 32 or I2S, LJ is right slot 0 33d = TDM is slot 33 or I2S, LJ is right slot 1 34d to 62d = Slot assigned as per configuration 63d = TDM is slot 30 or I2S, LJ is right slot 31 Address: Default Value: Definition ASI master or slave configuration register setting.	0x05 Description 通过SDOUT输出 ch6=slot10 0x13 0x02 Description	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 1 0
bit 7 6 5 4 3 2 1 0	00010010 0001011 00010011 00010011 00000101 0000010 001 001 001001	34d to 62d = Slot assigned as per configuration 63d = TDM is slot 63 or I2S, LJ is right slot 31 Address: Default Value: Definition Reserved Channel 6 output line. 0d = Channel 6 output is on the ASI primary output pin (SDOUT) 1d = Channel 6 output is on the ASI secondary output pin (GPIO1 or GPOx) Channel 6 slot assignment. 0d = TDM is slot 1 or I2S, LJ is left slot 0 1d = TDM is slot 1 or I2S, LJ is left slot 1 2d to 30d = Slot assigned as per configuration 31d = TDM is slot 31 or I2S, LJ is left slot 31 32d = TDM is slot 32 or I2S, LJ is right slot 0 33d = TDM is slot 33 or I2S, LJ is right slot 1 34d to 62d = Slot assigned as per configuration 63d = TDM is slot 30 or I2S, LJ is right slot 31 Address: Default Value: Definition ASI master or slave configuration register setting. 0d = Device is in slave mode (both BCLK and FSYNC are generated from the device) Automatic clock configuration setting.	Ox05 Description 通过SDOUT输出 Ox13 Ox02 Description slave mode	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 1 0 0 0 1 0 Setting 0 Setting
bit 7 6 5 4 3 2 1 0	00010000 0000101 default	34d to 62d = Slot assigned as per configuration 63d = TDM is slot 63 or I2S, LJ is right slot 31 Address: Default Value: Definition Reserved Channel 6 output line. 0d = Channel 6 output is on the ASI primary output pin (SDOUT) 1d = Channel 6 output is on the ASI secondary output pin (GPIO1 or GPOx) Channel 6 slot assignment. 0d = TDM is slot 0 or I2S, LJ is left slot 0 1d = TDM is slot 1 or I2S, LJ is left slot 1 2d to 30d = Slot assigned as per configuration 31d = TDM is slot 31 or I2S, LJ is right slot 0 33d = TDM is slot 32 or I2S, LJ is right slot 1 34d to 62d = Slot assigned as per configuration 63d = TDM is slot 30 or I2S, LJ is right slot 1 Address: Address: Default Value: Definition ASI master or slave configuration register setting. 0d = Device is in slave mode (both BCLK and FSYNC are inputs to the device) Automatic clock configuration is enabled (all internal clock divider and PLL configurations are auto derived)	Ox05 Description 通过SDOUT输出 Ox13 Ox02 Description slave mode	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 1 0 0 0 1 0 Setting
bit 7 6 5 4 3 2 1 0	00010000 0000101 default	34d to 62d = Slot assigned as per configuration 63d = TDM is slot 63 or I2S, LJ is right slot 31 Address: Default Value: Definition Reserved Channel 6 output line. Od = Channel 6 output is on the ASI primary output pin (SDOUT) Id = Channel 6 output is on the ASI secondary output pin (GPIO1 or GPOx) Channel 6 slot assignment. Od = TDM is slot 0 or I2S, LJ is left slot 0 Id = TDM is slot 1 or I2S, LJ is left slot 1 2d to 30d = Slot assigned as per configuration 3Id = TDM is slot 31 or I2S, LJ is left slot 31 32d = TDM is slot 32 or I2S, LJ is right slot 0 33d = TDM is slot 33 or I2S, LJ is right slot 0 34d to 62d = Slot assigned as per configuration 63d = TDM is slot 30 r I2S, LJ is right slot 1 34d to 62d = Slot assigned as per configuration 63d = TDM is slot 63 or I2S, LJ is right slot 31 Address: Default Value: Definition ASI master or slave configuration register setting. Od = Device is in slave mode (both BCLK and FSYNC are inputs to the device) Id = Device is in master mode (both BCLK and FSYNC are generated from the device) Automatic clock configuration setting. Od = Auto clock configuration is enabled (all internal clock divider and PLL	Ox05 Description 通过SDOUT输出 Ox13 Ox02 Description slave mode X9U(AK7738)做主,ADC做从	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 1 0 0 0 2 0000010 Setting

5	0	Automatic mode PLL setting. Od = PLL is enabled in auto clock configuration 1d = PLL is disabled in auto clock configuration	PLL自动启用	0
4	0	BCLK and FSYNC clock gate (valid when the device is in master mode). Od = Do not gate BCLK and FSYNC 1d = Force gate BCLK and FSYNC when being transmitted from the device in master mode	slave mode 设定无效	0
3	0	Sample rate setting (valid when the device is in master mode). Od = fS is a multiple (or submultiple) of 48 kHz 1d = fS is a multiple (or submultiple) of 44.1 kHz	slave mode 设定无效	0
2	0	These bits select the MCLK (GPIO or GPIx) frequency for the PLL source clock input (valid when the device is in master mode and MCLK_FREQ_SEL_MODE = 0). 0d = 12 MHz		0
1	_	00 - 12 Min2 1d = 12288 MHz 2d = 13 MHz 3d = 16 MHz 4d = 192 MHz	slave mode 设定无效	1
0		5d = 19.68 MHz 6d = 24 MHz 7d = 24.576 MHz		0

	00010100	Address :	0x14	. [0x48
	01001000	Default Value :	0x48	. [01001000
bit	default	Definition	Description	. [Setting
7	0	Programmed sample rate of the ASI bus (not used when the device is configured in slave mode auto clock configuration). 0d = 7.35 KHz or 8 kHz			0
6	1	1 d = 14.7 kHz or 16 kHz 1 d = 22.05 kHz or 24 kHz 3d = 29.4 kHz or 32 kHz 4d = 44.1 kHz or 48 kHz 5d = 88.2 kHz or 96 kHz 6d = 176.4 kHz or 192 kHz 7d = 352.8 kHz or 384 kHz		1	
5	0				0
4		8d = 705.6 kHz or 768 kHz 9d to 15d = Reserved			0
3	1	Programmed BCLK to FSYNC frequency ratio of the ASI bus (not used when the device is configured in slave mode auto clock configuration). 0d = Ratio of 16 1d = Ratio of 24			1
2	0	1d = Ratio of 24 2d = Ratio of 32 3d = Ratio of 48 0 4d = Ratio of 64 5d = Ratio of 96 6d = Ratio of 128	slave mode auto clock 设定无效		0
1	0	7d = Ratio of 192 8d = Ratio of 256 9d = Ratio of 384 10d = Ratio of 512 11d = Ratio of 1024	Slave mode date clock by EPLSX		0
0		12d = Ratio of 2048 13d = Reserved 14d = Ratio of 144 15d = Reserved			0

	00010101	Address :	0x15		0xFF
	11111111	Default Value :	0xFF		11111111
bit	default	Definition	Description	1	Setting
7	1	Detected sample rate of the ASI bus. 0d = 7.35 kHz or 8 kHz			1
6		1d = 14.7 kHz or 16 kHz 2d = 22.05 kHz or 24 kHz 3d = 29.4 kHz or 32 kHz 4d = 44.1 kHz or 48 kHz	read only		1
5	1	5d = 88.2 kHz or 96 kHz 6d = 176.4 kHz or 192 kHz 7d = 352.8 kHz or 384 kHz 8d = 705.6 kHz or 768 kHz			1
4		9d to 14d = Reserved 15d = Invalid sample rate			1
3	1	Detected BCLK to FSYNC frequency ratio of the ASI bus. 0d = Ratio of 16 1d = Ratio of 24			1
2	1	2d = Ratio of 32 3d = Ratio of 48 4d = Ratio of 64 5d = Ratio of 96 6d = Ratio of 128 7d = Ratio of 192	read only		1
1	1	8d = Ratio of 256 9d = Ratio of 384 10d = Ratio of 512 11d = Ratio of 1024 12d = Ratio of 2048	icua ony		1

0	1	13d = Reserved 14d = Ratio of 144 15d = Invalid ratio			1
				ı L	
	00010110	Address :		ΙF	0x08
bit	00010000 default	Default Value :	0x10 Description	-	00001000 Setting
7		Audio root clock source setting when the device is configured with the PLL disabled in the auto clock configuration for slave mode (AUTO_MODE_PLL_DIS = 1). 0d = BCLK is used as the audio root clock source 1d = MCLK (GPIOx or GPIx) is used as the audio root clock source (the MCLK to FSYNC ratio is as per MCLK_RATIO_SEL setting)	AUTO_MODE_PLL_DIS = 0,此设定无效		0
6	0	Master mode MCLK (GPIOx or GPIx) frequency selection mode (valid when the device is in auto clock configuration). dl = MCLK frequency is based on the MCLK_FREQ_SEL (PO_R19)configuration 1d = MCLK frequency is specified as a multiple of FSYNC in the MCLK_RATIO_SEL (PO_R22) configuration	slave mode,设定无效		0
4	1	mode or when MCLK is used as the audio root clock source in slave mode. 0d = Ratio of 64 1d = Ratio of 256 2d = Ratio of 384 3d = Ratio of 512 4d = Ratio of 768 5d = Ratio of 1024 6d = Ratio of 1536	slave mode and MCLK is used as the audio root clock source in slave mode.设定无效		0 0
2					0
1 0		Reserved		-	0
	100400004		0.01	. –	0.00
	00100001 00100010	Address : Default Value :		-	0x02 00000010
bit	default	Definition	Description		Setting
6	-	GPIO1 configuration. dd = GPIO1 is disabled 1d = GPIO1 is configured as a general-purpose output (GPO) 2d = GPIO1 is configured as a device interrupt output (IRQ) 3d = GPIO1 is configured as a secondary ASI output (SDOUT2) 4d = Reserved 5d = Reserved 6d = Reserved			0
5		7d = GPIO1 is configured as an input to power down all ADC channels 8d = GPIO1 is configured as an input to control when MICBIAS turns on or off (MICBIAS_EN) 9d = GPIO1 is configured as a general-purpose input (GPI) 10d = GPIO1 is configured as a master clock input (MCLK) 11d = GPIO1 is configured as an ASI input for daisy-chain (SDIN) 12d = Reserved 13d = Reserved 14d = Reserved	GPIO1未使用		0
3	0	Reserved		ı	0
2	0	GPIO1 output drive configuration (not used when GPIO1 is configured as SDOUT2). 0d = Hi-Z output 1d = Drive active low and active high 2d = Drive active low and weak high 3d = Drive active low and Hi-Z	GPIO1未使用		0
0	0	4d = Drive weak low and active high 5d = Drive Hi-Z and active high 6d to 7d = Reserved			0
				i L	
	00100010	Address :	0x22		0x00
	00000000	Default Value:		-	00000000
bit	default	Definition	Description		Setting
7		GPIO2 configuration. Od = GPIO2 is disabled 1d = GPIO2 is configured as a general-purpose output (GPO) 2d = GPIO2 is configured as a device interrupt output (IRQ) 3d = GPIO2 is configured as a secondary ASI output (SDOUT2) 4d = Reserved			0
6	0	5d = Reserved 6d = Reserved 7d = GPIO2 is configured as an input to power down all ADC channels	Not applicable for PCM6260-Q1.		0
5	0	8d = GPIO2 is configured as an input to control when MICBIAS turns on or off (MICBIAS EN)			0
4	0	13d – Reserved 14d = Reserved			0

0 Reserved

2	0	GPIO2 output drive configuration (not used when GPIO2 is configured as SDOUT2). Od = Hi-Z output		0
1	0	1d = Drive active low and active high 2d = Drive active low and weak high 3d = Drive active low and Hi-Z	Not applicable for PCM6260-Q1.	0
0	0	4d = Drive weak low and active high 5d = Drive Hi-Z and active high 6d to 7d = Reserved		0
	00100011	Address :	0x23	0x00
	00000000	Default Value :	0x00	00000000
bit	default	Definition	Description	Setting
7	0	Ud = GPIO3 is disabled 1d = GPIO3 is configured as a general-purpose output (GPO) 2d = GPIO3 is configured as a device interrupt output (IRQ)		0
6	0	5d = Reserved 6d = Reserved 7d = GPIO3 is configured as an input to power down all ADC channels	Not applicable for PCM6260-Q1.	0
5	0	9d = GPIO3 is configured as a general-purpose input (GPI) 10d = GPIO3 is configured as a master clock input (MCLK) 11d = GPIO3 is configured as an ASI input for daisy-chain (SDIN)		0
4	0	12d = Reserved 13d = Reserved 14d = Reserved Reserved		0
		GPIO3 output drive configuration (not used when GPIO3 is configured as		
2		SDOUT2). 0d = Hi-Z output 1d = Drive active low and active high		0
1	0	2d = Drive active low and weak high 3d = Drive active low and Hi-Z 4d = Drive weak low and active high	Not applicable for PCM6260-Q1.	0
0	0	5d = Drive Hi-Z and active high 6d to 7d = Reserved		0
	00100100	Address :	0v24	0.00
				0x00
hit	00000000	Default Value :	0x00	00000000
bit	00000000 default			
bit 7	default 0	Default Value: Definition GPI1 configuration. Od = GPI1 is disabled 1d to 6d = Reserved 7d = GPI1 is configured as an input to power down all ADC channels 8d = GPI1 is configured as an input to control when MICBIAS turns on or off	0x00 Description	00000000
7	default 0	Default Value: Definition GPI1 configuration. 0d = GPI1 is disabled 1d to 6d = Reserved 7d = GPI1 is configured as an input to power down all ADC channels 8d = GPI1 is configured as an input to control when MICBIAS turns on or off (MICBIAS_EN) 9d = GPI1 is configured as a general-purpose input (GPI) 10d = GPI1 is configured as a master clock input (MCLK) 11d = GPI1 is configured as an ASI input for daisy-chain (SDIN) 12d = Reserved	0x00	00000000 Setting 0
7 6 5	default 0 0 0 0	Default Value : Definition GPI1 configuration. Od = GPI1 is disabled 1d to 6d = Reserved 7d = GPI1 is configured as an input to power down all ADC channels 8d = GPI1 is configured as an input to control when MICBIAS turns on or off (MICBIAS_EN) 9d = GPI1 is configured as a general-purpose input (GPI) 10d = GPI1 is configured as a master clock input (MCLK) 11d = GPI1 is configured as an ASI input for daisy-chain (SDIN) 12d = Reserved 13d = Reserved	0x00 Description	00000000 Setting 0 0 0
7 6 5 4 3 2 1	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Default Value : Definition GPI1 configuration. Od = GPI1 is disabled Id to 6d = Reserved 7d = GPI1 is configured as an input to power down all ADC channels 8d = GPI1 is configured as an input to control when MICBIAS turns on or off (MICBIAS_EN) 9d = GPI1 is configured as a general-purpose input (GPI) 10d = GPI1 is configured as a master clock input (MCLK) 11d = GPI1 is configured as an ASI input for daisy-chain (SDIN) 12d = Reserved 13d = Reserved Reserved	0x00 Description	00000000 Setting 0 0 0 0 0 0 0 0 0 0 0
7 6 5 4 3 2 1 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Default Value : Definition GPI1 configuration. Od = GPI1 is disabled 1d to 6d = Reserved 7d = GPI1 is configured as an input to power down all ADC channels 8d = GPI1 is configured as an input to control when MICBIAS turns on or off (MICBIAS_EN) 9d = GPI1 is configured as a general-purpose input (GPI) 10d = GPI1 is configured as a master clock input (MCLK) 11d = GPI1 is configured as an ASI input for daisy-chain (SDIN) 12d = Reserved 13d = Reserved Reserved	0x00 Description Not applicable for PCM6260-Q1.	00000000 Setting 0 0 0 0 0 0 0 0 0 0 0 0 0
7 6 5 4 3 2 1 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Default Value : Definition GPI1 configuration. Od = GPI1 is disabled 1d to 6d = Reserved 7d = GPI1 is configured as an input to power down all ADC channels 8d = GPI1 is configured as an input to control when MICBIAS turns on or off (MICBIAS_EN) 9d = GPI1 is configured as a general-purpose input (GPI) 10d = GPI1 is configured as a master clock input (MCLK) 11d = GPI1 is configured as an ASI input for daisy-chain (SDIN) 12d = Reserved 13d = Reserved Reserved Reserved	0x00 Description Not applicable for PCM6260-Q1.	00000000 Setting 0 0 0 0 0 0 0 0 0 0 0 0 0 0
7 6 5 4 3 2 1 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Default Value : Definition GPI1 configuration. Od = GPI1 is disabled 1d to 6d = Reserved 7d = GPI1 is configured as an input to power down all ADC channels 8d = GPI1 is configured as an input to control when MICBIAS turns on or off (MICBIAS_EN) 9d = GPI1 is configured as a general-purpose input (GPI) 10d = GPI1 is configured as a master clock input (MCLK) 11d = GPI1 is configured as an ASI input for daisy-chain (SDIN) 12d = Reserved 13d = Reserved Reserved	0x00 Description Not applicable for PCM6260-Q1.	00000000 Setting 0 0 0 0 0 0 0 0 0 0 0 0 0
7 6 5 4 3 2 1 0	0000000000default	Default Value: Definition GPI1 configuration. Od = GPI1 is disabled 1d to 6d = Reserved 7d = GPI1 is configured as an input to power down all ADC channels 8d = GPI1 is configured as an input to control when MICBIAS turns on or off (MICBIAS_EN) 9d = GPI1 is configured as a general-purpose input (GPI) 10d = GPI1 is configured as a master clock input (MCLK) 11d = GPI1 is configured as an ASI input for daisy-chain (SDIN) 12d = Reserved 13d = Reserved 14d = Reserved Reserved Address: Default Value: Definition GPI2 configuration. Od = GPI2 is disabled	0x00 Description Not applicable for PCM6260-Q1. 0x25 0x00	00000000 Setting 0 0 0 0 0 0 0 0 0 0 0 0 0
7 6 5 4 3 2 1 0 bit	00100101 000000000 00100101 000000000 001001	Default Value: Definition GPI1 configuration. Od = GPI1 is disabled 1d to 6d = Reserved 7d = GPI1 is configured as an input to power down all ADC channels 8d = GPI1 is configured as an input to control when MICBIAS turns on or off (MICBIAS_EN) 9d = GPI1 is configured as a general-purpose input (GPI) 10d = GPI1 is configured as a master clock input (MCLK) 11d = GPI1 is configured as an ASI input for daisy-chain (SDIN) 12d = Reserved 13d = Reserved 14d = Reserved Reserved Address: Default Value: Definition GPI2 configuration. 0d = GPI2 is disabled 1d to 6d = Reserved 7d = GPI2 is configured as an input to power down all ADC channels 8d = GPI2 is configured as an input to control when MICBIAS turns on or off (MICBIAS_EN)	0x00 Description Not applicable for PCM6260-Q1. 0x25 0x00 Description	00000000 Setting 0 0 0 0 0 0 0 0 0 0 0 0 0
7 6 6 5 4 3 2 1 1 0 bit 7 7	00100101 00000000 00100101 00000000	Default Value: Definition GPI1 configuration. Od = GPI1 is disabled 1d to 6d = Reserved 7d = GPI1 is configured as an input to power down all ADC channels 8d = GPI1 is configured as an input to control when MICBIAS turns on or off (MICBIAS_EN) 9d = GPI1 is configured as a general-purpose input (GPI) 10d = GPI1 is configured as a master clock input (MCLK) 11d = GPI1 is configured as an ASI input for daisy-chain (SDIN) 12d = Reserved 13d = Reserved Reserved Address: Default Value: Definition GPI2 configuration. Od = GPI2 is disabled 1d to 6d = Reserved 7d = GPI2 is configured as an input to power down all ADC channels 8d = GPI2 is configured as an input to control when MICBIAS turns on or off (MICBIAS_EN) 9d = GPI2 is configured as a general-purpose input (GPI) 10d = GPI2 is configured as a master clock input (MCLK) 11d = GPI2 is configured as an ASI input for daisy-chain (SDIN) 12d = Reserved	0x00 Description Not applicable for PCM6260-Q1. 0x25 0x00	00000000 Setting 0 0 0 0 0 0 0 0 0 0 0 0 0
7 6 6 5 5 bit 7 6 6 5 5 4 4	00100101 00000000 000000000 00100101 000000	Default Value: Definition GPI1 configuration. Od = GPI1 is disabled 1d to 6d = Reserved 7d = GPI1 is configured as an input to power down all ADC channels 8d = GPI1 is configured as an input to control when MICBIAS turns on or off (MICBIAS_EN) 9d = GPI1 is configured as a general-purpose input (GPI) 10d = GPI1 is configured as a master clock input (MCLK) 11d = GPI1 is configured as an ASI input for daisy-chain (SDIN) 12d = Reserved 13d = Reserved 14d = Reserved Reserved Address: Default Value: Definition GPI2 configuration. Od = GPI2 is disabled 1d to 6d = Reserved 7d = GPI2 is configured as an input to power down all ADC channels 8d = GPI2 is configured as an input to control when MICBIAS turns on or off (MICBIAS_EN) 9d = GPI2 is configured as a general-purpose input (GPI) 10d = GPI2 is configured as a master clock input (MCLK) 11d = GPI2 is configured as an ASI input for daisy-chain (SDIN) 12d = Reserved 13d = Reserved 14d = Reserved	0x00 Description Not applicable for PCM6260-Q1. 0x25 0x00 Description	00000000 Setting 0 0 0 0 0 0 0 0 0 0 0 0 0
77 66 55 44 33 22 11 00 bitt 77 66 55 44 33 22 11	00100101 000000000 0000000000000000000	Definition GPI1 configuration. Od = GPI1 is disabled 1d to 6d = Reserved 7d = GPI1 is configured as an input to power down all ADC channels 8d = GPI1 is configured as an input to control when MICBIAS turns on or off (MICBIAS_EN) 9d = GPI1 is configured as a general-purpose input (GPI) 10d = GPI1 is configured as a master clock input (MCLK) 11d = GPI1 is configured as an ASI input for daisy-chain (SDIN) 12d = Reserved 13d = Reserved Reserved Address: Default Value: Definition GPI2 configuration. 0d = GPI2 is disabled 1d to 6d = Reserved 7d = GPI2 is configured as an input to power down all ADC channels 8d = GPI2 is configured as an input to control when MICBIAS turns on or off (MICBIAS_EN) 9d = GPI2 is configured as a master clock input (MCLK) 11d = GPI2 is configured as an ASI input for daisy-chain (SDIN) 12d = Reserved Reserved Reserved	0x00 Description Not applicable for PCM6260-Q1. 0x25 0x00 Description	00000000 Setting 0 0 0 0 0 0 0 0 0 0 0 0 0
77 66 55 bit 77 66 55 44 33 22 11 0	00000000000000000000000000000000000000	Default Value : Definition GPI1 configuration. Od = GPI1 is disabled 1d to 6d = Reserved 7d = GPI1 is configured as an input to power down all ADC channels 8d = GPI1 is configured as an input to control when MICBIAS turns on or off (MICBIAS_EN) 9d = GPI1 is configured as a general-purpose input (GPI) 10d = GPI1 is configured as a master clock input (MCLK) 11d = GPI1 is configured as an ASI input for daisy-chain (SDIN) 12d = Reserved 13d = Reserved Reserved Address: Default Value: Definition GPI2 configuration. 0d = GPI2 is disabled 1d to 6d = Reserved 7d = GPI2 is configured as an input to power down all ADC channels 8d = GPI2 is configured as an input to control when MICBIAS turns on or off (MICBIAS_EN) 9d = GPI2 is configured as a general-purpose input (GPI) 10d = GPI2 is configured as a master clock input (MCLK) 11d = GPI2 is configured as an ASI input for daisy-chain (SDIN) 12d = Reserved Reserved	0x25 0x00 Description Not applicable for PCM6260-Q1. Ox25 0x00 Description Not applicable for PCM6260-Q1.	00000000 Setting 0 0 0 0 0 0 0 0 0 0 0 0 0
77 66 55 44 33 22 11 00 bitt 77 66 55 44 33 22 11	001001101 0000000000000000000000000000	Default Value : Definition GPI1 configuration. Od = GPI1 is disabled 1d to 6d = Reserved 7d = GPI1 is configured as an input to power down all ADC channels 8d = GPI1 is configured as an input to control when MICBIAS turns on or off (MICBIAS_EN) 9d = GPI1 is configured as a general-purpose input (GPI) 10d = GPI1 is configured as a master clock input (MCLK) 11d = GPI1 is configured as an ASI input for daisy-chain (SDIN) 12d = Reserved 13d = Reserved Reserved Address: Default Value : Definition GPI2 configuration. 0d = GPI2 is disabled 1d to 6d = Reserved 7d = GPI2 is configured as an input to power down all ADC channels 8d = GPI2 is configured as an input to control when MICBIAS turns on or off (MICBIAS_EN) 9d = GPI2 is configured as a general-purpose input (GPI) 10d = GPI2 is configured as an ASI input for daisy-chain (SDIN) 12d = Reserved Reserved Reserved	0x25 0x20 Description Not applicable for PCM6260-Q1. Ox25 0x00 Description Not applicable for PCM6260-Q1.	000000000 Setting 0 0 0 0 0 0 0 0 0 0 0 0 0
77 66 55 bit 77 66 55 44 33 22 11 00	00000000000000000000000000000000000000	Default Value : Definition GPI1 configuration. Od = GPI1 is disabled 1d to 6d = Reserved 7d = GPI1 is configured as an input to power down all ADC channels 8d = GPI1 is configured as an input to control when MICBIAS turns on or off (MICBIAS_EN) 9d = GPI1 is configured as a general-purpose input (GPI) 10d = GPI1 is configured as a master clock input (MCLK) 11d = GPI1 is configured as an ASI input for daisy-chain (SDIN) 12d = Reserved 13d = Reserved Reserved Address: Default Value: Definition GPI2 configuration. 0d = GPI2 is disabled 1d to 6d = Reserved 7d = GPI2 is configured as an input to power down all ADC channels 8d = GPI2 is configured as an input to control when MICBIAS turns on or off (MICBIAS_EN) 9d = GPI2 is configured as a general-purpose input (GPI) 10d = GPI2 is configured as a master clock input (MCLK) 11d = GPI2 is configured as an ASI input for daisy-chain (SDIN) 12d = Reserved Reserved	0x25 0x20 Description Not applicable for PCM6260-Q1. Ox25 0x00 Description Not applicable for PCM6260-Q1.	000000000 Setting 0 0 0 0 0 0 0 0 0 0 0 0 0

7	0	GPIO1 output value when configured as a GPO. Od = Drive the output with a value of 0 1d = Drive the output with a value of 1	GPIO1未使用	0
6	0	GPIO2 output value when configured as a GPO. Not applicable for PCM6x60-Q1. Od = Drive the output with a value of 0 1d = Drive the output with a value of 1	Not applicable for PCM6260-Q1.	0
5	0	GPIO3 output value when configured as a GPO. Not applicable for PCM6x60-Q1. Od = Drive the output with a value of 0 1d = Drive the output with a value of 1	Not applicable for PCM6260-Q1.	0
4	0			0
3	0			0
2	0	Reserved		0
1	0			0
0	0			0

	00100111	Address :		0x00
	00000000	Default Value :	0x00	00000000
bit	default	Definition	Description	Setting
7	0	GPIO1 monitor value when configured as a GPI. 0d = Input monitor value 0 1d = Input monitor value 1		0
6	0	GPIO2 monitor value when configured as a GPI. Not applicable for PCM6x60-Q1. 0d = Input monitor value 0 1d = Input monitor value 1		0
5	0	GPIO3 monitor value when configured as a GPI. Not applicable for PCM6x60-Q1. 0d = Input monitor value 0 1d = Input monitor value 1		0
4	0	GPI1 monitor value when configured as a GPI. Not applicable for PCM6x60-Q1. 0d = Input monitor value 0 1d = Input monitor value 1		0
3	0	GPI2 monitor value when configured as a GPI. Not applicable for PCM6x60-Q1. 0d = Input monitor value 0 1d = Input monitor value 1		0
1	0	Reserved		0

	00101000	Address :	0x28	0x60
	00000000	Default Value :	0x00	01100000
bit	default	Definition	Description	Setting
7	0	Interrupt polarity. Od = Active low (IRQZ) 1d = Active high (IRQ)	中断低电平有效	0
6	0	Interrupt event configuration. Od = INT asserts on any unmasked latched interrupts event 1d = Reserved 2d = INT asserts for 2 ms (typical) for every 4-ms (typical) duration on any	中断在每个pluse上都有2ms	1
5	0	unmasked latched interrupts event 3d = INT asserts for 2 ms (typical) one time on each pulse for any unmasked interrupts event	Total process application	1
4	0	Powerdown configuration when fault detected for any channel or MICBIAS fault detected. Od = Faults event are not used for ADC and MICBIAS power down. It is recommend to set these bits as 2d to shutdown the blocks for which fault occurred. Id = Only unmasked faults are used for power down of respective ADC	不使用PD模式	0
3	0	channel; In case of MICBIAS fault detected, MICBIAS and all ADC channels gets powered-down based on P0_R58 settings 2d = Both masked or unmasked faults are used for power down of respective ADC channel; In case of MICBIAS fault detected, MICBIAS and all ADC channels gets powered-down based on P0_R58 settings. 3d = Reserved	TILMI UIRE	0
2	0	Interrupt latch registers readback configuration. Od = All interrupts can be read through the LTCH registers 1d = Only unmasked interrupts can be read through the LTCH registers	所有中断都能通过LTCH寄存器读取	0
1	0	Recovery configuration for ADC channels when fault goes away. Od = Auto recovery, ADC channels are re-powered up when fault goes away 1d = Manual recovery, ADC channels are required to power-up manually using P0_R119 when fault goes away	故障消失后自动复归	0
0	0	Configuration for clearing LTCH register bits. Od = LTCH register bits are cleared on register read only if live status is zero 1d = LTCH register bits are cleared on register read irrespective of live status and set only if live status goes again low to high	只在读取时clear	0

	00101001	Address :	0x29
	11111111	Default Value :	0xFF
bit	default	Definition	Description
7	1	ASI clock error mask. 0d = Unmask 1d = Mask	POC default setting
6	1	PLL lock interrupt mask. 0d = Unmask 1d = Mask	POC default setting

0xFF
11111111
Setting
1
1

5				
	1	Boost or MICBIAS over temperature interrupt mask. 0d = Unmask 1d = Mask	POC default setting	1
4	1	Boost or MICBIAS over current interrupt mask. Od = Unmask 1d = Mask	POC default setting	1
3		Reserved		1
2		Reserved Reserved		1
0		Reserved		1
	00101010	Address : Default Value :	0x2A 0x03	0x01 00000001
	default	Definition Definition	Description	Setting
7	0	Channel 1 input DC faults diagnostic interrupt mask. Od = Unmask 1d = Mask	POC default setting	0
6	0	Channel 2 input DC faults diagnostic interrupt mask. Od = Unmask 1d = Mask	POC default setting	0
5	0	Channel 3 input DC faults diagnostic interrupt mask. Od = Unmask 1d = Mask	POC default setting	0
4	0	Channel 4 input DC faults diagnostic interrupt mask. Od = Unmask 1d = Mask	POC default setting	0
3	0	Channel 5 input DC faults diagnostic interrupt mask. Applicable only for PCM6x60-Q1. Od = Unmask 1d = Mask	POC default setting	0
2	0	Channel 6 input DC faults diagnostic interrupt mask. Applicable only for PCM6x60-Q1. Od = Unmask 1d = Mask	POC default setting	0
1	1	Input faults diagnostic interrupt mask for "short to VBAT_IN" detect when VBAT_IN voltage is less than MICBIAS voltage. Od = Unmask 1d = Mask	POC_ICC VBAT_IN未使用	0
0	1	Reserved		1
		noorvou		
	00101011	Address :	0x2B	0x00
	00000000 default	Default Value : Definition	0x00	00000000
it	uelault	Input diagnostics; Open inputs fault interrupt mask.	Description	Setting
7	0	0d = Unmask 1d = Mask	POC default setting	0
6	0	1d = Mask	POC default setting	0
5	0	Input diagnostics; INxP shorted to ground fault interrupt mask. 0d = Unmask 1d = Mask	POC default setting	0
4	0	Input diagnostics; INxM shorted to ground fault interrupt mask. Od = Unmask 1d = Mask	POC default setting	0
3	0	Input diagnostics; INxP shorted to MICBIAS fault interrupt mask. Od = Unmask 1d = Mask	POC default setting	0
2	0	Input diagnostics; INxM shorted to MICBIAS fault interrupt mask. Od = Unmask 1d = Mask	POC default setting	0
1	0	Input diagnostics; INxP shorted to VBAT_IN fault interrupt mask. Od = Unmask 1d = Mask	POC default setting	0
1 0		0d = Unmask	POC default setting POC default setting	0
0	0	0d = Unmask 1d = Mask Input diagnostics; INxM shorted to VBAT_IN fault interrupt mask. 0d = Unmask 1d = Mask	POC default setting	0
0	00101100	0d = Unmask 1d = Mask Input diagnostics; INxM shorted to VBAT_IN fault interrupt mask. 0d = Unmask 1d = Mask Address:	POC default setting 0x2C	0 0x00
0	0	0d = Unmask 1d = Mask Input diagnostics; INxM shorted to VBAT_IN fault interrupt mask. 0d = Unmask 1d = Mask	POC default setting	0
0	0 00101100 00000000 default	0d = Unmask 1d = Mask Input diagnostics; INxM shorted to VBAT_IN fault interrupt mask. 0d = Unmask 1d = Mask Address : Default Value :	POC default setting 0x2C 0x00	0 0x00 00000000
0 Dit	00101100 00000000 default	0d = Unmask 1d = Mask 1d = Mask Input diagnostics; INxM shorted to VBAT_IN fault interrupt mask. 0d = Unmask 1d = Mask Address: Default Value: Definition Fault status for an ASI bus clock error (self-clearing bit). 0d = No fault detected	POC default setting 0x2C 0x00	0 0x00 00000000 Setting
0 bit 7	0 00101100 00000000 default 0	0d = Unmask 1d = Mask Input diagnostics; INxM shorted to VBAT_IN fault interrupt mask. 0d = Unmask 1d = Mask Input diagnostics; INxM shorted to VBAT_IN fault interrupt mask. 0d = Unmask 1d = Mask Address: Default Value: Definition Fault status for an ASI bus clock error (self-clearing bit). 0d = No fault detected 1d = Fault detected Status of PLL lock (self-clearing bit). 0d = No PLL lock detected	POC default setting 0x2C 0x00	0 0x00 00000000 Setting
0 Dit 7	0 00101100 00000000 default 0	0d = Unmask 1d = Mask Input diagnostics; INxM shorted to VBAT_IN fault interrupt mask. 0d = Unmask 1d = Mask Address: Default Value: Definition Fault status for an ASI bus clock error (self-clearing bit). 0d = No fault detected 1d = Fault detected Status of PLL lock (self-clearing bit). 0d = No PLL lock detected 1d = PLL lock detected Fault status for boost or MICBIAS over temperature (self-clearing bit). 0d = No fault detected	POC default setting 0x2C 0x00	0 0x00 00000000 Setting 0
0 oit 7 6 5 4 3	0 00101100 00000000 default 0 0	0d = Unmask 1d = Mask Input diagnostics; INxM shorted to VBAT_IN fault interrupt mask. 0d = Unmask 1d = Mask Input diagnostics; INxM shorted to VBAT_IN fault interrupt mask. 0d = Unmask 1d = Mask Address: Default Value: Definition Fault status for an ASI bus clock error (self-clearing bit). 0d = No fault detected 1d = Fault detected Status of PLL lock (self-clearing bit). 0d = No PLL lock detected 1d = PLL lock detected Fault status for boost or MICBIAS over temperature (self-clearing bit). 0d = No fault detected 1d = Fault detected Fault status for boost or MICBIAS over current (self-clearing bit). 0d = No fault detected 1d = Fault detected 1d = Fault detected Reserved	POC default setting 0x2C 0x00	0 0x00 00000000 Setting 0 0 0
0 0 7 6 5 4 3 2	0 00101100 00000000 default 0 0	0d = Unmask 1d = Mask Input diagnostics; INxM shorted to VBAT_IN fault interrupt mask. 0d = Unmask 1d = Mask Address: Default Value: Definition Fault status for an ASI bus clock error (self-clearing bit). 0d = No fault detected 1d = Fault detected Status of PLL lock (self-clearing bit). 0d = No PLL lock (self-clearing bit). 0d = No PLL lock detected 1d = PLL lock detected 1d = Pull detected Fault status for boost or MICBIAS over temperature (self-clearing bit). 0d = No fault detected 1d = Fault detected Fault status for boost or MICBIAS over current (self-clearing bit). 0d = No fault detected 1d = Fault detected Reserved Reserved	POC default setting 0x2C 0x00	0 0x00 00000000 Setting 0 0 0 0
0 ooit 7 6 5 4 3	0 00101100 00000000 default 0 0 0 0 0 0 0 0	0d = Unmask 1d = Mask Input diagnostics; INxM shorted to VBAT_IN fault interrupt mask. 0d = Unmask 1d = Mask Input diagnostics; INxM shorted to VBAT_IN fault interrupt mask. 0d = Unmask 1d = Mask Address: Default Value: Definition Fault status for an ASI bus clock error (self-clearing bit). 0d = No fault detected 1d = Fault detected Status of PLL lock (self-clearing bit). 0d = No PLL lock detected 1d = PLL lock detected Fault status for boost or MICBIAS over temperature (self-clearing bit). 0d = No fault detected 1d = Fault detected Fault status for boost or MICBIAS over current (self-clearing bit). 0d = No fault detected 1d = Fault detected 1d = Fault detected Reserved	POC default setting 0x2C 0x00	0 0x00 00000000 Setting 0 0 0
0	0 00101100 00000000 default 0 0 0 0 0 0 0 0	0d = Unmask 1d = Mask Input diagnostics; INxM shorted to VBAT_IN fault interrupt mask. 0d = Unmask 1d = Mask Address: Default Value: Definition Fault status for an ASI bus clock error (self-clearing bit). 0d = No fault detected 1d = Fault detected 1d = Fault lock (self-clearing bit). 0d = No PLL lock (self-clearing bit). 0d = No PLL lock detected 1d = PLL lock detected 1d = PLL lock detected 1d = PLL lock detected Fault status for boost or MICBIAS over temperature (self-clearing bit). 0d = No fault detected 1d = Fault detected Fault status for boost or MICBIAS over current (self-clearing bit). 0d = No fault detected Fault status for boost or MICBIAS over current (self-clearing bit). 0d = No fault detected Reserved Reserved Reserved Reserved Reserved	POC default setting 0x2C 0x00 Description	0 0x00 00000000 Setting 0 0 0 0 0 0 0

bit	default	Definition	Description	Setting
_	0	Status of CH1_LTCH (self-clearing bit).		
7	0	0d = No faults occurred in channel 1 1d = Atleast a fault has occurred in channel 1		0
6	0	Status of CH2_LTCH (self-clearing bit). 0d = No faults occurred in channel 2 1d = Atleast a fault has occurred in channel 2		0
5	0	Status of CH3_LTCH (self-clearing bit). 0d = No faults occurred in channel 3 1d = Atleast a fault has occurred in channel 3		0
4	0	Status of CH4_LTCH (self-clearing bit). 0d = No faults occurred in channel 4 1d = Atleast a fault has occurred in channel 4		0
3	0	Status of CH5_LTCH (self-clearing bit). Applicable only for PCM6x60-Q1. 0d = No faults occurred in channel 5 1d = Atleast a fault has occurred in channel 5		0
2	0	Status of CH6_LTCH (self-clearing bit). Applicable only for PCM6x60-Q1. 0d = No faults occurred in channel 6 1d = Atleast a fault has occurred in channel 6		0
1	0	Status of short to VBAT_IN fault detected when VBAT_IN is less than MICBIAS (self-clearing bit). 0d = Short to VBAT_IN fault when VBAT_IN is less than MICBIAS has not occurred in any channel 1d = Short to VBAT_IN fault when VBAT_IN is less than MICBIAS has occurred in atleast one channel		0
0	0	Reserved		0
	00101110	Address :		0x00
	00000000 default	Default Value : Definition	0x00 Description	00000000 Setting
7		Channel 1 open input fault status (self-clearing bit). 0d = No open input detected 1d = Open input detected	Description	0
6	0	Channel 1 input pair short fault status (self-clearing bit). 0d = No input pair short detected 1d = Input short to each other detected		0
5	0	Channel 1 IN1P short to ground fault status (self-clearing bit). 0d = IN1P no short to ground detected 1d = IN1P short to ground detected		0
4	0	Channel 1 IN1M short to ground fault status (self-clearing bit). 0d = IN1M no short to ground detected 1d = IN1M short to ground detected		0
3	0	Channel 1 IN1P short to MICBIAS fault status (self-clearing bit). 0d = IN1P no short to MICBIAS detected 1d = IN1P short to MICBIAS detected		0
2	0	Channel 1 IN1M short to MICBIAS fault status (self-clearing bit). 0d = IN1M no short to MICBIAS detected 1d = IN1M short to MICBIAS detected		0
1	0	Channel 1 IN1P short to VBAT_IN fault status (self-clearing bit). 0d = IN1P no short to VBAT_IN detected 1d = IN1P short to VBAT_IN detected		0
0	0	Channel 1 IN1M short to VBAT_IN fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-54d, INT_LTCH2 register). 0d = IN1M no short to VBAT_IN detected 1d = IN1M short to VBAT_IN detected		0
	00101111	Address :	0x2F	0x00
	00000000 default	Default Value : Definition	0x00 Description	00000000 Setting
7		Channel 2 open input fault status (self-clearing bit). 0d = No open input detected 1d = Open input detected	Societa	0
6	0	Channel 2 input pair short fault status (self-clearing bit). 0d = No input pair short detected 1d = Input short to each other detected		0
5	0	Channel 2 IN2P short to ground fault status (self-clearing bit). 0d = IN2P no short to ground detected 1d = IN2P short to ground detected		0
4	0	Channel 2 IN2M short to ground fault status (self-clearing bit). 0d = IN2M no short to ground detected 1d = IN2M short to ground detected		0
3	0	Channel 2 IN2P short to MICBIAS fault status (self-clearing bit). 0d = IN2P no short to MICBIAS detected 1d = IN2P short to MICBIAS detected		0
2	0	Channel 2 IN2M short to MICBIAS detected 0d = IN2M no short to MICBIAS detected 1d = IN2M short to MICBIAS detected		0
1	0	Channel 2 IN2P short to VBAT_IN fault status (self-clearing bit). 0d = IN2P no short to VBAT_IN detected 1d = IN2P short to VBAT_IN detected		0
0	0	Channel 2 IN2M short to VBAT_IN fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-54d, INT_LTCH2 register). 0d = IN2M no short to VBAT_IN detected 1d = IN2M short to VBAT_IN detected		0
	00110000	Address :	0x30	0x00
	00000000	Default Value :		00000000
bit	default	Definition	Description	Setting

Channel 4 (putp paid short status (self-clearing bit) O					
Contract of Imputing and both Basin status gold Externing Inity O Service of Service	7	0	0d = No open input detected		0
Service of the Common C	6	0	Channel 3 input pair short fault status (self-clearing bit). 0d = No input pair short detected		0
Channel 3 NSM short to ground descreted Other MSM south to MSM south to MSM south to see the south to MSM south	5	0	Channel 3 IN3P short to ground fault status (self-clearing bit). 0d = IN3P no short to ground detected		0
Comment of BRIDE and the Statistic Microsoft States (self-cleaning bid). On the State of States And States (self-cleaning bid). On the States of States And States (self-cleaning bid). On the States of States (self-cleaning bid). On the States (self-cleaning bid). On th	4	0	Channel 3 IN3M short to ground fault status (self-clearing bit). 0d = IN3M no short to ground detected		0
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Description Descr	2	0	Channel 3 IN3M short to MICBIAS fault status (self-clearing bit). 0d = IN3M no short to MICBIAS detected		0
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Default Value : CADO Definition Description Descri	0	0	Channel 3 IN3M short to VBAT_IN fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-54d, INT_LTCH2 register). 0d = IN3M no short to VBAT_IN detected		0
Default Value : CADO Definition Description Descri		00440004			
Setting Description Desc					
Channel 4 (per in pour fault status (self-clearing bit). Channel 4 (per page shout page short detected 1d = Open input detected 1d = Open input detected 1d = Open input page short p					Setting
7 Oct = No open input detected 1d = Open input detected 0 Oct = Oct open input detected 1d = Open input detected 1d = Open input detected 1d = Input short short fault status (self-clearing bit). 0 Oct = No oning para short fault status (self-clearing bit). 0 Oct = Input short to each other detected 1d = Input short to sook other short sook other					
6 10 0 0 1 No input pair short detected 10 11 Input phort to go one of other detected 5 0 0 1 Name 1 NMP short to ground fault status (self-clearing bit). 6 0 0 1 NAP no short to ground fault status (self-clearing bit). 7 0 0 1 NAP no short to ground detected 8 0 0 1 NAP no short to ground detected 9 0 0 1 NAP no short to ground detected 9 0 0 1 NAP no short to ground detected 9 0 0 1 NAP no short to ground detected 9 0 0 1 NAP no short to ground detected 9 0 0 1 NAP no short to MCRAS detected 9 0 1 NAP no short to MCRAS detected 9 0 1 NAP no short to MCRAS detected 1 NAP no short to MCRAS no short to MCRAS detected 1 NAP no short to MCRAS detected 1 NAP no short to MCRAS no short to MCR	7	0	0d = No open input detected 1d = Open input detected		0
5 0 0 d = INAP no short to ground detected 4 0 0 d = INAP no short to ground detected 4 0 0 d = INAP no short to ground faut status (self-cleaning bit). 5 0 channel a INAP short to ground faut status (self-cleaning bit). 6 0 d = INAP no short to ground detected 1 d = INAM short to ground detected 1 d = INAM short to ground detected 2 0 0 d = INAP no short to MICBAS detected 1 d = INAP short to MICBAS detected 2 0 0 d = INAP no short to MICBAS detected 1 d = INAP short to MICBAS detected 1 d = INAM short to MICBAS detected 1 d = INAM short to MICBAS detected 2 0 0 d = INAP no short to MICBAS detected 1 d = INAM short to MICBAS detected 2 0 0 d = INAP no short to WAT IN faut status (self-cleaning bit). 1 0 0 d = INAP no short to WAT IN faut status (self-cleaning bit). 2 0 0 d = INAP no short to WAT IN faut status (self-cleaning bit). 3 0 0 d = INAP no short to WAT IN faut status (self-cleaning bit). 4 0 0 d = INAP no short to WAT IN faut status (self-cleaning bit). 5 0 0 d = INAP no short to WAT IN faut status (self-cleaning bit). 6 0 0 d = INAP no short to WAT IN faut status (self-cleaning bit). 7 0 0 d = INAP no short to WAT IN faut status (self-cleaning bit). 8 0 d = INAP no short to WAT IN faut status (self-cleaning bit). 9 0 d = INAP no short to WAT IN faut status (self-cleaning bit). 10 d = INAP no short to WAT IN faut status (self-cleaning bit). 10 d = INAP no short to ground status (self-cleaning bit). 10 d = INAP no short to ground status (self-cleaning bit). 10 d = INAP no short to ground status (self-cleaning bit). 10 d = INAP no short to ground status (self-cleaning bit). 11 d = INAP no short to ground status (self-cleaning bit). 12 d = INAP no short to ground status (self-cleaning bit). 13 d = INAP no short to ground status status (self-cleaning bit). 14 d = INAP no short to ground status (self-cleaning bit). 15 d = INAP no short to ground status status (self-cleaning bit). 16 d = INAP no short to WAT IN faut status (self-cleaning bit). 17 d = INAP no short to WAT IN faut sta	6	0	0d = No input pair short detected 1d = Input short to each other detected		0
d is = NAM host to ground detected late = NAM host to to MICBIAS fault status (self-clearing bit). Channel 4 INAM host to MICBIAS detected late = NAM host to WBAT, IN fault status (self-clearing bit). Channel 4 INAM host to WBAT, IN detected late = NAM host to ground host to WBAT, IN detected late = NAM host to ground detected late = NAM host to MCBAS detected late = NAM host to MCB	5	0	0d = IN4P no short to ground detected		0
3 0 0 d = INAP no short to MICBIAS detected 1 d = INAP short to MICBIAS detected 2 d = INAP short to MICBIAS detected 3 d = INAP short to MICBIAS fault status (self-clearing bit). 0 d = INAP no short to MICBIAS detected 4 d = INAP short to MICBIAS detected 5 d = INAP short to MICBIAS detected 6 d = INAP no short to MICBIAS detected 6 d = INAP no short to VBAT_IN detected 6 d = INAP no short to VBAT_IN detected 6 d = INAP short to VBAT_IN detected 7 d = INAP no short to VBAT_IN detected 7 d = INAP no short to VBAT_IN detected 8 d = INAP short to VBAT_IN detected 9 d = INAP no short to VBAT_IN detected 9 d = INAP no short to VBAT_IN detected 9 d = INAP no short to VBAT_IN detected 9 d = INAP no short to VBAT_IN detected 9 d = INAP no short to VBAT_IN detected 9 d = INAP no short to VBAT_IN detected 9 d = INAP no short to VBAT_IN detected 9 d = INAP no short to VBAT_IN detected 9 d = INAP no short to ground featered 9 d = INA	4	0	0d = IN4M no short to ground detected		0
2 0 de = NMA no short to MiCBIAS detected 1 1 0 0 de = NMA no short to MiCBIAS detected 2 1 0 clammed NMP short to VBAT_IN fault status (self-clearing bit). 3 0 de = NMA no short to VBAT_IN detected 4 1 de = NMA short to VBAT_IN detected 5 0 de = NMA no short to VBAT_IN detected 6 0 de = NMA no short to VBAT_IN detected 7 0 de = NMA no short to VBAT_IN detected 8 0 default Definition Description Description 8 0 default Definition Description Description Description 9 0 default Definition Description Descrip	3	0	0d = IN4P no short to MICBIAS detected		0
1 0 0d = INAP no short to VBAT_IN detected Channel 4 INAM short to VBAT_IN detected Channel 4 INAM short to VBAT_IN fault status (self-clearing bit - This bit gets clear on reading Page-O, Register-SAd_INT_LTCH2 register). O 0 = INAM no short to VBAT_IN detected Default Value : 0x00 0x00000000 Default Value : 0x00 Oxo00000000 To 0 = No open input fault status (self-clearing bit). O 0 = No open input detected Channel 5 Iny pair short fault status (self-clearing bit). O 0 = No input pair short fault status (self-clearing bit). O 0 = No input pair short fault status (self-clearing bit). O 0 = No input pair short detected D channel 5 Iny pair short of each other detected at a large input fault status (self-clearing bit). O 0 = INSP no short to each other detected D channel 5 INSP short to ground fault status (self-clearing bit). O 0 = INSP no short to ground detected at a large input fault status (self-clearing bit). O 0 = INSP no short to ground detected at a large input fault status (self-clearing bit). O 0 = INSP no short to ground detected at a large input fault status (self-clearing bit). O 0 = INSP no short to function fault status (self-clearing bit). O 0 = INSP no short to MICBIAS detected at a large input fault status (self-clearing bit). O 0 = INSP no short to MICBIAS detected at a large input fault status (self-clearing bit). O 0 = INSP no short to MICBIAS detected at a large input fault status (self-clearing bit). O 0 = INSP no short to VBAT_IN fault status (self-clearing bit). O 0 = INSP no short to VBAT_IN detected D channel 5 INSP short to VBAT_IN fault status (self-clearing bit). O 0 = INSP no short to VBAT_IN detected D channel inspective input fault status (self-clearing bit). O 0 = INSP no short to VBAT_IN detected D channel inspective input fault status (self-clearing bit). O 0 = INSP no short to VBAT_IN detected D channel inspective input fault status (self-clearing bit). O 0 = INSP no poir to VBAT_IN detected D channel inspective input fault status (self-clear	2	0	0d = IN4M no short to MICBIAS detected		0
0 des sclear on reading Page-0. Register-34d, INT_LTCH2 register). 0 del = INMA moshor to VBAT_IN detected 00110010	1	0	0d = IN4P no short to VBAT_IN detected		0
Oct Default Value Coco Oct	0	0	gets clear on reading Page-0, Register-54d, INT_LTCH2 register). 0d = IN4M no short to VBAT_IN detected		0
Channel 5 open input detected O Od = No open input fault status (self-clearing bit). Od = No open input detected Id = Open input detected Id = Open input detected O Od = No input pair short detected O Od = InSt No short to ground fault status (self-clearing bit). Od = INSP no short to ground detected O Od = INSP no short to ground detected O Od = INSP short to ground detected Od = INSM short to ground detected Od = INSM short to ground detected Od = INSM short to MICBIAS fault status (self-clearing bit). Od = INSP short to MICBIAS detected Od = INSM short to MICBIAS detected Od = INSP short to MICBIAS detected Od = INSM short to MICBIAS detected Od		00110010	Address :	0x32	0x00
7		00000000	Default Value :	0x00	00000000
7 0 0d = No open input detected 1d = Open input detected 1d = Open input detected 2d = Open input detected 3d = Open input pair short fault status (self-clearing bit). 6 0 0d = No input pair short detected 2d = Open input fault status (self-clearing bit). 5 0 0d = INSP short to ground fault status (self-clearing bit). 6 0 0d = INSP no short to ground fault status (self-clearing bit). 7 0 0d = No input pair short detected 3d = Open input fault status (self-clearing bit). 9 0 0d = No input pair short to ground fault status (self-clearing bit). 9 0 0d = INSP short to ground detected 3d = Open input fault status (self-clearing bit). 9 0 0d = No input pair short to MICBIAS fault status (self-clearing bit). 9 0 0d = INSP short to MICBIAS fault status (self-clearing bit). 10 0d = INSP short to MICBIAS fault status (self-clearing bit). 11 0 0d = INSP short to MICBIAS fault status (self-clearing bit). 12 0 0d = INSP short to MICBIAS detected 3d = INSP short to MICBIAS detected 3d = INSP short to VBAT_IN fault status (self-clearing bit). 12 0 0d = INSP short to VBAT_IN detected 3d = INSP short to VBAT_IN fault status (self-clearing bit). 13 0 0d = INSP short to VBAT_IN fault status (self-clearing bit). 14 0 0d = INSP short to VBAT_IN detected 3d = INSP short to VBAT_IN fault status (self-clearing bit - This bit gets clear on reading Page-0. Register-5dd, INT_LTCH2 register). 15 0 0d = INSM short to VBAT_IN detected 3d = INSM short to VBAT_IN	bit	default		Description	Setting
6 0 0 da = No input pair short detected 1d = Input short to each other detected 2d = Input short to each other detected 3d = Input short to ground fault status (self-clearing bit). 0 0 da = INSP no short to ground detected 3d = INSP short to ground fault status (self-clearing bit). 0 0 da = INSP no short to ground fault status (self-clearing bit). 0 0 da = INSM no short to ground fault status (self-clearing bit). 0 0 da = INSM no short to ground detected 3d = INSM short to ground detected 3d = INSP short to MICBIAS fault status (self-clearing bit). 0 0 da = INSP no short to MICBIAS fault status (self-clearing bit). 0 0 da = INSP no short to MICBIAS detected 3d = INSM short to MICBIAS detected 3d = INSM short to MICBIAS detected 3d = INSM no short to MICBIAS detected 3d = INSM no short to VBAT_IN fault status (self-clearing bit). 0 0 da = INSP no short to VBAT_IN fault status (self-clearing bit). 0 0 da = INSP no short to VBAT_IN fault status (self-clearing bit - This bit 3d = INSP short to VBAT_IN fault status (self-clearing bit - This bit 3d = INSP short to VBAT_IN fault status (self-clearing bit - This bit 3d = INSP short to VBAT_IN fault status (self-clearing bit - This bit 3d = INSP short to VBAT_IN fault status (self-clearing bit - This bit 3d = INSP short to VBAT_IN fault status (self-clearing bit - This bit 3d = INSP short to VBAT_IN fault status (self-clearing bit - This bit 3d = INSP short to VBAT_IN fault status (self-clearing bit - This bit 3d = INSP short to VBAT_IN fault status (self-clearing bit - This bit 3d = INSP short to VBAT_IN fault status (self-clearing bit - This bit 3d = INSP short to VBAT_IN fault status (self-clearing bit - This bit 3d = INSP short to VBAT_IN fault status (self-clearing bit - This bit 3d = INSP short to VBAT_IN fault status (self-clearing bit - This bit 3d = INSP short to VBAT_IN fault status (self-clearing bit - This bit 3d = INSP short to VBAT_IN fault status (self-clearing bit - This bit 3d = INSP short to This bit 3d = INSP short to This bit 3d = INSP short to This	7	0	0d = No open input detected		0
5 0 0 d = IN5P no short to ground detected 1 d = IN5P short to ground detected 2 Channel 5 IN5M short to ground fault status (self-clearing bit). 3 0 d = IN5M no short to micinal status (self-clearing bit). 3 0 0 d = IN5M no short to MicBlAS fault status (self-clearing bit). 4 Channel 5 IN5P short to MicBlAS fault status (self-clearing bit). 5 0 0 d = IN5P no short to MicBlAS detected 6 0 channel 5 IN5M short to MicBlAS detected 7 0 0 d = IN5M no short to MicBlAS fault status (self-clearing bit). 9 0 d = IN5M no short to MicBlAS detected 1 0 0 d = IN5M short to MicBlAS detected 2 0 channel 5 IN5P short to VBAT_IN fault status (self-clearing bit). 1 0 0 d = IN5P no short to VBAT_IN fault status (self-clearing bit). 1 0 0 d = IN5P short to VBAT_IN fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-54d, INT_LTCH2 register). 1 0 0 d = IN5M short to VBAT_IN detected 2 0 d = IN5M short to VBAT_IN detected 3 d = IN5M short to VBAT_IN detected 4 d = IN5M short to VBAT_IN detected 5 d = IN5M short to VBAT_IN fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-54d, INT_LTCH2 register). 2 0 d = IN5M short to VBAT_IN detected 3 0 monodooo	6	0	0d = No input pair short detected		0
4 0 0 d = INS5M no short to ground detected 1 d = INS5M short to ground detected 2 Channel 5 INSP short to MICBIAS fault status (self-clearing bit). 3 0 0 d = INSP no short to MICBIAS detected 1 d = INS5M short to MICBIAS fault status (self-clearing bit). 2 0 0 d = INS5M short to MICBIAS fault status (self-clearing bit). 3 0 0 d = INS5M short to MICBIAS detected 2 0 Channel 5 INSM short to MICBIAS detected 3 0 0 d = INS5M no short to MICBIAS detected 4 1 0 0 d = INS5M short to VBAT_IN fault status (self-clearing bit). 4 0 0 d = INS5P short to VBAT_IN fault status (self-clearing bit). 5 0 0 d = INSP short to VBAT_IN fault status (self-clearing bit - This bit gets clear on reading Page- 0, Register-54d, INT_LTCH2 register). 6 0 d = INS5M short to VBAT_IN detected d = INS5M short to VBAT_IN detected d = INS5M short to VBAT_IN detected 6 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	5	0	0d = IN5P no short to ground detected		0
3	4	0	0d = IN5M no short to ground detected		0
Channel 5 IN5M short to MICBIAS fault status (self-clearing bit). O	3	0	0d = IN5P no short to MICBIAS detected		0
Channel 5 IN5P short to VBAT_IN fault status (self-clearing bit). 0	2	0	Channel 5 IN5M short to MICBIAS fault status (self-clearing bit). 0d = IN5M no short to MICBIAS detected		0
Channel 5 IN5M short to VBAT_IN fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-54d, INT_LTCH2 register). 0d = IN5M no short to VBAT_IN detected 1d = IN5M short to VBAT_IN detected 00110011	1	0	Channel 5 IN5P short to VBAT_IN fault status (self-clearing bit). 0d = IN5P no short to VBAT_IN detected		0
00000000 Default Value: 0x00 it default Definition Description Channel 6 open input fault status (self-clearing bit). 7 0 0d = No open input detected Default Value: 0x00 Setting	0	0	Channel 5 IN5M short to VBAT_IN fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-54d, INT_LTCH2 register). 0d = IN5M no short to VBAT_IN detected		0
00000000 Default Value: 0x00 it default Definition Description Channel 6 open input fault status (self-clearing bit). 7 0 0d = No open input detected Default Value: 0x00 Setting		00110011		0.00	
oit default Definition Description Setting Channel 6 open input fault status (self-clearing bit). O d = No open input detected 0					
Channel 6 open input fault status (self-clearing bit). 7 0 0d = No open input detected 0					
7 0 0 d = No open input detected 0					Joseffing
Id = Open input detected	7	0	0d = No open input detected		0
			1a - Open input detected		

6	0	Channel 6 input pair short fault status (self-clearing bit). Od = No input pair short detected		0
5	0	1d = Input short to each other detected Channel 6 IN6P short to ground fault status (self-clearing bit). Od = IN6P no short to ground detected		0
		1d = IN6P short to ground detected Channel 6 IN6M short to ground fault status (self-clearing bit).		
4	0	0d = IN6M no short to ground detected 1d = IN6M short to ground detected		0
3	0	Channel 6 IN6P short to MICBIAS fault status (self-clearing bit). 0d = IN6P no short to MICBIAS detected 1d = IN6P short to MICBIAS detected		0
2	0	Channel 6 IN6M short to MICBIAS fault status (self-clearing bit). 0d = IN6M no short to MICBIAS detected 1d = IN6M short to MICBIAS detected		0
1	0	Channel 6 IN6P short to VBAT_IN fault status (self-clearing bit). 0d = IN6P no short to VBAT_IN detected 1d = IN6P short to VBAT IN detected		0
0	0	Channel 6 IN6M short to VBAT_IN fault status (self-clearing bit - This bit		0
_	00110100	Address :	0v3/I	0x00
	00000000	Default Value:		00000000
bit	default	Definition	Description	Setting
7	0	INXP over voltage fault mask. Od = Unmask 1d = Mask	POC default setting	0
6	0	INxM over voltage fault mask. Od = Unmask 1d = Mask	POC default setting	0
5	O	MICBIAS high current fault mask. Od = Unmask 1d = Mask	POC default setting	0
4	0	MICBIAS low current fault mask. Od = Unmask 1d = Mask	POC default setting	0
3	0	MICBIAS over voltage fault mask. Od = Unmask 1d = Mask	POC default setting	0
2 1 0	0	Reserved		0 0 0
-	00110101	Address :		0x00
hit	00000000	Default Value :	0x00	00000000
bit 7				
	00000000 default	Default Value : Definition Channel 1 IN1P over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-46d, CH1_LTCH register). Od = No IN1P over voltage fault detected 1d = IN1P over voltage fault has detected Channel 2 IN2P over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-47d, CH2_LTCH register). Od = No IN2P over voltage fault detected	0x00	00000000 Setting
7	00000000 default 0	Default Value: Definition Channel 1 IN1P over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-46d, CH1_LTCH register). 0d = No IN1P over voltage fault detected 1d = IN1P over voltage fault has detected Channel 2 IN2P over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-47d, CH2_LTCH register). 0d = No IN2P over voltage fault detected 1d = IN2P over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-48d, CH3_LTCH register). Channel 3 IN3P over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-48d, CH3_LTCH register). Od = No IN3P over voltage fault detected	0x00	00000000 Setting 0
6	00000000 default 0	Definition Channel 1 IN1P over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-46d, CH1_LTCH register). 0d = No IN1P over voltage fault detected 1d = IN1P over voltage fault has detected Channel 2 IN2P over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-47d, CH2_LTCH register). 0d = No IN2P over voltage fault detected 1d = IN2P over voltage fault detected Channel 3 IN3P over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-48d, CH3_LTCH register).	0x00	00000000 Setting 0
6	00000000 default 0	Definition Channel 1 IN1P over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-46d, CH1_LTCH register). 0d = No IN1P over voltage fault detected 1d = IN1P over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-47d, CH2_LTCH register). 0d = No IN2P over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-47d, CH2_LTCH register). 0d = No IN2P over voltage fault detected 1d = IN2P over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-48d, CH3_LTCH register). 0d = No IN3P over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-48d, CH3_LTCH register). 0d = No IN3P over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-49d, CH4_LTCH register). 0d = No IN4P over voltage fault detected	0x00	00000000 Setting 0 0
7 6 5	00000000 default 0 0	Definition Channel 1 IN1P over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-46d, CH1_LTCH register). Od = No IN1P over voltage fault detected 1d = IN1P over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-47, CH2_LTCH register). Od = No IN2P over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-47, CH2_LTCH register). Od = No IN2P over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-48d, CH3_LTCH register). Od = No IN3P over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-48d, CH3_LTCH register). Od = No IN3P over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-49d, CH4_LTCH register). Od = No IN4P over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-49d, CH4_LTCH register). Channel 5 IN5P over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-50d, CH5_LTCH register). Applicable only for PCM6x60-Q1. Od = No IN6P over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-51d, CH6_LTCH register). Applicable only for PCM6x60-Q1. Channel 6 IN6P over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-51d, CH6_LTCH register). Applicable only for PCM6x60-Q1. Od = No IN6P over voltage fault detected Channel 6 IN6P over voltage fault detected Od = No IN6P over voltage fault detected Channel 6 IN6P over voltage fault detected	0x00	00000000 Setting 0 0 0 0 0
7 6 5 4	00000000 default 0	Definition Channel 1 IN1P over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-46d, CH1_LTCH register). Od = No IN1P over voltage fault detected 1d = IN1P over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-47, CH2_LTCH register). Od = No IN2P over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-47, CH2_LTCH register). Od = No IN2P over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-48d, CH3_LTCH register). Od = No IN3P over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-48d, CH3_LTCH register). Od = No IN3P over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-49d, CH4_LTCH register). Od = No IN4P over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-49d, CH4_LTCH register). Channel 5 IN5P over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-50d, CH5_LTCH register). Applicable only for PCM6x60-Q1. Od = No IN6P over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-51d, CH6_LTCH register). Applicable only for PCM6x60-Q1. Channel 6 IN6P over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-51d, CH6_LTCH register). Applicable only for PCM6x60-Q1. Od = No IN6P over voltage fault detected Channel 6 IN6P over voltage fault detected Od = No IN6P over voltage fault detected Channel 6 IN6P over voltage fault detected	0x00	00000000 Setting 0 0 0 0
7 6 5 4 3	00000000 default	Definition Channel 1 IN1P over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-46d, CH1_LTCH register). d = No IN1P over voltage fault detected 1d = IN1P over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-47d, CH2_LTCH register). d = No IN2P over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-47d, CH2_LTCH register). d = No IN2P over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-48d, CH3_LTCH register). d = No IN3P over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-48d, CH3_LTCH register). d = No IN3P over voltage fault detected 1d = IN3P over voltage fault detected 1d = IN3P over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-49d, CH4_LTCH register). d = No IN4P over voltage fault detected 1d = IN4P over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-50d, CH5_LTCH register). Applicable only for PCM6x60-Q1. d = No IN5P over voltage fault detected 1d = IN5P over voltage fault detected 1d = IN5P over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-51d, CH6_LTCH register). Applicable only for PCM6x60-Q1. Ohen 10 IN6P over voltage fault detected 1d = IN6P over voltage fault detected 1d = IN6P over voltage fault detected 1d = IN6P over voltage fault has detected 1d = IN6P over voltage fault has detected 1d = IN6P over voltage fault has detected 1d = IN6P over voltage fault detected 1d = IN6P over voltage fault detected 1d = IN6P over voltage fault has detected 1d = IN6P over voltage fault has detected 1d = IN6P over voltage fault detected 1d = I	Ox00 Description	00000000 Setting 0 0 0 0 0 0
7 6 5 4 3	00000000 default	Definition Channel 1 IN1P over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-46d, CH1_LTCH register). 0d = No IN1P over voltage fault detected 1d = IN1P over voltage fault has detected Channel 2 IN2P over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-47d, CH2_LTCH register). 0d = No IN2P over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-48d, CH3_LTCH register). 0d = No IN3P over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-48d, CH3_LTCH register). 0d = No IN3P over voltage fault detected 1d = IN3P over voltage fault detected 1d = IN3P over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-49d, CH4_LTCH register). 0d = No IN4P over voltage fault detected 1d = IN4P over voltage fault detected 1d = IN4P over voltage fault has detected Channel 5 IN5P over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-50d, CH5_LTCH register). Applicable only for PCM6x60-Q1. 0d = No IN5P over voltage fault detected 1d = IN5P over voltage fault has detected 1d = IN5P over voltage fault has detected 1d = IN5P over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-51d, CH6_LTCH register). Applicable only for PCM6x60-Q1. 0d = No IN6P over voltage fault detected 1d = IN6P over voltage fault has detected 1d = IN6P over voltage fault detected 1d = IN6P over voltage fault has detected 1d = IN6P over voltage fault has detected 1d = IN6P over voltage fault detected 1d = IN6P over voltage fault detected 1d = I	0x00 Description	00000000 Setting 0 0 0 0 0 0 0 0
7 6 5 4 3	00000000 default	Definition Channel 1 IN1P over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-46d, CH1_LTCH register). Od = No IN1P over voltage fault detected 1d = IN1P over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-47d, CH2_LTCH register). Od = No IN2P over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-47d, CH2_LTCH register). Od = No IN2P over voltage fault detected 1d = IN2P over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-48d, CH3_LTCH register). Od = No IN3P over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-48d, CH3_LTCH register). Od = No IN3P over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-49d, CH4_LTCH register). Od = No IN4P over voltage fault detected 1d = IN4P over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-50d, CH5_LTCH register). Applicable only for PCM6x60-Q1. Od = No IN5P over voltage fault detected 1d = IN5P over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-51d, CH6_LTCH register). Applicable only for PCM6x60-Q1. Od = No IN6P over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-51d, CH6_LTCH register). Applicable only for PCM6x60-Q1. Od = No IN6P over voltage fault detected Reserved	0x36	00000000 Setting 0 0 0 0 0 0 0 0 0 0 0 0 0
7 6 5 4 3	00000000 default	Definition Channel 1 IN1P over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-46d, CH1_LTCH register). Old = No IN1P over voltage fault detected Id = IN1P over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-47d, CH2_LTCH register). Channel 2 IN2P over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-47d, CH2_LTCH register). Channel 3 IN3P over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-48d, CH3_LTCH register). Channel 3 IN3P over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-48d, CH3_LTCH register). Channel 4 IN4P over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-49d, CH4_LTCH register). Od = No IN4P over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-50d, CH5_LTCH register). Applicable only for Pokok60-Q1. Od = No IN6P over voltage fault detected Channel 6 IN6P over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-50d, CH5_LTCH register). Applicable only for PCM6x60-Q1. Od = No IN6P over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-51d, CH6_LTCH register). Applicable only for PCM6x60-Q1. Od = No IN6P over voltage fault detected Channel 6 IN6P over voltage fault detected Id = IN6P over voltage fault has detected Reserved	0x36 0x00	00000000 Setting 0 0 0 0 0 0 0 0 0 0 0 0 0
7 6 5 4 3 2 1 0 bit	00000000 default	Definition Channel 1 IN1P over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-46d, CH1_LTCH register). Old = No IN1P over voltage fault detected Id = IN1P over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-47d, CH2_LTCH register). Channel 2 IN2P over voltage fault status (self-clearing bit - This bit gets clear on real/2p over voltage fault status (self-clearing bit - This bit gets clear on real/2p over voltage fault status (self-clearing bit - This bit gets clear on real/2p over voltage fault status (self-clearing bit - This bit gets clear on real/2p over voltage fault status (self-clearing bit - This bit gets clear on real/2p over voltage fault status (self-clearing bit - This bit gets clear on real/2p over voltage fault status (self-clearing bit - This bit gets clear on real/2p over voltage fault status (self-clearing bit - This bit gets clear on real/2p over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-50d, CH5_LTCH register). Applicable only for Power voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-50d, CH5_LTCH register). Applicable only for Power voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-51d, CH6_LTCH register). Applicable only for PCM6x60-Q1. Od = No IN6P over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-51d, CH6_LTCH register). Applicable only for PCM6x60-Q1. Od = No IN6P over voltage fault detected Reserved Address: Definition Channel 1 IN1M over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-46d, CH1_LTCH register).	0x36 0x00	00000000 Setting 0 0 0 0 0 0 0 0 0 0 0 0 0

5	0	Channel 3 IN3M over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-48d, CH3_LTCH register). 0d = No IN3M over voltage fault detected		0
		1d = IN3M over voltage fault has detected Channel 4 IN4M over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-49d, CH4_LTCH register).		
4	0	0d = No IN4M over voltage fault detected 1d = IN4M over voltage fault has detected		0
3	0	Channel 5 IN5M over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-50d, CH5_LTCH register). Applicable only for PCM6x60-Q1. Od = No IN5M over voltage fault detected 1d = IN5M over voltage fault has detected		0
		Channel 6 IN6M over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-51d, CH6_LTCH register). Applicable only		
2	0	for PCM6x60-Q1. 0d = No IN6M over voltage fault detected 1d = IN6M over voltage fault has detected		0
0	0	Reserved		0
	00110111	Address :	0x37	0x00
	00000000	Default Value:		00000000
bit	default	Definition	Description	Setting
7	0	Fault status for MICBIAS high current (self-clearing bit). 0d = No fault detected 1d = Fault detected		0
6	0	Fault status for MICBIAS low current (self-clearing bit) 0d = No fault detected 1d = Fault detected		0
5	0	Fault status for MICBIAS over voltage (self-clearing bit). 0d = No fault detected 1d = Fault detected		0
4	0			0
3	0	Reserved		0
1	0	Nesel ved		0
0	0			0
	00111000	Address :	0x38	0xBA
	10111010	Default Value :	0xBA	10111010
	default	Definition	Description	Setting
7	1	THE RELIGIOUS AND		1
6	0	Threshold for MICBIAS high load current fault diagnostic. Od to 56d = Reserved		0
5	1	57d = High load current threshold is set as 0 mA (typ)		1
4	1	58d = High load current threshold is set as 0.54 mA (typ) 59d = High load current threshold is set as 1.08 mA (typ)	POC used as default	1
3	1		POC used as delault	1
2	0	187d to 241d = High load current threshold is set as per configuration		0
1	1	242d = High load current threshold is set as 99.90 mA (typ) 243d to 255d = Reserved		1
0	0			0
	00111001	Address :	0x39	0x4B
	01001011	Default Value :		01001011
bit	default	Definition	Description	Setting
7	0	Threshold for MICBIAS low load current fault diagnostic.		0
6		0d to 56d = Reserved		1
5		57d = Low load current threshold is set as 0 mA (typ) 58d = Low load current threshold is set as 0.54 mA (typ)		0
4	. 0	59d = Low load current threshold is set as 1.08 mA (typ) 60d to 74d = Low load current threshold is set as per configuration	POC used as default	0
3		75d = Low load current threshold is set as 9.72 mA (typ)		0
1	1	76d to 241d = Low load current threshold is set as per configuration 242d = Low load current threshold is set as 99.90 mA (typ)		1
0	1	243d to 255d = Reserved		1
	00111010	Address :		0x00
	00010000	Default Value :	0x10	00000000
bit	default	Definition Development configuration of MICRIAS foult 1	Description	Setting
7	0	Powerdown configuration of MICBIAS fault 1 0d = No powerdown when MICBIAS fault detected 1d = MICBIAS and all ADC channels gets powerdown when low current fault occurs and PO_R40, PD_ON_FLT_CFG = 1d 1d = MICBIAS and all ADC channels gets powerdown when high current fault occurs and PO_R40, PD_ON_FLT_CFG = 2d	MICBIAS故障时不断电 PD_ON_FLT_CFG=0d	0
6	0	Powerdown configuration of MICBIAS fault 2 0d = No powerdown when MICBIAS fault detected 1d = MICBIAS and all ADC channels gets powerdown when over voltage fault occurs and PO_R40, PD_ON_FLT_CFG = 1d 1d = MICBIAS and all ADC channels gets powerdown when low current fault occurs and PO_R40, PD_ON_FLT_CFG = 2d	MICBIAS故障时不断电	0
5	0	Powerdown configuration of MICBIAS fault 3 Od = No powerdown when MICBIAS fault detected 1d = MICBIAS and all ADC channels gets powerdown when over temperature fault occurs and PQ_R40, PD_ON_FLT_CFG = 1d 1d = MICBIAS and all ADC channels gets powerdown when over voltage fault occurs and PQ_R40, PD_ON_FLT_CFG = 2d	MICBIAS故障时不断电	0

4		Powerdown configuration of MICBIAS fault 4 0d = No powerdown when MICBIAS fault detected 1d = MICBIAS and all ADC channels gets powerdown when high current fault occurs and PO_R40, PD_ON_FLT_CFG = 1d 1d = MICBIAS and all ADC channels gets powerdown when over temperature fault occurs and PO_R40, PD_ON_FLT_CFG = 2d. It is recommended to use this setting to protect chip from over temperature fault.	MICBIAS故障时不断电		0
3	0	Reserved			0
1 0	0 0	Reserved			0 0 0
	I			1	
	00111011	Address :			0xF0
	11010000	Default Value :			11110000
bit	default	Definition	Description		Setting
				1	

	00111011	Address :	0x3B
	11010000	Default Value :	0xD0
bit	default	Definition	Description
7	1	MICBIAS value. 0d = Reserved 1d = Reserved 2d = Reserved 3d = Reserved	
6	1	4d = Reserved 5d = Reserved 6d = Reserved 7d = Microphone bias is set to 5 V	ICC选定MIC模组供电电压7.2V~8V~8.8V
5	0	8d = Microphone bias is set to 5.5 V 9d = Microphone bias is set to 6 V 10d = Microphone bias is set to 6.5 V 11d = Microphone bias is set to 7 V 12d = Microphone bias is set to 7.5 V	考虑线束最长6m,将偏置电压选择9V
4	1	13d = Microphone bias is set to 8 V 14d = Microphone bias is set to 8.5 V 15d = Microphone bias is set to 9 V	
3	0	Reserved	
1 0	0	Reserved	

	00111100	Address :	0x3C	0x38
	00010000	Default Value :	0x10	00111000
bit	default	Definition	Description	Setting
7	0	Channel 1 input type. Od = Microphone input 1d = Line input	Microphone输入	0
6	0	Channel 1 input configuration. 0d = Analog differential input 1d = Analog single-ended input	单端输入	0
5	0	2d = Reserved 3d = Reserved	1 - 10 10/2	1
4	1	Channel 1 input coupling. 0d = AC-coupled input 1d = DC-coupled input	DC耦合	1
3	0	Channel 1 microphone input range. Od = Low swing mode; Differential input AC signal full-scale of 2-VRMS supported provided DC differential common mode voltage IN1P - IN1M < 4.2 V. Single-ended AC signal 1-VRMS supported provided DC common mode voltage is < 2.1 V. Id = High swing mode; Differential Input IN1P-IN1M peak voltage up to 14.14 V or single ended 7.07 V supported. User rquired to adjust the channel gain and digital volume control based on the max signal level used in system.	入力范围大模式	1
2	0	Channel 1 CMRR Configuration. Od = High SNR performance mode 1d = Reserved	Default	0
1	0	2d = High CMRR performance mode 3d = Reserved	Dorduit	0
0	0	Channel 1 automatic gain controller (AGC) setting. Od = AGC disabled 1d = AGC enabled based on the configuration of bit 3 in register 108 (PO_R108); This must be used only with AC-coupled input	自动增益调节关闭	0

	00111101	Address	0.20
		Address :	
	00000000	Default Value :	0x00
bit	default	Definition	Description
7	0	Channel 4 asia	
6	0	Channel 1 gain. 0d = Channel gain is set to 0 dB	
5	n	1d = Channel gain is set to 1 dB 2d = Channel gain is set to 2 dB	串扰、采样值问题对策: 8dB, 后续根据需要调整
4	0	3d to 41d = Channel gain is set as per configuration	中ル、不什直內處对來。000,但來似如而安例正
3	0	42d = Channel gain is set to 42 dB 43d to 63d = Reserved	
2	0	100 10 000 110001 100	
1	0	Reserved	
0	0	Reserved	

	00111110	Address :	0x3E
	11001001	Default Value :	0xC9
bit	default	Definition	Description
7	1		

0xDB
11011011
Setting
1

0 0 0

6 5 4 3 2 1	0 1 0	Description Description	串扰、采样值问题对策: 9dB, 后续根据需要调整	1 0 1 1 0 1
	00111111	Address :	0x3F	0x80
	10000000	Default Value :	0x80	10000000
bit	default	Definition	Description	Setting
6	0	Channel 1 gain calibration. Od = Gain calibration is set to -0.8 dB 1d = Gain calibration is set to -0.7 dB 2d = Gain calibration is set to -0.6 dB 3d to 7d = Gain calibration is set as per configuration 8d = Gain calibration is set to 0 dB	Used as default first,后续根据需要调整	0
4		9d = Gain calibration is set to 0.1 dB 10d to 13d = Gain calibration is set as per configuration 14d = Gain calibration is set to 0.6 dB 15d = Gain calibration is set to 0.7 dB		0 0
2 1 0	0 0	Reserved		0 0
	01000000	Address :	0x40	0x00
	00000000	Default Value :	0x00	00000000
bit	default	Definition	Description	Setting
7 6 5 4 3 2 1	0	Channel 1 phase calibration with modulator clock resolution. Od = No phase calibration Id = Phase calibration delay is set to one cycle of the modulator clock 2d = Phase calibration delay is set to two cycles of the modulator clock 3d to 254d = Phase calibration delay as per configuration 255d = Phase calibration delay is set to 255 cycles of the modulator clock	Used as default first,后续根据需要调整	0 0 0 0 0
	01000001	I Address	0.41	020
	01000001	Address : Default Value		0x38 00111000
bit	01000001 00010000 default	Address : Default Value : Definition	0x41 0x10 Description	0x38 00111000 Setting
bit 7	00010000 default	Default Value : Definition Channel 2 input type. Od = Microphone input 1d = Line input	0x10	00111000
	00010000 default 0	Definition Channel 2 input type. 0d = Microphone input 1d = Line input Channel 2 input configuration. 0d = Analog differential input 1d = Analog single-ended input 2d = Reserved.	0x10 Description	00111000 Setting
7	00010000 default 0	Default Value : Definition Channel 2 input type. Od = Microphone input 1d = Line input Channel 2 input configuration. Od = Analog differential input 1d = Analog single-ended input 2d = Reserved 3d = Reserved Channel 2 input coupling.	0x10 Description Microphone輸入	00111000 Setting 0
7 6 5	00010000 default 0 0	Definition Channel 2 input type. 0d = Microphone input 1d = Line input Channel 2 input configuration. 0d = Analog differential input 1d = Analog single-ended input 2d = Reserved 3d = Reserved Channel 2 input coupling. 0d = AC-coupled input	0x10 Description Microphone輸入 単端輸入	00111000 Setting 0 0 1
7 6 5	00010000 default 0 0	Definition Channel 2 input type. Od = Microphone input dd = Line input Channel 2 input configuration. Od = Analog differential input Id = Line insigle-ended input 2d = Reserved 3d = Reserved Channel 2 input coupling. Od = AC-coupled input Id = DC-coupled input Channel 2 microphone input range. Od = Low swing mode; Differential input AC signal full-scale of 2-VRMS supported provided DC differential common mode voltage INIP - INIM < 4.2 V. Single-ended AC signal 1-VRMS supported provided DC common mode voltage is < 2.1 V. Id = High swing mode; Differential input INIP-INIM peak voltage up to 14.14 V or single ended 7.07 V supported. User rquired to adjust the channel gain and digital volume control based on the max signal level used in system. Channel 2 CMRR Configuration. Od = High SNR performance mode Id = Reserved	0x10 Description Microphone輸入 単端輸入 DC耦合	00111000 Setting 0 0 1
7 6 5 4	00010000 default 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Definition Channel 2 input type. Od = Microphone input 1d = Line input Channel 2 input configuration. Od = Analog differential input 1d = Analog single-ended input 2d = Reserved 3d = Reserved Channel 2 input coupling. Od = AC-coupled input 1d = DC-coupled input 1d = DC-coupled input Channel 2 mode; Differential input AC signal full-scale of 2-VRMS supported provided DC differential common mode voltage IN1P - IN1M < 4.2 V. Single-ended AC signal 1-VRMS supported provided DC common mode voltage is < 2.1 V. 1d = High swing mode; Differential Input IN1P-IN1M peak voltage up to 14.14 V or single ended 7.07 V supported. User rquired to adjust the channel gain and digital volume control based on the max signal level used in system. Channel 2 CMRR Configuration. Od = High SNR performance mode 1d = Reserved 2d = High CMRR performance mode 3d = Reserved	0x10 Description Microphone輸入 単端輸入 DC耦合 入力范围大模式	00111000 Setting 0 0 1 1
7 6 5 4 4	00010000 default	Default Value: Definition Channel 2 input type. Od = Microphone input 1d = Line input Channel 2 input configuration. Od = Analog differential input 1d = Analog single-ended input 2d = Reserved 3d = Reserved Channel 2 input coupling. Od = AC-coupled input 1d = DC-coupled input 1d = DC-coupled input 1d = DC-coupled input Channel 2 mode; Differential input AC signal full-scale of 2-VRMS supported provided DC differential common mode voltage INIP - INIM < 4.2 V. Single-ended AC signal 1-VRMS supported provided DC common mode voltage is < 2.1 V. 1d = High swing mode; Differential Input INIP-INIM peak voltage up to 14.14 V or single ended 7.07 V supported. User rquired to adjust the channel gain and digital volume control based on the max signal level used in system. Channel 2 CMRR Configuration. Od = High SNR performance mode 1d = Reserved Channel 2 automatic gain controller (AGC) setting.	0x10 Description Microphone輸入 単端輸入 DC耦合 入力范围大模式	00111000 Setting 0 1 1 0
7 6 5 4	00010000 default	Default Value: Definition Channel 2 input type. Od = Microphone input 1d = Line input Channel 2 input configuration. Od = Analog differential input 1d = Analog single-ended input 2d = Reserved 3d = Reserved Channel 2 input coupling. Od = AC-coupled input 1d = DC-coupled input 1d = DC-coupled input Channel 2 of Line input coupling. Od = Low swing mode; Differential input AC signal full-scale of 2-VRMS supported provided DC differential common mode voltage IN1P - IN1M < 4.2 V. Single-ended AC signal 1-VRMS supported provided DC common mode voltage is < 2.1 V. 1d = High swing mode; Differential Input IN1P-IN1M peak voltage up to 14.14 V or single ended 7.07 V supported. User rquired to adjust the channel gain and digital volume control based on the max signal level used in system. Channel 2 CMRR Configuration. Od = High SNR performance mode 1d = Reserved Channel 2 automatic gain controller (AGC) setting. Od = AGC disabled 1d = AGC enabled based on the configuration of bit 3 in register 108	Ox10 Description Microphone輸入 単端輸入 DC耦合 入力范围大模式 Default	00111000 Setting 0 0 1 1 0 0 0 0
7 6 5 4	00010000 default	Definition Channel 2 input type. Od = Microphone input 1d = Line input Channel 2 input configuration. Od = Analog differential input 1d = Analog single-ended input 2d = Reserved 3d = Reserved 3d = Reserved Channel 2 input coupling. Od = AC-coupled input 1d = DC-coupled input 1d = DC-coupled input Channel 2 microphone input range. Od = Low swing mode; Differential input AC signal full-scale of 2-VRMS supported provided DC differential common mode voltage IN1P - IN1M < 4.2 V. Single-ended AC signal 1-VRMS supported provided DC common mode voltage is < 2.1 V. 1d = High swing mode; Differential Input IN1P-IN1M peak voltage up to 14.14 V or single ended 7.07 V supported. User rquired to adjust the channel gain and digital volume control based on the max signal level used in system. Channel 2 CMRR Configuration. Od = High SNR performance mode 1d = Reserved 2d = High CMRR performance mode 3d = Reserved Channel 2 automatic gain controller (AGC) setting. Od = AGC disabled 1d = AGC enabled based on the configuration of bit 3 in register 108 (PD_R108); This must be used only with AC-coupled input	0x10 Description Microphone輸入 単端輸入 DC耦合 入力范围大模式 Default 自动増益调节关闭 0x42 0x00 0x00	00111000 Setting 0 0 1 1 1 0 0 0
7 6 5 4 4 3 3 4 5 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	0010000 default	Definition Channel 2 input type. 0d = Microphone input 1d = Line input Channel 2 input configuration. 0d = Analog differential input 1d = Analog single-ended input 2d = Reserved 3d = Reserved 3d = Reserved Channel 2 input coupling. 0d = AC-coupled input 1d = DC-coupled input 1d = Low swing mode; Differential input AC signal full-scale of 2-VRMS supported provided DC differential common mode voltage IN1P - IN1M < 4.2 V. Single-ended AC signal 1-VRMS supported provided DC common mode voltage is < 2.1 V. 1d = High swing mode; Differential Input IN1P-IN1M peak voltage up to 14.14 V or single ended 7.07 V supported. User rquired to adjust the channel gain and digital volume control based on the max signal level used in system. Channel 2 CMRR Configuration. 0d = High SNR performance mode 1d = Reserved 2d = High CMRR performance mode 3d = Reserved Channel 2 automatic gain controller (AGC) setting. 0d = AGC disabled 1d = AGC enabled based on the configuration of bit 3 in register 108 (PO_R108); This must be used only with AC-coupled input Address: Default Value:	0x10 Description Microphone輸入 単端輸入 DC耦合 入力范围大模式 Default 自动増益调节关闭 0x42	00111000 Setting 0 0 1 1 1 0 0 0 0 0 0 0 0 0 0 Setting
7 6 5 4 4 3 3 5 1 1 0 0 bit 7	0010000 default	Definition Channel 2 input type. Od = Microphone input 1d = Line input Channel 2 input configuration. Od = Analog differential input 1d = Analog single-ended input 2d = Reserved 3d = Reserved Channel 2 input coupling. Od = AC-coupled input 1d = DC-coupled input 1d = DC-coupled input Channel 2 mode; Differential input AC signal full-scale of 2-VRMS supported provided DC differential common mode voltage IN1P - IN1M < 4.2 V. Single-ended AC signal 1-VRMS supported provided DC common mode voltage is < 2.1 V. 1d = High swing mode; Differential Input IN1P-IN1M peak voltage up to 14.14 V or single ended 7.07 V supported. User rquired to adjust the channel gain and digital volume control based on the max signal level used in system. Channel 2 CMRR Configuration. Od = High SNR performance mode 1d = Reserved Channel 2 automatic gain controller (AGC) setting. Od = AGC disabled 1d = AGC enabled based on the configuration of bit 3 in register 108 (PO_R108); This must be used only with AC-coupled input Address: Default Value: Definition	0x10 Description Microphone輸入 単端輸入 DC耦合 入力范围大模式 Default 自动増益调节关闭 0x42 0x00 0x00	00111000 Setting 0 0 1 1 1 0 0 0 0 0 0 0 0 0 Setting 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
7 6 5 4 3 3 2 1 1 0 bit 7 6 6	00010000 default	Definition Channel 2 input type. Od = Microphone input Id = Line input Channel 2 input configuration. Od = Analog differential input Id = Analog single-ended input 2d = Reserved 3d = Reserved Channel 2 input coupling. Od = AC-coupled input Id = Dr. coupled input Channel 2 microphone input range. Od = Low swing mode; Differential input AC signal full-scale of 2-VRMS supported provided DC differential common mode voltage INIP - INIM < 4.2 V. Single-ended AC signal 1-VRMS supported provided DC common mode voltage is < 2.1 V. Id = High swing mode; Differential Input INIP-INIM peak voltage up to 14.14 V or single ended 7.07 V supported. User rquired to adjust the channel gain and digital volume control based on the max signal level used in system. Channel 2 CMRR Configuration. Od = High SNR performance mode 1d = Reserved 2d = High CMRR performance mode 3d = Reserved Channel 2 automatic gain controller (AGC) setting. Od = AGC disabled 1d = AGC enabled based on the configuration of bit 3 in register 108 (PO_R108); This must be used only with AC-coupled input Address: Default Value: Definition	0x10 Description Microphone輸入 単端輸入 DC耦合 入力范围大模式 Default 自动増益调节关闭 0x42 0x00 0x00	00111000 Setting 0 1 1 1 0 0 0 0 0 0 0 0 0
7 6 5 4 4 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5	0010000 default	Definition Channel 2 input type. Od = Microphone input Id = Line input Channel 2 input configuration. Od = Analog differential input Id = Analog single-ended input 2d = Reserved 3d = Reserved Channel 2 input coupling. Od = AC-coupled input Id = DC-coupled input Channel 2 input coupling. Od = AC-coupled input Channel 2 more input range. Od = Low swing mode; Differential input AC signal full-scale of 2-VRMS supported provided DC differential common mode voltage INIP - INIM < 4.2 V. Single-ended AC signal 1-VRMS supported provided DC common mode voltage is < 2.1 V. Id = High swing mode; Differential Input INIP-INIM peak voltage up to 14.14 V or single ended 7.07 V supported. User rquired to adjust the channel gain and digital volume control based on the max signal level used in system. Channel 2 CMRR Configuration. Od = High SNR performance mode 1d = Reserved 2d = High CMRR performance mode 3d = Reserved Channel 2 automatic gain controller (AGC) setting. Od = AGC disabled 1d = AGC enabled based on the configuration of bit 3 in register 108 (PO_R108); This must be used only with AC-coupled input Address: Default Value: Definition Channel 2 gain. Od = Channel gain is set to 0 dB 1d = Channel gain is set to 1 dB	0x10 Description Microphone輸入 単端輸入 DC耦合 入力范围大模式 Default 自动増益调节关闭 0x42 0x00 0x00	00111000 Setting 0 1 1 1 0 0 0 0 0 1 1 1 1
7 6 5 4 4 5 5 5 4 4 5 5 5 4 4 5 5 5 5 5 5	0010000 default	Definition Channel 2 input type. Od = Microphone input Id = Line input Channel 2 input configuration. Od = Analog differential input Id = Analog single-ended input Id = Reserved Channel 2 input coupling. Od = AC-coupled input Channel 2 provential input and a common mode voltage input Channel 2 mode; Differential input AC signal full-scale of 2-VRMS supported provided DC differential common mode voltage in INIP - INIM < 4.2 V. Single-ended AC signal 1-VRMS supported provided DC common mode voltage is < 2.1 V. Id = High swing mode; Differential input INIP-INIM peak voltage up to 14.14 V or single ended 7.07 V supported. User rquired to adjust the channel gain and digital volume control based on the max signal level used in system. Channel 2 CMRR Configuration. Od = High SNR performance mode Id = Reserved Channel 2 automatic gain controller (AGC) setting. Od = AGC disabled Id = AGC enabled based on the configuration of bit 3 in register 108 (PO_R108); This must be used only with AC-coupled input Address: Default Value: Definition Channel 2 gain. Od = Channel gain is set to 1 dB Id = Channel gain is set to 1 dB Id = Channel gain is set to 2 dB Id = Channel gain is set to 2 dB Id = Channel gain is set to 2 dB Id = Channel gain is set to 2 dB	0x10 Description Microphone輸入 単端輸入 DC耦合 入力范围大模式 Default 自动增益调节关闭 0x42 0x00 Description	00111000 Setting 0 1 1 1 0 0 0 0 0 1 1 1 0 0
7 6 5 4 4 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5	0010000 default	Definition Channel 2 input type. Od = Microphone input Id = Line input Channel 2 input configuration. Od = Analog differential input Ld = Analog single-ended input 2d = Reserved 3d = Reserved Channel 2 input coupling. Od = AC-coupled input Ld = Dr. coupled input Ld = Dr. coupled input Channel 2 input coupling. Od = AC-coupled input Channel 2 more input range. Od = Low swing mode; Differential input AC signal full-scale of 2-VRMS supported provided DC differential common mode voltage INIP - INIM < 4.2 V. Single-ended AC signal 1-VRMS supported provided DC common mode voltage is < 2.1 V. Id = High swing mode; Differential input INIP-INIM peak voltage up to 14.14 V or single ended 7.07 V supported. User rquired to adjust the channel gain and digital volume control based on the max signal level used in system. Channel 2 CMRR Configuration. Od = High SNR performance mode Id = Reserved Channel 2 automatic gain controller (AGC) setting. Od = AGC disabled Id = AGC enabled based on the configuration of bit 3 in register 108 (PO_R108); This must be used only with AC-coupled input Address: Default Value: Definition Channel 2 gain. Od = Channel gain is set to 1 dB Id = Channel gain is set to 2 dB Id = Channel gain is set to 2 dB Id = Channel gain is set to 42 dB	0x10 Description Microphone輸入 単端輸入 DC耦合 入力范围大模式 Default 自动增益调节关闭 0x42 0x00 Description	00111000 Setting 0 1 1 1 0 0 0 0 0 1 1 1 1

0 Reserved 0 Reserved

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	01000011	Address :	0x43	0xDB
o.i+	11001001	Default Value :	0xC9	11011011
oit _	default	Definition	Description	Setting
7	1	Channel 2 digital volume control.		1
6	1	Od = Digital volume is muted		1
5		1d = Digital volume control is set to -100 dB		0
		2d = Digital volume control is set to -99.5 dB		
4		3d to 200d = Digital volume control is set as per configuration	串扰、采样值问题对策: 9dB, 后续根据需要调整	1
3	1	201d = Digital volume control is set to 0 dB 202d = Digital volume control is set to 0.5 dB	The state of the s	1
2	0	203d to 253d = Digital volume control is set to 0.5 db		0
		254d = Digital values control is set to 26 5 dB		
1		255d = Digital volume control is set to 27 dB		1
0	1			1
	01000100	Address :		0x80
	10000000	Default Value :	0x80	10000000
oit	default	Definition	Description	Setting
-	l ,			
7	1	Channel 2 gain calibration.		1
		0d = Gain calibration is set to -0.8 dB 1d = Gain calibration is set to -0.7 dB		-
6	0	2d = Gain calibration is set to -0.7 db		0
J		3d to 7d = Gain calibration is set as per configuration	Used as default first 一戶体担提爾爾和斯	
		8d = Gain calibration is set to 0 dB	Used as default first,后续根据需要调整	
5	0	9d = Gain calibration is set to 0.1 dB		0
	1	10d to 13d = Gain calibration is set as per configuration 14d = Gain calibration is set to 0.6 dB		
4	_	15d = Gain calibration is set to 0.6 dB		0
4	l "			Ι ΄
3	0			0
2				0
1	0	reserved		0
0	0			0
	01000101	Address :		0x00
	00000000	Default Value :	0x00	00000000
oit	default	Definition	Description	Setting
7	0			0
6	0	Channel 2 phase calibration with modulator clock resolution.		0
5	U	Jud = No phase calibration		0
4		1d = Phase calibration delay is set to one cycle of the modulator clock	Used as default first,后续根据需要调整	0
3		2d = Phase calibration delay is set to two cycles of the modulator clock 3d to 254d = Phase calibration delay as per configuration		0
2	0	255d = Phase calibration delay is set to 255 cycles of the modulator clock		0
0		2004 Made dampfatton adia, is det to 200 system of the mediator dreak		0
- 0		1		
				0
	01000110		0x46	
	01000110	Address : Default Value :	0x46 0x10	0 0x38 00111000
oit		Address :		0x38
oit	00010000	Address : Default Value :	0x10	0x38 00111000
oit 7	00010000 default	Address : Default Value :	0x10	0x38 00111000
oit 7	00010000 default	Address: Default Value: Definition Channel 3 input type.	0x10 Description	0x38 00111000 Setting
7	00010000 default	Address: Default Value: Definition Channel 3 input type. 0d = Microphone input 1d = Line input	0x10 Description	0x38 00111000 Setting
	00010000 default	Address: Default Value: Definition Channel 3 input type. 0d = Microphone input 1d = Line input Channel 3 input configuration.	0x10 Description	0x38 00111000 Setting
7	00010000 default	Address: Default Value: Definition Channel 3 input type. 0d = Microphone input 1d = Line input Channel 3 input configuration. 0d = Analog differential input	0x10 Description Microphone輸入	0x38 00111000 Setting
7	00010000 default	Address: Default Value: Default Value: Channel 3 input type. Od = Microphone input 1d = Line input Channel 3 input configuration. Od = Analog differential input 1d = Analog single-ended input 2d = Reserved.	0x10 Description	0x38 00111000 Setting 0
7	00010000 default	Address: Definition Channel 3 input type. 0d = Microphone input 1d = Line input Channel 3 input configuration. 0d = Analog differential input 1d = Analog single-ended input	0x10 Description Microphone輸入	0x38 00111000 Setting
7	00010000 default	Address: Default Value: Default Value: Channel 3 input type. 0d = Microphone input 1d = Line input Channel 3 input configuration. 0d = Analog differential input 1d = Analog single-ended input 2d = Reserved 3d = Reserved	0x10 Description Microphone輸入	0x38 00111000 Setting 0
7 6 5	00010000 default 0	Address: Default Value: Definition Channel 3 input type. Od = Microphone input 1d = Line input Channel 3 input configuration. Od = Analog differential input 1d = Analog single-ended input 2d = Reserved 3d = Reserved Channel 3 input coupling.	0x10 Description Microphone輸入 単端输入	0x38 00111000 Setting 0
7	00010000 default 0	Address: Default Value: Definition Channel 3 input type. Od = Microphone input 1d = Line input Channel 3 input configuration. Od = Analog differential input 1d = Analog single-ended input 2d = Reserved 3d = Reserved Channel 3 input coupling. Od = AC-coupled input	0x10 Description Microphone輸入	0x38 00111000 Setting 0
7 6 5	00010000 default 0	Address: Default Value: Definition Channel 3 input type. Od = Microphone input 1d = Line input Channel 3 input configuration. Od = Analog differential input 1d = Analog single-ended input 2d = Reserved 3d = Reserved Channel 3 input coupling. Od = AC-coupled input 1d = DC-coupled input	0x10 Description Microphone輸入 単端输入	0x38 00111000 Setting 0
7 6 5	00010000 default 0	Address: Default Value: Definition Channel 3 input type. 0d = Microphone input 1d = Line input Channel 3 input configuration. 0d = Analog differential input 1d = Analog single-ended input 2d = Reserved 3d = Reserved 3d = Reserved Channel 3 input coupling. 0d = AC-coupled input 1d = DC-coupled input 1d = DC-coupled input Channel 3 microphone input range.	0x10 Description Microphone輸入 単端输入	0x38 00111000 Setting 0
7 6 5	00010000 default 0	Address: Default Value: Default Value: Channel 3 input type. 0d = Microphone input 1d = Line input Channel 3 input configuration. 0d = Analog differential input 1d = Analog single-ended input 2d = Reserved 3d = Reserved Channel 3 input coupling. 0d = AC-coupled input 1d = DC-coupled input Channel 3 microphone input range. 0d = Low swing mode; Differential input AC signal full-scale of 2-VRMS	0x10 Description Microphone輸入 単端输入	0x38 00111000 Setting 0
7 6 5	00010000 default 0	Address: Default Value: Definition Channel 3 input type. Od = Microphone input 1d = Line input Channel 3 input configuration. Od = Analog differential input 1d = Analog single-ended input 2d = Reserved 3d = Reserved Channel 3 input coupling. Od = AC-coupled input 1d = DC-coupled input 1d = DC-coupled input Channel 3 microphone input range. Od = Low swing mode; Differential input AC signal full-scale of 2-VRMS supported provided DC differential common mode voltage INIP - INIM < 4.2	0x10 Description Microphone輸入 単端输入	0x38 0011100 Setting 0
7 6 5	00010000 default 0 0	Address: Default Value: Default Value: Default Value: Channel 3 input type. Od = Microphone input 1d = Line input Channel 3 input configuration. Od = Analog differential input 1d = Analog single-ended input 2d = Reserved 3d = Reserved 3d = Reserved Channel 3 input coupling. Od = AC-coupled input 1d = DC-coupled input Channel 3 microphone input range. Od = Low swing mode; Differential input AC signal full-scale of 2-VRMS supported provided DC differential common mode voltage INIP - INIM < 4.2 V. Single-ended AC signal 1-VRMS supported provided DC common mode	0x10 Description Microphone輸入 単端輸入 DC耦合	0x38 0011100 Setting 0
7 6 5	00010000 default 0 0	Address: Default Value: Definition Channel 3 input type. Od = Microphone input 1d = Line input Channel 3 input configuration. Od = Analog differential input 1d = Analog single-ended input 2d = Reserved 3d = Reserved Channel 3 input coupling. Od = AC-coupled input 1d = DC-coupled input 1d = DC-coupled input Channel 3 microphone input range. Od = Low swing mode; Differential input AC signal full-scale of 2-VRMS supported provided DC differential common mode voltage IN1P - IN1M < 4.2 V. Single-ended AC signal 1-VRMS supported provided DC common mode voltage is < 2.1 V. 1d = High swing mode; Differential Input IN1P-IN1M peak voltage up to	0x10 Description Microphone輸入 単端输入	0x38 0011100 Setting 0 0
7 6 5	00010000 default 0 0	Address: Default Value: Default Value: Default Value: Od = Microphone input Id = Line input Channel 3 input configuration. Od = Analog differential input Id = Analog single-ended input 2d = Reserved 3d = Reserved Channel 3 input coupling. Od = AC-coupled input Id = DC-coupled input Channel 3 microphone input range. Od = Low swing mode; Differential input AC signal full-scale of 2-VRMS supported provided DC differential common mode voltage INIP - INIM < 4.2 V. Single-ended AC signal 1-VRMS supported provided DC common mode voltage is < 2.1 V. Id = High swing mode; Differential Input INIP-INIM peak voltage up to 14.14 V or single ended 7.07 V supported. User rquired to adjust the	0x10 Description Microphone輸入 単端輸入 DC耦合	0x38 00111000 Setting 0 0
7 6 5	00010000 default 0 0	Address: Default Value: Default Value: Default Value: Channel 3 input type. Od = Microphone input 1d = Line input Channel 3 input configuration. Od = Analog differential input 1d = Analog single-ended input 2d = Reserved 3d = Reserved 3d = Reserved Channel 3 input coupling. Od = AC-coupled input 1d = DC-coupled input 1d = DC-coupled input Channel 3 microphone input range. Od = Low swing mode; Differential input AC signal full-scale of 2-VRMS supported provided DC differential common mode voltage INIP - INIM < 4.2 V. Single-ended AC signal 1-VRMS supported provided DC common mode voltage is < 2.1 V. 1d = High swing mode; Differential Input INIP-INIM peak voltage up to 14.14 V or single ended 7.07 V supported. User rquired to adjust the channel gain and digital volume control based on the max signal level used	0x10 Description Microphone輸入 単端輸入 DC耦合	0x38 00111000 Setting 0 0 1
7 6 5 4	00010000 default 0 0	Address: Default Value: Default Value: Default Value: Od = Microphone input Id = Line input Channel 3 input configuration. Od = Analog differential input Id = Analog single-ended input 2d = Reserved 3d = Reserved Channel 3 input coupling. Od = AC-coupled input Id = DC-coupled input Channel 3 microphone input range. Od = Low swing mode; Differential input AC signal full-scale of 2-VRMS supported provided DC differential common mode voltage INIP - INIM < 4.2 V. Single-ended AC signal 1-VRMS supported provided DC common mode voltage is < 2.1 V. Id = High swing mode; Differential Input INIP-INIM peak voltage up to 14.14 V or single ended 7.07 V supported. User rquired to adjust the	0x10 Description Microphone輸入 単端輸入 DC耦合	0x38 00111000 Setting 0 0 1
7 6 5 4	00010000 default 0 0 1	Address: Default Value: Default Value: Default Value: Channel 3 input type. Od = Microphone input 1d = Line input Channel 3 input configuration. Od = Analog differential input 1d = Analog single-ended input 2d = Reserved 3d = Reserved 3d = Reserved Channel 3 input coupling. Od = AC-coupled input 1d = DC-coupled input Channel 3 microphone input range. Od = Low swing mode; Differential input AC signal full-scale of 2-VRMS supported provided DC differential common mode voltage INIP - INIM < 4.2 V. Single-ended AC signal 1-VRMS supported provided DC common mode voltage is < 2.1 V. 1d = High swing mode; Differential Input INIP-INIM peak voltage up to 14.14 V or single ended 7.07 V supported. User rquired to adjust the channel gain and digital volume control based on the max signal level used in system.	0x10 Description Microphone輸入 単端輸入 DC耦合	0x38 00111000 Setting 0 0 1
7 6 5 4	00010000 default 0 0 1	Address: Default Value: Default Value: Default Value: Channel 3 input type. Od = Microphone input 1d = Line input Channel 3 input configuration. Od = Analog differential input 1d = Analog single-ended input 2d = Reserved 3d = Reserved 3d = Reserved 3d = Reserved Channel 3 input coupling. Od = AC-coupled input 1d = DC-coupled input Channel 3 microphone input range. Od = Low swing mode; Differential input AC signal full-scale of 2-VRMS supported provided DC differential common mode voltage INIP - INIM < 4.2 V. Single-ended AC signal 1-VRMS supported provided DC common mode voltage is < 2.1 V. 1d = High swing mode; Differential Input INIP-INIM peak voltage up to 14.14 V or single ended 7.07 V supported. User rquired to adjust the channel gain and digital volume control based on the max signal level used in system. Channel 3 CMRR Configuration.	0x10 Description Microphone輸入 単端輸入 DC耦合	0x38 00111000 Setting 0 0 1
7 6 5 4	00010000 default 0 0 1	Address: Default Value: Default Value: Default Value: Channel 3 input type. Od = Microphone input 1d = Line input Channel 3 input configuration. Od = Analog differential input 1d = Analog single-ended input 2d = Reserved 3d = Reserved 3d = Reserved Channel 3 input coupling. Od = AC-coupled input 1d = DC-coupled input Channel 3 microphone input range. Od = Low swing mode; Differential input AC signal full-scale of 2-VRMS supported provided DC differential common mode voltage INIP - INIM < 4.2 V. Single-ended AC signal 1-VRMS supported provided DC common mode voltage is < 2.1 V. 1d = High swing mode; Differential Input INIP-INIM peak voltage up to 14.14 V or single ended 7.07 V supported. User rquired to adjust the channel gain and digital volume control based on the max signal level used in system.	0x10 Description Microphone輸入 単端輸入 DC耦合	0x38 00111000 Setting 0 1 1
7 6 5 4 3	00010000 default 0 0 1	Address: Default Value: Default Value: Default Value: Channel 3 input type. Od = Microphone input 1d = Line input Channel 3 input configuration. Od = Analog differential input 1d = Analog single-ended input 2d = Reserved 3d = Reserved 3d = Reserved 3d = Reserved Channel 3 input coupling. Od = AC-coupled input 1d = DC-coupled input Channel 3 microphone input range. Od = Low swing mode; Differential input AC signal full-scale of 2-VRMS supported provided DC differential common mode voltage IN1P - IN1M < 4.2 V. Single-ended AC signal 1-VRMS supported provided DC common mode voltage is < 2.1 V. 1d = High swing mode; Differential Input IN1P-IN1M peak voltage up to 14.14 V or single ended 7.07 V supported. User rquired to adjust the channel gain and digital volume control based on the max signal level used in system. Channel 3 CMRR Configuration. Od = High SNR performance mode 1d = Reserved	0x10 Description Microphone輸入 単端輸入 DC耦合 大范围輸入	0x38 00111000 Setting 0 1 1 1
7 6 5 4	00010000 default 0 0 1	Address: Default Value: Default Value: Default Value: Channel 3 input type. Od = Microphone input 1d = Line input Channel 3 input configuration. Od = Analog differential input 1d = Analog single-ended input 2d = Reserved 3d = Reserved Channel 3 input coupling. Od = AC-coupled input 1d = DC-coupled input 1d = DC-coupled input Channel 3 microphone input range. Od = Low swing mode; Differential input AC signal full-scale of 2-VRMS supported provided DC differential common mode voltage INIP - INIM < 4.2 V. Single-ended AC signal 1-VRMS supported provided DC common mode voltage is < 2.1 V. 1d = High swing mode; Differential Input IN1P-IN1M peak voltage up to 14.14 V or single ended 7.07 V supported. User rquired to adjust the channel gain and digital volume control based on the max signal level used in system. Channel 3 CMRR Configuration. Od = High SNR performance mode 1d = Reserved 2d = High CMRR performance mode	0x10 Description Microphone輸入 単端輸入 DC耦合 大范围輸入	0x38 00111000 Setting 0 1 1
7 6 5 4 3	00010000 default 0 0 1	Address: Default Value: Definition Channel 3 input type. Od = Microphone input 1d = Line input Channel 3 input configuration. Od = Analog differential input 1d = Analog single-ended input 2d = Reserved 3d = Reserved Channel 3 input coupling. Od = AC-coupled input 1d = DC-coupled input 1d = DC-coupled input Channel 3 microphone input range. Od = Low swing mode; Differential input AC signal full-scale of 2-VRMS supported provided DC differential common mode voltage IN1P - IN1M < 4.2 V. Single-ended AC signal 1-VRMS supported provided DC common mode voltage is < 2.1 V. 1d = High swing mode; Differential Input IN1P-IN1M peak voltage up to 14.14 V or single ended 7.07 V supported. User rquired to adjust the channel gain and digital volume control based on the max signal level used in system. Channel 3 CMRR Configuration. Od = High SNR performance mode 1d = Reserved 2d = High CMRR performance mode 3d = Reserved	0x10 Description Microphone輸入 単端輸入 DC耦合 大范围輸入	0x38 00111000 Setting 0 0 1 1 0
7 6 5 4 3	00010000 default 0 0 1 0 0 0 0 0 0	Address: Default Value: Default Value: Default Value: Channel 3 input type. Od = Microphone input 1d = Line input Channel 3 input configuration. Od = Analog differential input 1d = Analog single-ended input 2d = Reserved 3d = Reserved 3d = Reserved Channel 3 input coupling. Od = AC-coupled input 1d = DC-coupled input 1d = DC-coupled input Channel 3 microphone input range. Od = Low swing mode; Differential input AC signal full-scale of 2-VRMS supported provided DC differential common mode voltage INIP - INIM < 4.2 V. Single-ended AC signal 1-VRMS supported provided DC common mode voltage is < 2.1 V. 1d = High swing mode; Differential Input INIP-INIM peak voltage up to 14.14 V or single ended 7.07 V supported. User rquired to adjust the channel gain and digital volume control based on the max signal level used in system. Channel 3 CMRR Configuration. Od = High SNR performance mode 1d = Reserved 2d = High CMRR performance mode 3d = Reserved Channel 3 automatic gain controller (AGC) setting	0x10 Description Microphone輸入 単端輸入 DC耦合 大范围輸入 Default	0x38 00111000 Setting 0 1 1 0 0 0
7 6 5 4	00010000 default 0 0 1 0 0 0 0 0 0	Address: Default Value: Definition Channel 3 input type. Od = Microphone input 1d = Line input Channel 3 input configuration. Od = Analog differential input 1d = Analog single-ended input 2d = Reserved 3d = Reserved Channel 3 input coupling. Od = AC-coupled input 1d = DC-coupled input 1d = DC-coupled input Channel 3 microphone input range. Od = Low swing mode; Differential input AC signal full-scale of 2-VRMS supported provided DC differential common mode voltage IN1P - IN1M < 4.2 V. Single-ended AC signal 1-VRMS supported provided DC common mode voltage is < 2.1 V. 1d = High swing mode; Differential Input IN1P-IN1M peak voltage up to 14.14 V or single ended 7.07 V supported. User rquired to adjust the channel gain and digital volume control based on the max signal level used in system. Channel 3 CMRR Configuration. Od = High SNR performance mode 1d = Reserved 2d = High CMRR performance mode 3d = Reserved	0x10 Description Microphone輸入 単端輸入 DC耦合 大范围輸入	0x38 00111000 Setting 0 0 1

	01000111		Address :	0x47
	00000000		Default Value :	0x00
bit	default	Definition		Description
7 6 5 4	0 0	Channel 3 gain. Od = Channel gain is set to 0 dB 1d = Channel gain is set to 1 dB 2d = Channel gain is set to 2 dB 3d to 41d = Channel gain is set as per configuration 42d = Channel gain is set to 42 dB 43d to 63d = Reserved		串扰、采样值问题对策: 8dB,后续根据需要调整

0x20
00100000
Setting
0
0
1
0
0

2	0			0
1		Reserved Reserved		0
	01001000 11001001	Address: Default Value:	0x48 0xC9	0xD 11011
	default	Definition Default value :	Description	Setti
7	1			1
6	1	Channel 3 digital volume control. 0d = Digital volume is muted		1
5	0	1d = Digital volume control is set to -100 dB		0
4	0	2d = Digital volume control is set to -99.5 dB 3d to 200d = Digital volume control is set as per configuration		1
3	1	201d = Digital volume control is set to 0 dB	串扰、采样值问题对策: 9dB, 后续根据需要调整	1
2	0	202d = Digital volume control is set to 0.5 dB 203d to 253d = Digital volume control is set as per configuration		0
1	0	254d = Digital volume control is set to 26.5 dB		1
0	1	255d = Digital volume control is set to 27 dB		1
	01001001 10000000	Address : Default Value :	0x49 0x80	0x8 10000
_	default	Definition Definition	Description	Setti
_				
7	1	Channel 3 gain calibration. Od = Gain calibration is set to -0.8 dB		1
		1d = Gain calibration is set to -0.6 db		
6	0	2d = Gain calibration is set to -0.6 dB		0
		3d to 7d = Gain calibration is set as per configuration 8d = Gain calibration is set to 0 dB	Default	
5	0	9d = Gain calibration is set to 0.1 dB 10d to 13d = Gain calibration is set as per configuration		0
		14d = Gain calibration is set to 0.6 dB		-
4	0	15d = Gain calibration is set to 0.7 dB		0
3	0			
2	0	Reserved		0
1	0			0
U	0			
	01001010	Address :	0x4A	0x0
	00000000 default	Definition Default Value :	0x00 Description	00000 Setti
7	0		Description	0
6	0			
	0	Channel 3 phase calibration with modulator clock resolution.		0
5	U	Channel 3 phase calibration with modulator clock resolution. Od = No phase calibration Id = Phase calibration delay is set to one cycle of the modulator clock		0
	0	Od = No phase calibration 1d = Phase calibration delay is set to one cycle of the modulator clock 2d = Phase calibration delay is set to two cycles of the modulator clock	Default	
5 4 3 2	0	0d = No phase calibration 1d = Phase calibration delay is set to one cycle of the modulator clock 2d = Phase calibration delay is set to two cycles of the modulator clock 3d to 254d = Phase calibration delay as per configuration	Default	0 0 0
5 4 3	0	Od = No phase calibration 1d = Phase calibration delay is set to one cycle of the modulator clock 2d = Phase calibration delay is set to two cycles of the modulator clock 3d to 254d = Phase calibration delay as per configuration 255d = Phase calibration delay is set to 255 cycles of the modulator clock	Default	0 0 0
5 4 3 2 1 0	0 0 0 0	Od = No phase calibration 1d = Phase calibration delay is set to one cycle of the modulator clock 2d = Phase calibration delay is set to two cycles of the modulator clock 3d to 254d = Phase calibration delay as per configuration 255d = Phase calibration delay is set to 255 cycles of the modulator clock		0 0 0 0 0
5 4 3 2 1 0	0 0 0	Od = No phase calibration 1d = Phase calibration delay is set to one cycle of the modulator clock 2d = Phase calibration delay is set to two cycles of the modulator clock 3d to 254d = Phase calibration delay as per configuration 255d = Phase calibration delay is set to 255 cycles of the modulator clock Address:	0x4B	0 0 0 0
5 4 3 2 1 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0	Od = No phase calibration 1d = Phase calibration delay is set to one cycle of the modulator clock 2d = Phase calibration delay is set to two cycles of the modulator clock 3d to 254d = Phase calibration delay as per configuration 255d = Phase calibration delay is set to 255 cycles of the modulator clock Address: Default Value:	0x4B	0 0 0 0 0
5 4 3 2 1 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Od = No phase calibration 1d = Phase calibration delay is set to one cycle of the modulator clock 2d = Phase calibration delay is set to two cycles of the modulator clock 3d to 254d = Phase calibration delay as per configuration 255d = Phase calibration delay is set to 255 cycles of the modulator clock Address: Default Value: Definition Channel 4 input type.	0x4B 0x10 Description	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
5 4 3 2 1 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Od = No phase calibration 1d = Phase calibration delay is set to one cycle of the modulator clock 2d = Phase calibration delay is set to two cycles of the modulator clock 3d to 254d = Phase calibration delay as per configuration 255d = Phase calibration delay is set to 255 cycles of the modulator clock Address: Default Value:	0x4B 0x10	0 0 0 0 0 0 0 0
5 4 3 2 1 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Od = No phase calibration 1d = Phase calibration delay is set to one cycle of the modulator clock 2d = Phase calibration delay is set to two cycles of the modulator clock 3d to 254d = Phase calibration delay as per configuration 255d = Phase calibration delay is set to 255 cycles of the modulator clock Address: Default Value: Definition Channel 4 input type. 0d = Microphone input 1d = Line input	0x4B 0x10 Description	0 0 0 0 0 0 0 0 0 00111 Setti
5 4 3 2 1 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Od = No phase calibration 1d = Phase calibration delay is set to one cycle of the modulator clock 2d = Phase calibration delay is set to two cycles of the modulator clock 3d to 254d = Phase calibration delay as per configuration 255d = Phase calibration delay is set to 255 cycles of the modulator clock Address: Default Value: Definition Channel 4 input type. 0d = Microphone input 1d = Line input Channel 4 input configuration. 0d = Analog differential input	0x4B 0x10 Description Microphone输入	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
5 4 3 2 1 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Od = No phase calibration	0x4B 0x10 Description	0 0 0 0 0 0 0 0 0 00111 Setti
5 4 3 2 1 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Od = No phase calibration 1d = Phase calibration delay is set to one cycle of the modulator clock 2d = Phase calibration delay is set to two cycles of the modulator clock 3d to 254d = Phase calibration delay as per configuration 255d = Phase calibration delay is set to 255 cycles of the modulator clock Address: Default Value: Definition Channel 4 input type. 0d = Microphone input 1d = Line input Channel 4 input configuration. 0d = Analog differential input	0x4B 0x10 Description Microphone输入	0 0 0 0 0 0 0 0 0 00111 Setti
5 4 3 2 1 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Od = No phase calibration 1d = Phase calibration delay is set to one cycle of the modulator clock 2d = Phase calibration delay is set to two cycles of the modulator clock 3d to 254d = Phase calibration delay as per configuration 255d = Phase calibration delay is set to 255 cycles of the modulator clock Address: Default Value: Default Value: Definition Channel 4 input type. 0d = Microphone input 1d = Line input Channel 4 input configuration. 0d = Analog differential input 1d = Analog single-ended input 2d = Reserved 3d = Reserved	0x4B 0x10 Description Microphone输入	0 0 0 0 0 0 0 0 0 00111 Setti
5 4 3 2 1 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Od = No phase calibration 1d = Phase calibration delay is set to one cycle of the modulator clock 2d = Phase calibration delay is set to two cycles of the modulator clock 3d to 254d = Phase calibration delay as per configuration 255d = Phase calibration delay is set to 255 cycles of the modulator clock Address: Default Value: Default Value: Definition Channel 4 input type. 0d = Microphone input 1d = Line input Channel 4 input configuration. 0d = Analog differential input 1d = Analog single-ended input 2d = Reserved 3d = Reserved 3d = Reserved Channel 4 input coupling. 0d = AC-coupled input	0x4B 0x10 Description Microphone输入	0 0 0 0 0 0 0 0 0 00111 Setti
5 4 3 2 1 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Od = No phase calibration 1d = Phase calibration delay is set to one cycle of the modulator clock 2d = Phase calibration delay is set to two cycles of the modulator clock 3d to 254d = Phase calibration delay as per configuration 255d = Phase calibration delay is set to 255 cycles of the modulator clock Address: Default Value : Definition Channel 4 input type. 0d = Microphone input 1d = Line input Channel 4 input configuration. 0d = Analog differential input 1d = Analog single-ended input 2d = Reserved 3d = Reserved Channel 4 input coupling.	Ox4B Ox10 Description Microphone输入 单端输入	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
5 4 3 2 1 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Od = No phase calibration 1d = Phase calibration delay is set to one cycle of the modulator clock 2d = Phase calibration delay is set to two cycles of the modulator clock 3d to 254d = Phase calibration delay as per configuration 255d = Phase calibration delay is set to 255 cycles of the modulator clock Address: Default Value: Definition Channel 4 input type. 0d = Microphone input 1d = Line input Channel 4 input configuration. 0d = Analog differential input 1d = Analog single-ended input 2d = Reserved 3d = Reserved Channel 4 input coupling. 0d = AC-coupled input 1d = DC-coupled input	Ox4B Ox10 Description Microphone输入 单端输入	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
5 4 3 2 1 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Od = No phase calibration 1d = Phase calibration delay is set to one cycle of the modulator clock 2d = Phase calibration delay is set to two cycles of the modulator clock 3d to 254d = Phase calibration delay as per configuration 255d = Phase calibration delay is set to 255 cycles of the modulator clock Address: Default Value : Definition Channel 4 input type. 0d = Microphone input 1d = Line input Channel 4 input configuration. 0d = Analog differential input 1d = Analog single-ended input 2d = Reserved 3d = Reserved Channel 4 input coupling. 0d = AC-coupled input 1d = DC-coupled input 1d = DC-coupled input 1d = DC-coupled input Channel 4 microphone input range. 0d = Low swing mode; Differential input AC signal full-scale of 2-VRMS supported provided DC differential common mode voltage INIP - INIM < 4.2	Ox4B Ox10 Description Microphone输入 单端输入	0 0 0 0 0 0 0 0 0 0 0 0 0 1111 Setti
5 4 3 2 1 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Od = No phase calibration 1d = Phase calibration delay is set to one cycle of the modulator clock 2d = Phase calibration delay is set to two cycles of the modulator clock 3d to 254d = Phase calibration delay as per configuration 255d = Phase calibration delay is set to 255 cycles of the modulator clock Address: Default Value: Channel 4 input type. 0d = Microphone input 1d = Line input Channel 4 input configuration. 0d = Analog differential input 1d = Analog single-ended input 2d = Reserved 3d = Reserved 3d = Reserved 3d = Reserved Channel 4 input coupling. 0d = AC-coupled input 1d = DC-coupled input 1d = DC-coupled input 1d = DC-coupled input Channel 4 microphone input range. 0d = Low swing mode; Differential input AC signal full-scale of 2-VRMS supported provided DC differential common mode voltage INIP - INIM < 4.2 V. Single-ended AC signal 1-VRMS supported provided DC common mode	0x4B 0x10 Description Microphone輸入 単端輸入	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
5 4 3 2 1 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Od = No phase calibration 1d = Phase calibration delay is set to one cycle of the modulator clock 2d = Phase calibration delay is set to two cycles of the modulator clock 3d to 254d = Phase calibration delay as per configuration 255d = Phase calibration delay is set to 255 cycles of the modulator clock Address: Default Value: Def	Ox4B Ox10 Description Microphone输入 单端输入	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
5 4 3 2 1 0 0 t 7 6	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Od = No phase calibration 1d = Phase calibration delay is set to one cycle of the modulator clock 2d = Phase calibration delay is set to two cycles of the modulator clock 3d to 254d = Phase calibration delay as per configuration 255d = Phase calibration delay is set to 255 cycles of the modulator clock Address: Default Value: Def	0x4B 0x10 Description Microphone輸入 単端輸入	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
5 4 3 2 1 0 0 t 4	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Od = No phase calibration 1d = Phase calibration delay is set to one cycle of the modulator clock 2d = Phase calibration delay is set to two cycles of the modulator clock 3d to 254d = Phase calibration delay as per configuration 255d = Phase calibration delay is set to 255 cycles of the modulator clock Address: Default Value: Def	0x4B 0x10 Description Microphone輸入 単端輸入	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
5 4 3 2 1 0 7 6 5	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Od = No phase calibration 1d = Phase calibration delay is set to one cycle of the modulator clock 2d = Phase calibration delay is set to two cycles of the modulator clock 3d to 254d = Phase calibration delay as per configuration 255d = Phase calibration delay is set to 255 cycles of the modulator clock Address: Default Value: Def	0x4B 0x10 Description Microphone輸入 単端輸入	0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0
5 4 3 2 1 0 0 t 4	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Od = No phase calibration 1d = Phase calibration delay is set to one cycle of the modulator clock 2d = Phase calibration delay is set to two cycles of the modulator clock 3d to 254d = Phase calibration delay as per configuration 255d = Phase calibration delay is set to 255 cycles of the modulator clock 3d to 254d = Phase calibration delay is set to 255 cycles of the modulator clock Address: Default Value: De	Ox4B Ox10 Description Microphone输入 单端输入 DC	0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0
5 4 3 2 1 0 6 5 4	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Od = No phase calibration d = Phase calibration delay is set to one cycle of the modulator clock 2d = Phase calibration delay is set to two cycles of the modulator clock 3d to 254d = Phase calibration delay as per configuration 255d = Phase calibration delay is set to 255 cycles of the modulator clock Address: Default Value:	0x4B 0x10 Description Microphone輸入 単端輸入	0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0
5 4 3 2 1 0 0 5 4	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Od = No phase calibration d = Phase calibration delay is set to one cycle of the modulator clock 2d = Phase calibration delay is set to two cycles of the modulator clock 3d to 254d = Phase calibration delay as per configuration 255d = Phase calibration delay is set to 255 cycles of the modulator clock Address: Default Value:	Ox4B Ox10 Description Microphone输入 单端输入 DC	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
5 4 4 3 2 1 0 0 1 1 6 5 4	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Od = No phase calibration dl = Phase calibration delay is set to one cycle of the modulator clock 2d = Phase calibration delay is set to two cycles of the modulator clock 3d to 254d = Phase calibration delay as per configuration 255d = Phase calibration delay is set to 255 cycles of the modulator clock 3d to 254d = Phase calibration delay is set to 255 cycles of the modulator clock Address: Default Value: De	Ox4B Ox10 Description Microphone输入 单端输入 DC	0 0 0 0 0 0 0 0 0 0 0 0 1 Setti
5 4 3 3 2 1 0 0 5 4 4 3 3 3 4 4 4 4 4 4 4 4 4 4 4 4 4 4	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Od = No phase calibration d = Phase calibration delay is set to one cycle of the modulator clock 2d = Phase calibration delay is set to two cycles of the modulator clock 3d to 254d = Phase calibration delay as per configuration 255d = Phase calibration delay is set to 255 cycles of the modulator clock Address: Default Value:	Ox4B Ox10 Description Microphone輸入 単端輸入 DC 大范围	0 0 0 0 0 0 0 0 0 0 1 Setti
5 4 3 2 1 0 7 6 5	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Od = No phase calibration	Ox4B Ox10 Description Microphone输入 单端输入 DC	0 0 0 0 0 0 0 0 0 0 0 0 1 Setti
5 4 3 2 1 0 0 5 4 4 3 3 3 4 4 4 4 4 4 4 4 4 4 4 4 4 4	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Od = No phase calibration d = Phase calibration delay is set to one cycle of the modulator clock 2d = Phase calibration delay is set to two cycles of the modulator clock 3d to 254d = Phase calibration delay as per configuration 255d = Phase calibration delay is set to 255 cycles of the modulator clock Address: Default Value:	Ox4B Ox10 Description Microphone輸入 単端輸入 DC 大范围	0 0 0 0 0 0 0 0 0 0 0 1 1 1
5 4 4 3 2 1 0 0 t t 3 3 3 2 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Od = No phase calibration	Ox4B Ox10 Description Microphone输入 单端输入 DC 大范围 Default 自动增益调节关闭	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
5 4 4 3 2 1 0 0 t t 7 6 6 3 3 2 2 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Dd = No phase calibration	Ox4B Ox10 Description Microphone输入 单端输入 DC 大范围 Default 自动增益调节关闭	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
5 4 4 3 2 1 0 0 t t 7 6 6 3 3 2 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Dd = No phase calibration	Ox4B Ox10 Description Microphone输入 单端输入 DC 大范围 Default 自动增益调节关闭	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

5		1d = Channel gain is set to 1 dB 2d = Channel gain is set to 2 dB	串扰、采样值问题对策: 8dB, 后续根据需要调整	1
4	0	3d to 41d = Channel gain is set as per configuration 42d = Channel gain is set to 42 dB		0
3		43d to 63d = Reserved		0
2	0			0
0		Reserved Reserved		0
	01001101 11001001	Address: Default Value:	0x4D 0xC9	0xD 11011
	default	Definition Definition	Description	Setti
7	1			1
6	1	Channel 4 digital volume control.		1
5	0	0d = Digital volume is muted 1d = Digital volume control is set to -100 dB		0
-+		2d = Digital volume control is set to -99.5 dB		
4	0	3d to 200d = Digital volume control is set as per configuration 201d = Digital volume control is set to 0 dB	串扰、采样值问题对策: 9dB, 后续根据需要调整	1
3		202d = Digital volume control is set to 0.5 dB		1
2	0	203d to 253d = Digital volume control is set as per configuration 254d = Digital volume control is set to 26.5 dB		0
1	0	255d = Digital volume control is set to 27 dB		1
0	1			1
	01001110	Address :	0x4E	0x8 10000
	L0000000 default	Default Value : Definition	0x80 Description	Setti
			· ·	
7	1	Channel 4 gain calibration.		1
+		0d = Gain calibration is set to -0.8 dB 1d = Gain calibration is set to -0.7 dB		
6	0	2d = Gain calibration is set to -0.6 dB		0
+		3d to 7d = Gain calibration is set as per configuration 8d = Gain calibration is set to 0 dB	Default	
5	0	9d = Gain calibration is set to 0.1 dB		0
+		10d to 13d = Gain calibration is set as per configuration 14d = Gain calibration is set to 0.6 dB		-
4	0	15d = Gain calibration is set to 0.7 dB		0
2	0			0
1	0	Reserved		0
0	0			0
0	01001111	Address :	0x4F	0x0
	00000000	Default Value :		00000
		Boldate Faldo :	0.000	00000
_	default	Definition	Description	Setti
7	0	Definition		
7 6 5	0 0 0	Definition Channel 4 phase calibration with modulator clock resolution. Od = No phase calibration		Setti 0 0 0
7 6 5 4	0 0 0	Definition Channel 4 phase calibration with modulator clock resolution. 0d = No phase calibration 1d = Phase calibration delay is set to one cycle of the modulator clock		Setti
7 6 5 4 3	0 0 0 0 0	Definition Channel 4 phase calibration with modulator clock resolution. Od = No phase calibration 1d = Phase calibration delay is set to one cycle of the modulator clock 2d = Phase calibration delay is set to two cycles of the modulator clock 3d to 254d = Phase calibration delay as per configuration	Description	Setti 0 0 0
7 6 5 4 3 2	0 0 0 0 0	Definition Channel 4 phase calibration with modulator clock resolution. Od = No phase calibration 1d = Phase calibration delay is set to one cycle of the modulator clock 2d = Phase calibration delay is set to two cycles of the modulator clock	Description	Setti 0 0 0 0 0 0 0 0 0 0 0 0
7 6 5 4 3 2	0 0 0 0 0	Definition Channel 4 phase calibration with modulator clock resolution. Od = No phase calibration 1d = Phase calibration delay is set to one cycle of the modulator clock 2d = Phase calibration delay is set to two cycles of the modulator clock 3d to 254d = Phase calibration delay as per configuration	Description	Setti
7 6 5 4 3 2 1	0 0 0 0 0	Definition Channel 4 phase calibration with modulator clock resolution. Od = No phase calibration 1d = Phase calibration delay is set to one cycle of the modulator clock 2d = Phase calibration delay is set to two cycles of the modulator clock 3d to 254d = Phase calibration delay as per configuration	Description Default	Setti 0 0 0 0 0 0 0 0 0 0 0 0
7 6 5 4 3 2 1 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Definition Channel 4 phase calibration with modulator clock resolution. Od = No phase calibration 1d = Phase calibration delay is set to one cycle of the modulator clock 2d = Phase calibration delay is set to two cycles of the modulator clock 3d to 254d = Phase calibration delay as per configuration 255d = Phase calibration delay is set to 255 cycles of the modulator clock Address: Default Value:	Description Default 0x50 0x10	Setti 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
7 6 5 4 3 2 1 0	0 0 0 0 0 0 0 0 0	Definition Channel 4 phase calibration with modulator clock resolution. Od = No phase calibration 1d = Phase calibration delay is set to one cycle of the modulator clock 2d = Phase calibration delay is set to two cycles of the modulator clock 3d to 254d = Phase calibration delay as per configuration 255d = Phase calibration delay is set to 255 cycles of the modulator clock Address: Default Value:	Description Default 0x50	Setti 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
7 6 5 4 3 2 1 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Definition Channel 4 phase calibration with modulator clock resolution. Od = No phase calibration 1d = Phase calibration delay is set to one cycle of the modulator clock 2d = Phase calibration delay is set to two cycles of the modulator clock 3d to 254d = Phase calibration delay as per configuration 255d = Phase calibration delay is set to 255 cycles of the modulator clock Address: Default Value: Definition Channel 5 input type. Od = Microphone input	Description Default 0x50 0x10	Setti 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
7 6 5 4 3 2 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Definition Channel 4 phase calibration with modulator clock resolution. Od = No phase calibration 1d = Phase calibration delay is set to one cycle of the modulator clock 2d = Phase calibration delay is set to two cycles of the modulator clock 3d to 254d = Phase calibration delay as per configuration 255d = Phase calibration delay is set to 255 cycles of the modulator clock Address: Default Value: Definition Channel 5 input type.	Description Default 0x50 0x10 Description	Setti 0 0 0 0 0 0 0 0 0 0 0 0 0 0 Setti
7 6 5 4 3 2 1 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Definition Channel 4 phase calibration with modulator clock resolution. Od = No phase calibration 1d = Phase calibration delay is set to one cycle of the modulator clock 2d = Phase calibration delay is set to two cycles of the modulator clock 3d to 254d = Phase calibration delay as per configuration 255d = Phase calibration delay is set to 255 cycles of the modulator clock Address: Default Value: Definition Channel 5 input type. Od = Microphone input 1d = Line input Channel 5 input configuration.	Description Default 0x50 0x10 Description	Setti 0 0 0 0 0 0 0 0 0 0 0 0 0 0 Setti
7 6 5 4 3 2 1 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Definition Channel 4 phase calibration with modulator clock resolution. Od = No phase calibration 1d = Phase calibration delay is set to one cycle of the modulator clock 2d = Phase calibration delay is set to two cycles of the modulator clock 3d to 254d = Phase calibration delay as per configuration 255d = Phase calibration delay is set to 255 cycles of the modulator clock Address: Default Value: Definition Channel 5 input type. Od = Microphone input 1d = Line input Channel 5 input configuration. 0d = Analog differential input 1d = Analog single-ended input	Description Default 0x50 0x10 Description	Setti 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
7 6 5 4 3 2 1 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Definition Channel 4 phase calibration with modulator clock resolution. Od = No phase calibration 1d = Phase calibration delay is set to one cycle of the modulator clock 2d = Phase calibration delay is set to two cycles of the modulator clock 3d to 254d = Phase calibration delay as per configuration 255d = Phase calibration delay is set to 255 cycles of the modulator clock Address: Default Value: Definition Channel 5 input type. Od = Microphone input 1d = Line input Channel 5 input configuration. Od = Analog differential input	Description Default 0x50 0x10 Description Microphone输入	Setti 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
7 6 5 4 3 2 1 0 C C C C 5 5 5 5 5 5 5 5 5 6 6 6 7 7 6 6 7 7 7 7	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Definition Channel 4 phase calibration with modulator clock resolution. Od = No phase calibration 1d = Phase calibration delay is set to one cycle of the modulator clock 2d = Phase calibration delay is set to two cycles of the modulator clock 3d to 254d = Phase calibration delay as per configuration 255d = Phase calibration delay is set to 255 cycles of the modulator clock Address: Default Value : Definition Channel 5 input type. Od = Microphone input 1d = Line input Channel 5 input configuration. Od = Analog differential input 1d = Analog single-ended input 2d = Reserved Channel 5 input coupling.	Description Default 0x50 0x10 Description Microphone输入 单端输入	Setti 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1
7 6 5 4 3 2 1 0 0 C C C 7 6 6	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Definition Channel 4 phase calibration with modulator clock resolution. Od = No phase calibration Id = Phase calibration delay is set to one cycle of the modulator clock 2d = Phase calibration delay is set to two cycles of the modulator clock 3d to 254d = Phase calibration delay as per configuration 255d = Phase calibration delay is set to 255 cycles of the modulator clock Address: Default Value: Definition Channel 5 input type. Od = Microphone input Id = Line input Channel 5 input configuration. Od = Analog differential input Id = Analog single-ended input 2d = Reserved Channel 5 input coupling. Od = AC-coupled input	Description Default 0x50 0x10 Description Microphone输入	Setti 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
7 6 5 4 3 2 1 0 C C C C 5 5 5 5 5 5 5 5 5 5 6 6 6 6 7 7 6 6 6 7 7 7 7	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Definition Channel 4 phase calibration with modulator clock resolution. Od = No phase calibration 1d = Phase calibration delay is set to one cycle of the modulator clock 2d = Phase calibration delay is set to two cycles of the modulator clock 3d to 254d = Phase calibration delay as per configuration 255d = Phase calibration delay is set to 255 cycles of the modulator clock Address: Default Value: Definition Channel 5 input type. Od = Microphone input 1d = Line input Channel 5 input configuration. Od = Analog differential input 1d = Analog single-ended input 2d = Reserved Channel 5 input coupling. Od = AC-coupled input 1d = DC-coupled input	Description Default 0x50 0x10 Description Microphone输入 单端输入	Setti 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1
7 6 5 4 3 2 1 0 C C C C 5 5 5 5 5 5 5 5 5 5 6 6 6 6 7 7 6 6 6 7 7 7 7	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Definition Channel 4 phase calibration with modulator clock resolution. Od = No phase calibration 1d = Phase calibration delay is set to one cycle of the modulator clock 2d = Phase calibration delay is set to two cycles of the modulator clock 3d to 254d = Phase calibration delay as per configuration 255d = Phase calibration delay is set to 255 cycles of the modulator clock Address: Default Value: Definition Channel 5 input type. 0d = Microphone input 1d = Line input Channel 5 input configuration. 0d = Analog differential input 1d = Analog single-ended input 2d = Reserved Channel 5 input coupling. 0d = AC-coupled input 1d = DC-coupled input 1d = DC-coupled input Channel 5 microphone input range.	Description Default 0x50 0x10 Description Microphone输入 单端输入	Setti 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1
7 6 5 4 3 2 1 0 0 0 7	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Definition Channel 4 phase calibration with modulator clock resolution. Od = No phase calibration 1d = Phase calibration delay is set to one cycle of the modulator clock 2d = Phase calibration delay is set to two cycles of the modulator clock 3d to 254d = Phase calibration delay as per configuration 255d = Phase calibration delay is set to 255 cycles of the modulator clock Address: Default Value: Definition Channel 5 input type. Od = Microphone input 1d = Line input Channel 5 input configuration. Od = Analog differential input 1d = Analog differential input 2d = Reserved Channel 5 input coupling. Od = AC-coupled input 1d = DC-coupled input Channel 5 microphone input range. Od = Low swing mode; Differential input AC signal full-scale of 2-VRMS supported provided DC differential common mode voltage INIP - INIM < 4.2	Description Default 0x50 0x10 Description Microphone输入 单端输入	Setti 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1
7 6 5 4 3 2 1 0 C C C C 5 5 5 5 5 5 5 5 5 6 6 6 7 7 6 6 7 7 7 7	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Definition Channel 4 phase calibration with modulator clock resolution. Od = No phase calibration 1d = Phase calibration delay is set to one cycle of the modulator clock 2d = Phase calibration delay is set to two cycles of the modulator clock 3d to 254d = Phase calibration delay as per configuration 255d = Phase calibration delay is set to 255 cycles of the modulator clock Address: Default Value: Definition Channel 5 input type. 0d = Microphone input 1d = Line input Channel 5 input configuration. 0d = Analog differential input 1d = Analog single-ended input 2d = Reserved Channel 5 input coupling. 0d = AC-coupled input 1d = DC-coupled input 1d = DC-coupled input 1d = DC-coupled input 2d = Reserved Channel 5 microphone input range. 0d = Low swing mode; Differential input AC signal full-scale of 2-VRMS supported provided DC differential common mode voltage INIP - INIM < 4.2 V. Single-ended AC signal 1-VRMS supported provided DC common mode	Description Default 0x50 0x10 Description Microphone输入 单端输入	Setti 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1
7 6 5 4 3 2 1 0 0 7 6 5 4 3 2 1 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Definition Channel 4 phase calibration with modulator clock resolution. Od = No phase calibration 1d = Phase calibration delay is set to one cycle of the modulator clock 2d = Phase calibration delay is set to two cycles of the modulator clock 3d to 254d = Phase calibration delay as per configuration 255d = Phase calibration delay is set to 255 cycles of the modulator clock Address: Default Value: Default V	Description Ox50 Ox10 Description Microphone输入 单端输入 DC	Setti
7 6 5 4 3 2 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Definition Channel 4 phase calibration with modulator clock resolution. Od = No phase calibration Id = Phase calibration delay is set to one cycle of the modulator clock 2d = Phase calibration delay is set to two cycles of the modulator clock 3d to 254d = Phase calibration delay as per configuration 255d = Phase calibration delay is set to 255 cycles of the modulator clock Address: Default Value: Definition Channel 5 input type. Od = Microphone input Id = Line input Channel 5 input configuration. Od = Analog differential input 2d = Reserved Channel 5 input coupling. Od = AC-coupled input Channel 5 microphone input range. Od = Low swing mode; Differential input AC signal full-scale of 2-VRMS supported provided DC differential common mode voltage INIP - INIM < 4.2 V. Single-ended AC signal 1-VRMS supported provided DC common mode voltage is < 2.1 V. Id = High swing mode; Differential Input INIP-INIM peak voltage up to 14.14 V or single ended 7.07 V supported. User rquired to adjust the	Description Ox50 Ox10 Description Microphone输入 单端输入 DC	Setti
7 6 5 4 3 2 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Definition Channel 4 phase calibration with modulator clock resolution. Od = No phase calibration 1d = Phase calibration delay is set to one cycle of the modulator clock 2d = Phase calibration delay is set to two cycles of the modulator clock 3d to 254d = Phase calibration delay as per configuration 255d = Phase calibration delay is set to 255 cycles of the modulator clock Address: Default Value: Default V	Description Ox50 Ox10 Description Microphone输入 单端输入 DC	Setti
7 6 5 4 3 2 1 1 0 0 C C C 7 6 5 4 4 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Definition Channel 4 phase calibration with modulator clock resolution. Od = No phase calibration 1d = Phase calibration delay is set to one cycle of the modulator clock 2d = Phase calibration delay is set to two cycles of the modulator clock 3d to 254d = Phase calibration delay as per configuration 255d = Phase calibration delay is set to 255 cycles of the modulator clock Address: Default Value: Definition Channel 5 input type. Od = Microphone input 1d = Line input Channel 5 input configuration. Od = Analog differential input 1d = Analog single-ended input 2d = Reserved Channel 5 input coupling. Od = AC-coupled input 1d = DC-coupled input 1d = DC-coupled input 2d = Reserved Channel 5 microphone input range. Od = Low swing mode; Differential common mode voltage INIP - INIM < 4.2 V. Single-ended AC signal 1-VRMS supported provided DC common mode voltage is < 2.1 V. 1d = High swing mode; Differential Input INIP-INIM peak voltage up to 14.14 V or single ended 7.07 V supported. User rquired to adjust the channel gain and digital volume control based on the max signal level used in system.	Description Ox50 Ox10 Description Microphone输入 单端输入 DC	Setti
7 6 5 4 3 2 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Definition Channel 4 phase calibration with modulator clock resolution. Od = No phase calibration 1d = Phase calibration delay is set to one cycle of the modulator clock 2d = Phase calibration delay is set to two cycles of the modulator clock 3d to 254d = Phase calibration delay as per configuration 255d = Phase calibration delay is set to 255 cycles of the modulator clock Address: Default Value: Default V	Description Ox50 Ox10 Description Microphone输入 单端输入 DC	Setti
7 6 5 4 3 2 1 0 0 7 6 5 4 4 3 7 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Definition Channel 4 phase calibration with modulator clock resolution. Od = No phase calibration 1d = Phase calibration delay is set to one cycle of the modulator clock 2d = Phase calibration delay is set to two cycles of the modulator clock 3d to 254d = Phase calibration delay as per configuration 255d = Phase calibration delay is set to 255 cycles of the modulator clock Address: Default Value: Definition Channel 5 input type. Od = Microphone input 1d = Line input Channel 5 input configuration. Od = Analog differential input 1d = Analog single-ended input 2d = Reserved Channel 5 input coupling. Od = AC-coupled input 1d = DC-coupled input 1	Description Ox50 Ox10 Description Microphone输入 单端输入 DC	Setti
7 6 5 4 3 2 1 0 0 7 6 5 4 4 3 7 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Definition Channel 4 phase calibration with modulator clock resolution. Od = No phase calibration 1d = Phase calibration delay is set to one cycle of the modulator clock 2d = Phase calibration delay is set to two cycles of the modulator clock 3d to 254d = Phase calibration delay as per configuration 255d = Phase calibration delay is set to 255 cycles of the modulator clock Address: Default Value: Default V	Description Ox50 Ox10 Description Microphone输入 单端输入 DC	Setti
7 6 5 4 4 3 2 1 0 0 7 6 5 7 6	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Definition Channel 4 phase calibration with modulator clock resolution. Od = No phase calibration 1d = Phase calibration delay is set to one cycle of the modulator clock 2d = Phase calibration delay is set to two cycles of the modulator clock 3d to 254d = Phase calibration delay as per configuration 255d = Phase calibration delay is set to 255 cycles of the modulator clock Address: Default Value: Definition Channel 5 input type. Od = Microphone input 1d = Line input Channel 5 input configuration. Od = Analog differential input 1d = Analog single-ended input 2d = Reserved Channel 5 input coupling. Od = AC-coupled input 1d = DC-coupled input 1d = Nisymported provided DC common mode voltage IN1P - IN1M < 4.2 V. Single-ended AC signal 1-VRMS supported provided DC common mode voltage is < 2.1 V. 1d = High swing mode; Differential input IN1P-IN1M peak voltage up to 14.14 V or single ended 7.07 V supported. User rquired to adjust the channel gain and digital volume control based on the max signal level used in system. Channel 5 CMRR Configuration. Od = High SNR performance mode 1d = Reserved 2d = High CMRR performance mode 3d = Reserved	Description Ox50 Ox10 Description Microphone输入 单端输入 DC	Setti
7 6 5 4 3 2 1 1 0 C C C 7 7 6 6 5 4 4 3 3 2 1 1 1 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Definition Channel 4 phase calibration with modulator clock resolution. Od = No phase calibration 1d = Phase calibration delay is set to one cycle of the modulator clock 2d = Phase calibration delay is set to two cycles of the modulator clock 3d to 254d = Phase calibration delay as per configuration 255d = Phase calibration delay is set to 255 cycles of the modulator clock Address: Default Value: Definition Channel 5 input type. Od = Microphone input 1d = Line input Channel 5 input configuration. Od = Analog differential input 2d = Reserved Channel 5 input coupling. Od = AC-coupled input 1d = DC-coupled Input Channel 5 microphone input range. Od = Low swing mode; Differential input AC signal full-scale of 2-VRMS supported provided DC cifferential common mode voltage IN1P - IN1M < 4.2 V. Single-ended AC signal 1-VRMS supported provided DC common mode voltage is < 2.1 V. 1d = High swing mode; Differential Input IN1P-IN1M peak voltage up to 14.14 V or single ended 7.07 V supported. User rquired to adjust the channel gain and digital volume control based on the max signal level used in system. Channel 5 CMRR Configuration. Od = High SNR performance mode 1d = Reserved 2d = High CMRR performance mode 3d = Reserved 2d = High CMRR performance mode 3d = Reserved Channel 5 automatic gain controller (AGC) setting. Od = AGC disabled	Description Default Ox50 Ox10 Description Microphone输入 单端输入 DC 大范围	Setti 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 0
7 6 5 4 3 2 1 0 0 7 6 5 7 7	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Definition Channel 4 phase calibration with modulator clock resolution. Od = No phase calibration 1d = Phase calibration delay is set to one cycle of the modulator clock 2d = Phase calibration delay is set to two cycles of the modulator clock 3d to 254d = Phase calibration delay as per configuration 255d = Phase calibration delay is set to 255 cycles of the modulator clock Address: Default Value: Definition Channel 5 input type. Od = Microphone input 1d = Line input Channel 5 input configuration. Od = Analog differential input 2d = Reserved Channel 5 input coupling. Od = AC-coupled input 1d = DC-coupled input 1d = DC-coupled input 2d = Reserved Channel 5 microphone input range. Od = Low swing mode; Differential input AC signal full-scale of 2-VRMS supported provided DC differential common mode voltage INIP - INIM < 4.2 V. Single-ended AC signal 1-VRMS supported provided DC common mode voltage is < 2.1 V. 1d = High swing mode; Differential Input INIP-INIM peak voltage up to 14.14 V or single ended 7.07 V supported. User rquired to adjust the channel gain and digital volume control based on the max signal level used in system. Channel 5 CMRR Configuration. Od = High SNR performance mode 1d = Reserved 2d = High CMRR performance mode 3d = Reserved Channel 5 automatic gain controller (AGC) setting.	Description Ox50 Ox10 Description Microphone输入 单端输入 DC	Setti

	00000000	Default Value :	0x00	00100000
	default	Definition	Description	Setting
7	0	Channer 5 gain.		0
6		0d = Channel gain is set to 0 dB		0
5	0	2d = Channel gain is set to 2 dP	串扰、采样值问题对策: 8dB, 后续根据需要调整	1
4	0	3d to 41d = Channel gain is set as per configuration	中, 八、不汗自己这对来。000, 石头很如而又两重	0
3	0	42a = Channel gain is set to 42 ab		0
2	0	43d to 63d = Reserved		0
1	0	Reserved		0
0	0	Reserved		0
	01010010		0.50	0.00
	01010010 11001001	Address : Default Value :	0x52 0xC9	0xDB 11011011
	default	Definition Definition	Description	Setting
7	1	Definition	Description	1
6		Channel 5 digital volume control.		
	1	0d = Digital volume is muted		1
5	0	1d = Digital volume control is set to -100 dB 2d = Digital volume control is set to -99.5 dB		0
4	0	3d to 200d = Digital volume control is set as per configuration	史比 文程传行题对策: Odb F楼相据需要调整	1
3	1	201d = Digital volume control is set to 0 dB	串扰、采样值问题对策: 9dB, 后续根据需要调整	1
2	0	202d = Digital volume control is set to 0.5 dB		0
_		203d to 253d = Digital volume control is set as per configuration 254d = Digital volume control is set to 26.5 dB		
1	0	255d = Digital volume control is set to 27 dB		1
0	1			1
	01010011		0x53	0x80
	10000000	Default Value :	0x80	10000000
bit	default	Definition	Description	Setting
7	1	0d = Gain calibration is set to -0.8 dB		1
Ī		1d = Gain calibration is set to -0.7 dB		
6	0	2d = Gain calibration is set to -0.6 dB		0
		3d to 7d = Gain calibration is set as per configuration 8d = Gain calibration is set to 0 dB	Default	
5	Λ	9d = Gain calibration is set to 0 dB		0
٦	U	10d to 13d = Gain calibration is set as per configuration		
		14d = Gain calibration is set to 0.6 dB		
4	0	15d = Gain calibration is set to 0.7 dB		0
3	0	4		0
2	0	1 Reserved		0
1	0			0
U	0			0
	01010100	Address :	0x54	0x00
	00000000	Default Value :	0x00	00000000
bit	default	Definition	Description	Setting
7	0	4		0
6	0	Chainlei 3 phase cambration with modulator clock resolution.		0
5 4		0d = No phase calibration		0
3		1d = Phase calibration delay is set to one cycle of the modulator clock 2d = Phase calibration delay is set to two cycles of the modulator clock	Default	0
2	0	3d to 254d = Phase calibration delay as per configuration		0
1	0	255d = Phase calibration delay is set to 255 cycles of the modulator clock		0
0	0			0
	01010101	Address :	0x55	0x38
	00010000	Default Value :	0x10	00111000
bit	default	Definition	Description	Setting
7	^	Channel 6 input type. Od = Microphone input	Microphone输入	0
′	U	1d = Line input	IVIIGIOPHONE#I/人	"
		·		
6	0	Channel 6 input configuration.		0
		0d = Analog differential input	单端输入	
5	n	1d = Analog single-ended input 2d = Reserved		1
″		La Rossived		
		Channel 6 input coupling.		
4	1	0d = AC-coupled input	DC	1
		1d = DC-coupled input		
		Channel 6 microphone input range.		
		0d = Low swing mode; Differential input AC signal full-scale of 2-VRMS		
		supported provided DC differential common mode voltage IN1P - IN1M < 4.2		
3	n	V. Single-ended AC signal 1-VRMS supported provided DC common mode voltage is < 2.1 V.	大范围	1
٦	U	1d = High swing mode; Differential Input IN1P-IN1M peak voltage up to	, ,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	1
		14.14 V or single ended 7.07 V supported. User rquired to adjust the		
		channel gain and digital volume control based on the max signal level used		
		in system.		
		Channel 6 CMPP Configuration		
2	0	Channel 6 CMRR Configuration. Od = High SNR performance mode		0
		1d = Reserved	Default	
				1
1	0	2d = High CMRR performance mode 3d = Reserved		0
		1d = Reserved	Default	

		Channel 6 automatic gain controller (AGC) setting.		
0	0	0d = AGC disabled	Default	0
		1d = AGC enabled based on the configuration of bit 3 in register 108 (P0_R108); This must be used only with AC-coupled input		
	04.04.04.4.0		0.50	0.00
	01010110	Address: Default Value:	0000	0x20 00100000
_	default	Definition	Description	Setting
7	0	Channel 6 gain.		0
6	0	0d = Channel gain is set to 0 dB		0
5	0	1d = Channel gain is set to 1 dB 2d = Channel gain is set to 2 dB	串扰、采样值问题对策: 8dB, 后续根据需要调整	1
4	0	3d to 41d = Channel gain is set as per configuration	ALTON SKILL WEST NO. COOL MAN WARRING THAT	0
3	0	42d = Channel gain is set to 42 dB 43d to 63d = Reserved		0
2	0			0
1		Reserved Reserved		0
	01010111 11001001	Address: Default Value:	0x57 0xC9	0xDB 11011011
	default	Definition Default value .	Description	Setting
7	1			1
6	1	Channel 6 digital volume control. 0d = Digital volume is muted		1
5	0	1d = Digital volume control is set to -100 dB		0
4	0	2d = Digital volume control is set to -99.5 dB 3d to 200d = Digital volume control is set as per configuration		1
3	1	201d = Digital volume control is set to 0 dB	串扰、采样值问题对策: 9dB, 后续根据需要调整	1
2	0	202d = Digital volume control is set to 0.5 dB 203d to 253d = Digital volume control is set as per configuration		0
1	0	254d = Digital volume control is set to 26.5 dB		1
0	1	255d = Digital volume control is set to 27 dB		1
	01011000	Address :	0x58	0x80
_	10000000 default	Default Value : Definition	0x80 Description	10000000 Setting
		Channel 6 gain calibration.	·	
7	1	Od = Gain calibration is set to -0.8 dB		1
6	0	1d = Gain calibration is set to -0.7 dB 2d = Gain calibration is set to -0.6 dB		0
	·	3d to 7d = Gain calibration is set as per configuration	Default	
5	0	8d = Gain calibration is set to 0 dB 9d = Gain calibration is set to 0.1 dB	Sidan	0
	_	10d to 13d = Gain calibration is set as per configuration 14d = Gain calibration is set to 0.6 dB		
4	0	15d = Gain calibration is set to 0.5 dB		0
3	0			0
2	0			0
1	0			0
0	0			
	01011001	Address :	0x59	0x00
	00000000 default	Default Value :	0x00 Description	00000000 Setting
7	0		S SSS. IPEIOTI	0
6	0	Channel 6 phase calibration with modulator clock resolution.		0
5 4	0	Od = No phase calibration 1d = Phase calibration delay is set to one cycle of the modulator clock	Default	0
3	0	2d = Phase calibration delay is set to two cycles of the modulator clock	Default	0
1	0	3d to 254d = Phase calibration delay as per configuration 255d = Phase calibration delay is set to 255 cycles of the modulator clock		0
0	0			0
	01100100	A 11	0x64	000
	01100100 00000000	Address: Default Value:	0x00	0x00 00000000
	default	Definition	Description	Setting
7	0	Channel 1 input (IN1P and IN1M) scan for diagnostics. Od = Diagnostic disabled 1d = Diagnostic enabled	Default	0
6	0	Channel 2 input (IN2P and IN2M) scan for diagnostics. Od = Diagnostic disabled 1d = Diagnostic enabled	Default	0
5	0	Channel 3 input (IN3P and IN3M) scan for diagnostics. Od = Diagnostic disabled 1d = Diagnostic enabled	Default	0
4	0	Channel 4 input (IN4P and IN4M) scan for diagnostics. Od = Diagnostic disabled 1d = Diagnostic enabled	Default	0
3	0	Channel 5 input (IN5P and IN5M) scan for diagnostics. Applicable only for PCM6x60-Q1. Od = Diagnostic disabled	Default	0
2	0	1d = Diagnostic enabled Channel 6 input (IN6P and IN6M) scan for diagnostics. Applicable only for PCM6x60-Q1. Od = Diagnostic disabled	Default	0
		1d = Diagnostic enabled		

1	0	INxM pin diagnostics scan selection for single-ended configuration. Od = INxM pins of single-ended channels are excluded for diagnosis 1d = INxM pins of single-ended channels are included for diagnosis	Default	0
0	0	AC-coupled channels pins scan selection for diagnostics. Od = INxP and INxM pins of AC-coupled channels are excluded for diagnosis Id = INxP and INxM pins of AC-coupled channels are included for diagnosis	DC-coupled, 对象外	0
	01100101	Address :	0x65	0x37
	00110111 default	Default Value : Definition	0x37 Description	00110111 Setting
7			Безаприон	0
		INxP and INxM terminal short detect threshold. 0d = INxP and INxM terminal short detect threshold value is 0 mV (typ)		
6	0	1d = INxP and INxM terminal short detect threshold value is 30 mV (typ) 2d = INxP and INxM terminal short detect threshold value is 60 mV (typ)	Default	0
5	1	10d to 13d = INxP and INxM terminal short detect threshold value is set as per configuration	Default	1
		14d = INXP and INXM terminal short detect threshold value is 420 mV (typ) 15d = INXP and INXM terminal short detect threshold value is 450 mV (typ)		
4	1	100 mar did mark terminal short detect all eshold value is 100 mv (typ)		1
3	0	SHOLL TO ADAI IN GELECT THESHOLD.		0
2	1	0d = Short to VBAT_IN detect threshold value is 0 mV (typ) 1d = Short to VBAT_IN detect threshold value is 30 mV (typ)		1
		2d = Short to VBAT_IN detect threshold value is 60 mV (typ) 10d to 13d = Short to VBAT_IN detect threshold value is set as per	Default	
1		configuration 14d = Short to VBAT IN detect threshold value is 420 mV (typ)		1
0	1	15d = Short to VBAT_IN detect threshold value is 420 mV (typ)		1
	01100110 10000111	Address: Default Value:	0x66 0x87	0x87 10000111
bit	default	Definition	Description	Setting
7	1	Short to ground detect threshold.		1
6	0	0d = Short to ground detect threshold value is 0 mV (typ) 1d = Short to ground detect threshold value is 60 mV (typ)		0
		2d = Short to ground detect threshold value is 120 mV (typ) 10d to 13d = Short to ground detect threshold value is set as per	Default	
5	0	configuration 14d = Short to ground detect threshold value is 840 mV (typ)		0
4	0	15d = Short to ground detect threshold value is 900 mV (typ)		0
3	0	Short to MICBIAS detect threshold.		0
		0d = Short to MICBIAS detect threshold value is 0 mV (typ)		
2	1	1d = Short to MICBIAS detect threshold value is 30 mV (typ) 2d = Short to MICBIAS detect threshold value is 60 mV (typ)	Default	1
1	1	10d to 13d = Short to MICBIAS detect threshold value is set as per configuration		1
0	1	14d = Short to MICBIAS detect threshold value is 420 mV (typ) 15d = Short to MICBIAS detect threshold value is 450 mV (typ)		1
	01100111 10111000	Address : Default Value :		0xB8
	default	Definition Definition	Description	10111000 Setting
		Fault monitoring scan repetition rate.		
7	1	0d = Continuos back to back scanning of selected channels input pins without any idle time		1
		1d = Fault monitoring repetition rate of 1 ms for selected channels input pins	ch1~6: Diagnostic disabled selected	
		scanning 2d = Fault monitoring repetition rate of 4 ms for selected channels input pins	ch1~6: Diagnostic disabled selected	
6	0	scanning 3d = Fault monitoring repetition rate of 8 ms for selected channels input pins		0
		scanning		
5 4	1	Reserved		1
3	1	Debounce count for all the faults (except VBAT_IN short when VBAT_IN < MICBIAS).		1
		0d = 16 counts for debounce to filter-out any false faults detection 1d = 8 counts for debounce to filter-out any false faults detection		
2	0	2d = 4 counts for debounce to filter-out any false faults detection		0
1	0	VBAT_IN short debounce count only when VBAT_IN < MICBIAS. Od = 16 counts for debounce to filter-out any false faults detection		0
		1d = 8 counts for debounce to filter-out any false faults detection		
0	0	Diagnostic thresholds range scale. Od = Thresholds same as configured in PO_R101 and PO_R102		0
Ш		1d = All the configuration thresholds gets scale by 2 times		
	01101000 00000000	Address : Default Value :	0x68 0x00	0x00 00000000
	default	Definition Definition	Description	Setting
		Moving average configuration.		
7	0	0d = Moving average disabled 1d = Moving average enabled with 0.5 weightage for old scanned data and		0
\Box		new scanned data	Moving average年	

6	0	2d = Moving average enabled with 0.75 weightage for old scanned data and 0.25 weightage for new scanned data 3d = Reserved	INTOVING AVELAGENTIS	0
5	0	Moving average configuration for MICBIAS high and low load current fault detection Od = Moving average as defined by DIAG_MOV_AVG_CFG setting 1d = Moving average is forced disabled for MICBIAS load current fault detection to achieve faster response time	Moving averag禁用,设定无效	0
4	0	Moving average configuration for over temperature fault detection 0d = Moving average as defined by DIAG_MOV_AVG_CFG setting 1d = Moving average is forced disabled for over temperature fault detection to achieve faster response time	Moving averag禁用,设定无效	0
3 2 1	0 0	Reserved		0 0 0
	01101011	Address : Default Value :		0x01 00000001
bit	default	Definition	Description	Setting
7	0			0
5		Decimation filter response. Od = Linear phase Id = Low latency		0
4	U	2d = Ultra-low latency		0
3	0	Id = 2-channel summation mode is enabled to generate a (CH1 + CH2) / 2 and a (CH3 + CH4) / 2 output 2d = 4-channel summation mode is enabled to generate a (CH1 + CH2 + CH3 + CH4) / 4 output	Channel summation mode关闭	0
	ا ا	3d = Reserved		
1	0	Od = Programmable first-order IIR filter for a custom HPF with default coefficient values in P4_R72 to P4_R83 set as the all-pass filter Id = HPF with a cutoff of 0.00025 x fS (12 Hz at fS = 48 kHz) is selected	通过右侧设置高通滤波器 *回路参照	0
0	1	2d = HPF with a cutoff of 0.002 x fS (96 Hz at fS = 48 kHz) is selected 3d = HPF with a cutoff of 0.008 x fS (384 Hz at fS = 48 kHz) is selected		1
	01101100			
	01101100	Address :	0x6C	0x48
la ia	01001000	Default Value :	0x48	01001000
bit 7	01001000 default			
	01001000 default	Default Value : Definition DVOL control ganged across channels. Od = Each channel has its own DVOL CTRL settings as programmed in the CHx_DVOL bits 1d = All active channels must use the channel 1 DVOL setting (CH_DVOL) irrespective of whether channel 1 is turned on or not Number of biquads per channel configuration. Od = No biquads per channel; biquads are all disabled 1d = 1 biquad per channel 2d = 2 biquads per channel	0x48 Description	01001000 Setting
6	01001000 default 0	Default Value: Definition DVOL control ganged across channels. Od = Each channel has its own DVOL CTRL settings as programmed in the CHx_DVOL bits 1d = All active channels must use the channel 1 DVOL setting (CH_DVOL) irrespective of whether channel 1 is turned on or not Number of biquads per channel configuration. Od = No biquads per channel; biquads are all disabled 1d = 1 biquad per channel 2d = 2 biquads per channel 2d = 2 biquads per channel 3d = 3 biquads per channel Soft-stepping disable during DVOL change, mute, and unmute. Od = Soft-stepping enabled 1d = Soft-stepping disabled	0x48 Description 每个通道数字增益分别控制	01001000 Setting 0
7 6 5 4	01001000 default 0 1	Default Value: Definition DVOL control ganged across channels. Od = Each channel has its own DVOL CTRL settings as programmed in the CHx_DVOL bits 1d = All active channels must use the channel 1 DVOL setting (CH_DVOL) irrespective of whether channel 1 is turned on or not Number of biquads per channel 1 is turned on or not Number of biquads per channel; biquads are all disabled 1d = No biquads per channel; biquads are all disabled 2d = 2 biquads per channel 2d = 2 biquads per channel 3d = 3 biquads per channel Soft-stepping disable during DVOL change, mute, and unmute. Od = Soft-stepping enabled 1d = Soft-stepping disabled AGC master enable setting. Od = Reserved; Write always 1 to this register bit 1d = AGC selected as configured for each channel using CHx_CFGO register	Description 每个通道数字增益分别控制 每个通道两个滤波器	01001000 Setting 0 1 0 1
7 6 5	01001000 default 0 1	Default Value: Definition DVOL control ganged across channels. Dd = Each channel has its own DVOL CTRL settings as programmed in the CHx, DVOL bits 1d = All active channels must use the channel 1 DVOL setting (CH_DVOL) irrespective of whether channel 1 is turned on or not Number of biquads per channel configuration. Dd = No biquads per channel; biquads are all disabled 1d = 1 biquad per channel 2d = 2 biquads per channel 2d = 2 biquads per channel 3d = 3 biquads per channel Soft-stepping disable during DVOL change, mute, and unmute. Dd = Soft-stepping disabled AGC master enable setting. Dd = Reserved; Write always 1 to this register bit 1d = AGC selected as configured for each channel using CHx_CFGO register Reserved	Description 每个通道数字增益分别控制 每个通道两个滤波器	01001000 Setting 0 1 0
7 6 5 4	01001000 default	Default Value: Definition DVOL control ganged across channels. Od = Each channel has its own DVOL CTRL settings as programmed in the CHx_DVOL bits Id = All active channels must use the channel 1 DVOL setting (CH_DVOL) irrespective of whether channel 1 is turned on or not Number of biquads per channel configuration. Od = No biquads per channel; biquads are all disabled Id = 1 biquad per channel 2d = 2 biquads per channel 3d = 3 biquads per channel Soft-stepping disable during DVOL change, mute, and unmute. Od = Soft-stepping enabled Id = Soft-stepping disabled AGC master enable setting. Od = Reserved; Write always 1 to this register bit Id = AGC selected as configured for each channel using CHx_CFGO register Reserved	Description 每个通道数字增益分别控制 每个通道两个滤波器	01001000 Setting 0 1 0 1 0
7 6 5 4 3 2 1	01001000 default	Default Value: Definition DVOL control ganged across channels. Od = Each channel has its own DVOL CTRL settings as programmed in the CHx_DVOL bits Id = All active channels must use the channel 1 DVOL setting (CH_DVOL) irrespective of whether channel 1 is turned on or not Number of biquads per channel configuration. Od = No biquads per channel; biquads are all disabled Id = 1 biquad per channel 2d = 2 biquads per channel 3d = 3 biquads per channel Soft-stepping disable during DVOL change, mute, and unmute. Od = Soft-stepping enabled Id = Soft-stepping disabled AGC master enable setting. Od = Reserved; Write always 1 to this register bit Id = AGC selected as configured for each channel using CHx_CFGO register Reserved	Description 每个通道数字增益分别控制 每个通道两个滤波器 Soft-stepping有效	01001000 Setting 0 1 0 1 0 0 0 1
7 6 5 4 3 2 1 0	01001000 default	Default Value: Definition DVOL control ganged across channels. Od = Each channel has its own DVOL CTRL settings as programmed in the CHx_DVOL bits 1d = All active channels must use the channel 1 DVOL setting (CH_DVOL) irrespective of whether channel 1 is turned on or not Number of biquads per channel configuration. Od = No biquads per channel; biquads are all disabled 1d = 1 biquad per channel 2d = 2 biquads per channel 2d = 2 biquads per channel 3d = 3 biquads per channel 3d = 3 biquads per channel 4d = Soft-stepping disable during DVOL change, mute, and unmute. Od = Soft-stepping disabled AGC master enable setting. Od = Reserved; Write always 1 to this register bit 1d = AGC selected as configured for each channel using CHx_CFGO register Reserved Address: Default Value:	Ox48 Description 每个通道数字增益分别控制 每个通道两个滤波器 Soft-stepping有效 Ox70 OxE7	01001000 Setting 0 1 0 0 1 0 0 0 0 0 0 0 0
7 6 5 4 3 2 1 0	01001000 default	Default Value: Definition DVOL control ganged across channels. Od = Each channel has its own DVOL CTRL settings as programmed in the CHx_DVOL bits 1d = All active channels must use the channel 1 DVOL setting (CH_DVOL) irrespective of whether channel 1 is turned on or not Number of biquads per channel configuration. Od = No biquads per channel; biquads are all disabled 1d = 1 biquad per channel 2d = 2 biquads per channel 3d = 3 biquads per channel Soft-stepping disable during DVOL change, mute, and unmute. Od = Soft-stepping disabled AGC master enable setting. Od = Reserved; Write always 1 to this register bit 1d = AGC selected as configured for each channel using CHx_CFG0 register Reserved Reserved Address:	Ox48 Description 每个通道数字增益分别控制 每个通道两个滤波器 Soft-stepping有效	01001000 Setting 0 1 0 0 1 0 0 0 0 0 0 0 0
7 6 5 4 3 2 1 0	01001000 default 0 0 1 1 0 0 0 0 0 01110000 11100111 default 1	Definition Definition DVOL control ganged across channels. Od = Each channel has its own DVOL CTRL settings as programmed in the CHx_DVOL bits 1d = All active channels must use the channel 1 DVOL setting (CH_DVOL) irrespective of whether channel 1 is turned on or not Number of biquads per channel configuration. Od = No biquads per channel; biquads are all disabled 1d = 1 biquad per channel 2d = 2 biquads per channel 3d = 3 biquads per channel Soft-stepping disable during DVOL change, mute, and unmute. Od = Soft-stepping disabled 1d = Soft-stepping disabled AGC master enable setting. Od = Reserved; Write always 1 to this register bit 1d = AGC selected as configured for each channel using CHx_CFG0 register Reserved Address: Default Value: Definition	Ox48 Description 每个通道数字增益分别控制 每个通道两个滤波器 Soft-stepping有效 Ox70 OxE7 Description	01001000 Setting 0 1 0 0 1 0 0 0 0 0 0 0 0
7 6 5 4 3 2 1 0 bit 7 6 5	01001000 default 0 0 1 1 0 0 0 0 11100111 default 1 1	Definition Definition DVOL control ganged across channels. Od = Each channel has its own DVOL CTRL settings as programmed in the CHx, DVOL bits 1d = All active channels must use the channel 1 DVOL setting (CH_DVOL) irrespective of whether channel 1 is turned on or not Number of biquads per channel configuration. Od = No biquads per channel; biquads are all disabled 1d = 1 biquad per channel 2d = 2 biquads per channel 3d = 3 biquads per channel Soft-stepping disable during DVOL change, mute, and unmute. Od = Soft-stepping disabled AGC master enable setting. Od = Reserved; Write always 1 to this register bit 1d = AGC selected as configured for each channel using CHx_CFGO register Reserved Reserved Address: Default Value: Definition AGC output signal target level is -6 dB 1d = Output signal target level is -6 dB 2d = Output signal target level is -10 dB 3d to 13d = Output signal target level is -34 dB 15d = Output signal target level is -34 dB 15d = Output signal target level is -34 dB 15d = Output signal target level is -36 dB	Ox48 Description 每个通道数字增益分别控制 每个通道两个滤波器 Soft-stepping有效 Ox70 OxE7	01001000 Setting 0 1 0 0 1 0 0 0 0 0 0 0 0
7 6 5 4 3 2 1 0 bit 7 6 5 4	01001000 default 0 0 1 0 0 0 0 0 0111000111 default 1	Definition Definition DVOL control ganged across channels. Od = Each channel has its own DVOL CTRL settings as programmed in the CHx, DVOL bits 1d = All active channels must use the channel 1 DVOL setting (CH_DVOL) irrespective of whether channel 1 is turned on or not Number of biquads per channel configuration. Od = No biquads per channel; biquads are all disabled 1d = 1 biquad per channel 2d = 2 biquads per channel 3d = 3 biquads per channel Soft-stepping disable during DVOL change, mute, and unmute. Od = Soft-stepping disabled AGC master enable setting. Od = Reserved; Write always 1 to this register bit 1d = AGC selected as configured for each channel using CHx_CFGO register Reserved Reserved Address: Default Value: Definition AGC output signal target level is -6 dB 1d = Output signal target level is -6 dB 2d = Output signal target level is -10 dB 3d to 13d = Output signal target level is -34 dB 15d = Output signal target level is -34 dB 15d = Output signal target level is -34 dB 15d = Output signal target level is -36 dB	Description 每个通道数字增益分别控制 每个通道两个滤波器 Soft-stepping有效 Ox70 OxE7 Description -6dB暂定	01001000 Setting 0 1 0 0 1 0 0 0 0 0 0 0 0
7 6 5 4 3 2 1 0 bit 7 6 5	01001000 default 0 0 1 1 0 0 0 0 1110000 0 11100111 default 1 1 0 0	Definition Definition DVOL control ganged across channels. Od = Each channel has its own DVOL CTRL settings as programmed in the CTHX_DVOL bits 1d = All active channels must use the channel 1 DVOL setting (CH_DVOL) irrespective of whether channel 1 is turned on or not Number of biquads per channel configuration. Od = No biquads per channel; biquads are all disabled 1d = 1 biquad per channel 2d = 2 biquads per channel 3d = 3 biquads per channel Soft-stepping disable during DVOL change, mute, and unmute. Od = Soft-stepping disabled AGC master enable setting. Od = Reserved; Write always 1 to this register bit 1d = AGC selected as configured for each channel using CHx_CFGO register Reserved Reserved Address: Default Value: Definition AGC output signal target level is -6 dB 1d = Output signal target level is -8 dB 2d = Output signal target level is -10 dB 3d to 13d = Output signal target level is -34 dB 15d = Output signal target level is -34 dB AGC maximum gain allowed. Od = Maximum gain allowed. Od = Maximum gain allowed. Od = Maximum gain allowed.	Description 每个通道数字增益分别控制 每个通道两个滤波器 Soft-stepping有效 Ox70 OxE7 Description -6dB暂定	01001000 Setting 0 1 0 0 1 0 0 0 0 0 0 0 0
7 6 5 4 3 2 1 0 bit 7 6 5 4	01001000 default 0 0 1 1 0 0 0 0 1110000 0 11100111 default 1 1 0 0	Definition Definition DVOL control ganged across channels. Od = Each channel has its own DVOL CTRL settings as programmed in the CHx_DVOL bits 1d = All active channels must use the channel 1 DVOL setting (CH_DVOL) irrespective of whether channel 1 is turned on or not Number of biquads per channel configuration. Od = No biquads per channel; biquads are all disabled 1d = 1 biquad per channel 2d = 2 biquads per channel 3d = 3 biquads per channel 3d = 3 biquads per channel Soft-stepping disable during DVOL change, mute, and unmute. Od = Soft-stepping disabled 1d = Soft-stepping disabled AGC master enable setting. Od = Reserved; Write always 1 to this register bit 1d = AGC selected as configured for each channel using CHx_CFG0 register Reserved Address: Default Value: Definition AGC output signal target level is -6 dB 1d = Output signal target level is -8 dB 2d = Output signal target level is -10 dB 3d to 13d = Output signal target level is -34 dB 15d = Output signal target level is -36 dB AGC maximum gain allowed. Od = Maximum gain allowed. Od = Maximum gain allowed is 3 dB 1d Maximum gain allowed is 6 dB 2d = Maximum gain allowed is 9 dB	Description 每个通道数字增益分别控制 每个通道两个滤波器 Soft-stepping有效 Ox70 OxE7 Description -6dB暂定 *回路参照	01001000 Setting 0 1 0 0 1 0 0 0 0 0 0 0 0
7 6 5 4 3 2 1 0 bit 7 6 5 4 3	01001000 default	Definition Definition DVOL control ganged across channels. Od = Each channel has its own DVOL CTRL settings as programmed in the CHx, DVOL bits 1d = All active channels must use the channel 1 DVOL setting (CH_DVOL) irrespective of whether channel 1 is turned on or not Number of biquads per channel configuration. Od = No biquads per channel; biquads are all disabled 1d = 1 biquad per channel 2d = 2 biquads per channel 3d = 3 biquads per channel Soft-stepping disable during DVOL change, mute, and unmute. Od = Soft-stepping disabled AGC master enable setting. Od = Reserved; Write always 1 to this register bit 1d = AGC selected as configured for each channel using CHx_CFGO register Reserved Reserved Address: Default Value: Definition AGC output signal target level is -6 dB 1d = Output signal target level is -8 dB 2d = Output signal target level is -10 dB 3d to 13d = Output signal target level is -34 dB 1d = Output signal target level is -36 dB AGC maximum gain allowed. Od = Maximum gain allowed. Od = Maximum gain allowed. Od = Maximum gain allowed is 3 dB 1d = Maximum gain allowed is 6 dB	Description 每个通道数字增益分别控制 每个通道两个滤波器 Soft-stepping有效 Ox70 OxE7 Description -6dB暂定 *回路参照	01001000 Setting 0 1 0 0 1 0 0 0 0 0 0 0 0

	01110011	Address :	0x73	0xFC
	11111100	Default Value :	0xFC	11111100
bit	default	Definition	Description	Setting
7		Input channel 1 enable setting. 0d = Channel 1 is disabled 1d = Channel 1 is enabled	Default	1
6		Input channel 2 enable setting. 0d = Channel 2 is disabled 1d = Channel 2 is enabled	Default	1
5		Input channel 3 enable setting. 0d = Channel 3 is disabled 1d = Channel 3 is enabled	Default	1
4		Input channel 4 enable setting. 0d = Channel 4 is disabled 1d = Channel 4 is enabled	Default	1
3		Input channel 5 enable setting. Applicable only for PCM6x60-Q1. 0d = Channel 5 is disabled 1d = Channel 5 is enabled	Default	1
2		Input channel 6 enable setting. Applicable only for PCM6x60-Q1. 0d = Channel 6 is disabled 1d = Channel 6 is enabled	Default	1
1		Reserved		0
0	0	Reserved		0

	01110100	Address :	0x74
	00000000	Default Value :	0x00
bit	default	Definition	Description
7	0	ASI output channel 1 enable setting. 0d = Channel 1 output slot is in a tri-state condition 1d = Channel 1 output slot is enabled	slot使用
6	0	ASI output channel 2 enable setting. Od = Channel 2 output slot is in a tri-state condition 1d = Channel 2 output slot is enabled	slot使用
5	0	ASI output channel 3 enable setting. 0d = Channel 3 output slot is in a tri-state condition 1d = Channel 3 output slot is enabled	slot使用
4	0	ASI output channel 4 enable setting. 0d = Channel 4 output slot is in a tri-state condition 1d = Channel 4 output slot is enabled	slot使用
3	0	ASI output channel 5 enable setting. Applicable only for PCM6x60-Q1. Od = Channel 5 output slot is in a tri-state condition 1d = Channel 5 output slot is enabled	slot使用
2	0	ASI output channel 6 enable setting. Applicable only for PCM6x60-Q1. Od = Channel 6 output slot is in a tri-state condition 1d = Channel 6 output slot is enabled	slot使用
1		Reserved	
0	0	Reserved	

	01110101	Address :	0x75
	00000000	Default Value :	0x00
bit	default	Definition	Description
7	0	Power control for MICBIAS. 0d = Power down MICBIAS 1d = Power up MICBIAS	打开MICBIAS
6		Power control for ADC channels. 0d = Power down all ADC channels 1d = Power up all enabled ADC channels	打开所有通道
5	0	Power control for the PLL. 0d = Power down the PLL 1d = Power up the PLL	打开PLL
4		Dynamic channel power-up, power-down enable. 0d = Channel power-up, power-down is not supported if any channel recording is on 1d = Channel can be powered up or down individually, even if channel recording is on. Do not powered-down channel 1 if this bit is set to '1'	
3	0	Dynamic mode maximum channel select configuration. 0d = Channel 1 and channel 2 are used with dynamic channel power-up, power-down feature enabled 1d = Channel 1 to channel 4 are used with dynamic channel power-up,	
2	0	power-down feature enabled 2d = Channel 1 to channel 6 are used with dynamic channel power-up, power-down feature enabled	
1		Reserved	
0	0	Reserved	

	01110110		Address : 0x76
	00000000		Default Value: 0x00
bit	default	Definition	Description
7	0	ADC channel 1 power status. 0d = ADC channel is powered down 1d = ADC channel is powered up	
6	0	ADC channel 2 power status. 0d = ADC channel is powered down 1d = ADC channel is powered up	
5	0	ADC channel 3 power status. 0d = ADC channel is powered down 1d = ADC channel is powered up	

0 0xF8 11111000 Setting
11111000 Setting
11111000 Setting
Setting
1
1
1
1
1
0
0
0

0xFC Setting

0x00
00000000
Setting
0
0
0

	4	0	ADC channel 4 power status. 0d = ADC channel is powered down		0
			1d = ADC channel is powered up ADC channel 5 power status. Applicable only for PCM6x60-Q1.		
	3	0	0d = ADC channel is powered down 1d = ADC channel is powered up		0
	2	0	ADC channel 6 power status. Applicable only for PCM6x60-Q1. 0d = ADC channel is powered down		0
	1		1d = ADC channel is powered up Reserved		0
	0	0	Reserved		0
		01110111	Address :	0x77	0x80
		10000000	Default Value :	0x80	10000000
	bit 7	default 1	Definition Device mode status.	Description	Setting 1
	6	0			0
	5	0	7d = Device is in active mode with at least one ADC channel turned on Boost power up status.		0
	4	0	0d = Boost is powered down 1d = Boost is powered up		0
	3	0	MICBIAS power up status. 0d = MICBIAS is powered down 1d = MICBIAS is powered up		0
	2	0	ADC channel power down status caused by INxx inputs faults. 0d = No ADC channel is powered down caused by INxx inputs faults		0
			1d = Atleast a ADC channel is powered down caused by INxx inputs faults ADC channel power down status caused by MICBIAS faults.		-
	1	0	0d = No ADC channel is powered down caused by MICBIAS faults 1d = All ADC channels are powered down caused by MICBIAS faults		0
			Manual recovery (self-clearing bit). Od = No effect		
	0	0	1d = Recheck all fault status and re-powerup ADC channels and/or MICBIAS if they do not have any faults. Before setting this bit, reset PO_R58 register and re-configure PO_R58 to desired setting only after manual recover gets over.		0
		01111110	Address :	∩v7F	0x00
		00000000	Default Value :		00000000
	bit	default	Definition	Description	Setting
	6	0			0
	5	0	Those hits return the ISC transactions shooks up value Writing to this		0
	3	0	register resets the checksum to the written value. This register is updated on	checksum用	0
	2	0	IWITIES TO OTHER REGISTERS OF All DAGES.		0
	1	0			0
	U	0	<u> </u>		0
page 0x01		00000000			
UXUI			Address:		0x01
		00000000 00000000 default	Address : Default Value : Definition	0x00 0x00 Description	0x01 00000001 Setting
	bit 7	00000000 default 0	Default Value : Definition	0x00	00000001 Setting 0
	bit	00000000 default 0	Default Value : Definition	0x00 Description	00000001 Setting 0 0
	bit 7 6 5 4	00000000 default 0 0 0	Default Value : Definition These bits set the device page. 0d = Page 0 1d = Page 1	0x00 Description page页选择	00000001 Setting 0 0 0 0
	bit 7 6 5 4	00000000 default 0 0 0 0	Default Value : Definition These bits set the device page. 0d = Page 0 1d = Page 1	0x00 Description	00000001 Setting 0 0 0 0 0 0
	bit 7 6 5 4	00000000 default 0 0 0	Default Value : Definition These bits set the device page. 0d = Page 0 1d = Page 1 255d = Page 255	0x00 Description page页选择 page0x00选择00	00000001 Setting 0 0 0 0
	bit 7 6 5 4 3 2	00000000 default 0 0 0 0 0	Default Value : Definition These bits set the device page. 0d = Page 0 1d = Page 1 255d = Page 255	0x00 Description page页选择 page0x00选择00	00000001 Setting 0 0 0 0 0 0 0
	bit 7 6 5 4 3 2 1 0	00000000 default 0 0 0 0 0	Default Value : Definition These bits set the device page. 0d = Page 0 1d = Page 1 255d = Page 255	Description page页选择 page0x00选择00 page0x01选择01	00000001 Setting 0 0 0 0 0 0 0 0 0
	bit 7 6 5 4 3 2 1 0 0	00000000 default 0 0 0 0 0 0 0 0 0 0 0 0 0	Default Value : Definition These bits set the device page. 0d = Page 0 1d = Page 1 255d = Page 255 Address : Default Value :	Ox00 Description page页选择 page0x00选择00 page0x01选择01 Ox16 Ox00	00000001 Setting 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0
	bit 7 6 5 4 3 2 1 0 0	000000000 default 0 0 0 0 0 0 0 0 0 0 0 0 0	Default Value : Definition These bits set the device page. 0d = Page 0 1d = Page 1 255d = Page 255 Address : Default Value :	Ox00 Description page页选择 page0x00选择00 page0x01选择01 Ox16	00000001 Setting 0 0 0 0 0 0 1
	bit 7 6 5 4 3 2 1 0 0	00000000 default 0 0 0 0 0 0 0 0 0 0 0 0 0	Default Value : Definition These bits set the device page. 0d = Page 0 1d = Page 1 255d = Page 255 Address : Default Value : Definition MICBIAS internal load sink setting.	Ox00 Description page页选择 page0x00选择00 page0x01选择01 Ox16 Ox00	00000001 Setting 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0
	bit 7 6 5 4 3 2 1 0 0	00000000 default 0 0 0 0 0 0 0 0 0 0 0 0 0	Default Value : Definition These bits set the device page. 0d = Page 0 1d = Page 1 255d = Page 255 Address : Default Value : Definition MICBIAS internal load sink setting. 0d = MICBIAS internal load sink is enabled with setting automatically calculated based on device configuration	Ox00 Description page页选择 page0x00选择00 page0x01选择01 Ox16 Ox00	00000001 Setting 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0
	bit 7 6 5 4 3 2 2 1 0	00000000 default 0 0 0 0 0 0 0 0 0 0 0 0 0	Default Value : Definition These bits set the device page. 0d = Page 0 1d = Page 1 255d = Page 255 Address : Default Value : Definition MICBIAS internal load sink setting. 0d = MICBIAS internal load sink is enabled with setting automatically	Ox00 Description page页选择 page0x00选择00 page0x01选择01 Ox16 Ox00 Description	00000001 Setting 0 0 0 0 0 0 1 0 0 0 Setting 0 Setting 0 Setting
	bit 7 6 5 4 3 2 2 1 0	00000000 default 0 0 0 0 0 0 0 0 0 0 0 0 0	Default Value : Definition These bits set the device page. Od = Page 0 1d = Page 1 255d = Page 255 Address : Default Value : Definition MICBIAS internal load sink setting. Od = MICBIAS internal load sink is enabled with setting automatically calculated based on device configuration 1d = MICBIAS internal load sink is enabled based on D6-4 register bits; This	Ox00 Description page页选择 page0x00选择00 page0x01选择01 Ox16 Ox00 Description	00000001 Setting 0 0 0 0 0 0 1 0 0 0 Setting 0 Setting 0 Setting
	bit 7 6 5 5 4 1 3 3 2 1 1 0 0 bit 7 7	00000000 default 0 0 0 0 0 0 0 0 0 0 0 0 0	Default Value : Definition These bits set the device page. 0d = Page 0 1d = Page 1	Ox00 Description page页选择 page0x00选择00 page0x01选择01 Ox16 Ox00 Description	00000001 Setting 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0
	bit 7 6 5 4 3 2 2 1 0	00000000 default 0 0 0 0 0 0 0 0 0 0 0 0 0	Default Value : Definition These bits set the device page. Od = Page 0 1d = Page 1 255d = Page 255 Address : Default Value : Definition MICBIAS internal load sink setting. Od = MICBIAS internal load sink is enabled with setting automatically calculated based on device configuration 1d = MICBIAS internal load sink is enabled based on D6-4 register bits; This setting must be used for single-ended AC-coupled input to support high signal swing MICBIAS internal load sink current value Od = MICBIAS internal load sink current value Od = MICBIAS internal load sink current value	Ox00 Description page页选择 page0x00选择00 page0x01选择01 Ox16 Ox00 Description	00000001 Setting 0 0 0 0 0 0 1 0 0 0 Setting 0 Setting 0 Setting
	bit 7 6 5 5 4 1 3 3 2 1 1 0 0 bit 7 7	00000000 default 0 0 0 0 0 0 0 0 0 0 0 0 0	Default Value : Definition These bits set the device page. Od = Page 0 1d = Page 1	Ox00 Description page页选择 page0x00选择00 page0x01选择01 Ox16 Ox00 Description	00000001 Setting 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0
	bit 7 6 5 5 4 1 3 3 2 1 1 0 0 bit 7 7	00000000 default 0 0 0 0 0 0 0 0 0 0 0 0 0	Default Value: Definition These bits set the device page. 0d = Page 0 1d = Page 1 255d = Page 255 Address: Default Value: Definition MICBIAS internal load sink setting. 0d = MICBIAS internal load sink is enabled with setting automatically calculated based on device configuration 1d = MICBIAS internal load sink is enabled based on D6-4 register bits; This setting must be used for single-ended AC-coupled input to support high signal swing MICBIAS internal load sink current value 0d = MICBIAS internal load sink current is set to 0 mA (typ) 1d = MICBIAS internal load sink current is set to 4.3 mA (typ) 2d = MICBIAS internal load sink current is set to 8.6 mA (typ) 3d = MICBIAS internal load sink current is set to 12.9 mA (typ) 3d = MICBIAS internal load sink current is set to 12.9 mA (typ)	Ox00 Description page页选择 page0x00选择00 page0x01选择01 Ox16 Ox00 Description	00000001 Setting 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0
	bit 7 6 5 5 4 3 3 2 1 1 0 0 bit 6 6	00000000 default 0 0 0 0 0 0 0 0 0 0 0 0 0	Default Value: Definition These bits set the device page. 0d = Page 0 1d = Page 1 255d = Page 255 Address: Default Value: Definition MICBIAS internal load sink setting. 0d = MICBIAS internal load sink is enabled with setting automatically calculated based on device configuration 1d = MICBIAS internal load sink is enabled based on D6-4 register bits; This setting must be used for single-ended AC-coupled input to support high signal swing MICBIAS internal load sink current value 0d = MICBIAS internal load sink current is set to 0 mA (typ) 1d = MICBIAS internal load sink current is set to 4.3 mA (typ) 2d = MICBIAS internal load sink current is set to 12.9 mA (typ) 3d = MICBIAS internal load sink current is set to 12.9 mA (typ) 4d = MICBIAS internal load sink current is set to 17.2 mA (typ)	Ox00 Description page页选择 page0x00选择00 page0x01选择01 Ox16 Ox00 Description Default	00000001 Setting 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0
	bit 7 6 5 5 4 3 3 2 1 1 0 0 bit 5 5	00000000 default 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Default Value : Definition These bits set the device page. 0d = Page 0 1d = Page 1 255d = Page 255 Address : Default Value : Definition MICBIAS internal load sink setting. 0d = MICBIAS internal load sink is enabled with setting automatically calculated based on device configuration 1d = MICBIAS internal load sink is enabled based on D6-4 register bits; This setting must be used for single-ended AC-coupled input to support high signal swing MICBIAS internal load sink current is set to 0 mA (typ) 1d = MICBIAS internal load sink current is set to 4.3 mA (typ) 2d = MICBIAS internal load sink current is set to 8.6 mA (typ) 3d = MICBIAS internal load sink current is set to 12.9 mA (typ) 3d = MICBIAS internal load sink current is set to 12.5 mA (typ) 3d = MICBIAS internal load sink current is set to 21.5 mA (typ) 3d = MICBIAS internal load sink current is set to 21.5 mA (typ) 3d = MICBIAS internal load sink current is set to 21.5 mA (typ) 3d = MICBIAS internal load sink current is set to 21.5 mA (typ) 6d = MICBIAS internal load sink current is set to 25.8 mA (typ)	Ox00 Description page页选择 page0x00选择00 page0x01选择01 Ox16 Ox00 Description Default	00000001 Setting 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0
	bit 7 6 5 5 4 3 3 2 1 1 0 0 bit 6 6	00000000 default 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Default Value: Definition These bits set the device page. 0d = Page 0 1d = Page 1 255d = Page 255 Address: Default Value: Definition MICBIAS internal load sink setting. 0d = MICBIAS internal load sink is enabled with setting automatically calculated based on device configuration 1d = MICBIAS internal load sink is enabled based on D6-4 register bits; This setting must be used for single-ended AC-coupled input to support high signal swing MICBIAS internal load sink current is set to 0 mA (typ) 1d = MICBIAS internal load sink current is set to 4.3 mA (typ) 2d = MICBIAS internal load sink current is set to 8.6 mA (typ) 3d = MICBIAS internal load sink current is set to 17.2 mA (typ) 4d = MICBIAS internal load sink current is set to 17.2 mA (typ) 5d = MICBIAS internal load sink current is set to 17.2 mA (typ)	Ox00 Description page页选择 page0x00选择00 page0x01选择01 Ox16 Ox00 Description Default	00000001 Setting 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0
	bit 77 66 55 41 33 22 11 00 bit 55 44 33 3	00000000 default 0 0 0 0 0 0 0 0 0 0 0 0 0	Default Value : Definition These bits set the device page. Od = Page 0 1d = Page 1	Description page页选择 page0x00选择00 page0x01选择01 Ox16 Ox00 Description Default	00000001 Setting 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0
	bit 7 6 6 5 5 4 4 3 3 2 2 1 1 0 0 1 5 1 5 1 6 6 5 5 4 4 1 6 1 6 1 6 1 6 1 6 1 6 1 6 1 6 1 6	00000000 default 0 0 0 0 0 0 0 0 0 0 0 0 0	Default Value : Definition These bits set the device page. Od = Page 0 1d = Page 1 255d = Page 255 Address : Default Value : Definition MICBIAS internal load sink setting. Od = MICBIAS internal load sink is enabled with setting automatically calculated based on device configuration 1d = MICBIAS internal load sink is enabled based on D6-4 register bits; This setting must be used for single-ended AC-coupled input to support high signal swing MICBIAS internal load sink current is set to 0 mA (typ) 1d = MICBIAS internal load sink current is set to 4.3 mA (typ) 2d = MICBIAS internal load sink current is set to 9.8 mA (typ) 3d = MICBIAS internal load sink current is set to 17.2 mA (typ) 4d = MICBIAS internal load sink current is set to 17.2 mA (typ) 5d = MICBIAS internal load sink current is set to 21.5 mA (typ) 6d = MICBIAS internal load sink current is set to 21.5 mA (typ) 6d = MICBIAS internal load sink current is set to 25.8 mA (typ) 7d = MICBIAS internal load sink current is set to 25.8 mA (typ)	Description page页选择 page0x00选择00 page0x01选择01 Ox16 Ox00 Description Default	00000001 Setting 0 0 0 0 0 0 1 1 0 0 0 0 0 0 0 0 0 0 0
	bit 77 66 55 41 33 22 11 00 bit 55 44 33 3	00000000 default 0 0 0 0 0 0 0 0 0 0 0 0 0	Default Value: Definition These bits set the device page. 0d = Page 0 1d = Page 1 255d = Page 255 Address: Default Value: Definition MICBIAS internal load sink setting. 0d = MICBIAS internal load sink is enabled with setting automatically calculated based on device configuration 1d = MICBIAS internal load sink is enabled based on D6-4 register bits; This setting must be used for single-ended AC-coupled input to support high signal swing MICBIAS internal load sink current is set to 0 mA (typ) 1d = MICBIAS internal load sink current is set to 4.3 mA (typ) 2d = MICBIAS internal load sink current is set to 12.9 mA (typ) 3d = MICBIAS internal load sink current is set to 12.9 mA (typ) 4d = MICBIAS internal load sink current is set to 17.2 mA (typ) 5d = MICBIAS internal load sink current is set to 21.5 mA (typ) 6d = MICBIAS internal load sink current is set to 25.8 mA (typ) 7d = MICBIAS internal load sink current is set to 25.8 mA (typ) 7d = MICBIAS internal load sink current is set to 25.8 mA (typ)	Description page页选择 page0x00选择00 page0x01选择01 Ox16 Ox00 Description Default	00000001 Setting 0 0 0 0 0 0 1 1 0 0 0 0 0 0 0 0 0 0 0
	bit 7 6 5 4 3 3 2 5 4 4 3 3 2 5 4 4 5 5 5 6 6 6 6 6 6 6 6 6 6 6 6 6 6	00000000 default 0 0 0 0 0 0 0 0 0 0 0 0 0	Default Value : Definition These bits set the device page. Od = Page 0 1d = Page 1 255d = Page 255 Address : Default Value : Definition MICBIAS internal load sink setting. Od = MICBIAS internal load sink is enabled with setting automatically calculated based on device configuration 1d = MICBIAS internal load sink is enabled based on D6-4 register bits; This setting must be used for single-ended AC-coupled input to support high signal swing MICBIAS internal load sink current value Od = MICBIAS internal load sink current is set to 0 mA (typ) 1d = MICBIAS internal load sink current is set to 4.3 mA (typ) 2d = MICBIAS internal load sink current is set to 12.9 mA (typ) 3d = MICBIAS internal load sink current is set to 12.9 mA (typ) 4d = MICBIAS internal load sink current is set to 17.2 mA (typ) 5d = MICBIAS internal load sink current is set to 21.5 mA (typ) 6d = MICBIAS internal load sink current is set to 25.8 mA (typ) 7d = MICBIAS internal load sink current is set to 30.1 mA (typ) Reserved	0x00 Description page页选择 page0x00选择00 page0x01选择01 0x16 0x00 Description Default	00000001 Setting 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0
	bit 77 6 6 5 5 4 4 3 3 2 5 4 4 3 3 2 2 1 1 0 0	00000000 default 0 0 0 0 0 0 0 0 0 0 0 0 0	Default Value: Definition These bits set the device page. 0d = Page 0 1d = Page 1 255d = Page 255 Address: Default Value: Definition MICBIAS internal load sink setting. 0d = MICBIAS internal load sink is enabled with setting automatically calculated based on device configuration 1d = MICBIAS internal load sink is enabled based on D6-4 register bits; This setting must be used for single-ended AC-coupled input to support high signal swing MICBIAS internal load sink current is set to 0 mA (typ) 1d = MICBIAS internal load sink current is set to 4.3 mA (typ) 2d = MICBIAS internal load sink current is set to 12.9 mA (typ) 3d = MICBIAS internal load sink current is set to 12.9 mA (typ) 4d = MICBIAS internal load sink current is set to 17.2 mA (typ) 5d = MICBIAS internal load sink current is set to 21.5 mA (typ) 6d = MICBIAS internal load sink current is set to 25.8 mA (typ) 7d = MICBIAS internal load sink current is set to 25.8 mA (typ) 7d = MICBIAS internal load sink current is set to 25.8 mA (typ)	Ox00 Description page页选择 page0x00选择00 page0x01选择01 Ox16 Ox00 Description Default Default	00000001 Setting 0 0 0 0 0 0 1 1 0x00 00000000 Setting 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
	bit 77 6 6 5 5 4 4 3 3 2 5 4 4 3 3 2 2 1 1 0 0	00000000 default 0 0 0 0 0 0 0 0 0 0 0 0 0	Default Value : Definition These bits set the device page. Od = Page 0 1d = Page 1	Ox00 Description page页选择 page0x00选择00 page0x01选择01 Ox16 Ox00 Description Default Default	00000001 Setting 0 0 0 0 0 0 1 1 0 0 0 0 0 0 0 0 0 0 0

7	15 1		
	Fault status for an ASI bus clock error. 0 0d = No fault detected 1d = Fault detected		0
6	Status of PLL lock. 0 0d = No PLL lock detected 1d = PLL lock detected		0
5	Fault status for boost or MICBIAS over temperature. 0 0d = No fault detected 1d = Fault detected		0
4	Fault status for boost or MICBIAS over current. 0 0d = No fault detected 1d = Fault detected		0
3	0 Reserved		0
2	0 Reserved		0
1	0 Reserved		0
0	0 Reserved		0
00101	101 Addres	s : 0x2D	0x00
00000			00000000
bit defau		Description	Setting
7	Status of CH1_LIVE. 0 0d = No faults occurred in channel 1 1d = Atleast a fault has occurred in channel 1		0
6	Status of CH2_LIVE. 0 0d = No faults occurred in channel 2 1d = Atleast a fault has occurred in channel 2		0
5	Status of CH3_LIVE. 0 0d = No faults occurred in channel 3 1d = Atleast a fault has occurred in channel 3		0
4	Status of CH4_LIVE. 0 0d = No faults occurred in channel 4 1d = Atleast a fault has occurred in channel 4		0
3	Status of CH5_LIVE. Applicable only for PCM6x60-Q1. 0 d = No faults occurred in channel 5 1d = Atleast a fault has occurred in channel 5		0
2	Status of CH6_LIVE. Applicable only for PCM6x60-Q1. 0 0d = No faults occurred in channel 6 1d = Atleast a fault has occurred in channel 6		0
1	Status of short to VBAT_IN fault detected when VBAT_IN is less than MICBIAS. 0 d = Short to VBAT_IN fault when VBAT_IN is less than MICBIAS has not occurred in any channel 1d = Short to VBAT_IN fault when VBAT_IN is less than MICBIAS has occurred in atleast one channel		0
0	0 Reserved		0
U	Nesel ved		0
00101		s: 0x2E	0x00
00000	000 Default Valu	e : 0x00	00000000
	000 Default Valu t Definition		
00000	t Definition Channel 1 open input fault status. 0 0d = No open input detected 1d = Open input detected	e : 0x00	00000000
00000 bit defau	t Definition Channel 1 open input fault status. 0 dd = No open input detected 1d = Open input detected Channel 1 input pair short fault status. 0 dd = No input pair short detected 1d = Input short fault status.	e : 0x00	00000000 Setting
bit defau	Default Valu t Definition Channel 1 open input fault status. 0 d = No open input detected 1d = Open input detected Channel 1 input pair short fault status. 0 dd = No input pair short feetected 1d = Input pair short to detected 1d = Input pair short to ground fault status. 0 dd = NI input pair short to ground fault status. 0 dd = INIP short to ground detected 1d = INIP short to ground detected	e : 0x00	00000000 Setting 0
000000 bit defau	t Definition Channel 1 open input fault status. 0 0d = No open input detected 1d = Open input detected Channel 1 input pair short fault status. 0 dd = No input pair short fault status. 0 dd = No input pair short detected 1d = Input short to each other detected Channel 1 IN1P short to ground fault status. 0 dd = IN1P no short to ground detected 1d = IN1P short to ground detected Channel 1 IN1M short to ground fault status. 0 dd = IN1M no short to ground detected 1d = IN1M no short to ground detected	e : 0x00	00000000 Setting 0
00000 bit defau 7 6	t Definition Channel 1 open input fault status. 0 0d = No open input detected 1d = Open input detected Channel 1 input pair short fault status. 0 0d = No input pair short detected 1d = Input short to each other detected Channel 1 INIP short to ground fault status. 0 0d = INIP no short to ground detected 1d = INIP short to ground detected 1d = ININ short to ground detected 1d = INIM short to ground detected Channel 1 INIM short to ground detected 1d = INIM short to ground detected 1d = INIM short to ground detected 1d = INIP short to MICBIAS fault status. 0 0d = INIP no short to MICBIAS detected 1d = INIP short to MICBIAS detected 1d = INIP short to MICBIAS detected	e : 0x00	00000000 Setting 0 0 0
00000 bit defau 7 6	t Definition Channel 1 open input fault status. 0 dd = No open input detected 1d = Open input detected Channel 1 input pair short fault status. 0 dd = No input pair short detected 1d = Input pair short to ground fault status. 0 dd = IN1P short to ground fault status. 0 dd = IN1P short to ground detected 1d = IN1P short to ground detected 1d = IN1M short to ground fault status. 0 dd = IN1M no short to ground fault status. 0 dd = IN1M short to ground detected 1d = IN1M short to ground detected 1d = IN1P short to MICBIAS fault status. 0 dd = IN1P short to MICBIAS detected 1d = IN1P short to MICBIAS fault status. 0 dd = IN1M no short to MICBIAS fault status. 0 dd = IN1M short to MICBIAS detected 1d = IN1M short to MICBIAS fault status. 0 dd = IN1M no short to MICBIAS detected	e : 0x00	00000000 Setting 0 0 0
00000 bit defau 7 6 5	t Definition Channel 1 open input fault status. 0 dd = No open input detected 1d = Open input detected 2d = Open input detected 3d = Open input detected 3d = Open input detected 4d = Open input pair short fault status. 0 dd = No input pair short detected 2d = Input short to ground fault status. 0 da = INIP short to ground fault status. 0 da = INIP short to ground detected 2d = INIP short to ground detected 2d = INIP short to ground fault status. 0 dd = INIM no short to ground detected 2d = INIM short to ground detected 2d = INIM short to ground detected 3d = INIM short to MICBIAS fault status. 0 dd = INIP no short to MICBIAS fault status. 0 dd = INIP short to MICBIAS detected 2d = INIM short to MICBIAS detected 3d = INIM short to MICBIAS detected 4d = INIM short to MICBIAS INIM sult status. 0d = INIM short to MICBIAS INIM sult status. 0d = INIM short to MBAT_IN detected 4d = INIM short to VBAT_IN detected	e : 0x00	00000000 Setting 0 0 0 0 0
00000 bit defau 7 6 5 4	t Definition Channel 1 open input fault status. 0 dd = No open input detected 1d = Open input detected Channel 1 input pair short fault status. 0 dd = No input pair short fault status. 0 dd = No input pair short detected 1d = Input short to each other detected Channel 1 INIP short to ground fault status. 0 dd = INIP no short to ground detected 1d = INIP short to ground fault status. 0 dd = INIP short to ground fault status. 0 dd = INIM short to ground detected 1d = INIP short to MICBIAS fault status. 0 dd = INIP no short to MICBIAS detected 1d = INIP short to MICBIAS detected 1d = INIM short to MICBIAS fault status. 0 dd = INIM short to MICBIAS fault status. 0 dd = INIM short to MICBIAS detected 1d = INIM short to MICBIAS detected	e : 0x00	00000000 Setting 0 0 0 0 0 0
000000 defau 7 6 5 4 3 2	t Definition Channel 1 open input fault status. 0 dd = No open input detected 1d = Open input detected Channel 1 input pair short fault status. 0 dd = No input pair short detected 1d = Input short to each other detected Channel 1 INIP short to ground fault status. 0 dd = INIP no short to ground detected 1d = INIP short to ground detected Channel 1 INIM short to ground detected 1d = INIM short to ground detected Channel 1 INIM short to ground detected Channel 1 INIP short to MICBIAS fault status. 0 dd = INIP short to MICBIAS fault status. 0 dd = INIP no short to MICBIAS fault status. 0 dd = INIP short to MICBIAS fault status. 0 dd = INIP short to MICBIAS fault status. 0 dd = INIP short to MICBIAS fault status. 0 dd = INIP short to MICBIAS fault status. 0 dd = INIM short to MICBIAS fault status. 0 dd = INIM short to MICBIAS detected 1d = INIM short to MICBIAS detected 1d = INIM short to VBAT_IN detected 1d = INIP short to VBAT_IN detected 1d = INIP short to VBAT_IN fault status. 0 dd = INIP no short to VBAT_IN fault status. 0 dd = INIP short to VBAT_IN detected 1d = INIM short to VBAT_IN fault status.	e: 0x00 Description	00000000 Setting 0 0 0 0 0 0 0
000000 defau 7 6 5 4 3 2 1	t Definition Channel 1 open input fault status. 0 dd = No open input detected 1d = Open input detected Channel 1 input pair short fault status. 0 dd = No input pair short detected 1d = Input short to detected 1d = Input short to ground fault status. 0 dd = IN1P short to ground fault status. 0 dd = IN1P short to ground detected 1d = IN1P short to ground fault status. 0 dd = IN1N short to ground fault status. 0 dd = IN1M no short to ground fault status. 0 dd = IN1M no short to ground detected Channel 1 IN1P short to ground detected 1d = IN1M short to ground detected Channel 1 IN1P short to MICBIAS fault status. 0 dd = IN1P no short to MICBIAS fault status. 0 dd = IN1P no short to MICBIAS detected 1d = IN1P short to MICBIAS detected 1d = IN1M no short to MICBIAS detected 1d = IN1M no short to MICBIAS detected 1d = IN1M short to VBAT_IN detected 1d = IN1P short to VBAT_IN detected 1d = IN1M no short to VBAT_IN detected 1d = IN1M short to VBAT_IN detected	e: 0x00 Description s: 0x2F	00000000 Setting 0 0 0 0 0 0 0 0
000000 defau 7 6 5 4 3 2 1 0 00101	t Definition Channel 1 open input fault status. 0 dd = No open input detected 1d = Open input detected Channel 1 input pair short fault status. 0 dd = No input pair short fault status. 0 dd = No input pair short detected 1d = Input pair short to ground fault status. 0 dd = INIP short to ground fault status. 0 dd = INIP short to ground detected 1d = INIP short to ground detected 1d = INIM short to ground fault status. 0 dd = INIM no short to ground fault status. 0 dd = INIM short to ground detected Channel 1 INIM short to ground detected 1d = INIM short to ground detected 1d = INIM short to MICBIAS fault status. 0 dd = ININ short to MICBIAS fault status. 0 dd = ININ short to MICBIAS detected 1d = INIM short to MICBIAS detected 1d = INIP short to VBAT_IN detected 1d = INIP short to VBAT_IN detected 1d = INIP short to VBAT_IN detected 1d = INIM short to VBAT_IN detected	e: 0x00 Description s: 0x2F	00000000 Setting 0 0 0 0 0 0 0 0 0 0 0 0 0
00000 bit defau 7 6 5 4 3 2 1 0 00101 00000	t Definition Channel 1 open input fault status. 0 dd = No open input detected 1d = Open input detected Channel 1 input pair short fault status. 0 dd = No input pair short fault status. 0 dd = No input pair short detected 1d = Input pair short to ground fault status. 0 dd = INIP short to ground fault status. 0 dd = INIP short to ground detected 1d = INIP short to ground detected 1d = INIM short to ground fault status. 0 dd = INIM no short to ground fault status. 0 dd = INIM short to ground detected Channel 1 INIM short to ground detected 1d = INIM short to ground detected 1d = INIM short to MICBIAS fault status. 0 dd = ININ short to MICBIAS fault status. 0 dd = ININ short to MICBIAS detected 1d = INIM short to MICBIAS detected 1d = INIP short to VBAT_IN detected 1d = INIP short to VBAT_IN detected 1d = INIP short to VBAT_IN detected 1d = INIM short to VBAT_IN detected	e: 0x00 Description s: 0x2F e: 0x00	00000000 Setting 0 0 0 0 0 0 0 0 0 0 0 0 0
00000 bit defau 7 6 5 4 3 2 1 0 00101 00000 bit defau	t Definition Channel 1 open input fault status. 0 dd = No open input detected Channel 1 input pair short fault status. 0 dd = No input pair short detected Channel 1 linput pair short detected dd = Input short to detected Channel 1 linput short to ground fault status. 0 dd = Iniput short to ground fault status. 0 dd = Iniput short to ground detected Channel 1 liniput short to ground fault status. 0 dd = Iniput short to ground detected Channel 1 liniput short to ground detected Channel 1 liniput short to ground detected Channel 1 liniput short to MicBiAS fault status. 0 dd = Iniput short to MicBiAS fault status. 0 dd = Iniput short to MicBiAS detected Channel 1 liniput short to MicBiAS detected Channel 1 liniput short to MicBiAS detected d = Iniput short to MicBiAS detected 1 d = Iniput short to MicBiAS detected 1 d = Iniput short to VBAT_In detected Channel 1 liniput short to VBAT_In detected Channel 1 linimut short to VBAT_In detected 1 d = Inimut short to VBAT_In detected Channel 1 linimut short to VBAT_In detected Channel 1 linimut short to VBAT_In detected Channel 1 linimut short to VBAT_In detected Channel 2 open input fault status. 0 dd = Inimut short to VBAT_In detected	e: 0x00 Description s: 0x2F e: 0x00	00000000 Setting 0 0 0 0 0 0 0 0 0 0 Setting
00000 bit defau 7 6 5 4 3 2 1 0 00101 00000 bit defau 7	t Definition Channel 1 open input fault status. 0 dd = No open input detected 1d = Open input detected 2d = No input pair short fault status. 0 dd = No input pair short detected 1d = Input short to each other detected 2d = Input short to ground fault status. 0 dd = IN1P short to ground fault status. 0 dd = IN1P short to ground detected 2d = IN1P short to ground detected 2d = IN1P short to ground detected 2d = IN1M short to ground detected 2d = IN1M short to ground detected 2d = IN1M short to ground detected 3d = IN1M short to ground detected 4d = IN1M short to MICBIAS fault status. 0 dd = IN1M short to MICBIAS detected 1d = IN1M short to MICBIAS detected 1d = IN1M short to MICBIAS detected 2d = IN1M short to WBAT_IN fault status. 0 dd = IN1P short to VBAT_IN detected 2d = IN1P short to VBAT_IN detected 2d = IN1M short to VBAT_IN detected 3d = IN	e: 0x00 Description s: 0x2F e: 0x00	00000000 Setting 0 0 0 0 0 0 0 0 0 0 0 0 0

3	0	Channel 2 IN2P short to MICBIAS fault status. 0d = IN2P no short to MICBIAS detected 1d = IN2P short to MICBIAS detected		0
2	0	Channel 2 IN2M short to MICBIAS fault status. 0d = IN2M no short to MICBIAS detected 1d = IN2M short to MICBIAS detected		0
1	0	10 = INZM SHOT tO MICBIAS detected Channel 2 IN2P short to VBAT_IN fault status. 0d = IN2P no short to VBAT_IN detected 1d = IN2P short to VBAT_IN detected		0
0	0	Channel 2 IN2M short to VBAT_IN fault status. 0d = IN2M no short to VBAT_IN detected 1d = IN2M short to VBAT_IN detected		0
	00110000	A	ddress: 0x30	0x00
	00000000		Value : 0x00	00000000
bit	default	Definition Channel 3 open input fault status.	Description	Setting
7	0	0d = No open input detected 1d = Open input detected		0
6	0	Channel 3 input pair short fault status. 0d = No input pair short detected 1d = Input short to each other detected		0
5	0	Channel 3 IN3P short to ground fault status. 0d = IN3P no short to ground detected 1d = IN3P short to ground detected		0
4	0	Channel 3 IN3M short to ground fault status. 0d = IN3M no short to ground detected 1d = IN3M short to ground detected		0
3	0	Channel 3 IN3P short to MICBIAS fault status. 0d = IN3P no short to MICBIAS detected 1d = IN3P short to MICBIAS detected		0
2	0	Channel 3 IN3M short to MICBIAS fault status. 0d = IN3M no short to MICBIAS detected 1d = IN3M short to MICBIAS detected		0
1	0	Channel 3 IN3P short to VBAT_IN fault status. 0d = IN3P no short to VBAT_IN detected 1d = IN3P short to VBAT_IN detected		0
0	0	Channel 3 IN3M short to VBAT_IN fault status. 0d = IN3M no short to VBAT_IN detected 1d = IN3M short to VBAT_IN detected		0
	00110001	Δ	ddress: 0x31	0x00
	00000000		: Value : 0x00	00000000
bit	default	Definition	Description	Setting
7	0	Channel 4 open input fault status. 0d = No open input detected 1d = Open input detected		0
6	0	Channel 4 input pair short fault status. 0d = No input pair short detected 1d = Input short to each other detected		0
5		Channel 4 IN4P short to ground fault status.		
	0	of all mer 4 may 1 stort to ground fault status. 0d = IN4P no short to ground detected 1d = IN4P short to ground detected		0
4		0d = IN4P no short to ground detected		0
3	0	0d = IN4P no short to ground detected 1d = IN4P short to ground detected Channel 4 IN4M short to ground fault status. 0d = IN4M no short to ground detected		
	0	0d = IN4P no short to ground detected 1d = IN4P short to ground detected Channel 4 IN4M short to ground fault status. 0d = IN4M no short to ground detected 1d = IN4M short to ground detected Channel 4 IN4P short to MICBIAS fault status. 0d = IN4P no short to MICBIAS detected		0
3	0	0d = IN4P no short to ground detected 1d = IN4P short to ground detected Channel 4 IN4M short to ground fault status. 0d = IN4M no short to ground detected 1d = IN4M short to ground detected Channel 4 IN4P short to MICBIAS fault status. 0d = IN4P no short to MICBIAS detected 1d = IN4P short to MICBIAS detected 1d = IN4P short to MICBIAS detected 0d = IN4P no short to MICBIAS fault status. 0d = IN4M no short to MICBIAS detected		0
3	0 0	0d = IN4P no short to ground detected 1d = IN4P short to ground detected 1d = IN4P short to ground detected 1d = IN4M short to ground fault status. 0d = IN4M no short to ground detected 1d = IN4M short to ground detected 1d = IN4P short to MICBIAS fault status. 0d = IN4P no short to MICBIAS detected 1d = IN4P short to MICBIAS detected 1d = IN4M short to MICBIAS fault status. 0d = IN4M no short to MICBIAS detected 1d = IN4M short to MICBIAS detected		0 0
2 1	0 0 0	0d = IN4P no short to ground detected 1d = IN4P short to ground detected 1d = IN4P short to ground detected 1d = IN4M short to ground fault status. 0d = IN4M no short to ground detected 1d = IN4M short to ground detected 1d = IN4M short to ground detected 1d = IN4P no short to MICBIAS fault status. 0d = IN4P no short to MICBIAS detected 1d = IN4P short to MICBIAS detected 1d = IN4M short to MICBIAS fault status. 0d = IN4M no short to MICBIAS detected 1d = IN4M short to MICBIAS detected 1d = IN4M short to MICBIAS detected 1d = IN4M short to VBAT_IN detected 1d = IN4P short to VBAT_IN detected 1d = IN4P short to VBAT_IN fault status. 0d = IN4P short to VBAT_IN fault status. 0d = IN4M no short to VBAT_IN fault status. 0d = IN4M no short to VBAT_IN fault status. 0d = IN4M no short to VBAT_IN detected 1d = IN4M short to VBAT_IN detected	ddress · 0v32	0 0 0
2 1 0	0 0	0d = IN4P no short to ground detected 1d = IN4P short to ground detected Channel 4 IN4M short to ground detected 0d = IN4M no short to ground detected 1d = IN4M short to ground detected 1d = IN4M short to ground detected Channel 4 IN4P short to MICBIAS fault status. 0d = IN4P no short to MICBIAS detected 1d = IN4P short to MICBIAS detected Channel 4 IN4M short to MICBIAS fault status. 0d = IN4M no short to MICBIAS fault status. 0d = IN4M no short to MICBIAS detected 1d = IN4M short to MICBIAS detected Channel 4 IN4P short to VBAT_IN detected 1d = IN4P short to VBAT_IN detected 1d = IN4P short to VBAT_IN fault status. 0d = IN4P short to VBAT_IN fault status. 0d = IN4M short to VBAT_IN fault status. 0d = IN4M short to VBAT_IN detected 1d = IN4M short to VBAT_IN detected	ddress: 0x32 2 Value: 0x00	0 0 0
3 2 1 0	0 0 0 0	0d = IN4P no short to ground detected 1d = IN4P short to ground detected Channel 4 IN4M short to ground fault status. 0d = IN4M no short to ground detected 1d = IN4M short to ground detected 1d = IN4M short to ground detected Channel 4 IN4P short to MICBIAS fault status. 0d = IN4P no short to MICBIAS detected 1d = IN4P short to MICBIAS detected 1d = IN4P short to MICBIAS detected 1d = IN4M short to MICBIAS detected 1d = IN4M short to MICBIAS detected 1d = IN4M short to MICBIAS detected Channel 4 IN4P short to VBAT_IN fault status. 0d = IN4P no short to VBAT_IN fault status. 0d = IN4P no short to VBAT_IN detected 1d = IN4P short to VBAT_IN detected 1d = IN4M short to VBAT_IN fault status. 0d = IN4M no short to VBAT_IN detected 1d = IN4M short to VBAT_IN detected		0 0 0 0
3 2 1	0 0 0 0 0 00110010 000000000 default	0d = IN4P no short to ground detected 1d = IN4P short to ground detected Channel 4 IN4M short to ground dault status. 0d = IN4M no short to ground detected 1d = IN4M short to ground detected 1d = IN4M short to ground detected Channel 4 IN4P short to MICBIAS fault status. 0d = IN4P no short to MICBIAS detected 1d = IN4P short to MICBIAS detected Channel 4 IN4M short to MICBIAS fault status. 0d = IN4M no short to MICBIAS detected 1d = IN4M short to MICBIAS detected 1d = IN4M short to MICBIAS letected Channel 4 IN4P short to VBAT_IN fault status. 0d = IN4P no short to VBAT_IN detected 1d = IN4P short to VBAT_IN detected 1d = IN4P short to VBAT_IN fault status. 0d = IN4M short to VBAT_IN detected 1d = IN4M short to VBAT_IN detected	Value : 0x00	0 0 0 0 0
3 2 1 0 bit	0 0 0 0 0 00110010 00000000 default	0d = IN4P no short to ground detected 1d = IN4P short to ground detected Channel 4 IN4M short to ground detected 0d = IN4M short to ground detected 1d = IN4M short to ground detected 1d = IN4M short to ground detected 1d = IN4M short to ground detected Channel 4 IN4P short to MICBIAS fault status. 0d = IN4P no short to MICBIAS detected 1d = IN4P short to MICBIAS detected 1d = IN4M short to MICBIAS detected 1d = IN4M short to MICBIAS detected 1d = IN4M short to MICBIAS detected Channel 4 IN4P short to VBAT_IN fault status. 0d = IN4P no short to VBAT_IN fault status. 0d = IN4P short to VBAT_IN detected 1d = IN4P short to VBAT_IN detected Channel 4 IN4M short to VBAT_IN fault status. 0d = IN4M no short to VBAT_IN detected 1d = IN4M short to VBAT_IN detected	Value : 0x00	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
3 2 1 0 0 bit 7	0 0 0 0 0 00110010 00000000 default	0d = IN4P no short to ground detected 1d = IN4P short to ground detected Channel 4 IN4M short to ground detected 0d = IN4M no short to ground detected 1d = IN4M short to ground detected 1d = IN4M short to ground detected 1d = IN4M short to ground detected Channel 4 IN4P short to MICBIAS fault status. 0d = IN4P no short to MICBIAS detected 1d = IN4M short to MICBIAS fault status. 0d = IN4M no short to MICBIAS fault status. 0d = IN4M no short to MICBIAS fault status. 0d = IN4M short to MICBIAS detected 1d = IN4M short to VBAT_IN fault status. 0d = IN4P no short to VBAT_IN detected 1d = IN4P short to VBAT_IN detected 1d = IN4M short to VBAT_IN fault status. 0d = IN4M no short to VBAT_IN fault status. 0d = IN4M no short to VBAT_IN detected 1d = IN4M short to VBAT_IN detected 1d = IN5M short to VBAT_IN detected	Value : 0x00	0 0 0 0 0 0 0 0 0 0 0 Setting
3 2 1 0 bit 7 6	0 0 0 0 0 000110010 00000000 default 0	0d = IN4P no short to ground detected 1d = IN4P short to ground detected Channel 4 IN4M short to ground detected 0d = IN4M no short to ground detected 1d = IN4M short to ground detected 1d = IN4M short to ground detected Channel 4 IN4P short to MICBIAS fault status. 0d = IN4P no short to MICBIAS detected 1d = IN4P short to MICBIAS detected Channel 4 IN4M short to MICBIAS fault status. 0d = IN4M no short to MICBIAS fault status. 0d = IN4M short to MICBIAS detected 1d = IN4M short to MICBIAS detected 1d = IN4M short to VBAT_IN fault status. 0d = IN4P no short to VBAT_IN detected 1d = IN4M short to VBAT_IN detected 1d = IN4M short to VBAT_IN fault status. 0d = IN4M no short to VBAT_IN fault status. 0d = IN4M short to VBAT_IN detected 1d = IN4M short to VBAT_IN detected	Value : 0x00	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
3 2 1 0 bit 7 6	0 0 0 0 0 0 00110010 00000000 default 0	Od = IN4P no short to ground detected 1d = IN4P short to ground detected 1d = IN4P short to ground detected 1d = IN4P short to ground detected 1d = IN4M short to ground detected 1d = IN4M short to ground detected 1d = IN4M short to ground detected 1d = IN4P short to MICBIAS fault status. 0d = IN4P no short to MICBIAS detected 1d = IN4P short to MICBIAS detected 1d = IN4M short to MICBIAS detected 1d = IN4M no short to MICBIAS detected 1d = IN4M short to MICBIAS detected 1d = IN4M short to VBAT_IN fault status. 0d = IN4P no short to VBAT_IN fault status. 0d = IN4P no short to VBAT_IN detected 1d = IN4M short to VBAT_IN detected 1d = IN4M short to VBAT_IN fault status. 0d = IN4M no short to VBAT_IN detected 1d = IN4M short to VBAT_IN detected 1d = IN5M short to VBAT_IN detected 1d = IN5M short to VBAT_IN detected 1d = IN5M short to ground fault status. 0d = No input pair short fault status. 0d = No input pair short to ground fault status. 0d = IN5P short to ground detected 1d = IN5P short to ground detected	Value : 0x00	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

1	0	Channel 5 IN5P short to VBAT_IN fault status. 0d = IN5P no short to VBAT_IN detected 1d = IN5P short to VBAT_IN detected		0
0	0	Channel 5 IN5M short to VBAT_IN fault status. 0d = IN5M no short to VBAT_IN detected 1d = IN5M short to VBAT_IN detected		0
	00110011	Address :	0^33	0x00
	00000000	Address : Default Value :		00000000
bit	default	Definition	Description	Setting
7	0	Channel 6 open input fault status. 0d = No open input detected 1d = Open input detected		0
6	0	Channel 6 input pair short fault status. 0d = No input pair short detected 1d = Input short to each other detected		0
5	0	Channel 6 IN6P short to ground fault status. 0d = IN6P no short to ground detected 1d = IN6P short to ground detected		0
4	0	Channel 6 IN6M short to ground fault status. 0d = IN6M no short to ground detected 1d = IN6M short to ground detected		0
3	0	Channel 6 IN6P short to MICBIAS fault status. 0d = IN6P no short to MICBIAS detected 1d = IN6P short to MICBIAS detected		0
2	0	Channel 6 IN6M short to MICBIAS fault status. 0d = IN6M no short to MICBIAS detected 1d = IN6M short to MICBIAS detected		0
1	0	Channel 6 IN6P short to VBAT_IN fault status. 0d = IN6P no short to VBAT_IN detected 1d = IN6P short to VBAT_IN detected		0
0	0	Channel 6 IN6M short to VBAT_IN fault status. 0d = IN6M no short to VBAT_IN detected 1d = IN6M short to VBAT_IN detected		0
-	00110101	Address: Default Value:	0x35 0x00	0x00 00000000
bit	default	Definition Definition	Description	Setting
7	0	Channel 1 IN1P over voltage fault status. 0d = No IN1P over voltage fault detected 1d = IN1P over voltage fault has detected		0
6	0	Channel 2 IN2P over voltage fault status. 0d = No IN2P over voltage fault detected 1d = IN2P over voltage fault has detected		0
5	0	Channel 3 IN3P over voltage fault status. 0d = No IN3P over voltage fault detected 1d = IN3P over voltage fault has detected		0
4	0	Channel 4 IN4P over voltage fault status. 0d = No IN4P over voltage fault detected 1d = IN4P over voltage fault has detected		0
3	0	Channel 5 IN5P over voltage fault status. Applicable only for PCM6x60-Q1. 0d = No IN5P over voltage fault detected 1d = IN5P over voltage fault has detected		0
2	0	Channel 6 IN6P over voltage fault status. Applicable only for PCM6x60-Q1. 0d = No IN6P over voltage fault detected 1d = IN6P over voltage fault has detected		0
1 0	0	Reserved		0
	00110111	Address : Default Value :	0x37 0x00	0x00 00000000
bit	default	Definition Definition	Description	Setting
7		Fault status for MICBIAS high current. 0d = No fault detected 1d = Fault detected		0
6	0	Fault status for MICBIAS low current 0d = No fault detected 1d = Fault detected		0
5		Fault status for MICBIAS over voltage. 0d = No fault detected 1d = Fault detected		0
4	0			0
3 2		Reserved		0
1 0	0			0
	01010101	Address :		0x40
h:t	01000000	Default Value :		01000000
bit 7	default 0	Definition MICBIAS overvoltage fault detection threshold above MICBIAS programmed	Description	Setting 0
-		voltage. 0d = No threshold over programmed voltage		
6	1	1d = 10 mV (typ) threshold over programmed voltage 2d = 40 mV (typ) threshold over programmed voltage (default) 3d to 6d = Threshold value is set as per configuration with step size of 30mV	MICBIAS过压40mV阈值	1
5		(typ) 7d = 190 mV (typ) threshold over programmed voltage (default)		0
4	0		ı	0

3	l 0]	1	0
2	0	Reserved		0
0				0
	01011001	Address : Default Value :	0x59 0x00	0x00 00000000
bit	default	Definition	Description	Setting
7	0			0
5	0	reserved		0
3				0
2		Reserved		0
1	0			0
		Hold SAR data update during register readback.		
0	0	0b= Data update is not held, data register is continuously updated; this setting must be used when moving average is enabled for fault detection 1b= Data update is held, data register readback can be done	Default	0
		1b= Data update is held, data register readback can be done		
	01011010	Address :		0x00
la la	00000000	Default Value :	0x00	00000000
bit 7	default 0		Description	Setting 0
6				0
5 4				0
3				0
2				0
0				0
	01011011	A.1.1	Oven	0.00
	01011011	Address : Default Value :	0x5B 0x00	0x00 00000000
bit	default	Definition	Description	Setting
- 7 6	0			0
5				0
3				0
2				0
1				0
0	0			0
	01011100	Address :	0x5C	0x00
bit	00000000 default	Default Value :	0x00 Description	00000000 Setting
7	0		Description	0
6				0
<u>5</u>				0
3				0
2 1				0
0	0			0
	01011101	Address :	0x5D	0x01
	00000001	Default Value :	0x01	00000001
bit 7	default 0	Definition	Description	Setting 0
6				0
5				0
3				0
2	0	Channel ID value		0
<u>1</u> 0				0
	01011110	Address : Default Value :	0x5E 0x00	0x00 00000000
bit	default	Definition Definition	Description	Setting
7	0			0
<u>6</u> 5				0
4	0	Diagnostic SAR monitor data MSR byte		0
3 2				0
1	0			0
0	0			0
	01011111	Address :		0x00
h	00000000	Default Value :	0x00	00000000
bit 7	default 0	Definition	Description	Setting 0
6	0	Diagnostic SAR monitor data LSR nibble		0
5 4				0
3	0			0
2	0			0

01100000	Addr	ess: 0x60	0x00
00000000	Default Va		000000
default	Definition Definition	Description	Settir
7 (2 550 (p. 15)	0
6 (0
5 (
4 (ī		0
3 (0
2 (0
1 (0
0 0			0
01100001	Addr	ess : 0x61	0x03
00000011	Default Va		000000
default	Definition	Description	Settir
7 (2000 paori	0
6 (0
5 (0
4 (0
3 (0
2 (ī		0
1 1			1
0 1			1
			·
01100010	Addr	ess : 0x62	0x00
00000000	Default Va		000000
default	Definition	Description	Settir
7 (0
6 (0
5 (0
4 (- 1		0
3 (0
2 (0
1 (0
0 (0
01100011	Addı		0x04
00000100	Default Va		000002
default	Definition	Description	Settir
7 (0
6 (0
5 (1		0
4 (0
3 (0
2 1			1
	TCHAILIEI ID Value		
1 (0
0 0			
0 (DAVI · see	0
01100100	Addr		0 0 0x00
0 0 01100100 00000000	Addr Default Va	lue : 0x00	0 0 0x00 000000
0 01100100 00000000 default	Addr Default Va		0 0 0 000000 Settir
0 01100100 00000000 default 7 (Addr Default Va	lue : 0x00	0 0 0 000000 Settir 0
0 01100100 00000000 default 7 0	Addr Default Va Definition	lue : 0x00	0 0 0 000000 Settir 0 0
0 01100100 00000000 default 7 0 6 0 5 0	Addr Default Va Definition	lue : 0x00	0 0 0 000000 Settir 0 0
0 01100100 00000000 default 7 0	Addr Default Va	lue : 0x00	0 0 0 000000 Settir 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Addr Default Va Definition Diagnostic SAR monitor data MSB byte	lue : 0x00	0 0 000000 Settir 0 0 0
01100100 00000000 default 7 6 0 5 0 4 0 2 0 1	Addr Default Va Definition Diagnostic SAR monitor data MSB byte	lue : 0x00	0 0 000000 Settin 0 0 0
01100100 00000000 default 7 (6 (7) 5 (7) 4 (7) 3 (7)	Addr Default Va Definition Diagnostic SAR monitor data MSB byte	lue : 0x00	0 0 000000 Settir 0 0 0 0
01100100 00000000 default 7 6 (5 (4 (3 (2 (0 (Addr Default Va Definition Diagnostic SAR monitor data MSB byte	lue : 0x00 Description	0 0 000000 Settin 0 0 0 0 0 0
01100100 000000000 default 7 6 0 5 0 4 0 2 0 0 0	Addr Default Va Definition Diagnostic SAR monitor data MSB byte Addr	lue: 0x00 Description ess: 0x65	0 0 000000 Settir 0 0 0 0 0 0
01100100 000000000 default 7 6 6 4 4 0 0 01100101 00000101	Addr Definition Diagnostic SAR monitor data MSB byte Addr Default Va	lue : 0x00 Description ess : 0x65 lue : 0x05	0 0 0 000000 Settir 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Addr Definition Diagnostic SAR monitor data MSB byte Addr Default Va	lue: 0x00 Description ess: 0x65	0 0 000000 Settir 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Addr Definition Diagnostic SAR monitor data MSB byte Addr Default Va	lue : 0x00 Description ess : 0x65 lue : 0x05	0 0 0 000000 Settir 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Addr Default Va Definition Diagnostic SAR monitor data MSB byte Addr Default Va Definition	lue : 0x00 Description ess : 0x65 lue : 0x05	0 0 000000 Settin 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
01100100 000000000 default 7 6 0 3 01100101 0000101 0000101 default 7 6 0 0 01100101 00000101 default 7 6 6 0 0	Addr Default Va Definition Diagnostic SAR monitor data MSB byte Addr Default Va Definition Diagnostic SAR monitor data LSB nibble	lue : 0x00 Description ess : 0x65 lue : 0x05	0 0 0 0 000000 Settir 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
01100100 000000000 default 7 6 6 01 3 02 01100101 0000101 default 7 (6 6 01 01100101 00000101 default 7 (6 6 01 01 01 0000101 default 7 (6 6 01 01 01 01 01 01 01 01 01 01 01 01 01	Addr Default Va Definition Diagnostic SAR monitor data MSB byte Addr Default Va Definition Diagnostic SAR monitor data LSB nibble	lue : 0x00 Description ess : 0x65 lue : 0x05	0 0 0 000000 Settir 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
01100100 00000000 default 7 6 6 7 6 1 1 01100101 0000101 00000101 default 7 6 6 6 6 6 6 6 6 6 6 6 6 6 6 6 6 6 6	Addr Definition Diagnostic SAR monitor data MSB byte Addr Definition Addr Default Va	lue : 0x00 Description ess : 0x65 lue : 0x05	0 0 0 0000000 Settin 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Addr Definition Diagnostic SAR monitor data MSB byte Addr Definition Addr Definition Diagnostic SAR monitor data LSB nibble	lue : 0x00 Description ess : 0x65 lue : 0x05	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
01100100 000000000 default 7 6 01100101 5 4 00 01100101 00000101 default 7 6 0 0 01100101 0000101 default 7 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Addr Default Va Definition Diagnostic SAR monitor data MSB byte Addr Default Va Definition Diagnostic SAR monitor data LSB nibble Channel ID value	lue : 0x00 Description ess : 0x65 lue : 0x05	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Addr Default Va Definition Diagnostic SAR monitor data MSB byte Addr Default Va Definition Diagnostic SAR monitor data LSB nibble Channel ID value	lue : 0x00 Description ess : 0x65 lue : 0x05	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Addr Default Va Definition Diagnostic SAR monitor data MSB byte Addr Default Va Definition Diagnostic SAR monitor data LSB nibble Channel ID value	lue : 0x00 Description	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Addr Definition Diagnostic SAR monitor data MSB byte Addr Definition Diagnostic SAR monitor data LSB nibble Channel ID value Addr Addr Addr Addr Addr Addr Addr Ad	lue: 0x00 Description ess: 0x65 lue: 0x05 Description ess: 0x66	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
01100100 00000000 default 7 6 01100101 5 00 01100101 00000101 default 7 6 0 01100101 000000000000000000000000	Addr Definition Diagnostic SAR monitor data MSB byte Addr Definition Addr Default Va Definition Diagnostic SAR monitor data LSB nibble Channel ID value Addr Default Va	lue : 0x00 Description ess : 0x65 lue : 0x05 Description ess : 0x66 lue : 0x00	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
01100100 00000000 default 7 6 (0100100 3 (01100101 00000101 default 7 (01100101 0000101 default 7 (01100101 0000101 0000101 default 7 (01100101 0000101 0000101 0000101 0000101 0000101 0000101 0000101 0000101 0000101	Addr Definition Diagnostic SAR monitor data MSB byte Addr Definition Diagnostic SAR monitor data LSB nibble Channel ID value Addr Default Va	lue: 0x00 Description ess: 0x65 lue: 0x05 Description ess: 0x66	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
01100100 00000000 default 7 6 01 3 01100101 00000101 default 7 6 0 01100101 00000101 default 7 6 0 0 0 01100101 00000000 default	Addr Definition Diagnostic SAR monitor data MSB byte Addr Definition Diagnostic SAR monitor data LSB nibble Channel ID value Addr Default Va	lue : 0x00 Description ess : 0x65 lue : 0x05 Description ess : 0x66 lue : 0x00	0
01100100 00000000 default 7 6 0100100 3 00000000 default 7 6 00 00000000 000000000 default 7 000000000 default 7 000000000 default 7 001100110 000000000 default 7	Addr Default Va Definition Diagnostic SAR monitor data MSB byte Addr Default Va Definition Diagnostic SAR monitor data LSB nibble Channel ID value Addr Default Va Definition	lue : 0x00 Description ess : 0x65 lue : 0x05 Description ess : 0x66 lue : 0x00	0
01100100 00000000 default 7 6 6 01 3 01100101 00000101 default 7 6 6 0 01100101 00000101 default 7 1 0 0 0 01100101 000000000 default 7 1 0 0 010011000100 00000000000000000	Addr Default Va Definition Diagnostic SAR monitor data MSB byte Addr Default Va Definition Diagnostic SAR monitor data LSB nibble Channel ID value Addr Default Va Definition	lue : 0x00 Description ess : 0x65 lue : 0x05 Description ess : 0x66 lue : 0x00	0
0 01100100 00000000 01100101 01100101 00000000	Addr Default Ve Definition Diagnostic SAR monitor data MSB byte Addr Default Va Definition Diagnostic SAR monitor data LSB nibble Channel ID value Addr Default Va Definition	lue : 0x00 Description ess : 0x65 lue : 0x05 Description ess : 0x66 lue : 0x00	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
01100100 00000000 default 7 6 0 01100101 00000101 default 7 6 0 01100101 00000101 default 7 6 0 0 01100101 00000000 default 7 01100110 00000000 default 7 6 0 01100110	Addr Default Ve Definition Diagnostic SAR monitor data MSB byte Addr Default Va Definition Diagnostic SAR monitor data LSB nibble Channel ID value Addr Default Va Definition Addr Default Va Definition Diagnostic SAR monitor data LSB nibble	lue : 0x00 Description ess : 0x65 lue : 0x05 Description ess : 0x66 lue : 0x00	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
01100100 00000000 default 7 6 0100101 7 6 01100101 00000101 default 7 6 0 01100101 00000101 default 7 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Addr Default Va Definition Diagnostic SAR monitor data MSB byte Addr Default Va Definition Diagnostic SAR monitor data LSB nibble Channel ID value Addr Default Va Definition Addr Default Va Definition	lue : 0x00 Description ess : 0x65 lue : 0x05 Description ess : 0x66 lue : 0x00	O
01100100 000000000 default 7 6 01100101 7 6 10100101 00000101 default 7 10 01100101 00000101 default 7 10 01100110 00000000 default 7 10 01100110 000000000000000000000000	Addr Definition Diagnostic SAR monitor data MSB byte Addr Definition Diagnostic SAR monitor data LSB nibble Channel ID value Addr Default Value	lue : 0x00 Description ess : 0x65 lue : 0x05 Description ess : 0x66 lue : 0x00	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
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<u>6</u> 5				0
4				0
3 2				0
1	1			1
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	01101000	Address :		0x00
bit	00000000 default	Default Value : Definition	0x00 Description	00000000 Setting
7	0		Description	0
<u>6</u> 5				0
4				0
3	0			0
2 1	0			0
0	0			0
	01101001	Address :	0x69	0x07
	00000111	Default Value :		00000111
bit 7	default 0	Definition	Description	Setting 0
6	0	Diagnostic SAR monitor data LSB nibble		0
<u>5</u>				0
3	0			0
2 1	1	Channel ID value		1
0				1
	01101010	Address :	0.60	0x00
	00000000	Default Value :		00000000
bit	default	Definition	Description	Setting
- 7 6	0			0
5	0			0
3				0
2	0			0
<u>1</u> 0	0			0
	01101011 00001000	Address: Default Value:	0x6B 0x08	0x08 00001000
bit	default	Definition Definition	Description	Setting
	0			0
5				0
3				0
2				0
1				0
0	0			0
	01101100 00000000	Address :		0x00 00000000
bit	default	Default Value : Definition	Description	Setting
7	0			0
<u>6</u> 5				0
4	0	Diagnostic SAR monitor data MSR byte		0
<u>3</u>				0
1	0			0
0	0			0
	01101101	Address :		0x09
bit	00001001 default	Default Value : Definition	0x09 Description	00001001 Setting
7	0			0
<u>6</u> 5				0
4	0			0
3				0
1	0			0
0	1			1
	01101110	Address :	0x6E	0x00
1.1.	00000000	Default Value :	0x00	00000000
bit 7	default 0	Definition	Description	Setting 0
6	0			0
5 4				0
3	0	Diagnostic SAR monitor data MSB byte		0
2	0			0
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5 (4 (3 (2 (Diagnostic SAR monitor data MSB byte		0 0 0 0 0 0
01110111	Address :		0x0E
00001110	Default Value :		00001110
bit default	Definition	Description	Setting
6 (5 (4 (Diagnostic SAR monitor data LSB nibble		0 0 0
2 1	Channel ID value		1 1 1 0
01111000	Address :	0x78	0x00
00000000	Default Value :		00000000
bit default	Definition	Description	Setting
6 6 6 6 6 6 6 6 6 6 6 6 6 6 6 6 6 6 6	Diagnostic SAR monitor data MSB byte		0 0 0 0 0 0 0
01111001	Address :	0v70	0x0F
00001111	Address : Default Value :		00001111
bit default	Definition Definition	Description	Setting
7 (6 (5 (Diagnostic SAR monitor data LSR nibble	2000,pt.0.1	0 0 0
	Channel ID value		1 1 1 1