page 0x00

| | 00000000 | Address : 0x00 | | 0x00 |
|---|---|---|---|---|
| | 00000000 | Default Value : 0x00 | | 00000000 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | These bits set the device page.<br>0d = Page 0<br>1d = Page 1<br>...<br>255d = Page 255 | page页选择<br>page0x00选择00<br>page0x01选择01 | 0 |
| 6 | 0 | | | 0 |
| 5 | 0 | | | 0 |
| 4 | 0 | | | 0 |
| 3 | 0 | | | 0 |
| 2 | 0 | | | 0 |
| 1 | 0 | | | 0 |
| 0 | 0 | | | 0 |

| | 00000001 | Address : 0x01 | | 0x00 |
|---|---|---|---|---|
| | 00000000 | Default Value : 0x00 | | 00000000 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | Reserved | | 0 |
| 6 | 0 | | | 0 |
| 5 | 0 | | | 0 |
| 4 | 0 | | | 0 |
| 3 | 0 | | | 0 |
| 2 | 0 | | | 0 |
| 1 | 0 | | | 0 |
| 0 | 0 | Software reset. This bit is self-clearing.<br>0d = Do not reset<br>1d = Reset | not reset | 0 |

| | 00000010 | Address : 0x02 | | 0x01 |
|---|---|---|---|---|
| | 00000000 | Default Value : 0x00 | | 00000001 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | Reserved | | 0 |
| 6 | 0 | Reserved | | 0 |
| 5 | 0 | | | 0 |
| 4 | 0 | The duration of the quick-charge for the VREF external capacitor is set using an internal series impedance of 200 Ω.<br>0d = VREF quick-charge duration of 3.5 ms (typical)<br>1d = VREF quick-charge duration of 10 ms (typical)<br>2d = VREF quick-charge duration of 50 ms (typical)<br>3d = VREF quick-charge duration of 100 ms (typical) | VREF decoupling 1uF对应延迟时间3.5ms | 0 |
| 3 | 0 | | | 0 |
| 2 | 0 | I2C broadcast addressing setting.<br>0d = I2C broadcast mode disabled; the I2C slave address is determined based on the ADDR pins<br>1d = I2C broadcast mode enabled; the I2C slave address is fixed at 1001 100 | I2C地址根据pin选择 | 0 |
| 1 | 0 | Reserved | | 0 |
| 0 | 0 | Sleep mode setting.<br>0d = Device is in sleep mode<br>1d = Device is not in sleep mode | 不进入sleep模式 | 1 |

| | 00000101 | Address : 0x05 | | 0x05 |
|---|---|---|---|---|
| | 00000101 | Default Value : 0x05 | | 00000101 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | Reserved | | 0 |
| 6 | 0 | | | 0 |
| 5 | 0 | | | 0 |
| 4 | 0 | | | 0 |
| 3 | 0 | Shutdown configuration.<br>0d = DREG is powered down immediately after SHDNZ asserts<br>1d = DREG remains active to enable a clean shut down until a time-out is reached; after the time-out period, DREG is forced to power off<br>2d = DREG remains active until the device cleanly shuts down<br>3d = Reserved | 掉电设置（default） | 0 |
| 2 | 1 | | | 1 |
| 1 | 0 | These bits set how long DREG remains active after SHDNZ asserts.<br>0d = DREG remains active for 30 ms (typical)<br>1d = DREG remains active for 25 ms (typical)<br>2d = DREG remains active for 10 ms (typical)<br>3d = DREG remains active for 5 ms (typical) | Remain active 25ms（default） | 0 |
| 0 | 1 | | | 1 |

| | 00000111 | Address : 0x07 | | 0x04 |
|---|---|---|---|---|
| | 00110000 | Default Value : 0x30 | | 00000100 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | ASI protocol format.<br>0d = TDM mode<br>1d = I2S mode<br>2d = LJ (left-justified) mode<br>3d = Reserved | TDM | 0 |
| 6 | 0 | | | 0 |
| 5 | 1 | ASI word or slot length.<br>0d = 16 bits<br>1d = 20 bits<br>2d = 24 bits<br>3d = 32 bits | 16bits | 0 |
| 4 | 1 | | | 0 |
| 3 | 0 | ASI FSYNC polarity.<br>0d = Default polarity as per standard protocol<br>1d = Inverted polarity with respect to standard protocol | Default polarity standard protocol | 0 |

| | | | | |
|---|---|---|---|---|
| 2 | 0 | ASI BCLK polarity.<br>0d = Default polarity as per standard protocol<br>1d = Inverted polarity with respect to standard protocol | Inverted polarity with respect to standard protocol | 1 |
| 1 | 0 | ASI data output (on the primary and secondary data pin) transmit edge.<br>0d = Default edge as per the protocol configuration setting in bit 2 (BCLK_POL)<br>1d = Inverted following edge (half cycle delay) with respect to the default edge setting | used as default | 0 |
| 0 | 0 | ASI data output (on the primary and secondary data pin) for any unused cycles<br>0d = Always transmit 0 for unused cycles<br>1d = Always use Hi-Z for unused cycles | used as default | 0 |

| | 00001000 | Address : 0x08 | | 0x01 |
|---|---|---|---|---|
| | 00000000 | Default Value : 0x00 | | 00000001 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | ASI data output (on the primary and secondary data pin) for LSB transmissions.<br>0d = Transmit the LSB for a full cycle<br>1d = Transmit the LSB for the first half cycle and Hi-Z for the second half cycle | used as default | 0 |
| 6 | 0 | ASI data output (on the primary and secondary data pin) bus keeper.<br>0d = Bus keeper is always disabled<br>1d = Bus keeper is always enabled<br>2d = Bus keeper is enabled during LSB transmissions only for one cycle<br>3d = Bus keeper is enabled during LSB transmissions only for one and half cycles | used as default | 0 |
| 5 | 0 | | | 0 |
| 4 | 0 | ASI data MSB slot 0 offset (on the primary and secondary data pin).<br>0d = ASI data MSB location has no offset and is as per standard protocol<br>1d = ASI data MSB location (TDM mode is slot 0 or I2S, LJ mode is the left and right slot 0) offset of one BCLK cycle with respect to standard protocol<br>2d = ASI data MSB location (TDM mode is slot 0 or I2S, LJ mode is the left and right slot 0) offset of two BCLK cycles with respect to standard protocol<br>3d to 30d = ASI data MSB location (TDM mode is slot 0 or I2S, LJ mode is the left and right slot 0) offset assigned as per configuration<br>31d = ASI data MSB location (TDM mode is slot 0 or I2S, LJ mode is the left and right slot 0) offset of 31 BCLK cycles with respect to standard protocol | offset=1 | 0 |
| 3 | 0 | | | 0 |
| 2 | 0 | | | 0 |
| 1 | 0 | | | 0 |
| 0 | 0 | | | 1 |

| | 00001001 | Address : 0x09 | | 0x00 |
|---|---|---|---|---|
| | 00000000 | Default Value : 0x00 | | 00000000 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | ASI daisy chain connection.<br>0d = All devices are connected in the common ASI bus<br>1d = All devices are daisy-chained for the ASI bus | 不采用菊花链方式 | 0 |
| 6 | 0 | Reserved | | 0 |
| 5 | 0 | ASI bus error detection.<br>0d = Enable bus error detection<br>1d = Disable bus error detection | used as default | 0 |
| 4 | 0 | ASI bus error auto resume.<br>0d = Enable auto resume after bus error recovery<br>1d = Disable auto resume after bus error recovery and remain powered down until the host configures the device | used as default | 0 |
| 3 | 0 | Reserved | | 0 |
| 2 | 0 | | | 0 |
| 1 | 0 | | | 0 |
| 0 | 0 | | | 0 |

| | 00001011 | Address : 0x0B | | 0x00 |
|---|---|---|---|---|
| | 00000000 | Default Value : 0x00 | | 00000000 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | Reserved | | 0 |
| 6 | 0 | Channel 1 output line.<br>0d = Channel 1 output is on the ASI primary output pin (SDOUT)<br>1d = Channel 1 output is on the ASI secondary output pin (GPIO1 or GPOx) | 通过SDOUT输出 | 0 |
| 5 | 0 | Channel 1 slot assignment.<br>0d = TDM is slot 0 or I2S, LJ is left slot 0<br>1d = TDM is slot 1 or I2S, LJ is left slot 1<br>2d to 30d = Slot assigned as per configuration<br>31d = TDM is slot 31 or I2S, LJ is left slot 31<br>32d = TDM is slot 32 or I2S, LJ is right slot 0<br>33d = TDM is slot 33 or I2S, LJ is right slot 1<br>34d to 62d = Slot assigned as per configuration<br>63d = TDM is slot 63 or I2S, LJ is right slot 31 | ch1=slot0 | 0 |
| 4 | 0 | | | 0 |
| 3 | 0 | | | 0 |
| 2 | 0 | | | 0 |
| 1 | 0 | | | 0 |
| 0 | 0 | | | 0 |

| | 00001100 | Address : 0x0C | | 0x02 |
|---|---|---|---|---|
| | 00000001 | Default Value : 0x01 | | 00000010 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | Reserved | | 0 |
| 6 | 0 | Channel 2 output line.<br>0d = Channel 2 output is on the ASI primary output pin (SDOUT)<br>1d = Channel 2 output is on the ASI secondary output pin (GPIO1 or GPOx) | 通过SDOUT输出 | 0 |
| 5 | 0 | Channel 2 slot assignment.<br>0d = TDM is slot 0 or I2S, LJ is left slot 0<br>1d = TDM is slot 1 or I2S, LJ is left slot 1<br>2d to 30d = Slot assigned as per configuration<br>31d = TDM is slot 31 or I2S, LJ is left slot 31<br>32d = TDM is slot 32 or I2S, LJ is right slot 0<br>33d = TDM is slot 33 or I2S, LJ is right slot 1 | ch2=slot2 | 0 |
| 4 | 0 | | | 0 |
| 3 | 0 | | | 0 |
| 2 | 0 | | | 0 |

| | | | | |
|---|---|---|---|---|
| 1 | 0 | 33d = TDM is slot 33 or I2S, LJ is right slot 1<br>34d to 62d = Slot assigned as per configuration<br>63d = TDM is slot 63 or I2S, LJ is right slot 31 | | 1 |
| 0 | 1 | | | 0 |

| | 00001101 | Address : 0x0D | | 0x04 |
|---|---|---|---|---|
| | 00000010 | Default Value : 0x02 | | 00000100 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | Reserved | | 0 |
| 6 | 0 | Channel 3 output line.<br>0d = Channel 3 output is on the ASI primary output pin (SDOUT)<br>1d = Channel 3 output is on the ASI secondary output pin (GPIO1 or GPOx) | 通过SDOUT输出 | 0 |
| 5 | 0 | Channel 3 slot assignment.<br>0d = TDM is slot 0 or I2S, LJ is left slot 0<br>1d = TDM is slot 1 or I2S, LJ is left slot 1<br>2d to 30d = Slot assigned as per configuration<br>31d = TDM is slot 31 or I2S, LJ is left slot 31<br>32d = TDM is slot 32 or I2S, LJ is right slot 0<br>33d = TDM is slot 33 or I2S, LJ is right slot 1<br>34d to 62d = Slot assigned as per configuration<br>63d = TDM is slot 63 or I2S, LJ is right slot 31 | ch3=slot4 | 0 |
| 4 | 0 | | | 0 |
| 3 | 0 | | | 0 |
| 2 | 0 | | | 1 |
| 1 | 1 | | | 0 |
| 0 | 0 | | | 0 |

| | 00001110 | Address : 0x0E | | 0x06 |
|---|---|---|---|---|
| | 00000011 | Default Value : 0x03 | | 00000110 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | Reserved | | 0 |
| 6 | 0 | Channel 4 output line.<br>0d = Channel 4 output is on the ASI primary output pin (SDOUT)<br>1d = Channel 4 output is on the ASI secondary output pin (GPIO1 or GPOx) | 通过SDOUT输出 | 0 |
| 5 | 0 | Channel 4 slot assignment.<br>0d = TDM is slot 0 or I2S, LJ is left slot 0<br>1d = TDM is slot 1 or I2S, LJ is left slot 1<br>2d to 30d = Slot assigned as per configuration<br>31d = TDM is slot 31 or I2S, LJ is left slot 31<br>32d = TDM is slot 32 or I2S, LJ is right slot 0<br>33d = TDM is slot 33 or I2S, LJ is right slot 1<br>34d to 62d = Slot assigned as per configuration<br>63d = TDM is slot 63 or I2S, LJ is right slot 31 | ch4=slot6 | 0 |
| 4 | 0 | | | 0 |
| 3 | 0 | | | 0 |
| 2 | 0 | | | 1 |
| 1 | 1 | | | 1 |
| 0 | 1 | | | 0 |

| | 00001111 | Address : 0x0F | | 0x08 |
|---|---|---|---|---|
| | 00000100 | Default Value : 0x04 | | 00001000 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | Reserved | | 0 |
| 6 | 0 | Channel 5 output line.<br>0d = Channel 5 output is on the ASI primary output pin (SDOUT)<br>1d = Channel 5 output is on the ASI secondary output pin (GPIO1 or GPOx) | 通过SDOUT输出 | 0 |
| 5 | 0 | Channel 5 slot assignment.<br>0d = TDM is slot 0 or I2S, LJ is left slot 0<br>1d = TDM is slot 1 or I2S, LJ is left slot 1<br>2d to 30d = Slot assigned as per configuration<br>31d = TDM is slot 31 or I2S, LJ is left slot 31<br>32d = TDM is slot 32 or I2S, LJ is right slot 0<br>33d = TDM is slot 33 or I2S, LJ is right slot 1<br>34d to 62d = Slot assigned as per configuration<br>63d = TDM is slot 63 or I2S, LJ is right slot 31 | ch5=slot8 | 0 |
| 4 | 0 | | | 0 |
| 3 | 0 | | | 1 |
| 2 | 1 | | | 0 |
| 1 | 0 | | | 0 |
| 0 | 0 | | | 0 |

| | 00010000 | Address : 0x10 | | 0x0A |
|---|---|---|---|---|
| | 00000101 | Default Value : 0x05 | | 00001010 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | Reserved | | 0 |
| 6 | 0 | Channel 6 output line.<br>0d = Channel 6 output is on the ASI primary output pin (SDOUT)<br>1d = Channel 6 output is on the ASI secondary output pin (GPIO1 or GPOx) | 通过SDOUT输出 | 0 |
| 5 | 0 | Channel 6 slot assignment.<br>0d = TDM is slot 0 or I2S, LJ is left slot 0<br>1d = TDM is slot 1 or I2S, LJ is left slot 1<br>2d to 30d = Slot assigned as per configuration<br>31d = TDM is slot 31 or I2S, LJ is left slot 31<br>32d = TDM is slot 32 or I2S, LJ is right slot 0<br>33d = TDM is slot 33 or I2S, LJ is right slot 1<br>34d to 62d = Slot assigned as per configuration<br>63d = TDM is slot 63 or I2S, LJ is right slot 31 | ch6=slot10 | 0 |
| 4 | 0 | | | 0 |
| 3 | 0 | | | 1 |
| 2 | 1 | | | 0 |
| 1 | 0 | | | 1 |
| 0 | 1 | | | 0 |

| | 00010011 | Address : 0x13 | | 0x02 |
|---|---|---|---|---|
| | 00000010 | Default Value : 0x02 | | 00000010 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | ASI master or slave configuration register setting.<br>0d = Device is in slave mode (both BCLK and FSYNC are inputs to the device)<br>1d = Device is in master mode (both BCLK and FSYNC are generated from the device) | slave mode<br>X9U(AK7738)做主，ADC做从 | 0 |
| 6 | 0 | Automatic clock configuration setting.<br>0d = Auto clock configuration is enabled (all internal clock divider and PLL configurations are auto derived)<br>1d = Auto clock configuration is disabled (custom mode and device GUI must be used for the device configuration settings) | 自动时钟配置 | 0 |

| | | | | |
|---|---|---|---|---|
| 5 | 0 | Automatic mode PLL setting.<br>0d = PLL is enabled in auto clock configuration<br>1d = PLL is disabled in auto clock configuration | PLL自动启用 | 0 |
| 4 | 0 | BCLK and FSYNC clock gate (valid when the device is in master mode).<br>0d = Do not gate BCLK and FSYNC<br>1d = Force gate BCLK and FSYNC when being transmitted from the device in master mode | slave mode 设定无效 | 0 |
| 3 | 0 | Sample rate setting (valid when the device is in master mode).<br>0d = fS is a multiple (or submultiple) of 48 kHz<br>1d = fS is a multiple (or submultiple) of 44.1 kHz | slave mode 设定无效 | 0 |
| 2 | 0 | These bits select the MCLK (GPIO or GPIx) frequency for the PLL source clock input (valid when the device is in master mode and MCLK_FREQ_SEL_MODE = 0).<br>0d = 12 MHz<br>1d = 12.288 MHz<br>2d = 13 MHz<br>3d = 16 MHz<br>4d = 19.2 MHz<br>5d = 19.68 MHz<br>6d = 24 MHz<br>7d = 24.576 MHz | slave mode 设定无效 | 0 |
| 1 | 1 | | | 1 |
| 0 | 0 | | | 0 |

| | 00010100 | Address : 0x14 | | 0x48 |
|---|---|---|---|---|
| | 01001000 | Default Value : 0x48 | | 01001000 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | Programmed sample rate of the ASI bus (not used when the device is configured in slave mode auto clock configuration).<br>0d = 7.35 kHz or 8 kHz<br>1d = 14.7 kHz or 16 kHz<br>2d = 22.05 kHz or 24 kHz<br>3d = 29.4 kHz or 32 kHz<br>4d = 44.1 kHz or 48 kHz<br>5d = 88.2 kHz or 96 kHz<br>6d = 176.4 kHz or 192 kHz<br>7d = 352.8 kHz or 384 kHz<br>8d = 705.6 kHz or 768 kHz<br>9d to 15d = Reserved | slave mode auto clock 设定无效 | 0 |
| 6 | 1 | | | 1 |
| 5 | 0 | | | 0 |
| 4 | 0 | | | 0 |
| 3 | 1 | Programmed BCLK to FSYNC frequency ratio of the ASI bus (not used when the device is configured in slave mode auto clock configuration).<br>0d = Ratio of 16<br>1d = Ratio of 24<br>2d = Ratio of 32<br>3d = Ratio of 48<br>4d = Ratio of 64<br>5d = Ratio of 96<br>6d = Ratio of 128<br>7d = Ratio of 192<br>8d = Ratio of 256<br>9d = Ratio of 384<br>10d = Ratio of 512<br>11d = Ratio of 1024<br>12d = Ratio of 2048<br>13d = Reserved<br>14d = Ratio of 144<br>15d = Reserved | slave mode auto clock 设定无效 | 1 |
| 2 | 0 | | | 0 |
| 1 | 0 | | | 0 |
| 0 | 0 | | | 0 |

| | 00010101 | Address : 0x15 | | 0xFF |
|---|---|---|---|---|
| | 11111111 | Default Value : 0xFF | | 11111111 |
| bit | default | Definition | Description | Setting |
| 7 | 1 | Detected sample rate of the ASI bus.<br>0d = 7.35 kHz or 8 kHz<br>1d = 14.7 kHz or 16 kHz<br>2d = 22.05 kHz or 24 kHz<br>3d = 29.4 kHz or 32 kHz<br>4d = 44.1 kHz or 48 kHz<br>5d = 88.2 kHz or 96 kHz<br>6d = 176.4 kHz or 192 kHz<br>7d = 352.8 kHz or 384 kHz<br>8d = 705.6 kHz or 768 kHz<br>9d to 14d = Reserved<br>15d = Invalid sample rate | read only | 1 |
| 6 | 1 | | | 1 |
| 5 | 1 | | | 1 |
| 4 | 1 | | | 1 |
| 3 | 1 | Detected BCLK to FSYNC frequency ratio of the ASI bus.<br>0d = Ratio of 16<br>1d = Ratio of 24<br>2d = Ratio of 32<br>3d = Ratio of 48<br>4d = Ratio of 64<br>5d = Ratio of 96<br>6d = Ratio of 128<br>7d = Ratio of 192<br>8d = Ratio of 256<br>9d = Ratio of 384<br>10d = Ratio of 512<br>11d = Ratio of 1024<br>12d = Ratio of 2048 | read only | 1 |
| 2 | 1 | | | 1 |
| 1 | 1 | | | 1 |

| | | | | |
|---|---|---|---|---|
| 0 | 1 | 13d = Reserved<br>14d = Ratio of 144<br>15d = Invalid ratio | | 1 |

| | 00010110 | Address : 0x16 | | 0x08 |
|---|---|---|---|---|
| | 00010000 | Default Value : 0x10 | | 00001000 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | Audio root clock source setting when the device is configured with the PLL disabled in the auto clock configuration for slave mode (AUTO_MODE_PLL_DIS = 1).<br>0d = BCLK is used as the audio root clock source<br>1d = MCLK (GPIOx or GPIx) is used as the audio root clock source (the MCLK to FSYNC ratio is as per MCLK_RATIO_SEL setting) | AUTO_MODE_PLL_DIS = 0，此设定无效 | 0 |
| 6 | 0 | Master mode MCLK (GPIOx or GPIx) frequency selection mode (valid when the device is in auto clock configuration).<br>0d = MCLK frequency is based on the MCLK_FREQ_SEL (P0_R19)configuration<br>1d = MCLK frequency is specified as a multiple of FSYNC in the MCLK_RATIO_SEL (P0_R22) configuration | slave mode，设定无效 | 0 |
| 5 | 0 | These bits select the MCLK (GPIOx or GPIx) to FSYNC ratio for master mode or when MCLK is used as the audio root clock source in slave mode.<br>0d = Ratio of 64 | | 0 |
| 4 | 1 | 1d = Ratio of 256<br>2d = Ratio of 384<br>3d = Ratio of 512<br>4d = Ratio of 768 | slave mode and MCLK is used as the audio root clock source in slave mode.设定无效 | 0 |
| 3 | 0 | 5d = Ratio of 1024<br>6d = Ratio of 1536<br>7d = Ratio of 2304 | | 1 |
| 2 | 0 | | | 0 |
| 1 | 0 | Reserved | | 0 |
| 0 | 0 | | | 0 |

| | 00100001 | Address : 0x21 | | 0x02 |
|---|---|---|---|---|
| | 00100010 | Default Value : 0x22 | | 00000010 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | GPIO1 configuration.<br>0d = GPIO1 is disabled<br>1d = GPIO1 is configured as a general-purpose output (GPO)<br>2d = GPIO1 is configured as a device interrupt output (IRQ)<br>3d = GPIO1 is configured as a secondary ASI output (SDOUT2)<br>4d = Reserved<br>5d = Reserved<br>6d = Reserved<br>7d = GPIO1 is configured as an input to power down all ADC channels<br>8d = GPIO1 is configured as an input to control when MICBIAS turns on or off (MICBIAS_EN)<br>9d = GPIO1 is configured as a general-purpose input (GPI)<br>10d = GPIO1 is configured as a master clock input (MCLK)<br>11d = GPIO1 is configured as an ASI input for daisy-chain (SDIN)<br>12d = Reserved<br>13d = Reserved<br>14d = Reserved | GPIO1未使用 | 0 |
| 6 | 0 | | | 0 |
| 5 | 1 | | | 0 |
| 4 | 0 | | | 0 |
| 3 | 0 | Reserved | | 0 |
| 2 | 0 | GPIO1 output drive configuration (not used when GPIO1 is configured as SDOUT2).<br>0d = Hi-Z output<br>1d = Drive active low and active high<br>2d = Drive active low and weak high<br>3d = Drive active low and Hi-Z<br>4d = Drive weak low and active high<br>5d = Drive Hi-Z and active high<br>6d to 7d = Reserved | GPIO1未使用 | 0 |
| 1 | 1 | | | 1 |
| 0 | 0 | | | 0 |

| | 00100010 | Address : 0x22 | | 0x00 |
|---|---|---|---|---|
| | 00000000 | Default Value : 0x00 | | 00000000 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | GPIO2 configuration.<br>0d = GPIO2 is disabled<br>1d = GPIO2 is configured as a general-purpose output (GPO)<br>2d = GPIO2 is configured as a device interrupt output (IRQ)<br>3d = GPIO2 is configured as a secondary ASI output (SDOUT2)<br>4d = Reserved<br>5d = Reserved<br>6d = Reserved<br>7d = GPIO2 is configured as an input to power down all ADC channels<br>8d = GPIO2 is configured as an input to control when MICBIAS turns on or off (MICBIAS_EN)<br>9d = GPIO2 is configured as a general-purpose input (GPI)<br>10d = GPIO2 is configured as a master clock input (MCLK)<br>11d = GPIO2 is configured as an ASI input for daisy-chain (SDIN)<br>12d = Reserved<br>13d = Reserved<br>14d = Reserved | Not applicable for PCM6260-Q1. | 0 |
| 6 | 0 | | | 0 |
| 5 | 0 | | | 0 |
| 4 | 0 | | | 0 |
| 3 | 0 | Reserved | | 0 |

| | | | | |
|---|---|---|---|---|
| 2 | 0 | GPIO2 output drive configuration (not used when GPIO2 is configured as SDOUT2).<br>0d = Hi-Z output<br>1d = Drive active low and active high<br>2d = Drive active low and weak high<br>3d = Drive active low and Hi-Z<br>4d = Drive weak low and active high<br>5d = Drive Hi-Z and active high<br>6d to 7d = Reserved | Not applicable for PCM6260-Q1. | 0 |
| 1 | 0 | | | 0 |
| 0 | 0 | | | 0 |

| | 00100011 | Address : 0x23 | | 0x00 |
|---|---|---|---|---|
| | 00000000 | Default Value : 0x00 | | 00000000 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | GPIO3 configuration.<br>0d = GPIO3 is disabled<br>1d = GPIO3 is configured as a general-purpose output (GPO)<br>2d = GPIO3 is configured as a device interrupt output (IRQ)<br>3d = GPIO3 is configured as a secondary ASI output (SDOUT2)<br>4d = Reserved<br>5d = Reserved<br>6d = Reserved<br>7d = GPIO3 is configured as an input to power down all ADC channels<br>8d = GPIO3 is configured as an input to control when MICBIAS turns on or off (MICBIAS_EN)<br>9d = GPIO3 is configured as a general-purpose input (GPI)<br>10d = GPIO3 is configured as a master clock input (MCLK)<br>11d = GPIO3 is configured as an ASI input for daisy-chain (SDIN)<br>12d = Reserved<br>13d = Reserved<br>14d = Reserved | Not applicable for PCM6260-Q1. | 0 |
| 6 | 0 | | | 0 |
| 5 | 0 | | | 0 |
| 4 | 0 | | | 0 |
| 3 | 0 | Reserved | | 0 |
| 2 | 0 | GPIO3 output drive configuration (not used when GPIO3 is configured as SDOUT2).<br>0d = Hi-Z output<br>1d = Drive active low and active high<br>2d = Drive active low and weak high<br>3d = Drive active low and Hi-Z<br>4d = Drive weak low and active high<br>5d = Drive Hi-Z and active high<br>6d to 7d = Reserved | Not applicable for PCM6260-Q1. | 0 |
| 1 | 0 | | | 0 |
| 0 | 0 | | | 0 |

| | 00100100 | Address : 0x24 | | 0x00 |
|---|---|---|---|---|
| | 00000000 | Default Value : 0x00 | | 00000000 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | GPI1 configuration.<br>0d = GPI1 is disabled<br>1d to 6d = Reserved<br>7d = GPI1 is configured as an input to power down all ADC channels<br>8d = GPI1 is configured as an input to control when MICBIAS turns on or off (MICBIAS_EN)<br>9d = GPI1 is configured as a general-purpose input (GPI)<br>10d = GPI1 is configured as a master clock input (MCLK)<br>11d = GPI1 is configured as an ASI input for daisy-chain (SDIN)<br>12d = Reserved<br>13d = Reserved<br>14d = Reserved | Not applicable for PCM6260-Q1. | 0 |
| 6 | 0 | | | 0 |
| 5 | 0 | | | 0 |
| 4 | 0 | | | 0 |
| 3 | 0 | Reserved | | 0 |
| 2 | 0 | | | 0 |
| 1 | 0 | | | 0 |
| 0 | 0 | | | 0 |

| | 00100101 | Address : 0x25 | | 0x00 |
|---|---|---|---|---|
| | 00000000 | Default Value : 0x00 | | 00000000 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | GPI2 configuration.<br>0d = GPI2 is disabled<br>1d to 6d = Reserved<br>7d = GPI2 is configured as an input to power down all ADC channels<br>8d = GPI2 is configured as an input to control when MICBIAS turns on or off (MICBIAS_EN)<br>9d = GPI2 is configured as a general-purpose input (GPI)<br>10d = GPI2 is configured as a master clock input (MCLK)<br>11d = GPI2 is configured as an ASI input for daisy-chain (SDIN)<br>12d = Reserved<br>13d = Reserved<br>14d = Reserved | Not applicable for PCM6260-Q1. | 0 |
| 6 | 0 | | | 0 |
| 5 | 0 | | | 0 |
| 4 | 0 | | | 0 |
| 3 | 0 | Reserved | | 0 |
| 2 | 0 | | | 0 |
| 1 | 0 | | | 0 |
| 0 | 0 | | | 0 |

| | 00100110 | Address : 0x26 | | 0x00 |
|---|---|---|---|---|
| | 00000000 | Default Value : 0x00 | | 00000000 |
| bit | default | Definition | Description | Setting |

| | | | | |
|---|---|---|---|---|
| 7 | 0 | GPIO1 output value when configured as a GPO.<br>0d = Drive the output with a value of 0<br>1d = Drive the output with a value of 1 | GPIO1未使用 | 0 |
| 6 | 0 | GPIO2 output value when configured as a GPO. Not applicable for PCM6x60-Q1.<br>0d = Drive the output with a value of 0<br>1d = Drive the output with a value of 1 | Not applicable for PCM6260-Q1. | 0 |
| 5 | 0 | GPIO3 output value when configured as a GPO. Not applicable for PCM6x60-Q1.<br>0d = Drive the output with a value of 0<br>1d = Drive the output with a value of 1 | Not applicable for PCM6260-Q1. | 0 |
| 4 | 0 | Reserved | | 0 |
| 3 | 0 | | | 0 |
| 2 | 0 | | | 0 |
| 1 | 0 | | | 0 |
| 0 | 0 | | | 0 |

| | 00100111 | Address : 0x27 | | 0x00 |
|---|---|---|---|---|
| | 00000000 | Default Value : 0x00 | | 00000000 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | GPIO1 monitor value when configured as a GPI.<br>0d = Input monitor value 0<br>1d = Input monitor value 1 | | 0 |
| 6 | 0 | GPIO2 monitor value when configured as a GPI. Not applicable for PCM6x60-Q1.<br>0d = Input monitor value 0<br>1d = Input monitor value 1 | | 0 |
| 5 | 0 | GPIO3 monitor value when configured as a GPI. Not applicable for PCM6x60-Q1.<br>0d = Input monitor value 0<br>1d = Input monitor value 1 | | 0 |
| 4 | 0 | GPI1 monitor value when configured as a GPI. Not applicable for PCM6x60-Q1.<br>0d = Input monitor value 0<br>1d = Input monitor value 1 | | 0 |
| 3 | 0 | GPI2 monitor value when configured as a GPI. Not applicable for PCM6x60-Q1.<br>0d = Input monitor value 0<br>1d = Input monitor value 1 | | 0 |
| 2 | 0 | Reserved | | 0 |
| 1 | 0 | | | 0 |
| 0 | 0 | | | 0 |

| | 00101000 | Address : 0x28 | | **0x60** |
|---|---|---|---|---|
| | 00000000 | Default Value : 0x00 | | 01100000 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | Interrupt polarity.<br>0d = Active low (IRQZ)<br>1d = Active high (IRQ) | 中断低电平有效 | 0 |
| 6 | 0 | Interrupt event configuration.<br>0d = INT asserts on any unmasked latched interrupts event<br>1d = Reserved<br>2d = INT asserts for 2 ms (typical) for every 4-ms (typical) duration on any unmasked latched interrupts event<br>3d = INT asserts for 2 ms (typical) one time on each pulse for any unmasked interrupts event | 中断在每个pluse上都有2ms | **1** |
| 5 | 0 | | | **1** |
| 4 | 0 | Powerdown configuration when fault detected for any channel or MICBIAS fault detected.<br>0d = Faults event are not used for ADC and MICBIAS power down. It is recommend to set these bits as 2d to shutdown the blocks for which fault occurred.<br>1d = Only unmasked faults are used for power down of respective ADC channel; In case of MICBIAS fault detected, MICBIAS and all ADC channels gets powered-down based on P0_R58 settings<br>2d = Both masked or unmasked faults are used for power down of respective ADC channel; In case of MICBIAS fault detected, MICBIAS and all ADC channels gets powered-down based on P0_R58 settings.<br>3d = Reserved | 不使用PD模式 | 0 |
| 3 | 0 | | | 0 |
| 2 | 0 | Interrupt latch registers readback configuration.<br>0d = All interrupts can be read through the LTCH registers<br>1d = Only unmasked interrupts can be read through the LTCH registers | 所有中断都能通过LTCH寄存器读取 | 0 |
| 1 | 0 | Recovery configuration for ADC channels when fault goes away.<br>0d = Auto recovery, ADC channels are re-powered up when fault goes away<br>1d = Manual recovery, ADC channels are required to power-up manually using P0_R119 when fault goes away | 故障消失后自动复归 | 0 |
| 0 | 0 | Configuration for clearing LTCH register bits.<br>0d = LTCH register bits are cleared on register read only if live status is zero<br>1d = LTCH register bits are cleared on register read irrespective of live status and set only if live status goes again low to high | 只在读取时clear | 0 |

| | 00101001 | Address : 0x29 | | 0xFF |
|---|---|---|---|---|
| | 11111111 | Default Value : 0xFF | | 11111111 |
| bit | default | Definition | Description | Setting |
| 7 | 1 | ASI clock error mask.<br>0d = Unmask<br>1d = Mask | POC default setting | 1 |
| 6 | 1 | PLL lock interrupt mask.<br>0d = Unmask<br>1d = Mask | POC default setting | 1 |

| | | | | |
|---|---|---|---|---|
| 5 | 1 | Boost or MICBIAS over temperature interrupt mask.<br>0d = Unmask<br>1d = Mask | POC default setting | 1 |
| 4 | 1 | Boost or MICBIAS over current interrupt mask.<br>0d = Unmask<br>1d = Mask | POC default setting | 1 |
| 3 | 1 | Reserved | | 1 |
| 2 | 1 | Reserved | | 1 |
| 1 | 1 | Reserved | | 1 |
| 0 | 1 | Reserved | | 1 |

| | | | | |
|---|---|---|---|---|
| | 00101010 | Address : 0x2A | | 0x01 |
| | 00000011 | Default Value : 0x03 | | 00000001 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | Channel 1 input DC faults diagnostic interrupt mask.<br>0d = Unmask<br>1d = Mask | POC default setting | 0 |
| 6 | 0 | Channel 2 input DC faults diagnostic interrupt mask.<br>0d = Unmask<br>1d = Mask | POC default setting | 0 |
| 5 | 0 | Channel 3 input DC faults diagnostic interrupt mask.<br>0d = Unmask<br>1d = Mask | POC default setting | 0 |
| 4 | 0 | Channel 4 input DC faults diagnostic interrupt mask.<br>0d = Unmask<br>1d = Mask | POC default setting | 0 |
| 3 | 0 | Channel 5 input DC faults diagnostic interrupt mask. Applicable only for PCM6x60-Q1.<br>0d = Unmask<br>1d = Mask | POC default setting | 0 |
| 2 | 0 | Channel 6 input DC faults diagnostic interrupt mask. Applicable only for PCM6x60-Q1.<br>0d = Unmask<br>1d = Mask | POC default setting | 0 |
| 1 | 1 | Input faults diagnostic interrupt mask for "short to VBAT_IN" detect when VBAT_IN voltage is less than MICBIAS voltage.<br>0d = Unmask<br>1d = Mask | POC_ICC VBAT_IN未使用 | 0 |
| 0 | 1 | Reserved | | 1 |

| | | | | |
|---|---|---|---|---|
| | 00101011 | Address : 0x2B | | 0x00 |
| | 00000000 | Default Value : 0x00 | | 00000000 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | Input diagnostics; Open inputs fault interrupt mask.<br>0d = Unmask<br>1d = Mask | POC default setting | 0 |
| 6 | 0 | Input diagnostics; Inputs shorted fault interrupt mask.<br>0d = Unmask<br>1d = Mask | POC default setting | 0 |
| 5 | 0 | Input diagnostics; INxP shorted to ground fault interrupt mask.<br>0d = Unmask<br>1d = Mask | POC default setting | 0 |
| 4 | 0 | Input diagnostics; INxM shorted to ground fault interrupt mask.<br>0d = Unmask<br>1d = Mask | POC default setting | 0 |
| 3 | 0 | Input diagnostics; INxP shorted to MICBIAS fault interrupt mask.<br>0d = Unmask<br>1d = Mask | POC default setting | 0 |
| 2 | 0 | Input diagnostics; INxM shorted to MICBIAS fault interrupt mask.<br>0d = Unmask<br>1d = Mask | POC default setting | 0 |
| 1 | 0 | Input diagnostics; INxP shorted to VBAT_IN fault interrupt mask.<br>0d = Unmask<br>1d = Mask | POC default setting | 0 |
| 0 | 0 | Input diagnostics; INxM shorted to VBAT_IN fault interrupt mask.<br>0d = Unmask<br>1d = Mask | POC default setting | 0 |

| | | | | |
|---|---|---|---|---|
| | 00101100 | Address : 0x2C | | 0x00 |
| | 00000000 | Default Value : 0x00 | | 00000000 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | Fault status for an ASI bus clock error (self-clearing bit).<br>0d = No fault detected<br>1d = Fault detected | | 0 |
| 6 | 0 | Status of PLL lock (self-clearing bit).<br>0d = No PLL lock detected<br>1d = PLL lock detected | | 0 |
| 5 | 0 | Fault status for boost or MICBIAS over temperature (self-clearing bit).<br>0d = No fault detected<br>1d = Fault detected | | 0 |
| 4 | 0 | Fault status for boost or MICBIAS over current (self-clearing bit).<br>0d = No fault detected<br>1d = Fault detected | | 0 |
| 3 | 0 | Reserved | | 0 |
| 2 | 0 | Reserved | | 0 |
| 1 | 0 | Reserved | | 0 |
| 0 | 0 | Reserved | | 0 |

| | | | |
|---|---|---|---|
| | 00101101 | Address : 0x2D | 0x00 |
| | 00000000 | Default Value : 0x00 | 00000000 |

| bit | default | Definition | Description | Setting |
|---|---|---|---|---|
| 7 | 0 | Status of CH1_LTCH (self-clearing bit).<br>0d = No faults occurred in channel 1<br>1d = Atleast a fault has occurred in channel 1 | | 0 |
| 6 | 0 | Status of CH2_LTCH (self-clearing bit).<br>0d = No faults occurred in channel 2<br>1d = Atleast a fault has occurred in channel 2 | | 0 |
| 5 | 0 | Status of CH3_LTCH (self-clearing bit).<br>0d = No faults occurred in channel 3<br>1d = Atleast a fault has occurred in channel 3 | | 0 |
| 4 | 0 | Status of CH4_LTCH (self-clearing bit).<br>0d = No faults occurred in channel 4<br>1d = Atleast a fault has occurred in channel 4 | | 0 |
| 3 | 0 | Status of CH5_LTCH (self-clearing bit). Applicable only for PCM6x60-Q1.<br>0d = No faults occurred in channel 5<br>1d = Atleast a fault has occurred in channel 5 | | 0 |
| 2 | 0 | Status of CH6_LTCH (self-clearing bit). Applicable only for PCM6x60-Q1.<br>0d = No faults occurred in channel 6<br>1d = Atleast a fault has occurred in channel 6 | | 0 |
| 1 | 0 | Status of short to VBAT_IN fault detected when VBAT_IN is less than MICBIAS (self-clearing bit).<br>0d = Short to VBAT_IN fault when VBAT_IN is less than MICBIAS has not occurred in any channel<br>1d = Short to VBAT_IN fault when VBAT_IN is less than MICBIAS has occurred in atleast one channel | | 0 |
| 0 | 0 | Reserved | | 0 |

| | 00101110 | Address : 0x2E | | 0x00 |
|---|---|---|---|---|
| | 00000000 | Default Value : 0x00 | | 00000000 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | Channel 1 open input fault status (self-clearing bit).<br>0d = No open input detected<br>1d = Open input detected | | 0 |
| 6 | 0 | Channel 1 input pair short fault status (self-clearing bit).<br>0d = No input pair short detected<br>1d = Input short to each other detected | | 0 |
| 5 | 0 | Channel 1 IN1P short to ground fault status (self-clearing bit).<br>0d = IN1P no short to ground detected<br>1d = IN1P short to ground detected | | 0 |
| 4 | 0 | Channel 1 IN1M short to ground fault status (self-clearing bit).<br>0d = IN1M no short to ground detected<br>1d = IN1M short to ground detected | | 0 |
| 3 | 0 | Channel 1 IN1P short to MICBIAS fault status (self-clearing bit).<br>0d = IN1P no short to MICBIAS detected<br>1d = IN1P short to MICBIAS detected | | 0 |
| 2 | 0 | Channel 1 IN1M short to MICBIAS fault status (self-clearing bit).<br>0d = IN1M no short to MICBIAS detected<br>1d = IN1M short to MICBIAS detected | | 0 |
| 1 | 0 | Channel 1 IN1P short to VBAT_IN fault status (self-clearing bit).<br>0d = IN1P no short to VBAT_IN detected<br>1d = IN1P short to VBAT_IN detected | | 0 |
| 0 | 0 | Channel 1 IN1M short to VBAT_IN fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-54d, INT_LTCH2 register).<br>0d = IN1M no short to VBAT_IN detected<br>1d = IN1M short to VBAT_IN detected | | 0 |

| | 00101111 | Address : 0x2F | | 0x00 |
|---|---|---|---|---|
| | 00000000 | Default Value : 0x00 | | 00000000 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | Channel 2 open input fault status (self-clearing bit).<br>0d = No open input detected<br>1d = Open input detected | | 0 |
| 6 | 0 | Channel 2 input pair short fault status (self-clearing bit).<br>0d = No input pair short detected<br>1d = Input short to each other detected | | 0 |
| 5 | 0 | Channel 2 IN2P short to ground fault status (self-clearing bit).<br>0d = IN2P no short to ground detected<br>1d = IN2P short to ground detected | | 0 |
| 4 | 0 | Channel 2 IN2M short to ground fault status (self-clearing bit).<br>0d = IN2M no short to ground detected<br>1d = IN2M short to ground detected | | 0 |
| 3 | 0 | Channel 2 IN2P short to MICBIAS fault status (self-clearing bit).<br>0d = IN2P no short to MICBIAS detected<br>1d = IN2P short to MICBIAS detected | | 0 |
| 2 | 0 | Channel 2 IN2M short to MICBIAS fault status (self-clearing bit).<br>0d = IN2M no short to MICBIAS detected<br>1d = IN2M short to MICBIAS detected | | 0 |
| 1 | 0 | Channel 2 IN2P short to VBAT_IN fault status (self-clearing bit).<br>0d = IN2P no short to VBAT_IN detected<br>1d = IN2P short to VBAT_IN detected | | 0 |
| 0 | 0 | Channel 2 IN2M short to VBAT_IN fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-54d, INT_LTCH2 register).<br>0d = IN2M no short to VBAT_IN detected<br>1d = IN2M short to VBAT_IN detected | | 0 |

| | 00110000 | Address : 0x30 | | 0x00 |
|---|---|---|---|---|
| | 00000000 | Default Value : 0x00 | | 00000000 |
| bit | default | Definition | Description | Setting |

| | | | | |
|---|---|---|---|---|
| 7 | 0 | Channel 3 open input fault status (self-clearing bit).<br>0d = No open input detected<br>1d = Open input detected | | 0 |
| 6 | 0 | Channel 3 input pair short fault status (self-clearing bit).<br>0d = No input pair short detected<br>1d = Input short to each other detected | | 0 |
| 5 | 0 | Channel 3 IN3P short to ground fault status (self-clearing bit).<br>0d = IN3P no short to ground detected<br>1d = IN3P short to ground detected | | 0 |
| 4 | 0 | Channel 3 IN3M short to ground fault status (self-clearing bit).<br>0d = IN3M no short to ground detected<br>1d = IN3M short to ground detected | | 0 |
| 3 | 0 | Channel 3 IN3P short to MICBIAS fault status (self-clearing bit).<br>0d = IN3P no short to MICBIAS detected<br>1d = IN3P short to MICBIAS detected | | 0 |
| 2 | 0 | Channel 3 IN3M short to MICBIAS fault status (self-clearing bit).<br>0d = IN3M no short to MICBIAS detected<br>1d = IN3M short to MICBIAS detected | | 0 |
| 1 | 0 | Channel 3 IN3P short to VBAT_IN fault status (self-clearing bit).<br>0d = IN3P no short to VBAT_IN detected<br>1d = IN3P short to VBAT_IN detected | | 0 |
| 0 | 0 | Channel 3 IN3M short to VBAT_IN fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-54d, INT_LTCH2 register).<br>0d = IN3M no short to VBAT_IN detected<br>1d = IN3M short to VBAT_IN detected | | 0 |

| | 00110001 | Address : 0x31 | | 0x00 |
|---|---|---|---|---|
| | 00000000 | Default Value : 0x00 | | 00000000 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | Channel 4 open input fault status (self-clearing bit).<br>0d = No open input detected<br>1d = Open input detected | | 0 |
| 6 | 0 | Channel 4 input pair short fault status (self-clearing bit).<br>0d = No input pair short detected<br>1d = Input short to each other detected | | 0 |
| 5 | 0 | Channel 4 IN4P short to ground fault status (self-clearing bit).<br>0d = IN4P no short to ground detected<br>1d = IN4P short to ground detected | | 0 |
| 4 | 0 | Channel 4 IN4M short to ground fault status (self-clearing bit).<br>0d = IN4M no short to ground detected<br>1d = IN4M short to ground detected | | 0 |
| 3 | 0 | Channel 4 IN4P short to MICBIAS fault status (self-clearing bit).<br>0d = IN4P no short to MICBIAS detected<br>1d = IN4P short to MICBIAS detected | | 0 |
| 2 | 0 | Channel 4 IN4M short to MICBIAS fault status (self-clearing bit).<br>0d = IN4M no short to MICBIAS detected<br>1d = IN4M short to MICBIAS detected | | 0 |
| 1 | 0 | Channel 4 IN4P short to VBAT_IN fault status (self-clearing bit).<br>0d = IN4P no short to VBAT_IN detected<br>1d = IN4P short to VBAT_IN detected | | 0 |
| 0 | 0 | Channel 4 IN4M short to VBAT_IN fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-54d, INT_LTCH2 register).<br>0d = IN4M no short to VBAT_IN detected<br>1d = IN4M short to VBAT_IN detected | | 0 |

| | 00110010 | Address : 0x32 | | 0x00 |
|---|---|---|---|---|
| | 00000000 | Default Value : 0x00 | | 00000000 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | Channel 5 open input fault status (self-clearing bit).<br>0d = No open input detected<br>1d = Open input detected | | 0 |
| 6 | 0 | Channel 5 input pair short fault status (self-clearing bit).<br>0d = No input pair short detected<br>1d = Input short to each other detected | | 0 |
| 5 | 0 | Channel 5 IN5P short to ground fault status (self-clearing bit).<br>0d = IN5P no short to ground detected<br>1d = IN5P short to ground detected | | 0 |
| 4 | 0 | Channel 5 IN5M short to ground fault status (self-clearing bit).<br>0d = IN5M no short to ground detected<br>1d = IN5M short to ground detected | | 0 |
| 3 | 0 | Channel 5 IN5P short to MICBIAS fault status (self-clearing bit).<br>0d = IN5P no short to MICBIAS detected<br>1d = IN5P short to MICBIAS detected | | 0 |
| 2 | 0 | Channel 5 IN5M short to MICBIAS fault status (self-clearing bit).<br>0d = IN5M no short to MICBIAS detected<br>1d = IN5M short to MICBIAS detected | | 0 |
| 1 | 0 | Channel 5 IN5P short to VBAT_IN fault status (self-clearing bit).<br>0d = IN5P no short to VBAT_IN detected<br>1d = IN5P short to VBAT_IN detected | | 0 |
| 0 | 0 | Channel 5 IN5M short to VBAT_IN fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-54d, INT_LTCH2 register).<br>0d = IN5M no short to VBAT_IN detected<br>1d = IN5M short to VBAT_IN detected | | 0 |

| | 00110011 | Address : 0x33 | | 0x00 |
|---|---|---|---|---|
| | 00000000 | Default Value : 0x00 | | 00000000 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | Channel 6 open input fault status (self-clearing bit).<br>0d = No open input detected<br>1d = Open input detected | | 0 |

| | | | | |
|---|---|---|---|---|
| 6 | 0 | Channel 6 input pair short fault status (self-clearing bit).<br>0d = No input pair short detected<br>1d = Input short to each other detected | | 0 |
| 5 | 0 | Channel 6 IN6P short to ground fault status (self-clearing bit).<br>0d = IN6P no short to ground detected<br>1d = IN6P short to ground detected | | 0 |
| 4 | 0 | Channel 6 IN6M short to ground fault status (self-clearing bit).<br>0d = IN6M no short to ground detected<br>1d = IN6M short to ground detected | | 0 |
| 3 | 0 | Channel 6 IN6P short to MICBIAS fault status (self-clearing bit).<br>0d = IN6P no short to MICBIAS detected<br>1d = IN6P short to MICBIAS detected | | 0 |
| 2 | 0 | Channel 6 IN6M short to MICBIAS fault status (self-clearing bit).<br>0d = IN6M no short to MICBIAS detected<br>1d = IN6M short to MICBIAS detected | | 0 |
| 1 | 0 | Channel 6 IN6P short to VBAT_IN fault status (self-clearing bit).<br>0d = IN6P no short to VBAT_IN detected<br>1d = IN6P short to VBAT_IN detected | | 0 |
| 0 | 0 | Channel 6 IN6M short to VBAT_IN fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-54d, INT_LTCH2 register).<br>0d = IN6M no short to VBAT_IN detected<br>1d = IN6M short to VBAT_IN detected | | 0 |

| | 00110100 | Address : 0x34 | | 0x00 |
|---|---|---|---|---|
| | 00000000 | Default Value : 0x00 | | 00000000 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | INxP over voltage fault mask.<br>0d = Unmask<br>1d = Mask | POC default setting | 0 |
| 6 | 0 | INxM over voltage fault mask.<br>0d = Unmask<br>1d = Mask | POC default setting | 0 |
| 5 | 0 | MICBIAS high current fault mask.<br>0d = Unmask<br>1d = Mask | POC default setting | 0 |
| 4 | 0 | MICBIAS low current fault mask.<br>0d = Unmask<br>1d = Mask | POC default setting | 0 |
| 3 | 0 | MICBIAS over voltage fault mask.<br>0d = Unmask<br>1d = Mask | POC default setting | 0 |
| 2 | 0 | | | 0 |
| 1 | 0 | Reserved | | 0 |
| 0 | 0 | | | 0 |

| | 00110101 | Address : 0x35 | | 0x00 |
|---|---|---|---|---|
| | 00000000 | Default Value : 0x00 | | 00000000 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | Channel 1 IN1P over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-46d, CH1_LTCH register).<br>0d = No IN1P over voltage fault detected<br>1d = IN1P over voltage fault has detected | | 0 |
| 6 | 0 | Channel 2 IN2P over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-47d, CH2_LTCH register).<br>0d = No IN2P over voltage fault detected<br>1d = IN2P over voltage fault has detected | | 0 |
| 5 | 0 | Channel 3 IN3P over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-48d, CH3_LTCH register).<br>0d = No IN3P over voltage fault detected<br>1d = IN3P over voltage fault has detected | | 0 |
| 4 | 0 | Channel 4 IN4P over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-49d, CH4_LTCH register).<br>0d = No IN4P over voltage fault detected<br>1d = IN4P over voltage fault has detected | | 0 |
| 3 | 0 | Channel 5 IN5P over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-50d, CH5_LTCH register). Applicable only for PCM6x60-Q1.<br>0d = No IN5P over voltage fault detected<br>1d = IN5P over voltage fault has detected | | 0 |
| 2 | 0 | Channel 6 IN6P over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-51d, CH6_LTCH register). Applicable only for PCM6x60-Q1.<br>0d = No IN6P over voltage fault detected<br>1d = IN6P over voltage fault has detected | | 0 |
| 1 | 0 | Reserved | | 0 |
| 0 | 0 | | | 0 |

| | 00110110 | Address : 0x36 | | 0x00 |
|---|---|---|---|---|
| | 00000000 | Default Value : 0x00 | | 00000000 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | Channel 1 IN1M over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-46d, CH1_LTCH register).<br>0d = No IN1M over voltage fault detected<br>1d = IN1M over voltage fault has detected | | 0 |
| 6 | 0 | Channel 2 IN2M over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-47d, CH2_LTCH register).<br>0d = No IN2M over voltage fault detected<br>1d = IN2M over voltage fault has detected | | 0 |

| | | | | |
|---|---|---|---|---|
| 5 | 0 | Channel 3 IN3M over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-48d, CH3_LTCH register).<br>0d = No IN3M over voltage fault detected<br>1d = IN3M over voltage fault has detected | | 0 |
| 4 | 0 | Channel 4 IN4M over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-49d, CH4_LTCH register).<br>0d = No IN4M over voltage fault detected<br>1d = IN4M over voltage fault has detected | | 0 |
| 3 | 0 | Channel 5 IN5M over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-50d, CH5_LTCH register). Applicable only for PCM6x60-Q1.<br>0d = No IN5M over voltage fault detected<br>1d = IN5M over voltage fault has detected | | 0 |
| 2 | 0 | Channel 6 IN6M over voltage fault status (self-clearing bit - This bit gets clear on reading Page-0, Register-51d, CH6_LTCH register). Applicable only for PCM6x60-Q1.<br>0d = No IN6M over voltage fault detected<br>1d = IN6M over voltage fault has detected | | 0 |
| 1 | 0 | Reserved | | 0 |
| 0 | 0 | | | 0 |

| | 00110111 | Address : 0x37 | | 0x00 |
|---|---|---|---|---|
| | 00000000 | Default Value : 0x00 | | 00000000 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | Fault status for MICBIAS high current (self-clearing bit).<br>0d = No fault detected<br>1d = Fault detected | | 0 |
| 6 | 0 | Fault status for MICBIAS low current (self-clearing bit)<br>0d = No fault detected<br>1d = Fault detected | | 0 |
| 5 | 0 | Fault status for MICBIAS over voltage (self-clearing bit).<br>0d = No fault detected<br>1d = Fault detected | | 0 |
| 4 | 0 | Reserved | | 0 |
| 3 | 0 | | | 0 |
| 2 | 0 | | | 0 |
| 1 | 0 | | | 0 |
| 0 | 0 | | | 0 |

| | 00111000 | Address : 0x38 | | 0xBA |
|---|---|---|---|---|
| | 10111010 | Default Value : 0xBA | | 10111010 |
| bit | default | Definition | Description | Setting |
| 7 | 1 | Threshold for MICBIAS high load current fault diagnostic.<br>0d to 56d = Reserved<br>57d = High load current threshold is set as 0 mA (typ)<br>58d = High load current threshold is set as 0.54 mA (typ)<br>59d = High load current threshold is set as 1.08 mA (typ)<br>60d to 185d = High load current threshold is set as per configuration<br>186d = High load current threshold is set as 69.66 mA (typ)<br>187d to 241d = High load current threshold is set as per configuration<br>242d = High load current threshold is set as 99.90 mA (typ)<br>243d to 255d = Reserved | POC used as default | 1 |
| 6 | 0 | | | 0 |
| 5 | 1 | | | 1 |
| 4 | 1 | | | 1 |
| 3 | 1 | | | 1 |
| 2 | 0 | | | 0 |
| 1 | 1 | | | 1 |
| 0 | 0 | | | 0 |

| | 00111001 | Address : 0x39 | | 0x4B |
|---|---|---|---|---|
| | 01001011 | Default Value : 0x4B | | 01001011 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | Threshold for MICBIAS low load current fault diagnostic.<br>0d to 56d = Reserved<br>57d = Low load current threshold is set as 0 mA (typ)<br>58d = Low load current threshold is set as 0.54 mA (typ)<br>59d = Low load current threshold is set as 1.08 mA (typ)<br>60d to 74d = Low load current threshold is set as per configuration<br>75d = Low load current threshold is set as 9.72 mA (typ)<br>76d to 241d = Low load current threshold is set as per configuration<br>242d = Low load current threshold is set as 99.90 mA (typ)<br>243d to 255d = Reserved | POC used as default | 0 |
| 6 | 1 | | | 1 |
| 5 | 0 | | | 0 |
| 4 | 0 | | | 0 |
| 3 | 1 | | | 1 |
| 2 | 0 | | | 0 |
| 1 | 1 | | | 1 |
| 0 | 1 | | | 1 |

| | 00111010 | Address : 0x3A | | 0x00 |
|---|---|---|---|---|
| | 00010000 | Default Value : 0x10 | | 00000000 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | Powerdown configuration of MICBIAS fault 1<br>0d = No powerdown when MICBIAS fault detected<br>1d = MICBIAS and all ADC channels gets powerdown when low current fault occurs and P0_R40, PD_ON_FLT_CFG = 1d<br>1d = MICBIAS and all ADC channels gets powerdown when high current fault occurs and P0_R40, PD_ON_FLT_CFG = 2d | MICBIAS故障时不断电<br>PD_ON_FLT_CFG=0d | 0 |
| 6 | 0 | Powerdown configuration of MICBIAS fault 2<br>0d = No powerdown when MICBIAS fault detected<br>1d = MICBIAS and all ADC channels gets powerdown when over voltage fault occurs and P0_R40, PD_ON_FLT_CFG = 1d<br>1d = MICBIAS and all ADC channels gets powerdown when low current fault occurs and P0_R40, PD_ON_FLT_CFG = 2d | MICBIAS故障时不断电 | 0 |
| 5 | 0 | Powerdown configuration of MICBIAS fault 3<br>0d = No powerdown when MICBIAS fault detected<br>1d = MICBIAS and all ADC channels gets powerdown when over temperature fault occurs and P0_R40, PD_ON_FLT_CFG = 1d<br>1d = MICBIAS and all ADC channels gets powerdown when over voltage fault occurs and P0_R40, PD_ON_FLT_CFG = 2d | MICBIAS故障时不断电 | 0 |

| | | | | |
|---|---|---|---|---|
| 4 | 1 | Powerdown configuration of MICBIAS fault 4<br>0d = No powerdown when MICBIAS fault detected<br>1d = MICBIAS and all ADC channels gets powerdown when high current fault occurs and P0_R40, PD_ON_FLT_CFG = 1d<br>1d = MICBIAS and all ADC channels gets powerdown when over temperature fault occurs and P0_R40, PD_ON_FLT_CFG = 2d. It is recommended to use this setting to protect chip from over temperature fault. | MICBIAS故障时不断电 | **0** |
| 3 | 0 | Reserved | | 0 |
| 2 | 0 | Reserved | | 0 |
| 1 | 0 | | | 0 |
| 0 | 0 | | | 0 |

| | 00111011 | Address : 0x3B | | **0xF0** |
|---|---|---|---|---|
| | 11010000 | Default Value : 0xD0 | | 11110000 |
| bit | default | Definition | Description | Setting |
| 7 | 1 | MICBIAS value.<br>0d = Reserved<br>1d = Reserved<br>2d = Reserved<br>3d = Reserved<br>4d = Reserved<br>5d = Reserved<br>6d = Reserved<br>7d = Microphone bias is set to 5 V<br>8d = Microphone bias is set to 5.5 V<br>9d = Microphone bias is set to 6 V<br>10d = Microphone bias is set to 6.5 V<br>11d = Microphone bias is set to 7 V<br>12d = Microphone bias is set to 7.5 V<br>13d = Microphone bias is set to 8 V<br>14d = Microphone bias is set to 8.5 V<br>15d = Microphone bias is set to 9 V | ICC选定MIC模组供电电压7.2V~8V~8.8V<br>考虑线束最长6m，将偏置电压选择9V | 1 |
| 6 | 1 | | | 1 |
| 5 | 0 | | | **1** |
| 4 | 1 | | | 1 |
| 3 | 0 | Reserved | | 0 |
| 2 | 0 | | | 0 |
| 1 | 0 | Reserved | | 0 |
| 0 | 0 | | | 0 |

| | 00111100 | Address : 0x3C | | **0x38** |
|---|---|---|---|---|
| | 00010000 | Default Value : 0x10 | | 00111000 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | Channel 1 input type.<br>0d = Microphone input<br>1d = Line input | Microphone输入 | 0 |
| 6 | 0 | Channel 1 input configuration.<br>0d = Analog differential input<br>1d = Analog single-ended input<br>2d = Reserved<br>3d = Reserved | 单端输入 | 0 |
| 5 | 0 | | | **1** |
| 4 | 1 | Channel 1 input coupling.<br>0d = AC-coupled input<br>1d = DC-coupled input | DC耦合 | 1 |
| 3 | 0 | Channel 1 microphone input range.<br>0d = Low swing mode; Differential input AC signal full-scale of 2-VRMS supported provided DC differential common mode voltage IN1P - IN1M < 4.2 V. Single-ended AC signal 1-VRMS supported provided DC common mode voltage is < 2.1 V.<br>1d = High swing mode; Differential Input IN1P-IN1M peak voltage up to 14.14 V or single ended 7.07 V supported. User rquired to adjust the channel gain and digital volume control based on the max signal level used in system. | 入力范围大模式 | **1** |
| 2 | 0 | Channel 1 CMRR Configuration.<br>0d = High SNR performance mode<br>1d = Reserved<br>2d = High CMRR performance mode<br>3d = Reserved | Default | 0 |
| 1 | 0 | | | 0 |
| 0 | 0 | Channel 1 automatic gain controller (AGC) setting.<br>0d = AGC disabled<br>1d = AGC enabled based on the configuration of bit 3 in register 108 (P0_R108); This must be used only with AC-coupled input | 自动增益调节关闭 | 0 |

| | 00111101 | Address : 0x3D | | **0x20** |
|---|---|---|---|---|
| | 00000000 | Default Value : 0x00 | | 00100000 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | Channel 1 gain.<br>0d = Channel gain is set to 0 dB<br>1d = Channel gain is set to 1 dB<br>2d = Channel gain is set to 2 dB<br>3d to 41d = Channel gain is set as per configuration<br>42d = Channel gain is set to 42 dB<br>43d to 63d = Reserved | 串扰、采样值问题对策：8dB，后续根据需要调整 | 0 |
| 6 | 0 | | | 0 |
| 5 | 0 | | | **1** |
| 4 | 0 | | | 0 |
| 3 | 0 | | | 0 |
| 2 | 0 | | | 0 |
| 1 | 0 | Reserved | | 0 |
| 0 | 0 | Reserved | | 0 |

| | 00111110 | Address : 0x3E | | **0xDB** |
|---|---|---|---|---|
| | 11001001 | Default Value : 0xC9 | | 11011011 |
| bit | default | Definition | Description | Setting |
| 7 | 1 | | | 1 |

| | | | | |
|---|---|---|---|---|
| 6 | 1 | Channel 1 digital volume control.<br>0d = Digital volume is muted<br>1d = Digital volume control is set to -100 dB<br>2d = Digital volume control is set to -99.5 dB<br>3d to 200d = Digital volume control is set as per configuration<br>201d = Digital volume control is set to 0 dB<br>202d = Digital volume control is set to 0.5 dB<br>203d to 253d = Digital volume control is set as per configuration<br>254d = Digital volume control is set to 26.5 dB<br>255d = Digital volume control is set to 27 dB | 串扰、采样值问题对策：9dB，后续根据需要调整 | 1 |
| 5 | 0 | | | 0 |
| 4 | 0 | | | **1** |
| 3 | 1 | | | 1 |
| 2 | 0 | | | 0 |
| 1 | 0 | | | **1** |
| 0 | 1 | | | 1 |

| | 00111111 | Address : 0x3F | | 0x80 |
|---|---|---|---|---|
| | 10000000 | Default Value : 0x80 | | 10000000 |
| bit | default | Definition | Description | Setting |
| 7 | 1 | Channel 1 gain calibration.<br>0d = Gain calibration is set to -0.8 dB<br>1d = Gain calibration is set to -0.7 dB<br>2d = Gain calibration is set to -0.6 dB<br>3d to 7d = Gain calibration is set as per configuration<br>8d = Gain calibration is set to 0 dB<br>9d = Gain calibration is set to 0.1 dB<br>10d to 13d = Gain calibration is set as per configuration<br>14d = Gain calibration is set to 0.6 dB<br>15d = Gain calibration is set to 0.7 dB | Used as default first，后续根据需要调整 | 1 |
| 6 | 0 | | | 0 |
| 5 | 0 | | | 0 |
| 4 | 0 | | | 0 |
| 3 | 0 | Reserved | | 0 |
| 2 | 0 | | | 0 |
| 1 | 0 | | | 0 |
| 0 | 0 | | | 0 |

| | 01000000 | Address : 0x40 | | 0x00 |
|---|---|---|---|---|
| | 00000000 | Default Value : 0x00 | | 00000000 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | Channel 1 phase calibration with modulator clock resolution.<br>0d = No phase calibration<br>1d = Phase calibration delay is set to one cycle of the modulator clock<br>2d = Phase calibration delay is set to two cycles of the modulator clock<br>3d to 254d = Phase calibration delay as per configuration<br>255d = Phase calibration delay is set to 255 cycles of the modulator clock | Used as default first，后续根据需要调整 | 0 |
| 6 | 0 | | | 0 |
| 5 | 0 | | | 0 |
| 4 | 0 | | | 0 |
| 3 | 0 | | | 0 |
| 2 | 0 | | | 0 |
| 1 | 0 | | | 0 |
| 0 | 0 | | | 0 |

| | 01000001 | Address : 0x41 | | **0x38** |
|---|---|---|---|---|
| | 00010000 | Default Value : 0x10 | | 00111000 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | Channel 2 input type.<br>0d = Microphone input<br>1d = Line input | Microphone输入 | 0 |
| 6 | 0 | Channel 2 input configuration.<br>0d = Analog differential input<br>1d = Analog single-ended input<br>2d = Reserved<br>3d = Reserved | 单端输入 | 0 |
| 5 | 0 | | | **1** |
| 4 | 1 | Channel 2 input coupling.<br>0d = AC-coupled input<br>1d = DC-coupled input | DC耦合 | 1 |
| 3 | 0 | Channel 2 microphone input range.<br>0d = Low swing mode; Differential input AC signal full-scale of 2-VRMS supported provided DC differential common mode voltage IN1P - IN1M < 4.2 V. Single-ended AC signal 1-VRMS supported provided DC common mode voltage is < 2.1 V.<br>1d = High swing mode; Differential Input IN1P-IN1M peak voltage up to 14.14 V or single ended 7.07 V supported. User rquired to adjust the channel gain and digital volume control based on the max signal level used in system. | 入力范围大模式 | **1** |
| 2 | 0 | Channel 2 CMRR Configuration.<br>0d = High SNR performance mode<br>1d = Reserved<br>2d = High CMRR performance mode<br>3d = Reserved | Default | 0 |
| 1 | 0 | | | 0 |
| 0 | 0 | Channel 2 automatic gain controller (AGC) setting.<br>0d = AGC disabled<br>1d = AGC enabled based on the configuration of bit 3 in register 108 (P0_R108); This must be used only with AC-coupled input | 自动增益调节关闭 | 0 |

| | 01000010 | Address : 0x42 | | **0x20** |
|---|---|---|---|---|
| | 00000000 | Default Value : 0x00 | | 00100000 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | Channel 2 gain.<br>0d = Channel gain is set to 0 dB<br>1d = Channel gain is set to 1 dB<br>2d = Channel gain is set to 2 dB<br>3d to 41d = Channel gain is set as per configuration<br>42d = Channel gain is set to 42 dB<br>43d to 63d = Reserved | 串扰、采样值问题对策：8dB，后续根据需要调整 | 0 |
| 6 | 0 | | | 0 |
| 5 | 0 | | | **1** |
| 4 | 0 | | | 0 |
| 3 | 0 | | | 0 |
| 2 | 0 | | | 0 |
| 1 | 0 | Reserved | | 0 |
| 0 | 0 | Reserved | | 0 |

| | 01000011 | Address : 0x43 | | 0xDB |
|---|---|---|---|---|
| | 11001001 | Default Value : 0xC9 | | 11011011 |
| bit | default | Definition | Description | Setting |
| 7 | 1 | Channel 2 digital volume control.<br>0d = Digital volume is muted<br>1d = Digital volume control is set to -100 dB<br>2d = Digital volume control is set to -99.5 dB<br>3d to 200d = Digital volume control is set as per configuration<br>201d = Digital volume control is set to 0 dB<br>202d = Digital volume control is set to 0.5 dB<br>203d to 253d = Digital volume control is set as per configuration<br>254d = Digital volume control is set to 26.5 dB<br>255d = Digital volume control is set to 27 dB | 串扰、采样值问题对策：9dB，后续根据需要调整 | 1 |
| 6 | 1 | | | 1 |
| 5 | 0 | | | 0 |
| 4 | 0 | | | 1 |
| 3 | 1 | | | 1 |
| 2 | 0 | | | 0 |
| 1 | 0 | | | 1 |
| 0 | 1 | | | 1 |

| | 01000100 | Address : 0x44 | | 0x80 |
|---|---|---|---|---|
| | 10000000 | Default Value : 0x80 | | 10000000 |
| bit | default | Definition | Description | Setting |
| 7 | 1 | Channel 2 gain calibration.<br>0d = Gain calibration is set to -0.8 dB<br>1d = Gain calibration is set to -0.7 dB<br>2d = Gain calibration is set to -0.6 dB<br>3d to 7d = Gain calibration is set as per configuration<br>8d = Gain calibration is set to 0 dB<br>9d = Gain calibration is set to 0.1 dB<br>10d to 13d = Gain calibration is set as per configuration<br>14d = Gain calibration is set to 0.6 dB<br>15d = Gain calibration is set to 0.7 dB | Used as default first，后续根据需要调整 | 1 |
| 6 | 0 | | | 0 |
| 5 | 0 | | | 0 |
| 4 | 0 | | | 0 |
| 3 | 0 | Reserved | | 0 |
| 2 | 0 | | | 0 |
| 1 | 0 | | | 0 |
| 0 | 0 | | | 0 |

| | 01000101 | Address : 0x45 | | 0x00 |
|---|---|---|---|---|
| | 00000000 | Default Value : 0x00 | | 00000000 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | Channel 2 phase calibration with modulator clock resolution.<br>0d = No phase calibration<br>1d = Phase calibration delay is set to one cycle of the modulator clock<br>2d = Phase calibration delay is set to two cycles of the modulator clock<br>3d to 254d = Phase calibration delay as per configuration<br>255d = Phase calibration delay is set to 255 cycles of the modulator clock | Used as default first，后续根据需要调整 | 0 |
| 6 | 0 | | | 0 |
| 5 | 0 | | | 0 |
| 4 | 0 | | | 0 |
| 3 | 0 | | | 0 |
| 2 | 0 | | | 0 |
| 1 | 0 | | | 0 |
| 0 | 0 | | | 0 |

| | 01000110 | Address : 0x46 | | 0x38 |
|---|---|---|---|---|
| | 00010000 | Default Value : 0x10 | | 00111000 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | Channel 3 input type.<br>0d = Microphone input<br>1d = Line input | Microphone输入 | 0 |
| 6 | 0 | Channel 3 input configuration.<br>0d = Analog differential input<br>1d = Analog single-ended input<br>2d = Reserved<br>3d = Reserved | 单端输入 | 0 |
| 5 | 0 | | | 1 |
| 4 | 1 | Channel 3 input coupling.<br>0d = AC-coupled input<br>1d = DC-coupled input | DC耦合 | 1 |
| 3 | 0 | Channel 3 microphone input range.<br>0d = Low swing mode; Differential input AC signal full-scale of 2-VRMS supported provided DC differential common mode voltage IN1P - IN1M < 4.2 V. Single-ended AC signal 1-VRMS supported provided DC common mode voltage is < 2.1 V.<br>1d = High swing mode; Differential Input IN1P-IN1M peak voltage up to 14.14 V or single ended 7.07 V supported. User rquired to adjust the channel gain and digital volume control based on the max signal level used in system. | 大范围输入 | 1 |
| 2 | 0 | Channel 3 CMRR Configuration.<br>0d = High SNR performance mode<br>1d = Reserved<br>2d = High CMRR performance mode<br>3d = Reserved | Default | 0 |
| 1 | 0 | | | 0 |
| 0 | 0 | Channel 3 automatic gain controller (AGC) setting.<br>0d = AGC disabled<br>1d = AGC enabled based on the configuration of bit 3 in register 108 (P0_R108); This must be used only with AC-coupled input | 自动增益调节关闭 | 0 |

| | 01000111 | Address : 0x47 | | 0x20 |
|---|---|---|---|---|
| | 00000000 | Default Value : 0x00 | | 00100000 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | Channel 3 gain.<br>0d = Channel gain is set to 0 dB<br>1d = Channel gain is set to 1 dB<br>2d = Channel gain is set to 2 dB<br>3d to 41d = Channel gain is set as per configuration<br>42d = Channel gain is set to 42 dB<br>43d to 63d = Reserved | 串扰、采样值问题对策：8dB，后续根据需要调整 | 0 |
| 6 | 0 | | | 0 |
| 5 | 0 | | | 1 |
| 4 | 0 | | | 0 |
| 3 | 0 | | | 0 |

| | | | | |
|---|---|---|---|---|
| 2 | 0 | [illegible] | | 0 |
| 1 | 0 | Reserved | | 0 |
| 0 | 0 | Reserved | | 0 |

| | 01001000 | Address : 0x48 | | 0xDB |
|---|---|---|---|---|
| | 11001001 | Default Value : 0xC9 | | 11011011 |
| bit | default | Definition | Description | Setting |
| 7 | 1 | Channel 3 digital volume control.<br>0d = Digital volume is muted<br>1d = Digital volume control is set to -100 dB<br>2d = Digital volume control is set to -99.5 dB<br>3d to 200d = Digital volume control is set as per configuration<br>201d = Digital volume control is set to 0 dB<br>202d = Digital volume control is set to 0.5 dB<br>203d to 253d = Digital volume control is set as per configuration<br>254d = Digital volume control is set to 26.5 dB<br>255d = Digital volume control is set to 27 dB | 串扰、采样值问题对策：9dB，后续根据需要调整 | 1 |
| 6 | 1 | | | 1 |
| 5 | 0 | | | 0 |
| 4 | 0 | | | 1 |
| 3 | 1 | | | 1 |
| 2 | 0 | | | 0 |
| 1 | 0 | | | 1 |
| 0 | 1 | | | 1 |

| | 01001001 | Address : 0x49 | | 0x80 |
|---|---|---|---|---|
| | 10000000 | Default Value : 0x80 | | 10000000 |
| bit | default | Definition | Description | Setting |
| 7 | 1 | Channel 3 gain calibration.<br>0d = Gain calibration is set to -0.8 dB<br>1d = Gain calibration is set to -0.7 dB<br>2d = Gain calibration is set to -0.6 dB<br>3d to 7d = Gain calibration is set as per configuration<br>8d = Gain calibration is set to 0 dB<br>9d = Gain calibration is set to 0.1 dB<br>10d to 13d = Gain calibration is set as per configuration<br>14d = Gain calibration is set to 0.6 dB<br>15d = Gain calibration is set to 0.7 dB | Default | 1 |
| 6 | 0 | | | 0 |
| 5 | 0 | | | 0 |
| 4 | 0 | | | 0 |
| 3 | 0 | Reserved | | 0 |
| 2 | 0 | | | 0 |
| 1 | 0 | | | 0 |
| 0 | 0 | | | 0 |

| | 01001010 | Address : 0x4A | | 0x00 |
|---|---|---|---|---|
| | 00000000 | Default Value : 0x00 | | 00000000 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | Channel 3 phase calibration with modulator clock resolution.<br>0d = No phase calibration<br>1d = Phase calibration delay is set to one cycle of the modulator clock<br>2d = Phase calibration delay is set to two cycles of the modulator clock<br>3d to 254d = Phase calibration delay as per configuration<br>255d = Phase calibration delay is set to 255 cycles of the modulator clock | Default | 0 |
| 6 | 0 | | | 0 |
| 5 | 0 | | | 0 |
| 4 | 0 | | | 0 |
| 3 | 0 | | | 0 |
| 2 | 0 | | | 0 |
| 1 | 0 | | | 0 |
| 0 | 0 | | | 0 |

| | 01001011 | Address : 0x4B | | 0x38 |
|---|---|---|---|---|
| | 00010000 | Default Value : 0x10 | | 00111000 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | Channel 4 input type.<br>0d = Microphone input<br>1d = Line input | Microphone输入 | 0 |
| 6 | 0 | Channel 4 input configuration.<br>0d = Analog differential input<br>1d = Analog single-ended input<br>2d = Reserved<br>3d = Reserved | 单端输入 | 0 |
| 5 | 0 | | | 1 |
| 4 | 1 | Channel 4 input coupling.<br>0d = AC-coupled input<br>1d = DC-coupled input | DC | 1 |
| 3 | 0 | Channel 4 microphone input range.<br>0d = Low swing mode; Differential input AC signal full-scale of 2-VRMS supported provided DC differential common mode voltage IN1P - IN1M < 4.2 V. Single-ended AC signal 1-VRMS supported provided DC common mode voltage is < 2.1 V.<br>1d = High swing mode; Differential Input IN1P-IN1M peak voltage up to 14.14 V or single ended 7.07 V supported. User rquired to adjust the channel gain and digital volume control based on the max signal level used in system. | 大范围 | 1 |
| 2 | 0 | Channel 4 CMRR Configuration.<br>0d = High SNR performance mode<br>1d = Reserved<br>2d = High CMRR performance mode<br>3d = Reserved | Default | 0 |
| 1 | 0 | | | 0 |
| 0 | 0 | Channel 4 automatic gain controller (AGC) setting.<br>0d = AGC disabled<br>1d = AGC enabled based on the configuration of bit 3 in register 108 (P0_R108); This must be used only with AC-coupled input | 自动增益调节关闭 | 0 |

| | 01001100 | Address : 0x4C | | 0x20 |
|---|---|---|---|---|
| | 00000000 | Default Value : 0x00 | | 00100000 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | Channel 4 gain.<br>0d = Channel gain is set to 0 dB | | 0 |
| 6 | 0 | | | 0 |

| | | | | |
|---|---|---|---|---|
| 5 | 0 | 1d = Channel gain is set to 1 dB<br>2d = Channel gain is set to 2 dB<br>3d to 41d = Channel gain is set as per configuration<br>42d = Channel gain is set to 42 dB<br>43d to 63d = Reserved | 串扰、采样值问题对策：8dB，后续根据需要调整 | 1 |
| 4 | 0 | | | 0 |
| 3 | 0 | | | 0 |
| 2 | 0 | | | 0 |
| 1 | 0 | Reserved | | 0 |
| 0 | 0 | Reserved | | 0 |

| | 01001101 | Address : 0x4D | | 0xDB |
|---|---|---|---|---|
| | 11001001 | Default Value : 0xC9 | | 11011011 |
| bit | default | Definition | Description | Setting |
| 7 | 1 | Channel 4 digital volume control.<br>0d = Digital volume is muted<br>1d = Digital volume control is set to -100 dB<br>2d = Digital volume control is set to -99.5 dB<br>3d to 200d = Digital volume control is set as per configuration<br>201d = Digital volume control is set to 0 dB<br>202d = Digital volume control is set to 0.5 dB<br>203d to 253d = Digital volume control is set as per configuration<br>254d = Digital volume control is set to 26.5 dB<br>255d = Digital volume control is set to 27 dB | 串扰、采样值问题对策：9dB，后续根据需要调整 | 1 |
| 6 | 1 | | | 1 |
| 5 | 0 | | | 0 |
| 4 | 0 | | | 1 |
| 3 | 1 | | | 1 |
| 2 | 0 | | | 0 |
| 1 | 0 | | | 1 |
| 0 | 1 | | | 1 |

| | 01001110 | Address : 0x4E | | 0x80 |
|---|---|---|---|---|
| | 10000000 | Default Value : 0x80 | | 10000000 |
| bit | default | Definition | Description | Setting |
| 7 | 1 | Channel 4 gain calibration.<br>0d = Gain calibration is set to -0.8 dB<br>1d = Gain calibration is set to -0.7 dB<br>2d = Gain calibration is set to -0.6 dB<br>3d to 7d = Gain calibration is set as per configuration<br>8d = Gain calibration is set to 0 dB<br>9d = Gain calibration is set to 0.1 dB<br>10d to 13d = Gain calibration is set as per configuration<br>14d = Gain calibration is set to 0.6 dB<br>15d = Gain calibration is set to 0.7 dB | Default | 1 |
| 6 | 0 | | | 0 |
| 5 | 0 | | | 0 |
| 4 | 0 | | | 0 |
| 3 | 0 | Reserved | | 0 |
| 2 | 0 | | | 0 |
| 1 | 0 | | | 0 |
| 0 | 0 | | | 0 |

| | 01001111 | Address : 0x4F | | 0x00 |
|---|---|---|---|---|
| | 00000000 | Default Value : 0x00 | | 00000000 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | Channel 4 phase calibration with modulator clock resolution.<br>0d = No phase calibration<br>1d = Phase calibration delay is set to one cycle of the modulator clock<br>2d = Phase calibration delay is set to two cycles of the modulator clock<br>3d to 254d = Phase calibration delay as per configuration<br>255d = Phase calibration delay is set to 255 cycles of the modulator clock | Default | 0 |
| 6 | 0 | | | 0 |
| 5 | 0 | | | 0 |
| 4 | 0 | | | 0 |
| 3 | 0 | | | 0 |
| 2 | 0 | | | 0 |
| 1 | 0 | | | 0 |
| 0 | 0 | | | 0 |

| | 01010000 | Address : 0x50 | | 0x38 |
|---|---|---|---|---|
| | 00010000 | Default Value : 0x10 | | 00111000 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | Channel 5 input type.<br>0d = Microphone input<br>1d = Line input | Microphone输入 | 0 |
| 6 | 0 | Channel 5 input configuration.<br>0d = Analog differential input<br>1d = Analog single-ended input<br>2d = Reserved | 单端输入 | 0 |
| 5 | 0 | | | 1 |
| 4 | 1 | Channel 5 input coupling.<br>0d = AC-coupled input<br>1d = DC-coupled input | DC | 1 |
| 3 | 0 | Channel 5 microphone input range.<br>0d = Low swing mode; Differential input AC signal full-scale of 2-VRMS supported provided DC differential common mode voltage IN1P - IN1M < 4.2 V. Single-ended AC signal 1-VRMS supported provided DC common mode voltage is < 2.1 V.<br>1d = High swing mode; Differential Input IN1P-IN1M peak voltage up to 14.14 V or single ended 7.07 V supported. User rquired to adjust the channel gain and digital volume control based on the max signal level used in system. | 大范围 | 1 |
| 2 | 0 | Channel 5 CMRR Configuration.<br>0d = High SNR performance mode<br>1d = Reserved<br>2d = High CMRR performance mode<br>3d = Reserved | Default | 0 |
| 1 | 0 | | | 0 |
| 0 | 0 | Channel 5 automatic gain controller (AGC) setting.<br>0d = AGC disabled<br>1d = AGC enabled based on the configuration of bit 3 in register 108 (P0_R108); This must be used only with AC-coupled input | Default | 0 |

| | 01010001 | Address : 0x51 | | 0x20 |
|---|---|---|---|---|

| | 00000000 | Default Value ： 0x00 | | 00100000 |
|---|---|---|---|---|
| bit | default | Definition | Description | Setting |
| 7 | 0 | Channel 5 gain.<br>0d = Channel gain is set to 0 dB<br>1d = Channel gain is set to 1 dB<br>2d = Channel gain is set to 2 dB<br>3d to 41d = Channel gain is set as per configuration<br>42d = Channel gain is set to 42 dB<br>43d to 63d = Reserved | 串扰、采样值问题对策：8dB，后续根据需要调整 | 0 |
| 6 | 0 | | | 0 |
| 5 | 0 | | | 1 |
| 4 | 0 | | | 0 |
| 3 | 0 | | | 0 |
| 2 | 0 | | | 0 |
| 1 | 0 | Reserved | | 0 |
| 0 | 0 | Reserved | | 0 |

| | 01010010 | Address ： 0x52 | | 0xDB |
|---|---|---|---|---|
| | 11001001 | Default Value ： 0xC9 | | 11011011 |
| bit | default | Definition | Description | Setting |
| 7 | 1 | Channel 5 digital volume control.<br>0d = Digital volume is muted<br>1d = Digital volume control is set to -100 dB<br>2d = Digital volume control is set to -99.5 dB<br>3d to 200d = Digital volume control is set as per configuration<br>201d = Digital volume control is set to 0 dB<br>202d = Digital volume control is set to 0.5 dB<br>203d to 253d = Digital volume control is set as per configuration<br>254d = Digital volume control is set to 26.5 dB<br>255d = Digital volume control is set to 27 dB | 串扰、采样值问题对策：9dB，后续根据需要调整 | 1 |
| 6 | 1 | | | 1 |
| 5 | 0 | | | 0 |
| 4 | 0 | | | 1 |
| 3 | 1 | | | 1 |
| 2 | 0 | | | 0 |
| 1 | 0 | | | 1 |
| 0 | 1 | | | 1 |

| | 01010011 | Address ： 0x53 | | 0x80 |
|---|---|---|---|---|
| | 10000000 | Default Value ： 0x80 | | 10000000 |
| bit | default | Definition | Description | Setting |
| 7 | 1 | Channel 5 gain calibration.<br>0d = Gain calibration is set to -0.8 dB<br>1d = Gain calibration is set to -0.7 dB<br>2d = Gain calibration is set to -0.6 dB<br>3d to 7d = Gain calibration is set as per configuration<br>8d = Gain calibration is set to 0 dB<br>9d = Gain calibration is set to 0.1 dB<br>10d to 13d = Gain calibration is set as per configuration<br>14d = Gain calibration is set to 0.6 dB<br>15d = Gain calibration is set to 0.7 dB | Default | 1 |
| 6 | 0 | | | 0 |
| 5 | 0 | | | 0 |
| 4 | 0 | | | 0 |
| 3 | 0 | Reserved | | 0 |
| 2 | 0 | | | 0 |
| 1 | 0 | | | 0 |
| 0 | 0 | | | 0 |

| | 01010100 | Address ： 0x54 | | 0x00 |
|---|---|---|---|---|
| | 00000000 | Default Value ： 0x00 | | 00000000 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | Channel 5 phase calibration with modulator clock resolution.<br>0d = No phase calibration<br>1d = Phase calibration delay is set to one cycle of the modulator clock<br>2d = Phase calibration delay is set to two cycles of the modulator clock<br>3d to 254d = Phase calibration delay as per configuration<br>255d = Phase calibration delay is set to 255 cycles of the modulator clock | Default | 0 |
| 6 | 0 | | | 0 |
| 5 | 0 | | | 0 |
| 4 | 0 | | | 0 |
| 3 | 0 | | | 0 |
| 2 | 0 | | | 0 |
| 1 | 0 | | | 0 |
| 0 | 0 | | | 0 |

| | 01010101 | Address ： 0x55 | | 0x38 |
|---|---|---|---|---|
| | 00010000 | Default Value ： 0x10 | | 00111000 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | Channel 6 input type.<br>0d = Microphone input<br>1d = Line input | Microphone输入 | 0 |
| 6 | 0 | Channel 6 input configuration.<br>0d = Analog differential input<br>1d = Analog single-ended input<br>2d = Reserved | 单端输入 | 0 |
| 5 | 0 | | | 1 |
| 4 | 1 | Channel 6 input coupling.<br>0d = AC-coupled input<br>1d = DC-coupled input | DC | 1 |
| 3 | 0 | Channel 6 microphone input range.<br>0d = Low swing mode; Differential input AC signal full-scale of 2-VRMS supported provided DC differential common mode voltage IN1P - IN1M < 4.2 V. Single-ended AC signal 1-VRMS supported provided DC common mode voltage is < 2.1 V.<br>1d = High swing mode; Differential Input IN1P-IN1M peak voltage up to 14.14 V or single ended 7.07 V supported. User rquired to adjust the channel gain and digital volume control based on the max signal level used in system. | 大范围 | 1 |
| 2 | 0 | Channel 6 CMRR Configuration.<br>0d = High SNR performance mode<br>1d = Reserved<br>2d = High CMRR performance mode<br>3d = Reserved | Default | 0 |
| 1 | 0 | | | 0 |

| | | | | |
|---|---|---|---|---|
| 0 | 0 | Channel 6 automatic gain controller (AGC) setting.<br>0d = AGC disabled<br>1d = AGC enabled based on the configuration of bit 3 in register 108 (P0_R108); This must be used only with AC-coupled input | Default | 0 |

| | 01010110 | Address : 0x56 | | 0x20 |
|---|---|---|---|---|
| | 00000000 | Default Value : 0x00 | | 00100000 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | Channel 6 gain.<br>0d = Channel gain is set to 0 dB<br>1d = Channel gain is set to 1 dB<br>2d = Channel gain is set to 2 dB<br>3d to 41d = Channel gain is set as per configuration<br>42d = Channel gain is set to 42 dB<br>43d to 63d = Reserved | 串扰、采样值问题对策：8dB，后续根据需要调整 | 0 |
| 6 | 0 | | | 0 |
| 5 | 0 | | | 1 |
| 4 | 0 | | | 0 |
| 3 | 0 | | | 0 |
| 2 | 0 | | | 0 |
| 1 | 0 | Reserved | | 0 |
| 0 | 0 | Reserved | | 0 |

| | 01010111 | Address : 0x57 | | 0xDB |
|---|---|---|---|---|
| | 11001001 | Default Value : 0xC9 | | 11011011 |
| bit | default | Definition | Description | Setting |
| 7 | 1 | Channel 6 digital volume control.<br>0d = Digital volume is muted<br>1d = Digital volume control is set to -100 dB<br>2d = Digital volume control is set to -99.5 dB<br>3d to 200d = Digital volume control is set as per configuration<br>201d = Digital volume control is set to 0 dB<br>202d = Digital volume control is set to 0.5 dB<br>203d to 253d = Digital volume control is set as per configuration<br>254d = Digital volume control is set to 26.5 dB<br>255d = Digital volume control is set to 27 dB | 串扰、采样值问题对策：9dB，后续根据需要调整 | 1 |
| 6 | 1 | | | 1 |
| 5 | 0 | | | 0 |
| 4 | 0 | | | 1 |
| 3 | 1 | | | 1 |
| 2 | 0 | | | 0 |
| 1 | 0 | | | 1 |
| 0 | 1 | | | 1 |

| | 01011000 | Address : 0x58 | | 0x80 |
|---|---|---|---|---|
| | 10000000 | Default Value : 0x80 | | 10000000 |
| bit | default | Definition | Description | Setting |
| 7 | 1 | Channel 6 gain calibration.<br>0d = Gain calibration is set to -0.8 dB<br>1d = Gain calibration is set to -0.7 dB<br>2d = Gain calibration is set to -0.6 dB<br>3d to 7d = Gain calibration is set as per configuration<br>8d = Gain calibration is set to 0 dB<br>9d = Gain calibration is set to 0.1 dB<br>10d to 13d = Gain calibration is set as per configuration<br>14d = Gain calibration is set to 0.6 dB<br>15d = Gain calibration is set to 0.7 dB | Default | 1 |
| 6 | 0 | | | 0 |
| 5 | 0 | | | 0 |
| 4 | 0 | | | 0 |
| 3 | 0 | Reserved | | 0 |
| 2 | 0 | | | 0 |
| 1 | 0 | | | 0 |
| 0 | 0 | | | 0 |

| | 01011001 | Address : 0x59 | | 0x00 |
|---|---|---|---|---|
| | 00000000 | Default Value : 0x00 | | 00000000 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | Channel 6 phase calibration with modulator clock resolution.<br>0d = No phase calibration<br>1d = Phase calibration delay is set to one cycle of the modulator clock<br>2d = Phase calibration delay is set to two cycles of the modulator clock<br>3d to 254d = Phase calibration delay as per configuration<br>255d = Phase calibration delay is set to 255 cycles of the modulator clock | Default | 0 |
| 6 | 0 | | | 0 |
| 5 | 0 | | | 0 |
| 4 | 0 | | | 0 |
| 3 | 0 | | | 0 |
| 2 | 0 | | | 0 |
| 1 | 0 | | | 0 |
| 0 | 0 | | | 0 |

| | 01100100 | Address : 0x64 | | 0x00 |
|---|---|---|---|---|
| | 00000000 | Default Value : 0x00 | | 00000000 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | Channel 1 input (IN1P and IN1M) scan for diagnostics.<br>0d = Diagnostic disabled<br>1d = Diagnostic enabled | Default | 0 |
| 6 | 0 | Channel 2 input (IN2P and IN2M) scan for diagnostics.<br>0d = Diagnostic disabled<br>1d = Diagnostic enabled | Default | 0 |
| 5 | 0 | Channel 3 input (IN3P and IN3M) scan for diagnostics.<br>0d = Diagnostic disabled<br>1d = Diagnostic enabled | Default | 0 |
| 4 | 0 | Channel 4 input (IN4P and IN4M) scan for diagnostics.<br>0d = Diagnostic disabled<br>1d = Diagnostic enabled | Default | 0 |
| 3 | 0 | Channel 5 input (IN5P and IN5M) scan for diagnostics. Applicable only for PCM6x60-Q1.<br>0d = Diagnostic disabled<br>1d = Diagnostic enabled | Default | 0 |
| 2 | 0 | Channel 6 input (IN6P and IN6M) scan for diagnostics. Applicable only for PCM6x60-Q1.<br>0d = Diagnostic disabled<br>1d = Diagnostic enabled | Default | 0 |

| | | | | |
|---|---|---|---|---|
| 1 | 0 | INxM pin diagnostics scan selection for single-ended configuration.<br>0d = INxM pins of single-ended channels are excluded for diagnosis<br>1d = INxM pins of single-ended channels are included for diagnosis | Default | 0 |
| 0 | 0 | AC-coupled channels pins scan selection for diagnostics.<br>0d = INxP and INxM pins of AC-coupled channels are excluded for diagnosis<br>1d = INxP and INxM pins of AC-coupled channels are included for diagnosis | DC-coupled，对象外 | 0 |

| | 01100101 | Address : 0x65 | | 0x37 |
|---|---|---|---|---|
| | 00110111 | Default Value : 0x37 | | 00110111 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | INxP and INxM terminal short detect threshold.<br>0d = INxP and INxM terminal short detect threshold value is 0 mV (typ)<br>1d = INxP and INxM terminal short detect threshold value is 30 mV (typ)<br>2d = INxP and INxM terminal short detect threshold value is 60 mV (typ)<br>10d to 13d = INxP and INxM terminal short detect threshold value is set as per configuration<br>14d = INxP and INxM terminal short detect threshold value is 420 mV (typ)<br>15d = INxP and INxM terminal short detect threshold value is 450 mV (typ) | Default | 0 |
| 6 | 0 | | | 0 |
| 5 | 1 | | | 1 |
| 4 | 1 | | | 1 |
| 3 | 0 | Short to VBAT_IN detect threshold.<br>0d = Short to VBAT_IN detect threshold value is 0 mV (typ)<br>1d = Short to VBAT_IN detect threshold value is 30 mV (typ)<br>2d = Short to VBAT_IN detect threshold value is 60 mV (typ)<br>10d to 13d = Short to VBAT_IN detect threshold value is set as per configuration<br>14d = Short to VBAT_IN detect threshold value is 420 mV (typ)<br>15d = Short to VBAT_IN detect threshold value is 450 mV (typ) | Default | 0 |
| 2 | 1 | | | 1 |
| 1 | 1 | | | 1 |
| 0 | 1 | | | 1 |

| | 01100110 | Address : 0x66 | | 0x87 |
|---|---|---|---|---|
| | 10000111 | Default Value : 0x87 | | 10000111 |
| bit | default | Definition | Description | Setting |
| 7 | 1 | Short to ground detect threshold.<br>0d = Short to ground detect threshold value is 0 mV (typ)<br>1d = Short to ground detect threshold value is 60 mV (typ)<br>2d = Short to ground detect threshold value is 120 mV (typ)<br>10d to 13d = Short to ground detect threshold value is set as per configuration<br>14d = Short to ground detect threshold value is 840 mV (typ)<br>15d = Short to ground detect threshold value is 900 mV (typ) | Default | 1 |
| 6 | 0 | | | 0 |
| 5 | 0 | | | 0 |
| 4 | 0 | | | 0 |
| 3 | 0 | Short to MICBIAS detect threshold.<br>0d = Short to MICBIAS detect threshold value is 0 mV (typ)<br>1d = Short to MICBIAS detect threshold value is 30 mV (typ)<br>2d = Short to MICBIAS detect threshold value is 60 mV (typ)<br>10d to 13d = Short to MICBIAS detect threshold value is set as per configuration<br>14d = Short to MICBIAS detect threshold value is 420 mV (typ)<br>15d = Short to MICBIAS detect threshold value is 450 mV (typ) | Default | 0 |
| 2 | 1 | | | 1 |
| 1 | 1 | | | 1 |
| 0 | 1 | | | 1 |

| | 01100111 | Address : 0x67 | | 0xB8 |
|---|---|---|---|---|
| | 10111000 | Default Value : 0xB8 | | 10111000 |
| bit | default | Definition | Description | Setting |
| 7 | 1 | Fault monitoring scan repetition rate.<br>0d = Continuos back to back scanning of selected channels input pins without any idle time<br>1d = Fault monitoring repetition rate of 1 ms for selected channels input pins scanning<br>2d = Fault monitoring repetition rate of 4 ms for selected channels input pins scanning<br>3d = Fault monitoring repetition rate of 8 ms for selected channels input pins scanning | ch1~6：Diagnostic disabled selected | 1 |
| 6 | 0 | | | 0 |
| 5 | 1 | Reserved | | 1 |
| 4 | 1 | | | 1 |
| 3 | 1 | Debounce count for all the faults (except VBAT_IN short when VBAT_IN < MICBIAS).<br>0d = 16 counts for debounce to filter-out any false faults detection<br>1d = 8 counts for debounce to filter-out any false faults detection<br>2d = 4 counts for debounce to filter-out any false faults detection<br>3d = No debounce count | | 1 |
| 2 | 0 | | | 0 |
| 1 | 0 | VBAT_IN short debounce count only when VBAT_IN < MICBIAS.<br>0d = 16 counts for debounce to filter-out any false faults detection<br>1d = 8 counts for debounce to filter-out any false faults detection | | 0 |
| 0 | 0 | Diagnostic thresholds range scale.<br>0d = Thresholds same as configured in P0_R101 and P0_R102<br>1d = All the configuration thresholds gets scale by 2 times | | 0 |

| | 01101000 | Address : 0x68 | | 0x00 |
|---|---|---|---|---|
| | 00000000 | Default Value : 0x00 | | 00000000 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | Moving average configuration.<br>0d = Moving average disabled<br>1d = Moving average enabled with 0.5 weightage for old scanned data and new scanned data | Moving averag禁用 | 0 |

| | | | | |
|---|---|---|---|---|
| 6 | 0 | new scanned data<br>2d = Moving average enabled with 0.75 weightage for old scanned data and 0.25 weightage for new scanned data<br>3d = Reserved | Moving averag禁用 | 0 |
| 5 | 0 | Moving average configuration for MICBIAS high and low load current fault detection<br>0d = Moving average as defined by DIAG_MOV_AVG_CFG setting<br>1d = Moving average is forced disabled for MICBIAS load current fault detection to achieve faster response time | Moving averag禁用，设定无效 | 0 |
| 4 | 0 | Moving average configuration for over temperature fault detection<br>0d = Moving average as defined by DIAG_MOV_AVG_CFG setting<br>1d = Moving average is forced disabled for over temperature fault detection to achieve faster response time | Moving averag禁用，设定无效 | 0 |
| 3 | 0 | Reserved | | 0 |
| 2 | 0 | | | 0 |
| 1 | 0 | | | 0 |
| 0 | 0 | | | 0 |

| | 01101011 | Address : 0x6B | | 0x01 |
|---|---|---|---|---|
| | 00000001 | Default Value : 0x01 | | 00000001 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | Reserved | | 0 |
| 6 | 0 | | | 0 |
| 5 | 0 | Decimation filter response.<br>0d = Linear phase<br>1d = Low latency<br>2d = Ultra-low latency | | 0 |
| 4 | 0 | | | 0 |
| 3 | 0 | Channel summation mode for higher SNR<br>0d = Channel summation mode is disabled<br>1d = 2-channel summation mode is enabled to generate a (CH1 + CH2) / 2 and a (CH3 + CH4) / 2 output<br>2d = 4-channel summation mode is enabled to generate a (CH1 + CH2 + CH3 + CH4) / 4 output<br>3d = Reserved | Channel summation mode关闭 | 0 |
| 2 | 0 | | | 0 |
| 1 | 0 | High-pass filter (HPF) selection.<br>0d = Programmable first-order IIR filter for a custom HPF with default coefficient values in P4_R72 to P4_R83 set as the all-pass filter<br>1d = HPF with a cutoff of 0.00025 x fS (12 Hz at fS = 48 kHz) is selected<br>2d = HPF with a cutoff of 0.002 x fS (96 Hz at fS = 48 kHz) is selected<br>3d = HPF with a cutoff of 0.008 x fS (384 Hz at fS = 48 kHz) is selected | 通过右侧设置高通滤波器<br>*回路参照 | 0 |
| 0 | 1 | | | 1 |

| | 01101100 | Address : 0x6C | | 0x48 |
|---|---|---|---|---|
| | 01001000 | Default Value : 0x48 | | 01001000 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | DVOL control ganged across channels.<br>0d = Each channel has its own DVOL CTRL settings as programmed in the CHx_DVOL bits<br>1d = All active channels must use the channel 1 DVOL setting (CH_DVOL) irrespective of whether channel 1 is turned on or not | 每个通道数字增益分别控制 | 0 |
| 6 | 1 | Number of biquads per channel configuration.<br>0d = No biquads per channel; biquads are all disabled<br>1d = 1 biquad per channel<br>2d = 2 biquads per channel<br>3d = 3 biquads per channel | 每个通道两个滤波器 | 1 |
| 5 | 0 | | | 0 |
| 4 | 0 | Soft-stepping disable during DVOL change, mute, and unmute.<br>0d = Soft-stepping enabled<br>1d = Soft-stepping disabled | Soft-stepping有效 | 0 |
| 3 | 1 | AGC master enable setting.<br>0d = Reserved; Write always 1 to this register bit<br>1d = AGC selected as configured for each channel using CHx_CFG0 register | | 1 |
| 2 | 0 | Reserved | | 0 |
| 1 | 0 | Reserved | | 0 |
| 0 | 0 | | | 0 |

| | 01110000 | Address : 0x70 | | 0x00 |
|---|---|---|---|---|
| | 11100111 | Default Value : 0xE7 | | 00000000 |
| bit | default | Definition | Description | Setting |
| 7 | 1 | AGC output signal target level.<br>0d = Output signal target level is -6 dB<br>1d = Output signal target level is -8 dB<br>2d = Output signal target level is -10 dB<br>3d to 13d = Output signal target level is as per configuration<br>14d = Output signal target level is -34 dB<br>15d = Output signal target level is -36 dB | -6dB暂定<br>*回路参照 | 0 |
| 6 | 1 | | | 0 |
| 5 | 1 | | | 0 |
| 4 | 0 | | | 0 |
| 3 | 0 | AGC maximum gain allowed.<br>0d = Maximum gain allowed is 3 dB<br>1d = Maximum gain allowed is 6 dB<br>2d = Maximum gain allowed is 9 dB<br>3d to 11d = Maximum gain allowed is as per configuration<br>12d = Maximum gain allowed is 39 dB<br>13d = Maximum gain allowed is 42 dB<br>14d to 15d = Reserved | 3dB暂定<br>*回路参照 | 0 |
| 2 | 1 | | | 0 |
| 1 | 1 | | | 0 |
| 0 | 1 | | | 0 |

| | 01110011 | Address : 0x73 | | 0xFC |
|---|---|---|---|---|
| | 11111100 | Default Value : 0xFC | | 11111100 |
| bit | default | Definition | Description | Setting |
| 7 | 1 | Input channel 1 enable setting.<br>0d = Channel 1 is disabled<br>1d = Channel 1 is enabled | Default | 1 |
| 6 | 1 | Input channel 2 enable setting.<br>0d = Channel 2 is disabled<br>1d = Channel 2 is enabled | Default | 1 |
| 5 | 1 | Input channel 3 enable setting.<br>0d = Channel 3 is disabled<br>1d = Channel 3 is enabled | Default | 1 |
| 4 | 1 | Input channel 4 enable setting.<br>0d = Channel 4 is disabled<br>1d = Channel 4 is enabled | Default | 1 |
| 3 | 1 | Input channel 5 enable setting. Applicable only for PCM6x60-Q1.<br>0d = Channel 5 is disabled<br>1d = Channel 5 is enabled | Default | 1 |
| 2 | 1 | Input channel 6 enable setting. Applicable only for PCM6x60-Q1.<br>0d = Channel 6 is disabled<br>1d = Channel 6 is enabled | Default | 1 |
| 1 | 0 | Reserved | | 0 |
| 0 | 0 | Reserved | | 0 |

| | 01110100 | Address : 0x74 | | **0xFC** |
|---|---|---|---|---|
| | 00000000 | Default Value : 0x00 | | 11111100 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | ASI output channel 1 enable setting.<br>0d = Channel 1 output slot is in a tri-state condition<br>1d = Channel 1 output slot is enabled | slot使用 | **1** |
| 6 | 0 | ASI output channel 2 enable setting.<br>0d = Channel 2 output slot is in a tri-state condition<br>1d = Channel 2 output slot is enabled | slot使用 | **1** |
| 5 | 0 | ASI output channel 3 enable setting.<br>0d = Channel 3 output slot is in a tri-state condition<br>1d = Channel 3 output slot is enabled | slot使用 | **1** |
| 4 | 0 | ASI output channel 4 enable setting.<br>0d = Channel 4 output slot is in a tri-state condition<br>1d = Channel 4 output slot is enabled | slot使用 | **1** |
| 3 | 0 | ASI output channel 5 enable setting. Applicable only for PCM6x60-Q1.<br>0d = Channel 5 output slot is in a tri-state condition<br>1d = Channel 5 output slot is enabled | slot使用 | **1** |
| 2 | 0 | ASI output channel 6 enable setting. Applicable only for PCM6x60-Q1.<br>0d = Channel 6 output slot is in a tri-state condition<br>1d = Channel 6 output slot is enabled | slot使用 | **1** |
| 1 | 0 | Reserved | | 0 |
| 0 | 0 | Reserved | | 0 |

| | 01110101 | Address : 0x75 | | **0xF8** |
|---|---|---|---|---|
| | 00000000 | Default Value : 0x00 | | 11111000 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | Power control for MICBIAS.<br>0d = Power down MICBIAS<br>1d = Power up MICBIAS | 打开MICBIAS | **1** |
| 6 | 0 | Power control for ADC channels.<br>0d = Power down all ADC channels<br>1d = Power up all enabled ADC channels | 打开所有通道 | **1** |
| 5 | 0 | Power control for the PLL.<br>0d = Power down the PLL<br>1d = Power up the PLL | 打开PLL | **1** |
| 4 | 0 | Dynamic channel power-up, power-down enable.<br>0d = Channel power-up, power-down is not supported if any channel recording is on<br>1d = Channel can be powered up or down individually, even if channel recording is on. Do not powered-down channel 1 if this bit is set to '1' | | **1** |
| 3 | 0 | Dynamic mode maximum channel select configuration.<br>0d = Channel 1 and channel 2 are used with dynamic channel power-up, power-down feature enabled<br>1d = Channel 1 to channel 4 are used with dynamic channel power-up, power-down feature enabled<br>2d = Channel 1 to channel 6 are used with dynamic channel power-up, power-down feature enabled | | **1** |
| 2 | 0 | | | 0 |
| 1 | 0 | Reserved | | 0 |
| 0 | 0 | Reserved | | 0 |

| | 01110110 | Address : 0x76 | | 0x00 |
|---|---|---|---|---|
| | 00000000 | Default Value : 0x00 | | 00000000 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | ADC channel 1 power status.<br>0d = ADC channel is powered down<br>1d = ADC channel is powered up | | 0 |
| 6 | 0 | ADC channel 2 power status.<br>0d = ADC channel is powered down<br>1d = ADC channel is powered up | | 0 |
| 5 | 0 | ADC channel 3 power status.<br>0d = ADC channel is powered down<br>1d = ADC channel is powered up | | 0 |

| | | | | |
|---|---|---|---|---|
| 4 | 0 | ADC channel 4 power status.<br>0d = ADC channel is powered down<br>1d = ADC channel is powered up | | 0 |
| 3 | 0 | ADC channel 5 power status. Applicable only for PCM6x60-Q1.<br>0d = ADC channel is powered down<br>1d = ADC channel is powered up | | 0 |
| 2 | 0 | ADC channel 6 power status. Applicable only for PCM6x60-Q1.<br>0d = ADC channel is powered down<br>1d = ADC channel is powered up | | 0 |
| 1 | 0 | Reserved | | 0 |
| 0 | 0 | Reserved | | 0 |

| | 01110111 | Address : 0x77 | | 0x80 |
|---|---|---|---|---|
| | 10000000 | Default Value : 0x80 | | 10000000 |
| bit | default | Definition | Description | Setting |
| 7 | 1 | Device mode status.<br>4d = Device is in sleep mode or software shutdown mode | | 1 |
| 6 | 0 | 6d = Device is in active mode with all ADC channels turned off | | 0 |
| 5 | 0 | 7d = Device is in active mode with at least one ADC channel turned on | | 0 |
| 4 | 0 | Boost power up status.<br>0d = Boost is powered down<br>1d = Boost is powered up | | 0 |
| 3 | 0 | MICBIAS power up status.<br>0d = MICBIAS is powered down<br>1d = MICBIAS is powered up | | 0 |
| 2 | 0 | ADC channel power down status caused by INxx inputs faults.<br>0d = No ADC channel is powered down caused by INxx inputs faults<br>1d = Atleast a ADC channel is powered down caused by INxx inputs faults | | 0 |
| 1 | 0 | ADC channel power down status caused by MICBIAS faults.<br>0d = No ADC channel is powered down caused by MICBIAS faults<br>1d = All ADC channels are powered down caused by MICBIAS faults | | 0 |
| 0 | 0 | Manual recovery (self-clearing bit).<br>0d = No effect<br>1d = Recheck all fault status and re-powerup ADC channels and/or MICBIAS if they do not have any faults. Before setting this bit, reset P0_R58 register and re-configure P0_R58 to desired setting only after manual recover gets over. | | 0 |

| | 01111110 | Address : 0x7E | | 0x00 |
|---|---|---|---|---|
| | 00000000 | Default Value : 0x00 | | 00000000 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | These bits return the I2C transactions checksum value. Writing to this register resets the checksum to the written value. This register is updated on writes to other registers on all pages. | checksum用 | 0 |
| 6 | 0 | | | 0 |
| 5 | 0 | | | 0 |
| 4 | 0 | | | 0 |
| 3 | 0 | | | 0 |
| 2 | 0 | | | 0 |
| 1 | 0 | | | 0 |
| 0 | 0 | | | 0 |

| page<br>0x01 | | 00000000 | Address : 0x00 | | **0x01** |
|---|---|---|---|---|---|
| | | 00000000 | Default Value : 0x00 | | 00000001 |
| | bit | default | Definition | Description | Setting |
| | 7 | 0 | These bits set the device page.<br>0d = Page 0<br>1d = Page 1<br>...<br>255d = Page 255 | page页选择<br>page0x00选择00<br>page0x01选择01 | 0 |
| | 6 | 0 | | | 0 |
| | 5 | 0 | | | 0 |
| | 4 | 0 | | | 0 |
| | 3 | 0 | | | 0 |
| | 2 | 0 | | | 0 |
| | 1 | 0 | | | 0 |
| | 0 | 0 | | | **1** |

| | 00010110 | Address : 0x16 | | 0x00 |
|---|---|---|---|---|
| | 00000000 | Default Value : 0x00 | | 00000000 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | MICBIAS internal load sink setting.<br>0d = MICBIAS internal load sink is enabled with setting automatically calculated based on device configuration<br>1d = MICBIAS internal load sink is enabled based on D6-4 register bits; This setting must be used for single-ended AC-coupled input to support high signal swing | Default | 0 |
| 6 | 0 | MICBIAS internal load sink current value<br>0d = MICBIAS internal load sink current is set to 0 mA (typ)<br>1d = MICBIAS internal load sink current is set to 4.3 mA (typ)<br>2d = MICBIAS internal load sink current is set to 8.6 mA (typ)<br>3d = MICBIAS internal load sink current is set to 12.9 mA (typ)<br>4d = MICBIAS internal load sink current is set to 17.2 mA (typ)<br>5d = MICBIAS internal load sink current is set to 21.5 mA (typ)<br>6d = MICBIAS internal load sink current is set to 25.8 mA (typ)<br>7d = MICBIAS internal load sink current is set to 30.1 mA (typ) | Default | 0 |
| 5 | 0 | | | 0 |
| 4 | 0 | | | 0 |
| 3 | 0 | Reserved | | 0 |
| 2 | 0 | | | 0 |
| 1 | 0 | | | 0 |
| 0 | 0 | | | 0 |

| | 00101100 | Address : 0x2C | | 0x00 |
|---|---|---|---|---|
| | 00000000 | Default Value : 0x00 | | 00000000 |
| bit | default | Definition | Description | Setting |

| | | | | |
|---|---|---|---|---|
| 7 | 0 | Fault status for an ASI bus clock error.<br>0d = No fault detected<br>1d = Fault detected | | 0 |
| 6 | 0 | Status of PLL lock.<br>0d = No PLL lock detected<br>1d = PLL lock detected | | 0 |
| 5 | 0 | Fault status for boost or MICBIAS over temperature.<br>0d = No fault detected<br>1d = Fault detected | | 0 |
| 4 | 0 | Fault status for boost or MICBIAS over current.<br>0d = No fault detected<br>1d = Fault detected | | 0 |
| 3 | 0 | Reserved | | 0 |
| 2 | 0 | Reserved | | 0 |
| 1 | 0 | Reserved | | 0 |
| 0 | 0 | Reserved | | 0 |

| | 00101101 | Address : 0x2D | | 0x00 |
|---|---|---|---|---|
| | 00000000 | Default Value : 0x00 | | 00000000 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | Status of CH1_LIVE.<br>0d = No faults occurred in channel 1<br>1d = Atleast a fault has occurred in channel 1 | | 0 |
| 6 | 0 | Status of CH2_LIVE.<br>0d = No faults occurred in channel 2<br>1d = Atleast a fault has occurred in channel 2 | | 0 |
| 5 | 0 | Status of CH3_LIVE.<br>0d = No faults occurred in channel 3<br>1d = Atleast a fault has occurred in channel 3 | | 0 |
| 4 | 0 | Status of CH4_LIVE.<br>0d = No faults occurred in channel 4<br>1d = Atleast a fault has occurred in channel 4 | | 0 |
| 3 | 0 | Status of CH5_LIVE. Applicable only for PCM6x60-Q1.<br>0d = No faults occurred in channel 5<br>1d = Atleast a fault has occurred in channel 5 | | 0 |
| 2 | 0 | Status of CH6_LIVE. Applicable only for PCM6x60-Q1.<br>0d = No faults occurred in channel 6<br>1d = Atleast a fault has occurred in channel 6 | | 0 |
| 1 | 0 | Status of short to VBAT_IN fault detected when VBAT_IN is less than MICBIAS.<br>0d = Short to VBAT_IN fault when VBAT_IN is less than MICBIAS has not occurred in any channel<br>1d = Short to VBAT_IN fault when VBAT_IN is less than MICBIAS has occurred in atleast one channel | | 0 |
| 0 | 0 | Reserved | | 0 |

| | 00101110 | Address : 0x2E | | 0x00 |
|---|---|---|---|---|
| | 00000000 | Default Value : 0x00 | | 00000000 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | Channel 1 open input fault status.<br>0d = No open input detected<br>1d = Open input detected | | 0 |
| 6 | 0 | Channel 1 input pair short fault status.<br>0d = No input pair short detected<br>1d = Input short to each other detected | | 0 |
| 5 | 0 | Channel 1 IN1P short to ground fault status.<br>0d = IN1P no short to ground detected<br>1d = IN1P short to ground detected | | 0 |
| 4 | 0 | Channel 1 IN1M short to ground fault status.<br>0d = IN1M no short to ground detected<br>1d = IN1M short to ground detected | | 0 |
| 3 | 0 | Channel 1 IN1P short to MICBIAS fault status.<br>0d = IN1P no short to MICBIAS detected<br>1d = IN1P short to MICBIAS detected | | 0 |
| 2 | 0 | Channel 1 IN1M short to MICBIAS fault status.<br>0d = IN1M no short to MICBIAS detected<br>1d = IN1M short to MICBIAS detected | | 0 |
| 1 | 0 | Channel 1 IN1P short to VBAT_IN fault status.<br>0d = IN1P no short to VBAT_IN detected<br>1d = IN1P short to VBAT_IN detected | | 0 |
| 0 | 0 | Channel 1 IN1M short to VBAT_IN fault status.<br>0d = IN1M no short to VBAT_IN detected<br>1d = IN1M short to VBAT_IN detected | | 0 |

| | 00101111 | Address : 0x2F | | 0x00 |
|---|---|---|---|---|
| | 00000000 | Default Value : 0x00 | | 00000000 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | Channel 2 open input fault status.<br>0d = No open input detected<br>1d = Open input detected | | 0 |
| 6 | 0 | Channel 2 input pair short fault status.<br>0d = No input pair short detected<br>1d = Input short to each other detected | | 0 |
| 5 | 0 | Channel 2 IN2P short to ground fault status.<br>0d = IN2P no short to ground detected<br>1d = IN2P short to ground detected | | 0 |
| 4 | 0 | Channel 2 IN2M short to ground fault status.<br>0d = IN2M no short to ground detected<br>1d = IN2M short to ground detected | | 0 |

| | | | | |
|---|---|---|---|---|
| 3 | 0 | Channel 2 IN2P short to MICBIAS fault status.<br>0d = IN2P no short to MICBIAS detected<br>1d = IN2P short to MICBIAS detected | | 0 |
| 2 | 0 | Channel 2 IN2M short to MICBIAS fault status.<br>0d = IN2M no short to MICBIAS detected<br>1d = IN2M short to MICBIAS detected | | 0 |
| 1 | 0 | Channel 2 IN2P short to VBAT_IN fault status.<br>0d = IN2P no short to VBAT_IN detected<br>1d = IN2P short to VBAT_IN detected | | 0 |
| 0 | 0 | Channel 2 IN2M short to VBAT_IN fault status.<br>0d = IN2M no short to VBAT_IN detected<br>1d = IN2M short to VBAT_IN detected | | 0 |

| | 00110000 | Address : 0x30 | | 0x00 |
|---|---|---|---|---|
| | 00000000 | Default Value : 0x00 | | 00000000 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | Channel 3 open input fault status.<br>0d = No open input detected<br>1d = Open input detected | | 0 |
| 6 | 0 | Channel 3 input pair short fault status.<br>0d = No input pair short detected<br>1d = Input short to each other detected | | 0 |
| 5 | 0 | Channel 3 IN3P short to ground fault status.<br>0d = IN3P no short to ground detected<br>1d = IN3P short to ground detected | | 0 |
| 4 | 0 | Channel 3 IN3M short to ground fault status.<br>0d = IN3M no short to ground detected<br>1d = IN3M short to ground detected | | 0 |
| 3 | 0 | Channel 3 IN3P short to MICBIAS fault status.<br>0d = IN3P no short to MICBIAS detected<br>1d = IN3P short to MICBIAS detected | | 0 |
| 2 | 0 | Channel 3 IN3M short to MICBIAS fault status.<br>0d = IN3M no short to MICBIAS detected<br>1d = IN3M short to MICBIAS detected | | 0 |
| 1 | 0 | Channel 3 IN3P short to VBAT_IN fault status.<br>0d = IN3P no short to VBAT_IN detected<br>1d = IN3P short to VBAT_IN detected | | 0 |
| 0 | 0 | Channel 3 IN3M short to VBAT_IN fault status.<br>0d = IN3M no short to VBAT_IN detected<br>1d = IN3M short to VBAT_IN detected | | 0 |

| | 00110001 | Address : 0x31 | | 0x00 |
|---|---|---|---|---|
| | 00000000 | Default Value : 0x00 | | 00000000 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | Channel 4 open input fault status.<br>0d = No open input detected<br>1d = Open input detected | | 0 |
| 6 | 0 | Channel 4 input pair short fault status.<br>0d = No input pair short detected<br>1d = Input short to each other detected | | 0 |
| 5 | 0 | Channel 4 IN4P short to ground fault status.<br>0d = IN4P no short to ground detected<br>1d = IN4P short to ground detected | | 0 |
| 4 | 0 | Channel 4 IN4M short to ground fault status.<br>0d = IN4M no short to ground detected<br>1d = IN4M short to ground detected | | 0 |
| 3 | 0 | Channel 4 IN4P short to MICBIAS fault status.<br>0d = IN4P no short to MICBIAS detected<br>1d = IN4P short to MICBIAS detected | | 0 |
| 2 | 0 | Channel 4 IN4M short to MICBIAS fault status.<br>0d = IN4M no short to MICBIAS detected<br>1d = IN4M short to MICBIAS detected | | 0 |
| 1 | 0 | Channel 4 IN4P short to VBAT_IN fault status.<br>0d = IN4P no short to VBAT_IN detected<br>1d = IN4P short to VBAT_IN detected | | 0 |
| 0 | 0 | Channel 4 IN4M short to VBAT_IN fault status.<br>0d = IN4M no short to VBAT_IN detected<br>1d = IN4M short to VBAT_IN detected | | 0 |

| | 00110010 | Address : 0x32 | | 0x00 |
|---|---|---|---|---|
| | 00000000 | Default Value : 0x00 | | 00000000 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | Channel 5 open input fault status.<br>0d = No open input detected<br>1d = Open input detected | | 0 |
| 6 | 0 | Channel 5 input pair short fault status.<br>0d = No input pair short detected<br>1d = Input short to each other detected | | 0 |
| 5 | 0 | Channel 5 IN5P short to ground fault status.<br>0d = IN5P no short to ground detected<br>1d = IN5P short to ground detected | | 0 |
| 4 | 0 | Channel 5 IN5M short to ground fault status.<br>0d = IN5M no short to ground detected<br>1d = IN5M short to ground detected | | 0 |
| 3 | 0 | Channel 5 IN5P short to MICBIAS fault status.<br>0d = IN5P no short to MICBIAS detected<br>1d = IN5P short to MICBIAS detected | | 0 |
| 2 | 0 | Channel 5 IN5M short to MICBIAS fault status.<br>0d = IN5M no short to MICBIAS detected<br>1d = IN5M short to MICBIAS detected | | 0 |

| | | | | |
|---|---|---|---|---|
| 1 | 0 | Channel 5 IN5P short to VBAT_IN fault status.<br>0d = IN5P no short to VBAT_IN detected<br>1d = IN5P short to VBAT_IN detected | | 0 |
| 0 | 0 | Channel 5 IN5M short to VBAT_IN fault status.<br>0d = IN5M no short to VBAT_IN detected<br>1d = IN5M short to VBAT_IN detected | | 0 |

| | 00110011 | Address : 0x33 | | 0x00 |
|---|---|---|---|---|
| | 00000000 | Default Value : 0x00 | | 00000000 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | Channel 6 open input fault status.<br>0d = No open input detected<br>1d = Open input detected | | 0 |
| 6 | 0 | Channel 6 input pair short fault status.<br>0d = No input pair short detected<br>1d = Input short to each other detected | | 0 |
| 5 | 0 | Channel 6 IN6P short to ground fault status.<br>0d = IN6P no short to ground detected<br>1d = IN6P short to ground detected | | 0 |
| 4 | 0 | Channel 6 IN6M short to ground fault status.<br>0d = IN6M no short to ground detected<br>1d = IN6M short to ground detected | | 0 |
| 3 | 0 | Channel 6 IN6P short to MICBIAS fault status.<br>0d = IN6P no short to MICBIAS detected<br>1d = IN6P short to MICBIAS detected | | 0 |
| 2 | 0 | Channel 6 IN6M short to MICBIAS fault status.<br>0d = IN6M no short to MICBIAS detected<br>1d = IN6M short to MICBIAS detected | | 0 |
| 1 | 0 | Channel 6 IN6P short to VBAT_IN fault status.<br>0d = IN6P no short to VBAT_IN detected<br>1d = IN6P short to VBAT_IN detected | | 0 |
| 0 | 0 | Channel 6 IN6M short to VBAT_IN fault status.<br>0d = IN6M no short to VBAT_IN detected<br>1d = IN6M short to VBAT_IN detected | | 0 |

| | 00110101 | Address : 0x35 | | 0x00 |
|---|---|---|---|---|
| | 00000000 | Default Value : 0x00 | | 00000000 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | Channel 1 IN1P over voltage fault status.<br>0d = No IN1P over voltage fault detected<br>1d = IN1P over voltage fault has detected | | 0 |
| 6 | 0 | Channel 2 IN2P over voltage fault status.<br>0d = No IN2P over voltage fault detected<br>1d = IN2P over voltage fault has detected | | 0 |
| 5 | 0 | Channel 3 IN3P over voltage fault status.<br>0d = No IN3P over voltage fault detected<br>1d = IN3P over voltage fault has detected | | 0 |
| 4 | 0 | Channel 4 IN4P over voltage fault status.<br>0d = No IN4P over voltage fault detected<br>1d = IN4P over voltage fault has detected | | 0 |
| 3 | 0 | Channel 5 IN5P over voltage fault status. Applicable only for PCM6x60-Q1.<br>0d = No IN5P over voltage fault detected<br>1d = IN5P over voltage fault has detected | | 0 |
| 2 | 0 | Channel 6 IN6P over voltage fault status. Applicable only for PCM6x60-Q1.<br>0d = No IN6P over voltage fault detected<br>1d = IN6P over voltage fault has detected | | 0 |
| 1 | 0 | Reserved | | 0 |
| 0 | 0 | | | 0 |

| | 00110111 | Address : 0x37 | | 0x00 |
|---|---|---|---|---|
| | 00000000 | Default Value : 0x00 | | 00000000 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | Fault status for MICBIAS high current.<br>0d = No fault detected<br>1d = Fault detected | | 0 |
| 6 | 0 | Fault status for MICBIAS low current<br>0d = No fault detected<br>1d = Fault detected | | 0 |
| 5 | 0 | Fault status for MICBIAS over voltage.<br>0d = No fault detected<br>1d = Fault detected | | 0 |
| 4 | 0 | Reserved | | 0 |
| 3 | 0 | | | 0 |
| 2 | 0 | | | 0 |
| 1 | 0 | | | 0 |
| 0 | 0 | | | 0 |

| | 01010101 | Address : 0x55 | | 0x40 |
|---|---|---|---|---|
| | 01000000 | Default Value : 0x40 | | 01000000 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | MICBIAS overvoltage fault detection threshold above MICBIAS programmed voltage.<br>0d = No threshold over programmed voltage<br>1d = 10 mV (typ) threshold over programmed voltage<br>2d = 40 mV (typ) threshold over programmed voltage (default)<br>3d to 6d = Threshold value is set as per configuration with step size of 30mV (typ)<br>7d = 190 mV (typ) threshold over programmed voltage (default) | MICBIAS过压40mV阈值 | 0 |
| 6 | 1 | | | 1 |
| 5 | 0 | | | 0 |
| 4 | 0 | | | 0 |

| | | | | |
|---|---|---|---|---|
| 3 | 0 | Reserved | | 0 |
| 2 | 0 | | | 0 |
| 1 | 0 | | | 0 |
| 0 | 0 | | | 0 |

| | 01011001 | Address : 0x59 | | 0x00 |
|---|---|---|---|---|
| | 00000000 | Default Value : 0x00 | | 00000000 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | Reserved | | 0 |
| 6 | 0 | | | 0 |
| 5 | 0 | | | 0 |
| 4 | 0 | | | 0 |
| 3 | 0 | Reserved | | 0 |
| 2 | 0 | | | 0 |
| 1 | 0 | | | 0 |
| 0 | 0 | Hold SAR data update during register readback.<br>0b= Data update is not held, data register is continuously updated; this setting must be used when moving average is enabled for fault detection<br>1b= Data update is held, data register readback can be done | Default | 0 |

| | 01011010 | Address : 0x5A | | 0x00 |
|---|---|---|---|---|
| | 00000000 | Default Value : 0x00 | | 00000000 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | Diagnostic SAR monitor data MSB byte | | 0 |
| 6 | 0 | | | 0 |
| 5 | 0 | | | 0 |
| 4 | 0 | | | 0 |
| 3 | 0 | | | 0 |
| 2 | 0 | | | 0 |
| 1 | 0 | | | 0 |
| 0 | 0 | | | 0 |

| | 01011011 | Address : 0x5B | | 0x00 |
|---|---|---|---|---|
| | 00000000 | Default Value : 0x00 | | 00000000 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | Diagnostic SAR monitor data LSB nibble | | 0 |
| 6 | 0 | | | 0 |
| 5 | 0 | | | 0 |
| 4 | 0 | | | 0 |
| 3 | 0 | Channel ID value | | 0 |
| 2 | 0 | | | 0 |
| 1 | 0 | | | 0 |
| 0 | 0 | | | 0 |

| | 01011100 | Address : 0x5C | | 0x00 |
|---|---|---|---|---|
| | 00000000 | Default Value : 0x00 | | 00000000 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | Diagnostic SAR monitor data MSB byte | | 0 |
| 6 | 0 | | | 0 |
| 5 | 0 | | | 0 |
| 4 | 0 | | | 0 |
| 3 | 0 | | | 0 |
| 2 | 0 | | | 0 |
| 1 | 0 | | | 0 |
| 0 | 0 | | | 0 |

| | 01011101 | Address : 0x5D | | 0x01 |
|---|---|---|---|---|
| | 00000001 | Default Value : 0x01 | | 00000001 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | Diagnostic SAR monitor data LSB nibble | | 0 |
| 6 | 0 | | | 0 |
| 5 | 0 | | | 0 |
| 4 | 0 | | | 0 |
| 3 | 0 | Channel ID value | | 0 |
| 2 | 0 | | | 0 |
| 1 | 0 | | | 0 |
| 0 | 1 | | | 1 |

| | 01011110 | Address : 0x5E | | 0x00 |
|---|---|---|---|---|
| | 00000000 | Default Value : 0x00 | | 00000000 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | Diagnostic SAR monitor data MSB byte | | 0 |
| 6 | 0 | | | 0 |
| 5 | 0 | | | 0 |
| 4 | 0 | | | 0 |
| 3 | 0 | | | 0 |
| 2 | 0 | | | 0 |
| 1 | 0 | | | 0 |
| 0 | 0 | | | 0 |

| | 01011111 | Address : 0x5F | | 0x00 |
|---|---|---|---|---|
| | 00000000 | Default Value : 0x00 | | 00000000 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | Diagnostic SAR monitor data LSB nibble | | 0 |
| 6 | 0 | | | 0 |
| 5 | 0 | | | 0 |
| 4 | 0 | | | 0 |
| 3 | 0 | Channel ID value | | 0 |
| 2 | 0 | | | 0 |
| 1 | 0 | | | 0 |

| | | | | |
|---|---|---|---|---|
| 0 | 0 | | | 0 |

| | | | | |
|---|---|---|---|---|
| | 01100000 | Address : 0x60 | | 0x00 |
| | 00000000 | Default Value : 0x00 | | 00000000 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | Diagnostic SAR monitor data MSB byte | | 0 |
| 6 | 0 | | | 0 |
| 5 | 0 | | | 0 |
| 4 | 0 | | | 0 |
| 3 | 0 | | | 0 |
| 2 | 0 | | | 0 |
| 1 | 0 | | | 0 |
| 0 | 0 | | | 0 |

| | | | | |
|---|---|---|---|---|
| | 01100001 | Address : 0x61 | | 0x03 |
| | 00000011 | Default Value : 0x03 | | 00000011 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | Diagnostic SAR monitor data LSB nibble | | 0 |
| 6 | 0 | | | 0 |
| 5 | 0 | | | 0 |
| 4 | 0 | | | 0 |
| 3 | 0 | Channel ID value | | 0 |
| 2 | 0 | | | 0 |
| 1 | 1 | | | 1 |
| 0 | 1 | | | 1 |

| | | | | |
|---|---|---|---|---|
| | 01100010 | Address : 0x62 | | 0x00 |
| | 00000000 | Default Value : 0x00 | | 00000000 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | Diagnostic SAR monitor data MSB byte | | 0 |
| 6 | 0 | | | 0 |
| 5 | 0 | | | 0 |
| 4 | 0 | | | 0 |
| 3 | 0 | | | 0 |
| 2 | 0 | | | 0 |
| 1 | 0 | | | 0 |
| 0 | 0 | | | 0 |

| | | | | |
|---|---|---|---|---|
| | 01100011 | Address : 0x63 | | 0x04 |
| | 00000100 | Default Value : 0x04 | | 00000100 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | Diagnostic SAR monitor data LSB nibble | | 0 |
| 6 | 0 | | | 0 |
| 5 | 0 | | | 0 |
| 4 | 0 | | | 0 |
| 3 | 0 | Channel ID value | | 0 |
| 2 | 1 | | | 1 |
| 1 | 0 | | | 0 |
| 0 | 0 | | | 0 |

| | | | | |
|---|---|---|---|---|
| | 01100100 | Address : 0x64 | | 0x00 |
| | 00000000 | Default Value : 0x00 | | 00000000 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | Diagnostic SAR monitor data MSB byte | | 0 |
| 6 | 0 | | | 0 |
| 5 | 0 | | | 0 |
| 4 | 0 | | | 0 |
| 3 | 0 | | | 0 |
| 2 | 0 | | | 0 |
| 1 | 0 | | | 0 |
| 0 | 0 | | | 0 |

| | | | | |
|---|---|---|---|---|
| | 01100101 | Address : 0x65 | | 0x05 |
| | 00000101 | Default Value : 0x05 | | 00000101 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | Diagnostic SAR monitor data LSB nibble | | 0 |
| 6 | 0 | | | 0 |
| 5 | 0 | | | 0 |
| 4 | 0 | | | 0 |
| 3 | 0 | Channel ID value | | 0 |
| 2 | 1 | | | 1 |
| 1 | 0 | | | 0 |
| 0 | 1 | | | 1 |

| | | | | |
|---|---|---|---|---|
| | 01100110 | Address : 0x66 | | 0x00 |
| | 00000000 | Default Value : 0x00 | | 00000000 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | Diagnostic SAR monitor data MSB byte | | 0 |
| 6 | 0 | | | 0 |
| 5 | 0 | | | 0 |
| 4 | 0 | | | 0 |
| 3 | 0 | | | 0 |
| 2 | 0 | | | 0 |
| 1 | 0 | | | 0 |
| 0 | 0 | | | 0 |

| | | | | |
|---|---|---|---|---|
| | 01100111 | Address : 0x67 | | 0x06 |
| | 00000110 | Default Value : 0x06 | | 00000110 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | | | 0 |

| | | | | |
|---|---|---|---|---|
| 6 | 0 | Diagnostic SAR monitor data LSB nibble | | 0 |
| 5 | 0 | | | 0 |
| 4 | 0 | | | 0 |
| 3 | 0 | Channel ID value | | 0 |
| 2 | 1 | | | 1 |
| 1 | 1 | | | 1 |
| 0 | 0 | | | 0 |

| | 01101000 | Address : 0x68 | | 0x00 |
|---|---|---|---|---|
| | 00000000 | Default Value : 0x00 | | 00000000 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | Diagnostic SAR monitor data MSB byte | | 0 |
| 6 | 0 | | | 0 |
| 5 | 0 | | | 0 |
| 4 | 0 | | | 0 |
| 3 | 0 | | | 0 |
| 2 | 0 | | | 0 |
| 1 | 0 | | | 0 |
| 0 | 0 | | | 0 |

| | 01101001 | Address : 0x69 | | 0x07 |
|---|---|---|---|---|
| | 00000111 | Default Value : 0x07 | | 00000111 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | Diagnostic SAR monitor data LSB nibble | | 0 |
| 6 | 0 | | | 0 |
| 5 | 0 | | | 0 |
| 4 | 0 | | | 0 |
| 3 | 0 | Channel ID value | | 0 |
| 2 | 1 | | | 1 |
| 1 | 1 | | | 1 |
| 0 | 1 | | | 1 |

| | 01101010 | Address : 0x6A | | 0x00 |
|---|---|---|---|---|
| | 00000000 | Default Value : 0x00 | | 00000000 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | Diagnostic SAR monitor data MSB byte | | 0 |
| 6 | 0 | | | 0 |
| 5 | 0 | | | 0 |
| 4 | 0 | | | 0 |
| 3 | 0 | | | 0 |
| 2 | 0 | | | 0 |
| 1 | 0 | | | 0 |
| 0 | 0 | | | 0 |

| | 01101011 | Address : 0x6B | | 0x08 |
|---|---|---|---|---|
| | 00001000 | Default Value : 0x08 | | 00001000 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | Diagnostic SAR monitor data LSB nibble | | 0 |
| 6 | 0 | | | 0 |
| 5 | 0 | | | 0 |
| 4 | 0 | | | 0 |
| 3 | 1 | Channel ID value | | 1 |
| 2 | 0 | | | 0 |
| 1 | 0 | | | 0 |
| 0 | 0 | | | 0 |

| | 01101100 | Address : 0x6C | | 0x00 |
|---|---|---|---|---|
| | 00000000 | Default Value : 0x00 | | 00000000 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | Diagnostic SAR monitor data MSB byte | | 0 |
| 6 | 0 | | | 0 |
| 5 | 0 | | | 0 |
| 4 | 0 | | | 0 |
| 3 | 0 | | | 0 |
| 2 | 0 | | | 0 |
| 1 | 0 | | | 0 |
| 0 | 0 | | | 0 |

| | 01101101 | Address : 0x6D | | 0x09 |
|---|---|---|---|---|
| | 00001001 | Default Value : 0x09 | | 00001001 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | Diagnostic SAR monitor data LSB nibble | | 0 |
| 6 | 0 | | | 0 |
| 5 | 0 | | | 0 |
| 4 | 0 | | | 0 |
| 3 | 1 | Channel ID value | | 1 |
| 2 | 0 | | | 0 |
| 1 | 0 | | | 0 |
| 0 | 1 | | | 1 |

| | 01101110 | Address : 0x6E | | 0x00 |
|---|---|---|---|---|
| | 00000000 | Default Value : 0x00 | | 00000000 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | Diagnostic SAR monitor data MSB byte | | 0 |
| 6 | 0 | | | 0 |
| 5 | 0 | | | 0 |
| 4 | 0 | | | 0 |
| 3 | 0 | | | 0 |
| 2 | 0 | | | 0 |
| 1 | 0 | | | 0 |

| | | | | |
|---|---|---|---|---|
| 0 | 0 | | | 0 |

| | | | | |
|---|---|---|---|---|
| | 01101111 | Address : 0x6F | | 0x0A |
| | 00001010 | Default Value : 0x0A | | 00001010 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | Diagnostic SAR monitor data LSB nibble | | 0 |
| 6 | 0 | | | 0 |
| 5 | 0 | | | 0 |
| 4 | 0 | | | 0 |
| 3 | 1 | Channel ID value | | 1 |
| 2 | 0 | | | 0 |
| 1 | 1 | | | 1 |
| 0 | 0 | | | 0 |

| | | | | |
|---|---|---|---|---|
| | 01110000 | Address : 0x70 | | 0x00 |
| | 00000000 | Default Value : 0x00 | | 00000000 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | Diagnostic SAR monitor data MSB byte | | 0 |
| 6 | 0 | | | 0 |
| 5 | 0 | | | 0 |
| 4 | 0 | | | 0 |
| 3 | 0 | | | 0 |
| 2 | 0 | | | 0 |
| 1 | 0 | | | 0 |
| 0 | 0 | | | 0 |

| | | | | |
|---|---|---|---|---|
| | 01110001 | Address : 0x71 | | 0x0B |
| | 00001011 | Default Value : 0x0B | | 00001011 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | Diagnostic SAR monitor data LSB nibble | | 0 |
| 6 | 0 | | | 0 |
| 5 | 0 | | | 0 |
| 4 | 0 | | | 0 |
| 3 | 1 | Channel ID value | | 1 |
| 2 | 0 | | | 0 |
| 1 | 1 | | | 1 |
| 0 | 1 | | | 1 |

| | | | | |
|---|---|---|---|---|
| | 01110010 | Address : 0x72 | | 0x00 |
| | 00000000 | Default Value : 0x00 | | 00000000 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | Diagnostic SAR monitor data MSB byte | | 0 |
| 6 | 0 | | | 0 |
| 5 | 0 | | | 0 |
| 4 | 0 | | | 0 |
| 3 | 0 | | | 0 |
| 2 | 0 | | | 0 |
| 1 | 0 | | | 0 |
| 0 | 0 | | | 0 |

| | | | | |
|---|---|---|---|---|
| | 01110011 | Address : 0x73 | | 0x0C |
| | 00001100 | Default Value : 0x0C | | 00001100 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | Diagnostic SAR monitor data LSB nibble | | 0 |
| 6 | 0 | | | 0 |
| 5 | 0 | | | 0 |
| 4 | 0 | | | 0 |
| 3 | 1 | Channel ID value | | 1 |
| 2 | 1 | | | 1 |
| 1 | 0 | | | 0 |
| 0 | 0 | | | 0 |

| | | | | |
|---|---|---|---|---|
| | 01110100 | Address : 0x74 | | 0x00 |
| | 00000000 | Default Value : 0x00 | | 00000000 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | Diagnostic SAR monitor data MSB byte | | 0 |
| 6 | 0 | | | 0 |
| 5 | 0 | | | 0 |
| 4 | 0 | | | 0 |
| 3 | 0 | | | 0 |
| 2 | 0 | | | 0 |
| 1 | 0 | | | 0 |
| 0 | 0 | | | 0 |

| | | | | |
|---|---|---|---|---|
| | 01110101 | Address : 0x75 | | 0x0D |
| | 00001101 | Default Value : 0x0D | | 00001101 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | Diagnostic SAR monitor data LSB nibble | | 0 |
| 6 | 0 | | | 0 |
| 5 | 0 | | | 0 |
| 4 | 0 | | | 0 |
| 3 | 1 | Channel ID value | | 1 |
| 2 | 1 | | | 1 |
| 1 | 0 | | | 0 |
| 0 | 1 | | | 1 |

| | | | | |
|---|---|---|---|---|
| | 01110110 | Address : 0x76 | | 0x00 |
| | 00000000 | Default Value : 0x00 | | 00000000 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | | | 0 |

| | | | | |
|---|---|---|---|---|
| 6 | 0 | Diagnostic SAR monitor data MSB byte | | 0 |
| 5 | 0 | | | 0 |
| 4 | 0 | | | 0 |
| 3 | 0 | | | 0 |
| 2 | 0 | | | 0 |
| 1 | 0 | | | 0 |
| 0 | 0 | | | 0 |

| | 01110111 | Address : 0x77 | | 0x0E |
|---|---|---|---|---|
| | 00001110 | Default Value : 0x0E | | 00001110 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | Diagnostic SAR monitor data LSB nibble | | 0 |
| 6 | 0 | | | 0 |
| 5 | 0 | | | 0 |
| 4 | 0 | | | 0 |
| 3 | 1 | Channel ID value | | 1 |
| 2 | 1 | | | 1 |
| 1 | 1 | | | 1 |
| 0 | 0 | | | 0 |

| | 01111000 | Address : 0x78 | | 0x00 |
|---|---|---|---|---|
| | 00000000 | Default Value : 0x00 | | 00000000 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | Diagnostic SAR monitor data MSB byte | | 0 |
| 6 | 0 | | | 0 |
| 5 | 0 | | | 0 |
| 4 | 0 | | | 0 |
| 3 | 0 | | | 0 |
| 2 | 0 | | | 0 |
| 1 | 0 | | | 0 |
| 0 | 0 | | | 0 |

| | 01111001 | Address : 0x79 | | 0x0F |
|---|---|---|---|---|
| | 00001111 | Default Value : 0x0F | | 00001111 |
| bit | default | Definition | Description | Setting |
| 7 | 0 | Diagnostic SAR monitor data LSB nibble | | 0 |
| 6 | 0 | | | 0 |
| 5 | 0 | | | 0 |
| 4 | 0 | | | 0 |
| 3 | 1 | Channel ID value | | 1 |
| 2 | 1 | | | 1 |
| 1 | 1 | | | 1 |
| 0 | 1 | | | 1 |