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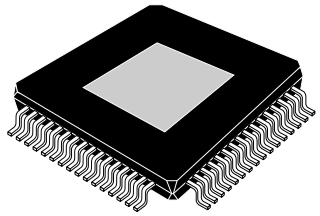
HFDA801L

Datasheet

4 channels digital input class-D automotive audio amplifier with Hi-Fi audio quality, advanced diagnostics, 2 MHz switching frequency and high resolution bandwidth



LQFP64
(exposed pad up)

Product summary		
Order code	**Package**	**Packing**
HFDA801L-VYY	LQFP64 (exp. pad up)	Tray
HFDA801L-VYT		Tape and reel

Features

- AEC-Q100 qualified
- Integrated 120 dB D/A conversion
- I^2S and TDM digital input (up to 16 CH TDM)
- Selectable input sample rate frequency (44.1/48/96/192 kHz)
- Wide supply operating range: 4.5 V - 18 V (5 V min at turn-on transition)
- PWM 2 MHz switching PWM:
  - Reduced size and cost of output LC
- High resolution bandwidth support:
  - Up to 40 kHz (I^2S 96 kHz) with attenuation [0 dB, -2 dB]
  - Up to 80 kHz (I^2S 192 kHz) with attenuation [0 dB, -2 dB]
- 4 I^2C addresses
- 4 Ω, 2 Ω, 1 Ω driving with output channels parallelization
- MOSFET power outputs allowing high output power capability:
  - Typ 4 x 30 W/4 Ω at 14.4 V, 1 kHz THD = 10%
  - Typ 4 x 25 W/4 Ω at 14.4 V, 1 kHz THD = 1%
  - Typ 4 x 50 W/2 Ω at 14.4 V 1 kHz THD = 10 %
- I^2C full configurability and diagnostic:
  - 4 x thermal warning and average junction temperature measurement on I^2C (8 bits)
  - AC and DC diagnostic (independent of channel)
  - OCP protection scheme configurable (4 x OCP limit selectable)
  - Mute time configuration
  - DIM (digital impedance meter)
  - Feedback after filter configuration
- Capability to run complete diagnostic in play:
  - Short to GND/VCC
  - DC offset detector
- Extremely low noise:
  - 13 µV A-weighted; 20 kHz (high gain) typ
- Very low THD:
  - 0.02% at 1 W 1 kHz on 4 and 2 Ω loads typ
  - 0.08% 20-20 kHz (full audio band) on 4 and 2 Ω loads (1 W)
- CD/diag pin (3 selectable CD thresholds)
- Synchronization output pin (only with TDM input stream, on I^2Sdata2)
- Channel independent mute/play/gain selection/diagnostic
- Open load in play
- Battery load dump compatible (40 V)
- Immune to pop/tick noise at turn on/off, battery variations (inside the operative range), during diagnostic

- EMI compliance evaluated according to CISPR25
- Legacy (no I^2C mode)
- Integrated short circuit protections
- ESD integrated protections (2 kV HBM, 500 V/750 V corner CDM)
- LQFP64 exposed pad up package

Description

HFDA801L is the new ST class-D audio amplifier, specifically designed for automotive applications in the latest BCD technology. The HFDA801L integrates a 24-bit 120 dB DAC conversion, and features 2 MHz switching PWM class D output stage. This configuration enables the design of a compact and inexpensive application, reaching at the same time outstanding level of audio performances. HFDA801L supports wide band applications (80 kHz), with extremely low level of noise and low THD. Moreover it features the most complete diagnostic matrix, including full diagnostic in play to support the most demanding OEM requirements in terms of speaker control and system robustness/ reliability. HFDA801L supports start stop cranking down to 4.5 V (5 V at turn on) and it is housed in a very compact and thin LQFP 10x10 package. Thus the HFDA801L is suitable for any level of automotive application.

1 Block diagram and pins description

Figure 1. **Block diagram**

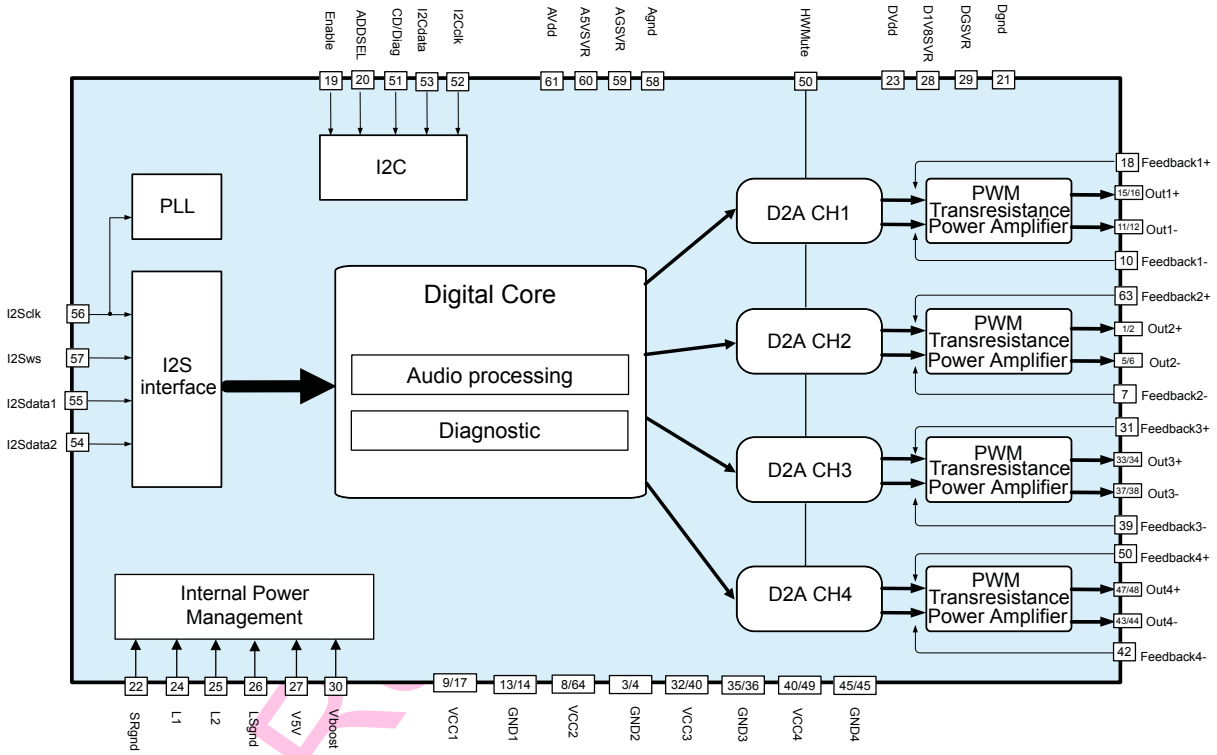


Figure 2. **Pin connection diagram (top view)**

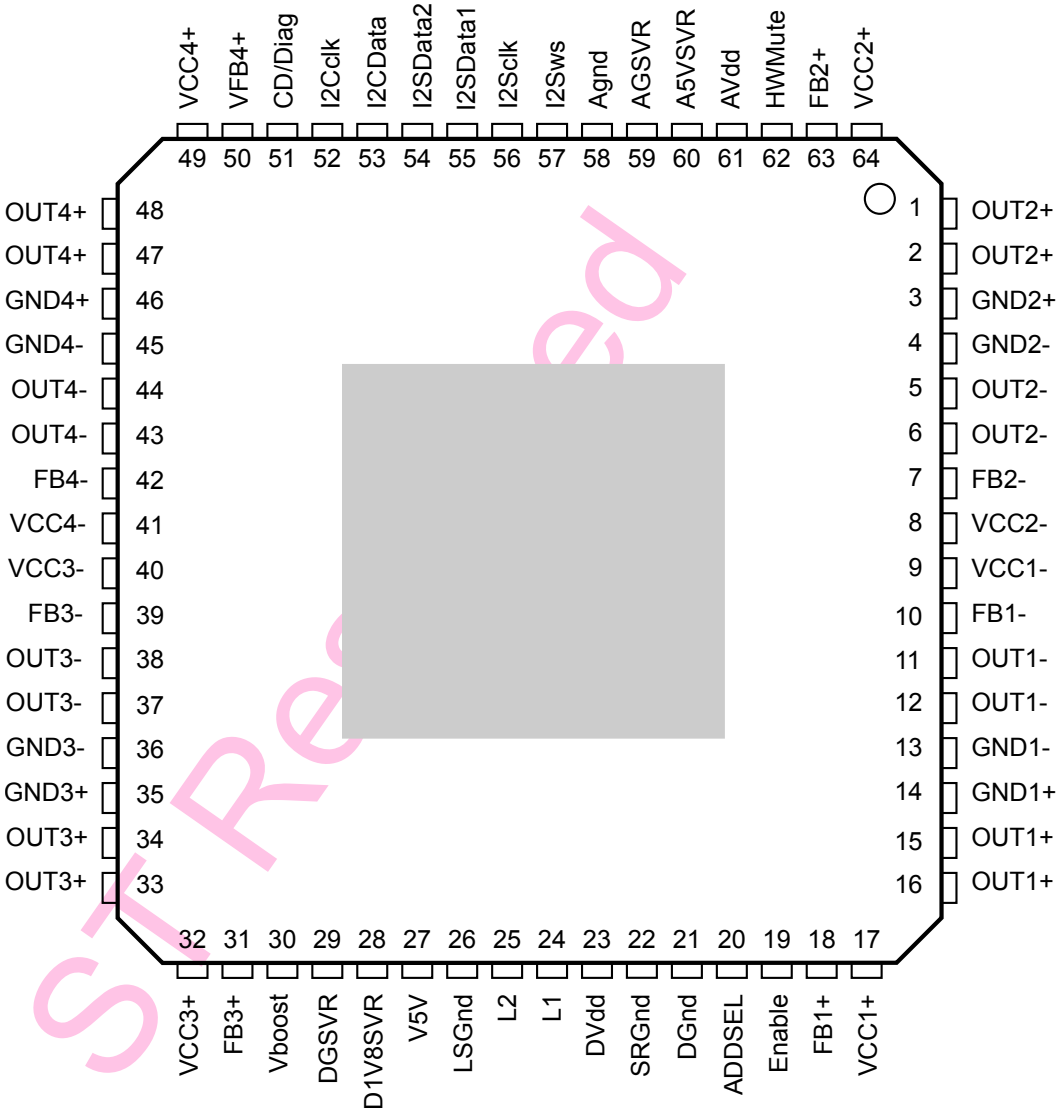


Table 1. **Pins list description**

#	Pin	Function
1	OUT2+	Channel 2, half bridge plus, output
2	OUT2+	Channel 2, half bridge plus, output
3	GND2+	Channel 2, half bridge plus, power ground
4	GND2-	Channel 2, half bridge minus, power ground
5	OUT2-	Channel 2, half bridge minus, output
6	OUT2-	Channel 2, half bridge minus, output
7	FB2-	Channel 2, half bridge minus, feedback
8	VCC2-	Channel 2, half bridge minus, power supply
9	VCC1-	Channel 1, half bridge minus, power supply
10	FB1-	Channel 1, half bridge minus, feedback
11	OUT1-	Channel 1, half bridge minus, output
12	OUT1-	Channel 1, half bridge minus, output

#	Pin	Function
13	GND1-	Channel 1, half bridge minus, power ground
14	GND1+	Channel 1, half bridge plus, power ground
15	OUT1+	Channel 1, half bridge plus, output
16	OUT1+	Channel 1, half bridge plus, output
17	VCC1+	Channel 1, half bridge plus, power supply
18	FB1+	Channel 1, half bridge plus, feedback
19	Enable	Enable pin
20	ADDSel	Address selection pin, input
21	DGnd	Digital ground
22	SRGnd	Power management ground 1
23	DVdd	Digital power Supply
24	L1	Power management inductor side1
25	L2	Power management inductor side2
26	LSGnd	Power management ground 2
27	V5V	Internal 5 V supply
28	D1V8SVR	Positive digital supply V(SVR) + 0.9 V (internally generated)
29	DGSVR	Negative digital supply V(SVR) - 0.9 V (internally generated)
30	Vboost	Internal boost supply
31	FB3+	Channel 3, half bridge plus, feedback
32	VCC3+	Channel 1, half bridge plus, power supply
33	OUT3+	Channel 3, half bridge plus, output
34	OUT3+	Channel 3, half bridge plus, output
35	GND3+	Channel 3, half bridge plus, power ground
36	GND3-	Channel 3, half bridge minus, power ground
37	OUT3-	Channel 3, half bridge minus, output
38	OUT3-	Channel 3, half bridge minus, output
39	FB3-	Channel 3, half bridge minus, feedback
40	VCC3-	Channel 3, half bridge minus, power Supply
41	VCC4-	Channel 4, half bridge minus, power Supply
42	FB4-	Channel 4, half bridge minus, feedback
43	OUT4-	Channel 4, half bridge minus, output
44	OUT4-	Channel 4, half bridge minus, output
45	GND4-	Channel 4, half bridge minus, power ground
46	GND4+	Channel 4, half bridge plus, power ground
47	OUT4+	Channel 4, half bridge plus, output
48	OUT4+	Channel 4, half bridge plus, output
49	VCC4+	Channel 4, half bridge plus, Power Supply
50	FB4+	Channel 4, half bridge plus, Feedback
51	CD/Diag	Clipping detector and diagnostic output pin
52	I2CClk	I^2C clock
53	I2CData	I^2C data

#	Pin	Function
54	I2SData2	I²S/TDM data input 2
55	I2SData1	I²S/TDM data input 1
56	I2Sclk	I²S/TDM clock input
57	I2Sws	I²S/TDM sync input
58	Agnd	Analog ground
59	AGSVR	Negative analog supply V(SVR) - 2.5 V (internally generated)(1)
60	A5VSVR	Positive analog supply V(SVR) + 2.5 V (Internally generated)
61	AVdd	Analog supply
62	HWMute	Hardware mute pin
63	FB2+	Channel 2, half bridge plus, feedback
64	VCC2+	Channel 2, half bridge plus, power supply

1. *Internal circuit output pin: not to be controlled externally. AMR not applicable.*

2 Application diagram

Figure 3. **Application diagram (damping network: for example 4 Ω load application)**

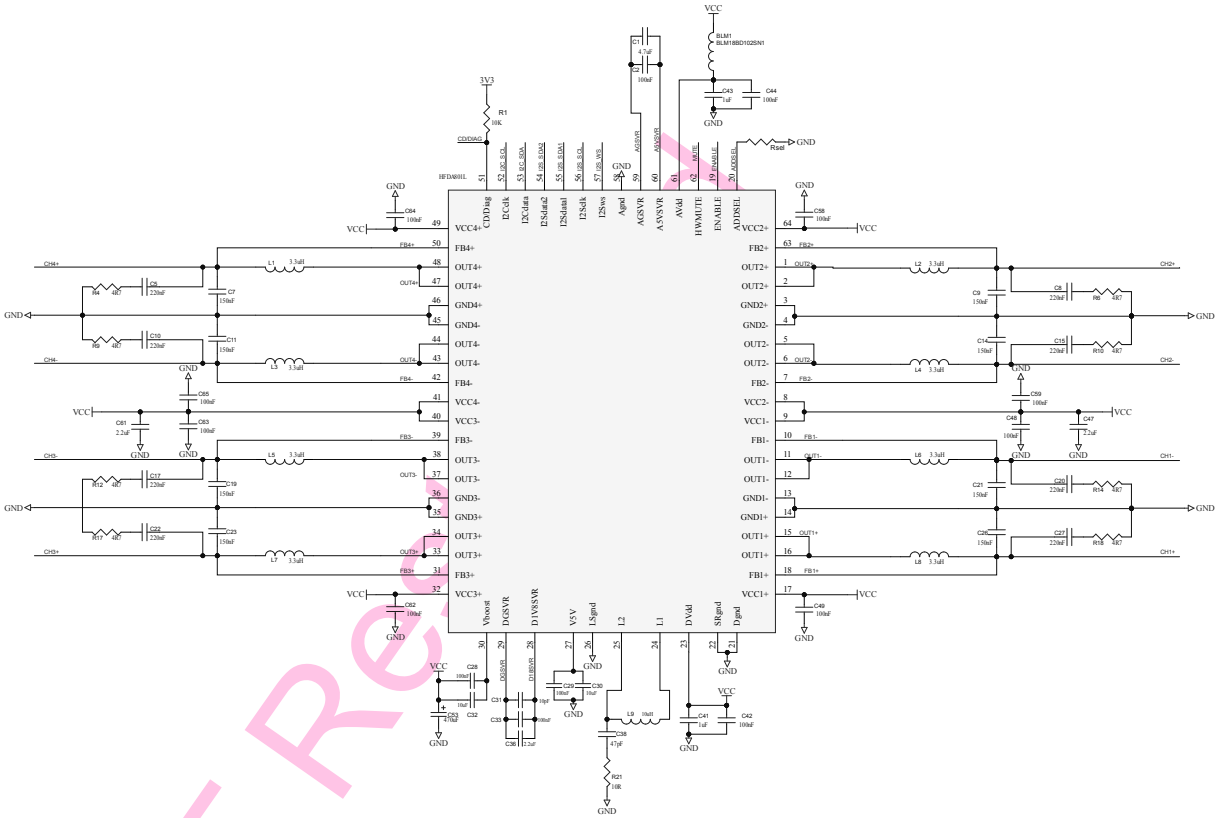
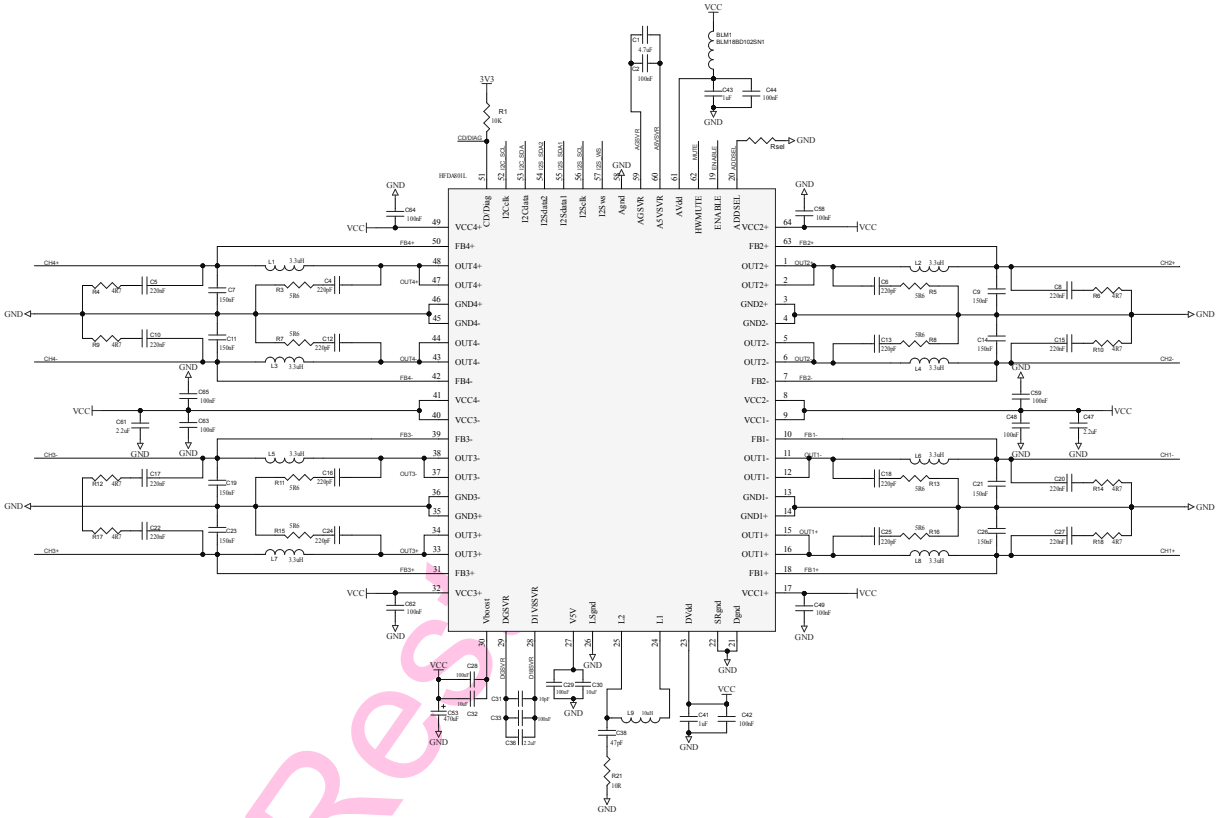


Figure 4. **Application diagram (damping and snubber network: for example 2 Ω load application)**



3 Electrical specifications

3.1 Absolute maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
VCC	DC supply voltage	-0.3 to 32	V
$[V_{CC(x)}+, V_{CC(x)}-, A_{VDD}, D_{VDD}]$	Transient supply voltage for t = 100 ms(1)	-0.3 to 40	V
GND_{max} $[GND_{(x)}+, GND_{(x)}-, A_{GND}, D_{GND}, SR_{GND}, LS_{GND}]$	Ground pin voltage difference	-0.3 to 0.3	V
$FB_{(x)}+, FB_{(x)}-$	Feedback pin	-0.3 to 32	V
$OUT_{(x)}+, OUT_{(x)}-$	Output pin	-0.3 to 32	V
L1	Internal regulator pin	-0.3 to 32	V
L2	Internal regulator pin	-0.3 to 40	V
I^2C_{data}, I^2C_{clk}	I²C bus pins voltage	-0.3 to 5.5	V
$I^2S_{data1}, I^2S_{data2}, I^2S_{clk}, I^2S_{WS}$	I²S bus pins voltage	-0.3 to 5.5	V
Enable	Enable pin voltage	-0.3 to 5.5	V
CD/Diag	CD/DIAG pin	-0.3 to 5.5	V
HWMute	Hardware Mute	-0.3 to 5.5	V
T_A	Ambient operating temperature	-40 to 105	°C
T_{stg}, T_J	Storage and junction temperature	-55 to 150	°C
ESD_{HBM}	ESD protection HBM(2)	2000	V
ESD_{CDM}	ESD protection CDM(2)	500	V

1. *Ramp time T_r = 2 ms.*
2. *Definition according to the international standard.*

3.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case(1)	1.26	°C/W

1. *Top cold plate as per Jedec best practice guidelines (JESD51) in contact with package top side (e-pad). Ambient temperature set to 85 °C.*

3.3 Electrical characteristics

V_{CC} = 14.4 V; R_L = 4 Ω; f = 1 kHz; T_A = 25 °C; F_S = 44.1 kHz; I^2C settings as per Table 15, unless otherwise specified. LC filter as specified in Section 9.4 External components guideline. Feedback after filter, PWM in In-phase modulation. Refer to application diagram in Figure 3.

Table 4. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
General characteristics						
V_{CC}	Supply voltage range	R_L = 4 Ω	4.5(1)	-	18	V
		R_L = 2 Ω	4.5(1)	-	18	V
I_{Vcc}	Quiescent current	Device in standby	-	-	2	µA
		Device ON(2)	-	225	265	mA
		Device in eco-mode	-	115	140	mA
OCP	Overcurrent protection(3)	OCP_0 (IB12 D5D4 = 00)	10.7	11.7	12.7	A
		OCP_1 (IB12 D5D4 = 01)	7.4	8.4	9.4	A
		OCP_2 (IB12 D5D4 = 10)	5.2	6.2	7.2	A
		OCP_3 (IB12 D5D4 = 11)	2.7	3.7	4.7	A
	Efficiency(4)	4x25 W, sine 1 kHz	-	85	-	%
V_{lowM}	V_{CC} low supply mute threshold(5)	During start stop crank, attenuation ≥ 60 dB (digital mute disabled)	-	4.2	4.4	V
	Start mute attenuation(5)	Mute attenuation at VCC = 4.5 V	-	2.2	2.8	dB
V_{ovsd}	V_{CC} overvoltage shutdown(5)	-	28	29	30	V
V_{highM}	High supply voltage mute threshold(4)(5)	V_{CC} = 18 V	27	28	29	V
$UVLO_{VCC}$	UVLO threshold	-	-	4	4.2	V
I2C_resth	I^2C reset threshold	-	-	3	3.25	V
Tsh	Thermal shutdown	-	175	185	195	°C
Tph	Thermal mute threshold(6)	Attenuation = 60 dB	165	175	185	°C
Tpl	Thermal mute threshold(6)	Attenuation = 0.5 dB	155	165	175	°C
Tw1	Thermal warning	-	145	155	165	°C
Tw2		-	135	145	155	°C
Tw3		-	122	132	142	°C
Tw4		-	105	115	125	°C
K_{TADC}	Thermal ADC data correlation factor	-	-	1.08	-	-
Audio characteristics						
Po	Output Power(7)	Max power; V_{CC} = 18 V	65	71	-	W
		Max power	42	48	-	W
		THD = 10%	27	30	-	W
		THD = 1%	22	24	-	W
		R_L = 2 Ω; THD 10%	47	52	-	W
		R_L = 2 Ω; THD 1%	41	45	-	W

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Po	Output Power(7)	R_L = 2 Ω; max power	81	85	-	W
Gv1	Voltage gain 1	Measured at -10 dB Fs	7.5	8.3	9.1	Vp
Gv2	Voltage gain 2		5.5	6.1	6.7	Vp
Gv3	Voltage gain 3		3.15	3.5	3.85	Vp
Gv4	Voltage gain 4		2.3	2.5	2.8	Vp
THD	Total harmonic distortion	f = 1 kHz, Po = 1 W	-	0.015	0.03	%
VOS	Output DC offset	-	-10	-	10	mV
CT	Cross talk(4)	f = 1 kHz	-	100	-	dB
PSRR	Power supply rejection ratio(4)	f = 1 kHz; Vr = 1Vpk	-	90	-	dB
EOUT1	Output noise(8)	A-wtd and brick wall 20 kHz filter used, no output signal; Gv = Gv1	-	13	18	µV
		A-wtd and brick wall 20 kHz filter used, no output signal; Gv = Gv4	-	10	15	µV
EOUT2	Output noise(8)	ITU-R 468 and brickwall filter, no output signal	-	45	65	µV
SNR	Signal to noise ratio(8)	A-wtd and brick wall 20 kHz filter, Gv = Gv1	118	121	-	dB
DR	Dynamic range	A-wtd and brick wall 20 kHz filter, Gv = Gv1	116	120	-	dB
ΔVOITU	Peak of absolute value of output voltage (ITU-R ARM filtered)	Standby to eco-mode and Eco to Standby transition	-	-	7.5	mV
		Eco mode to play and play to Eco mode transition	-	-	7.5	mV
Control pins						
V_{Mth}	Mute pin voltage threshold	Attenuation < 0.5 dB	2.6	-	-	V
		Attenuation ≥ 60 dB	-	-	1.5	V
I_M	Mute pin source current	-	2.2	3.4	4.6	µA
V_{Mcl}	Mute pin internal clamp voltage	-	4.3	5	5.5	V
V_{enl}	Enable pin low voltage	-	-	-	0.9	V
V_{enh}	Enable pin high voltage	-	2.4	-	-	V
CD_{THD}	Clip detection(4)	CD_1 (IB11 D2D1 = 01) - THD at 100 Hz	-	1	-	%
		CD_2 (IB11 D2D1 = 10) - THD at 100 Hz	-	5	-	%
		CD_3 (IB11 D2D1 = 11) - THD at 100 Hz	-	10	-	%
CD_{SAT}	Clip det sat. voltage	CD on; ICD = 1 mA	-	100	-	mV
CD_{LK}	Clip det leakage current	CD pin at 3.6 V	-	-	1	µA
V_{ADDSEL}	Address selection voltage level	R = ∞ (pin open)	-	1.5	-	V
R_{ADDSEL_0}	Address selection resistance for address 0 selection	-	-	-	18	kΩ
R_{ADDSEL_1}	Address selection resistance for address 1 selection	-	32	-	38	kΩ
R_{ADDSEL_2}	Address selection resistance for address 2 selection	-	49	-	57	kΩ

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
R_{ADDSEL_3}	Address selection resistance for address 3 selection	-	71	-	79	kΩ
R_{LEGACY}	Address selection resistance for legacy mode	-	108	-	-	kΩ
I_{ADDSEL}	Address selection source current	R = 0 Ω (pin shorted to GND)	-	30	-	µA
I²C bus interface						
f_{SCL}	Clock frequency	-	-	-	400	kHz
V_{IL}	I²C pins low voltage	-	-	-	0.7	V
V_{IH}	I²C pins high voltage	-	1.3	-	-	V
V_{OLMAX}	I²C data pin low voltage when current Isink is sinked	Isink = 3 mA	-	-	0.4	V
I_{LIMAX}	Maximum input leakage current	V = 3.6 V	-	-	500	nA
I²S interface						
V_{IL}	I²S pins low voltage	-	-	-	0.7	V
V_{IH}	I²S pins high voltage	-	1.3	-	-	V
I_L	Input logic current, low	VI = 0 V	-	-	500	nA
I_H	Input logic current, high	VI = 3.6 V	-	-	500	nA
V_{OH-I2S}	High level output voltage	At Iout = 1 mA	1.4	-	-	V
V_{OL-I2S}	Low level output voltage	At Iout = 1 mA	-	-	0.2	V
Diagnostic thresholds						
Ldcsl1	DC diagnostic, short load	Speaker Diagnostic default I²C, IB11-d7 = 0	0.6	0.75	0.9	Ω
Ldcsl2		Speaker Diagnostic I²C IB11-d7 = 1	0.38	0.5	0.62	Ω
Ldol1	DC diagnostic, open load	Speaker Diagnostic default I²C, IB11-d6 = 0	19	25	31	Ω
Ldol2		Speaker Diagnostic I²C IB11-d6 = 1	11	15	18	Ω
Lac	AC diagnostic load threshold(4)	-	-	25	-	Ω
I_{pgnd}	No short to GND detected	-	-	-	4	mA
	Short to GND detected	-	35	-	-	mA
I_{pps}	No short to Supply detected	-	-	-	-4	mA
	Short to supply detected	-	-35	-	-	mA
Voffout	Output offset detector threshold	-	1.2	1.9	2.6	V
Voffin	Input DC offset detection threshold	-	-	-18	-	dB
Internal supply						
A5VSVR-AGSVR	Delta voltage level	-	4.5	5.0	5.5	V
D1V8SVR-DGSVR	Delta voltage level	-	1.62	1.8	1.98	V
V_{BOOST}	Boosted voltage level above V_{CC}	-	6.8	7.3	7.8	V
V5V	-	-	4.4	4.8	5.2	V
I_{L1L2}	Inductor current	-	-	-	2	A

1. *5 V minimum operating at turn on, 4.5 V minimum at supply cranking.*
2. *Tested as specified in Section 9.4 External components guideline (with NO snubber and with damping networks).*

3. *Values from bench measurement, measured at pin level. Guaranteed by correlation factor at ATE.*
4. *Typical value from bench, measured on ST demo-board as specified Section 9.4 External components guideline*
5. *All the voltage threshold values are in tracking.*
6. *For thermal warning/mute/shutdown typical shape and description please refer to dedicated chapter.*
7. *Parameter not directly measured at ATE. Values measured directly on the load.*
8. *Values measured at bench and guaranteed by correlation factor at ATE.*

3.4 Typical curves of the main electrical parameters

I²C settings as per Table 15, unless otherwise specified.

Figure 5. Efficiency and power dissipation (Vcc = 14.4 V, RL = 4 x 4 Ω, f = 1 kHz sine wave)

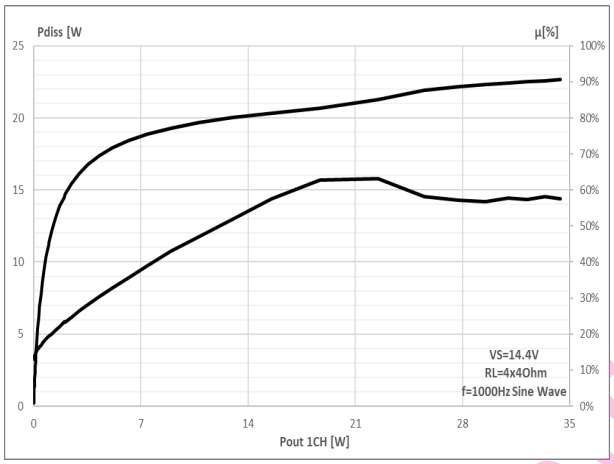


Figure 6. Efficiency and power dissipation (Vcc = 14.4 V, RL = 4 x 4 Ω, pink noise)

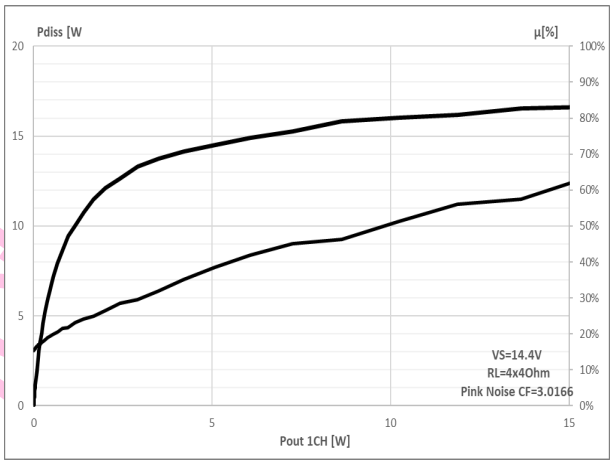


Figure 7. Efficiency and power dissipation (Vcc = 14.4 V, RL = 4 x 2 Ω, f = 1 kHz sine wave)

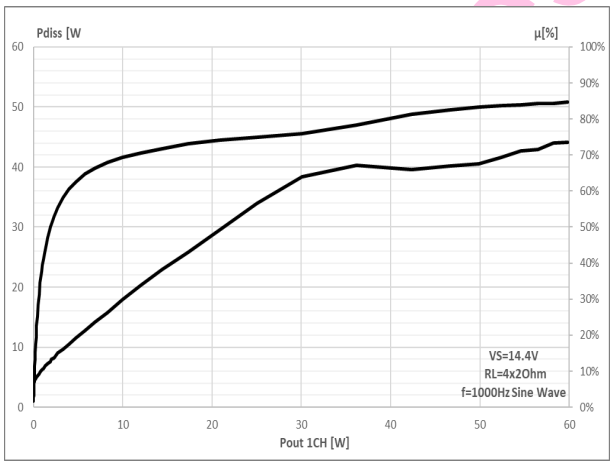


Figure 8. Efficiency and power dissipation (Vcc = 14.4 V, RL = 4 x 2 Ω, pink noise)

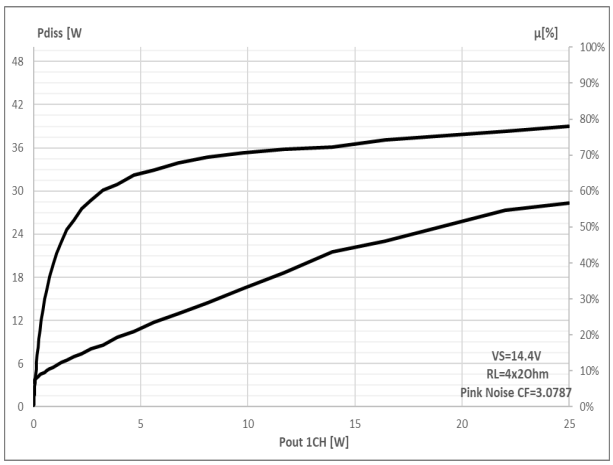


Figure 9. Efficiency and power dissipation (Vcc = 14.4 V, RL = 4 x 8 Ω f = 1 kHz sine wave)

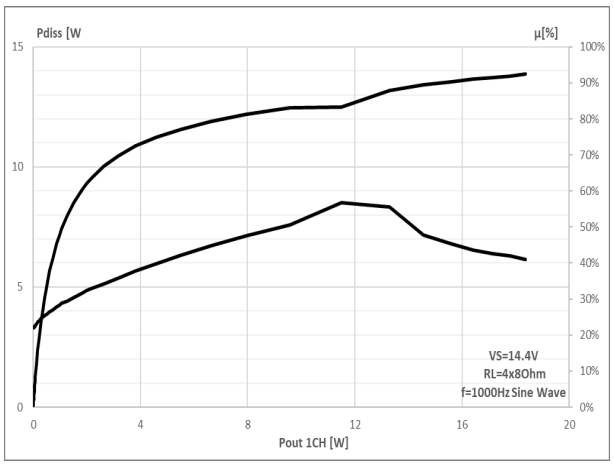


Figure 10. Efficiency and power dissipation (Vcc = 14.4 V, RL = 4 x 8 Ω, pink noise)

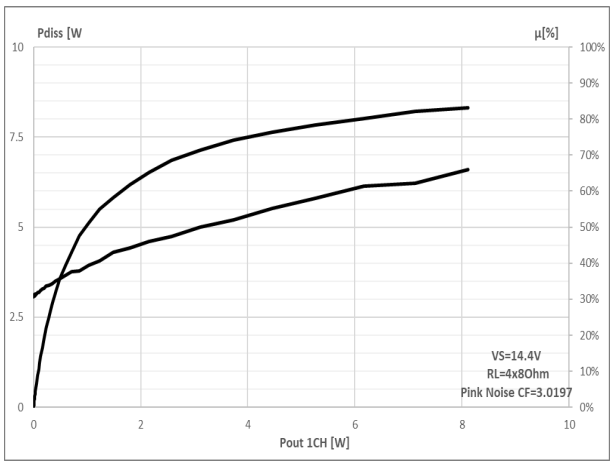


Figure 11. Efficiency and power dissipation (Vcc = 14.4 V, RL = 2 x 1 Ω, f = 1 kHz sine wave)

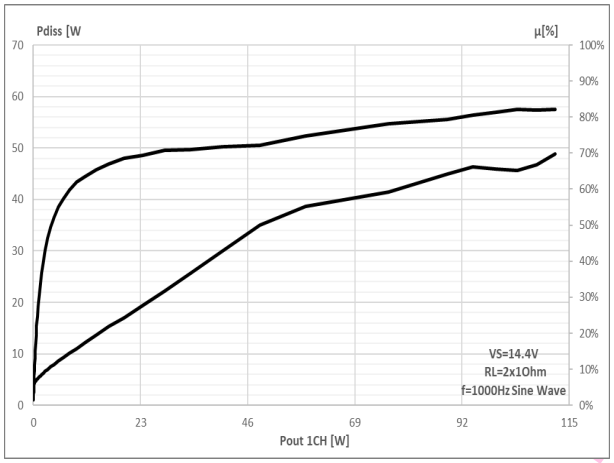


Figure 12. Efficiency and power dissipation (Vcc = 14.4 V, RL = 2 x 1 Ω, pink noise)

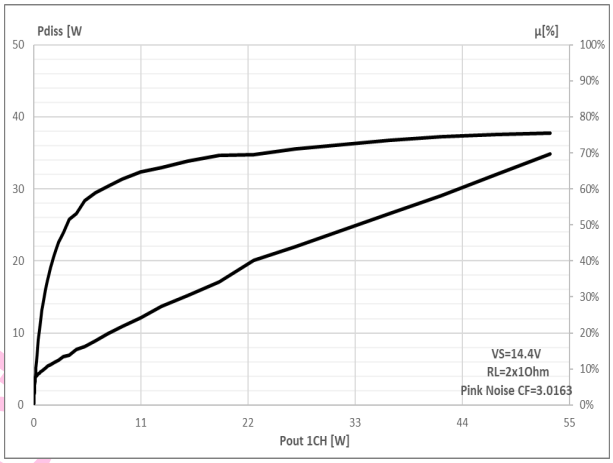


Figure 13. Output power vs supply voltage (RL = 4 Ω, sine)

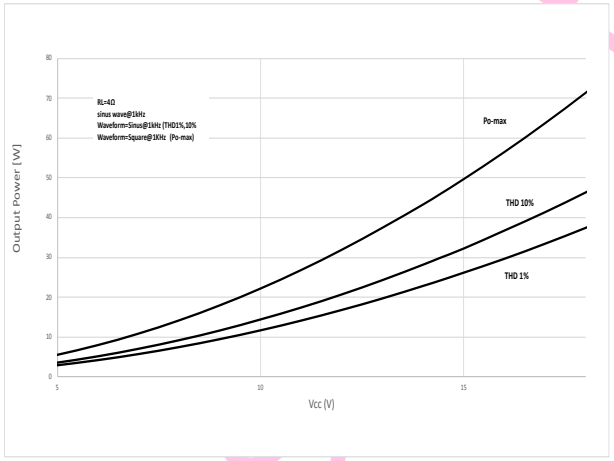


Figure 14. Output power vs supply voltage (RL = 2 Ω, sine)

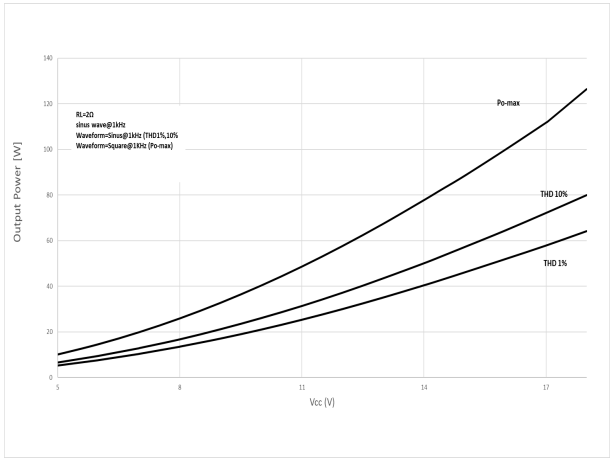


Figure 15. Output power vs supply voltage (RL = 8 Ω,v sine wave)

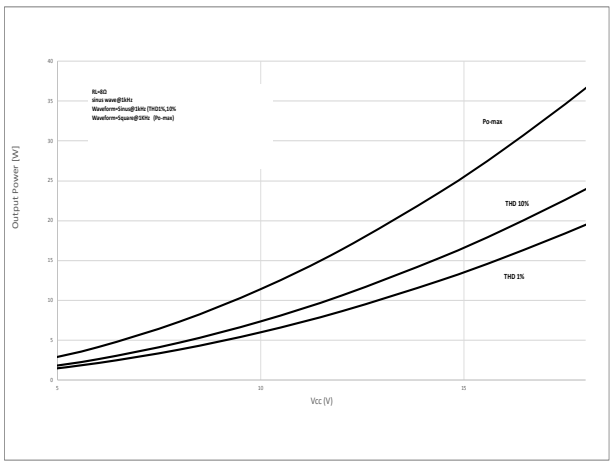


Figure 16. Output power vs supply voltage (RL = 2 Ω, parallel mode sine wave)

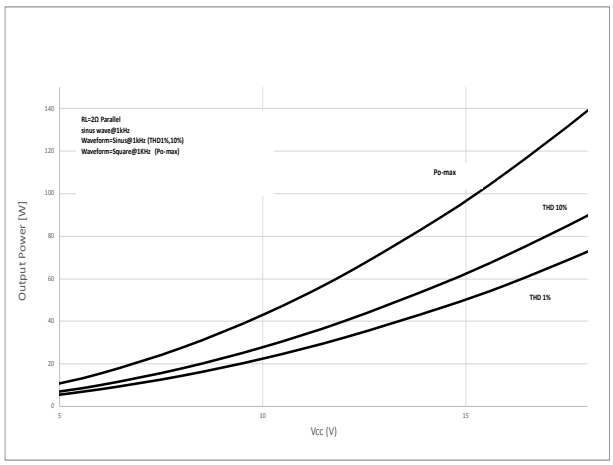


Figure 17. Output power vs supply voltage (RL = 1 Ω, parallel mode, sine)

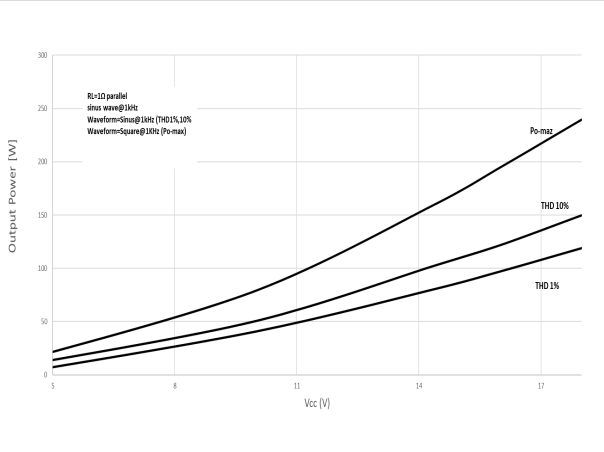


Figure 18. THD vs output power (Vcc = 14.4 V, RL = 4 Ω)

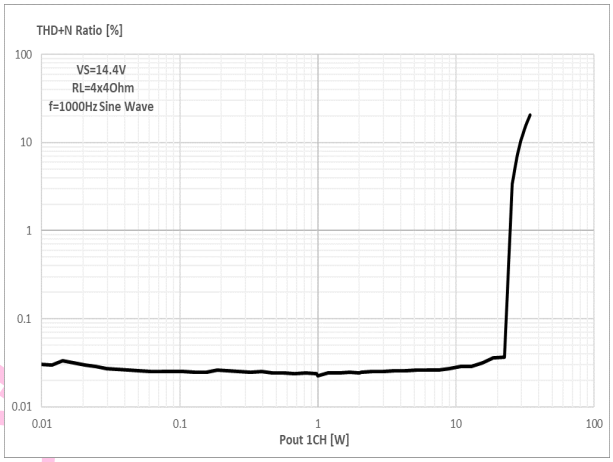


Figure 19. THD vs output power (Vcc = 14.4 V, RL = 2 Ω)

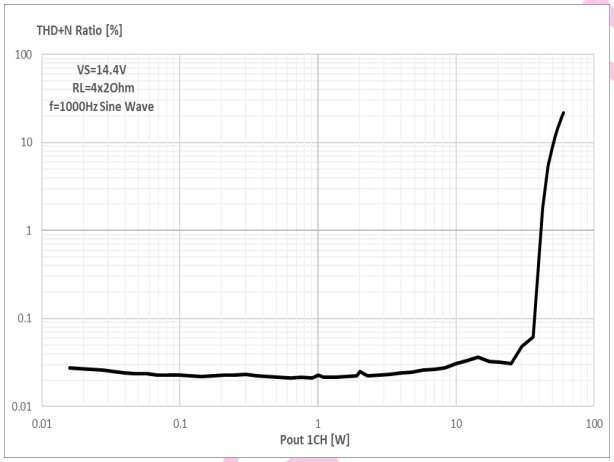


Figure 20. THD vs output power (Vcc = 14.4 V, RL = 8 Ω)

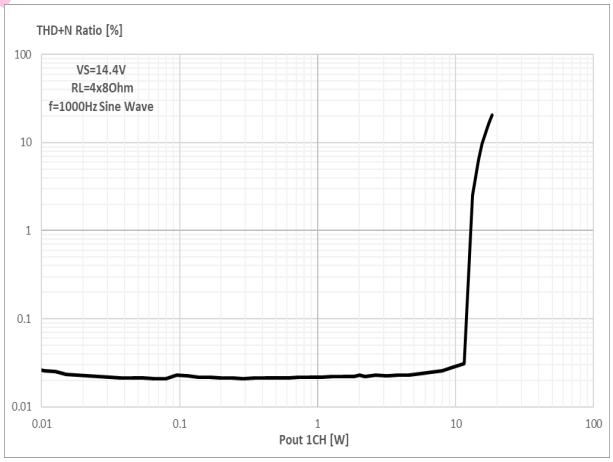


Figure 21. THD vs output power (Vcc = 14.4 V, RL = 1 Ω)

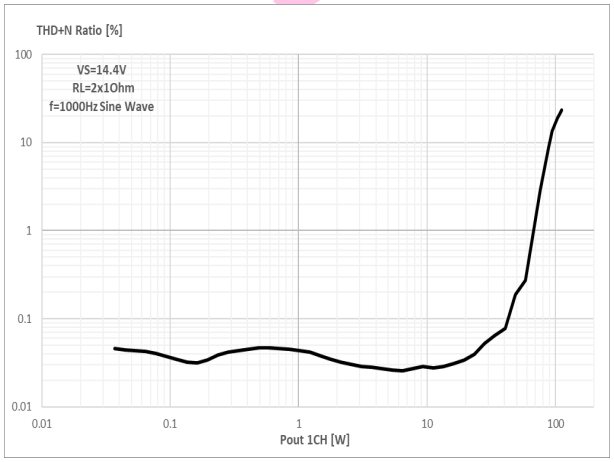


Figure 22. THD vs Frequency (Vcc = 14.4 V, RL = 4 Ω, Po = 1 W)

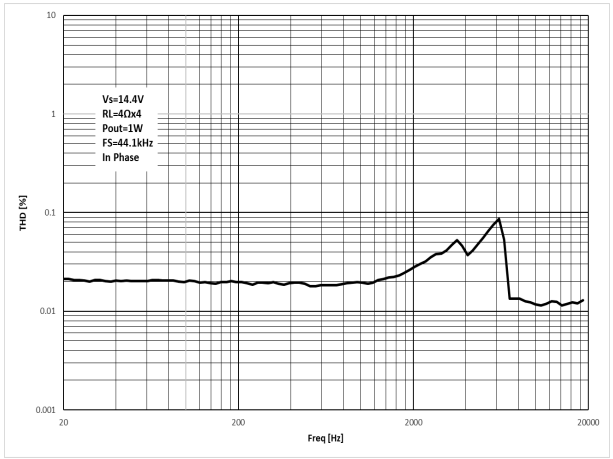


Figure 23. THD vs Frequency (Vcc = 14.4 V, RL = 2 Ω, Po = 2 W)

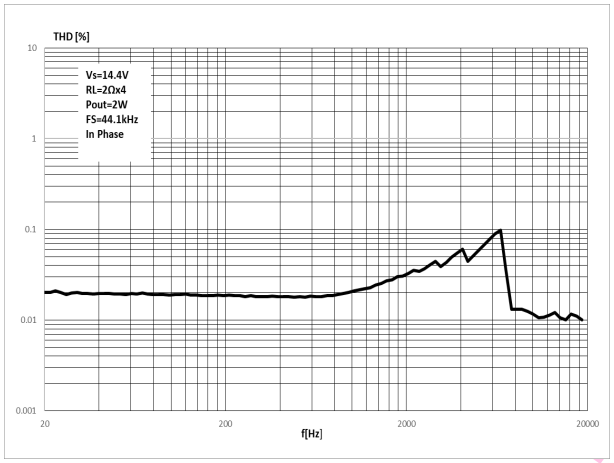


Figure 24. THD vs Frequency (Vcc = 14.4 V, RL = 8 Ω, Po = 1 W)

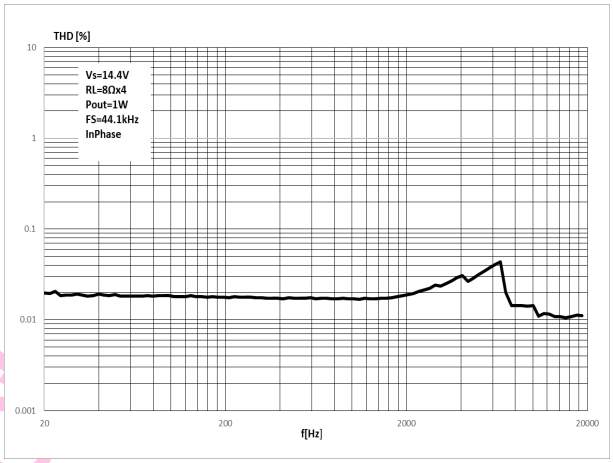


Figure 25. Crosstalk vs 3frequency

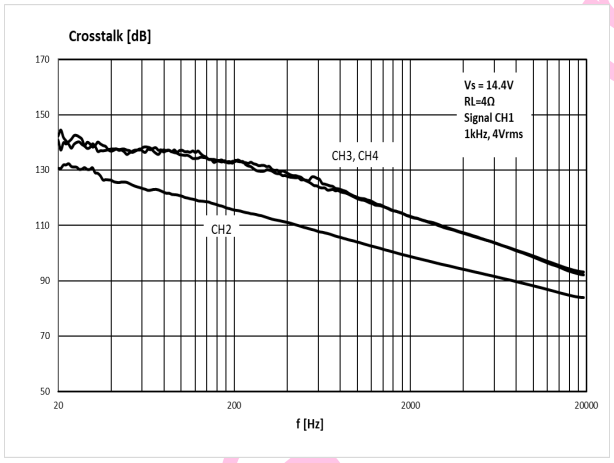


Figure 26. PSRR vs frequency

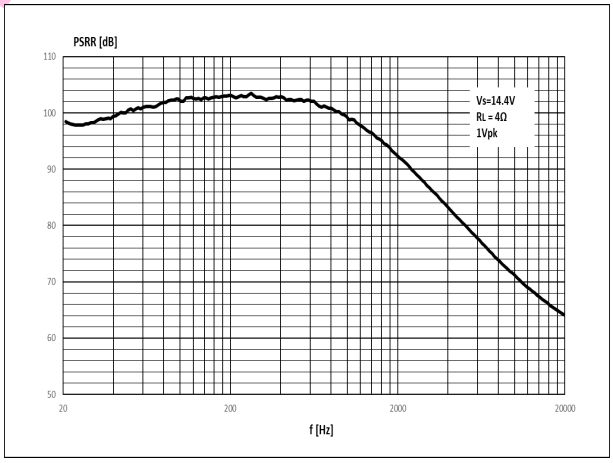


Figure 27. Frequency response (RL = 4 x 4 Ω, Po = 1 W, sine wave @ 1 kHz)

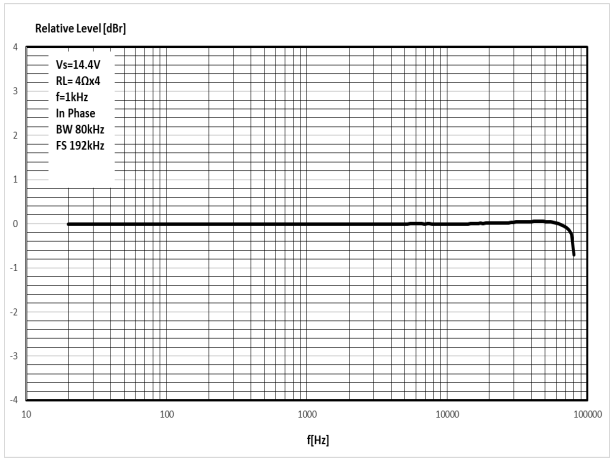


Figure 28. Frequency response (RL = 4 x 2 Ω, Po = 1 W, sine wave @ 1 kHz)

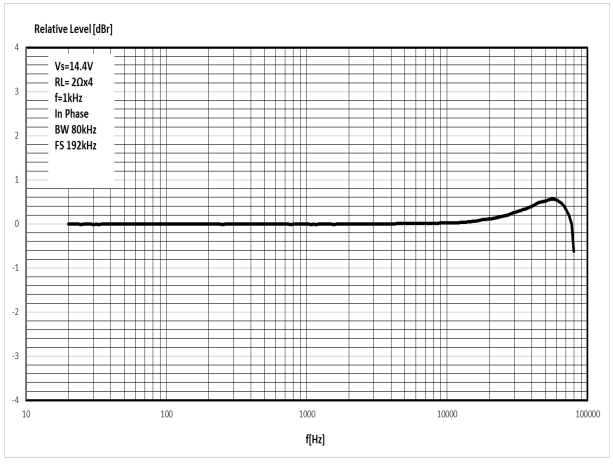


Figure 29. Frequency response (RL = 4 x 8 Ω, Po = 1 W, sine wave @ 1 kHz)

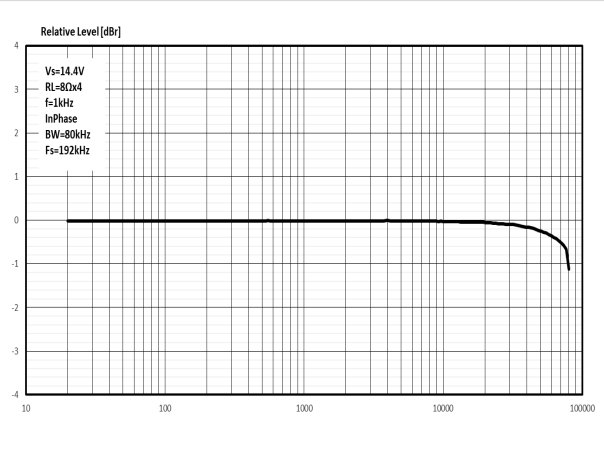
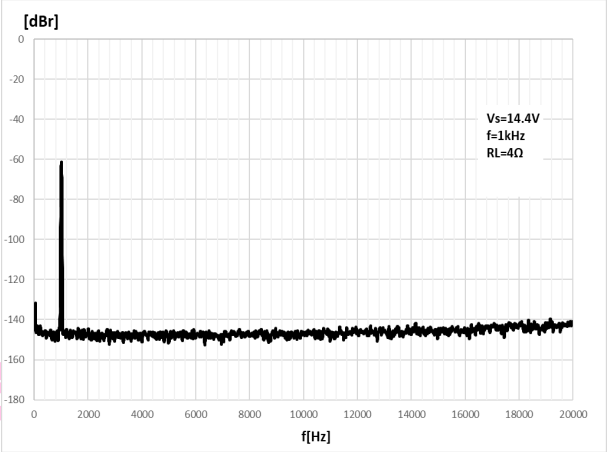


Figure 30. FFT - Output spectrum (-60 dBFS input signal)



4 General description

HFDA801L is a fully digital single chip class-D amplifier with high immunity to the demodulation filter effects. The high integration level and the on-board signal processing allow excellent audio performance to be achieved.

Thanks to the digital input and to the feedback strategy in the power stage, HFDA801L makes the amplifier immune from the output filter components non-linearity. The number and size of the external components are minimized.

HFDA801L includes: digital I^2C and I^2S interfaces, internal 24 bits DAC conversion, digital signal processing for interpolation and noise shaping, innovative self-diagnostic functions and automatic detection of wrong load connections or variation of the load, internal PLL for a clock generation. Moreover HFDA801L provides a breakthrough innovative digital impedance-meter which can communicate via I²C the output load value.

4.1 Feedback topology and switching frequency

HFDA801L adopts an innovative feedback topology, where the LC filter is included in the feedback loop making the amplifier highly insensitive to the characteristics of such demodulation circuit. This solution optimizes the system performance in terms of THD and frequency response in any load condition.

Regardless of the big phase shifting introduced by the output filter the device shows an adequate phase margin for any load condition. The system stability has been designed considering:

- PWM switching variation (from 2.1 MHz to 2.3 MHz)
- Silicon temperature variation (from -40 to 150 °C)
- Load variation (both inductive and capacitive considered)
- LC demodulator filter variation and tolerance
- Voltage supply variation (from 4.5 to 18 V)
  - Minimum supply voltage level during turn-on transition = 5 V

The system has been designed to guarantee a phase margin > 45 degrees for any working condition.

The new feedback topology assures a strong control of voltage and current across the load making the diagnostic load detection reliable.

4.2 PWM frequencies

HFDA801L PWM frequency is well above the AM band, avoiding by architecture the EMC interference of PWM switching first harmonic. Moreover, this choice permits to optimize the size and cost of the external LC demodulation filter.

The PWM frequency depends on the I^2S WS frequency as reported in the table below:

Table 5. PWM frequency relation with I^2S WS frequency

WS frequency [kHz]	Nominal PWM frequency [MHz]
44.1	2.1168
48	2.304
96	2.304
192	2.304

4.3 Load possibilities

HFDA801L supports several load possibilities and configurations. The default configuration is suitable for a 4-channel application (front/rear - left/right). By means of the I^2C bus bit IB1-d7,d6 it is possible to choose a 2-channel solution with parallel outputs (left/right) or a 2.1 configuration for sub-woofer application.

Possible channel configurations:

- 4 x 4 Ω
- 4 x 2 Ω
- 2 x 1 Ω (through channels connected in parallel)
- 2 x 4 Ω + 1 x 2 Ω (through parallelized channels)

4.3.1 Parallel mode control and recommendation

HFDA801L provides the possibility to parallelize the channels to increase the output current capability. During this operation one of the two channels in the parallel configuration become the “controller” channel, the other one is the “secondary” channel.

The possible parallel configurations are:

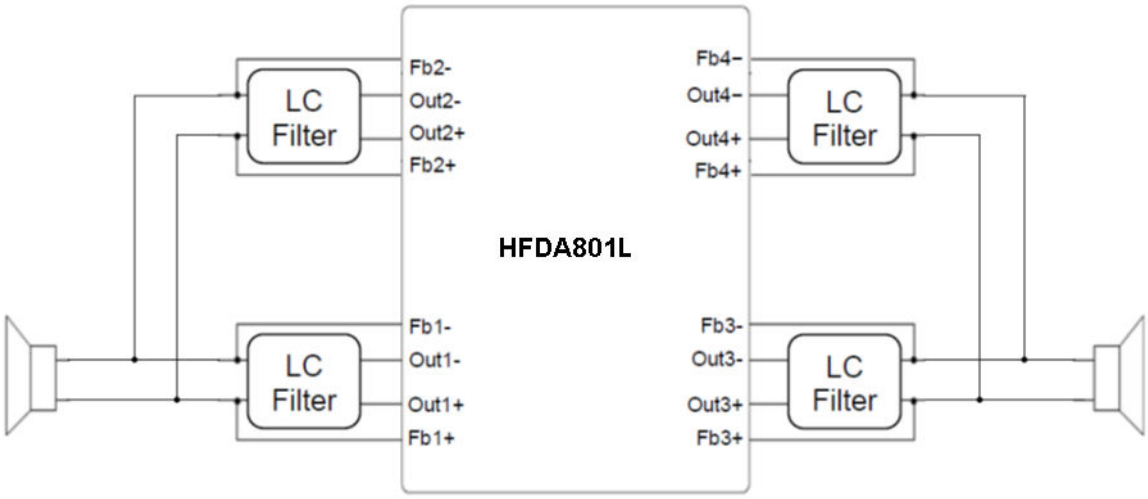
- CH1 and CH2 in parallel: CH1 is the controller, CH2 is the secondary
- CH3 and CH4 in parallel: CH3 is the controller, CH4 is the secondary

To properly control the parallel mode configuration the following recommendations must be followed:

- Connect the two channels outputs after the demodulation filter, (see Figure 31).
- Connect the feedback of both channels after the demodulation filter, (see Figure 31).
- Select the parallel operation, by means of IB1-d7/d6, before writing I^2C IB23-d0 = 1 bit, (FIRST setup programmed–ready to work).
- Write secondary channels control bytes, IB15 for CH2 and IB17 for CH4, with the settings “00000000”.

In addition to these recommendations, remember that the parallel configuration influences diagnostic operation, as described in Section 8.1.7 Diagnostic in parallel mode.

Figure 31. Parallel mode configuration



4.4 LC filter design general guidelines

The audio performance of a class-D amplifier is heavily influenced by the characteristics of the output LC filter. The choice of its components is quite critical because a lot of constraints must be fulfilled at the same time: size, cost, EMI filtering, efficiency. Both the inductor and the capacitor exhibit a non-linear behavior: the value of the inductance is a function of the instantaneous current in it and similarly the value of the capacitor is a function of the voltage across it.

In the classical approach, where the feedback loop is closed right at the output of the power stage, the LC filter is placed outside the loop and these non-linearities cause the total harmonic distortion (THD) to increase. The only way to avoid this phenomenon would be to use components which are highly linear, but this means they are also bigger and/or more expensive.

Furthermore, when the LC filter is outside the loop, its frequency response heavily depends on the impedance of the loudspeaker; this is one of the most critical aspects of class-D amplifiers. In standard class-D this can be mitigated, but not solved, thus increasing cost, volume and power dissipation. HFDA801L, instead, provides a very flat frequency response over audio-band which cannot be achieved by standard class-D without feedback after LC filter.

Since the demodulator group is now in the feedback path, some constraints regarding the inductor and capacitor choice are still present but of course less stringent than in the case of a typical switching application.

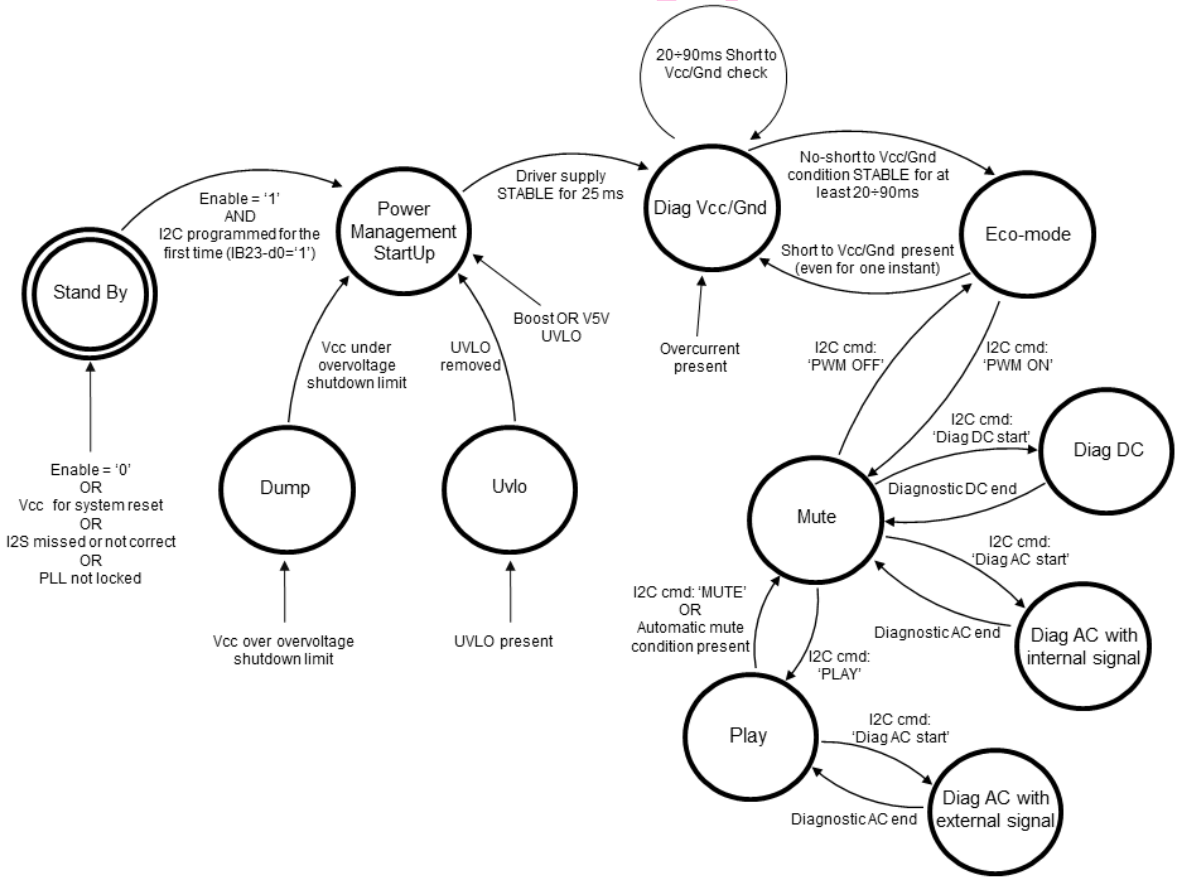
5 Operation state

HFDA801L has a finite state machine which manages the amplifier functionality, reacting to the user and system inputs.

5.1 Finite state machine

The finite state machine is represented by the following diagram:

Figure 32. Finite state machine diagram



5.2 Out of standby and address selection

5.2.1 Address selection

To select the proper I²C address a resistor must be connected between ADDSEL pin and GND as follows:

Table 6. Address selection threshold

Chip Address	R Load
0xD8	R_{ADDSEL_0}
0xDA	R_{ADDSEL_1}
0xDC	R_{ADDSEL_2}
0xDE	R_{ADDSEL_3}
Legacy Mode	R_{LEGACY}

Note: Reference value can be found in Table 4.

5.3 Startup sequencing

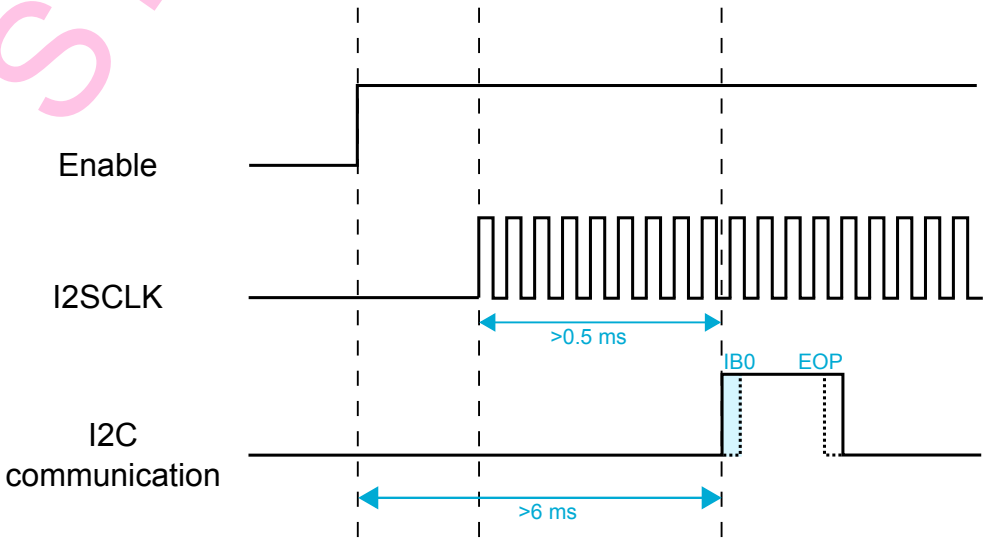
5.3.1 Startup sequence

The ENABLE pin has the function of starting up the system. If ENABLE is low, (“0”), then the HFDA801L is in standby, the outputs remain biased to ground and the current consumption is limited to standby quiescent current. In this case the FSM (finite state machine) is in “standby” state.

When a valid high level on the ENABLE pin is recognized the device turns on: all the internal supply voltages and outputs are biased to $V_{CC}/2$.

The internal I²C registers are pre-settled in “default condition”, waiting for the next I²C instruction.

Figure 33. Startup sequence



The device moves from standby state when the end of programming is reached (EOP) by writing the IB23-d0 = 1 (FIRST setup programmed–ready to work).

The return in the standby condition, (ENABLE pin at 0), will cause the reset of the amplifier. As defined in the finite state machine, the same event happens if the PLL is not locked, I²S is missing or not correct, V_{CC} under or overvoltage.

5.3.2 V_{CC} rise time with enable low

To avoid the effect of spurious noise on the speaker due to the uncontrolled high impedance outputs when the device is disabled (ENABLE pin low), it is suggested to rise the V_{CC} not faster than 400 µs.

5.3.3 Device reset when enable pin low

When the ENABLE pin is driven low (ENABLE pin at 0) the device stops playing. If the enable pin is maintained low for a period longer than 200 µs, the device goes in reset losing the I^2C programming.

5.4 Diagnostic V_{CC}/GND state

After exiting from standby state the device passes through the diagnostic V_{CC}/GND state. In this state the amplifier checks the presence of the following faults:

- Shorts to ground or to V_{CC}
- Undervoltage (UVLO)
- Overvoltage

HFDA801L will move to the next state (eco-mode) only if there are not any of these faults for at least the diagnostic time window duration, I^2C (IB6, d3-d2), thus avoiding any danger for the amplifier and the user system.

Meanwhile, if a stable fault is present, it will be communicated to the user via I^2C after the diagnostic time window duration, I^2C (IB6, d3-d2), in order to always provide only stable information about the system. In this case the device will not move to eco-mode, waiting for the fault cause to be removed.

While the amplifier is in diagnostic V_{CC}/GND state it can receive all the I^2C commands, but it will actuate the PWM turn-on only when it enters in the next state: eco-mode. This procedure guarantees that wrong or unwanted I^2C communication can lead the amplifier to a dangerous situation if a short to V_{CC} or GND is present. Three conditions move the amplifier in the diagnostic V_{CC}/GND state from any other functional state:

- Overcurrent protection trigger
- UVLO
- Overvoltage (through DUMP condition)

5.5 Eco-mode state

In eco-mode state the amplifier is fully operative from a communication point of view and can receive and actuate all the commands given by the user.

In eco-mode the output switching is disabled, permitting a low quiescent current and power dissipation. The device is also able to move from eco-mode state to MUTE state, turning on the output switching, in about 1ms without experiencing POP-noise. This permits a very fast transition from eco-mode to PLAY.

5.6 Mute-play state

The amplifier can move from eco-mode state to MUTE state selecting “PWM-ON” via I^2C (IB14, d4; IB15, d4; IB16, d4; IB17, d4). This operation turns on the output PWM. From MUTE state HFDA801L can move to PLAY state via “PLAY” I^2C command and returns to MUTE state from PLAY state acting on the same bit. The transition time between mute and play states could be selected via I^2C (IB5 d6-d7).

Some external conditions could lead the amplifier in mute state automatically:

- Low battery mute
- High battery mute
- Thermal mute
- Hardware pin mute

Once the mute condition is no more present the HFDA801L returns automatically in the PLAY state. Of course the user can decide to change the amplifier programming in the meanwhile, thus avoiding the automatic return in PLAY.

In normal cases the transition between eco-mode to MUTE state (PWM-ON) must be done in sequence, one channel at a time, with a delay of about 100 µs between channels.

In case a fast TurnOn is required with 4 channels to be turned ON simultaneously, the IB4-d5 bit should be set to "1", fast TurnOn boost enabled. This bit setting, by enabling a slightly higher quiescent current, allows the simultaneous TurnOn of all the 4 channels. It can be reset to "0" in any time after the TurnOn.

5.7 Diagnostic state

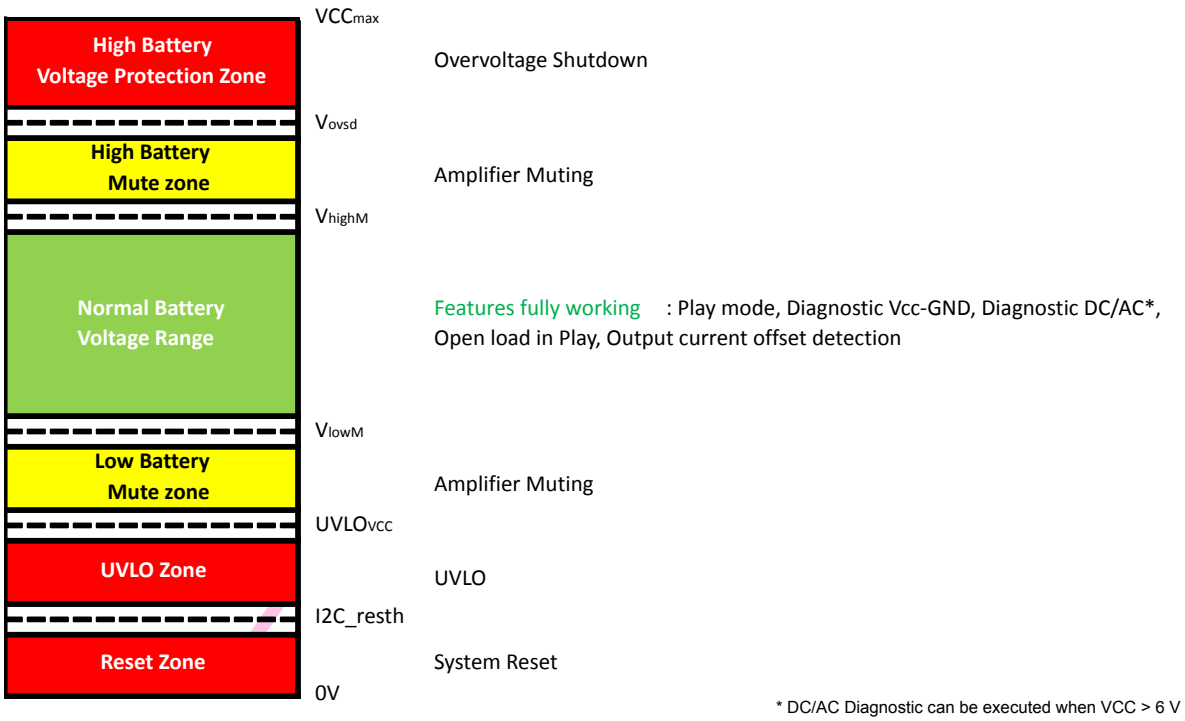
Starting from MUTE state, the user can decide to start the DC or AC diagnostic procedures with an internal generated signal.

When the device is in PLAY the user can also activate the AC diagnostic with an external signal. In this way the HFDA801L will process the input signal received in order to perform a reliable AC diagnostic. The diagnostic functionality is explained in detail in Section 8 Diagnostic and protection function and the diagnostic state sequences are described in Section 8.1.6 Diagnostic timelines.

6 Operation compatibility vs battery

The HFDA801L operation compatibility vs the battery value is reported in the figure below:

Figure 34. Operation vs battery charge

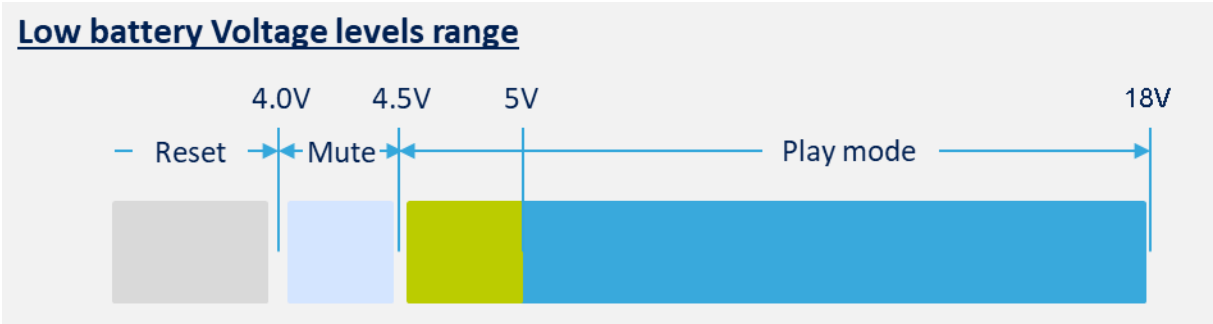


Note: For detailed values range please refer to Table 4.

6.1 Mute zone and play mode attenuation

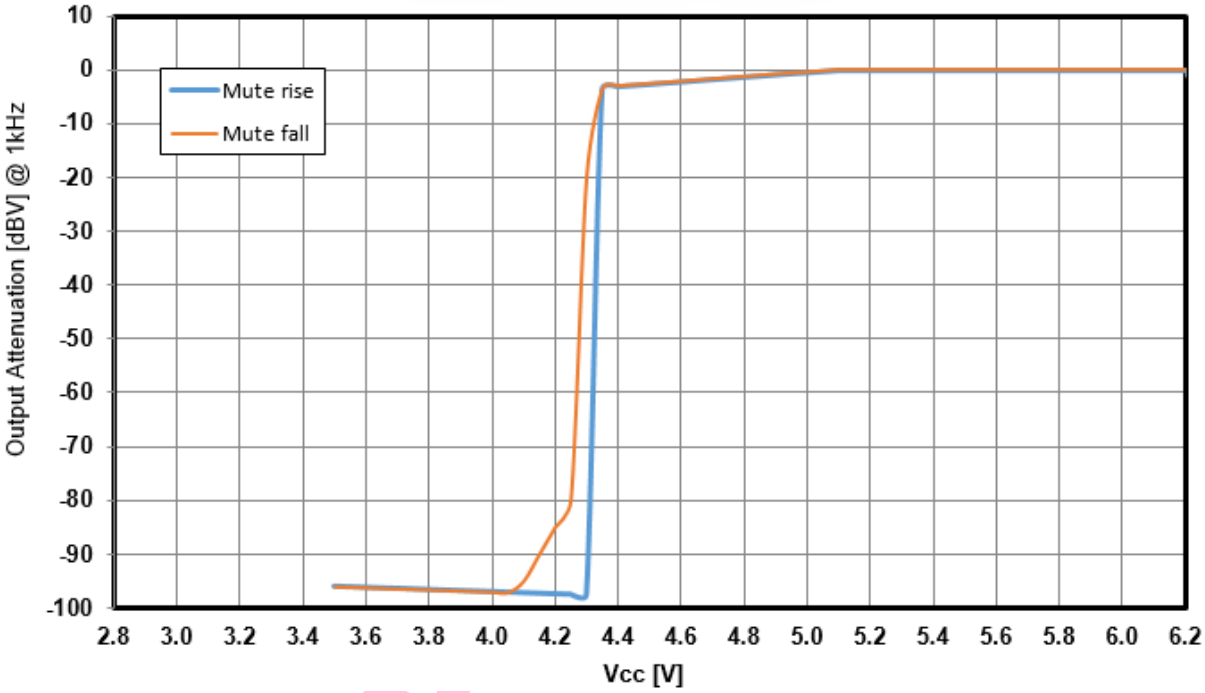
Amplifier mute zone is defined for a voltage level lower than 4.5 V.

Figure 35. Mute zone



When the voltage level is lower than 4 V the amplifier is in the reset zone where internal logic is not working. As soon as the supply voltage level rises over 4 V the logic starts working but the output stage is maintained in mute state until the supply voltage level goes higher than 4.5 V. Once the amplifier has moved in play mode it is maintained in that state, no mute, until the supply voltage level falls down to a level lower than 4.5 V. The amplifier starts to slightly mute when the supply voltage falls down lower than 5 V as shown in Figure 36.

Figure 36. **Auto mute attenuation**



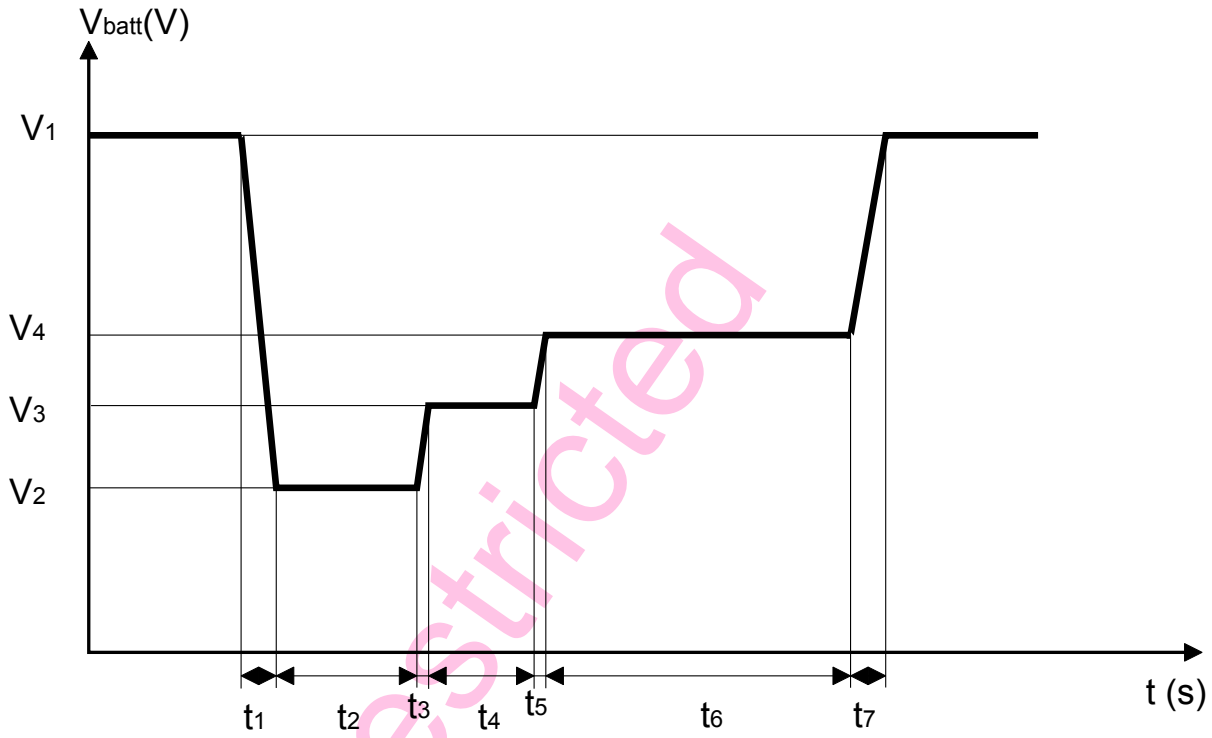
Note: Numeric values indicated in Figure 35 and Figure 36 are expressed as typical. For detailed values range please refer to Table 4.

6.2 Low voltage (cranking) operation

The most recent OEM specifications require the automatic stop of the car engine at traffic light, in order to reduce the emissions of polluting substances. The engine re-start induces cranks on the battery voltage that bring the supply down lower than 6 V. HFDA801L allows a continuous operation when battery applied to the IC falls down to 4.5 V, without producing pop noise, thus supporting this new specification (the maximum system power will be reduced accordingly as reported in the electrical characteristics).

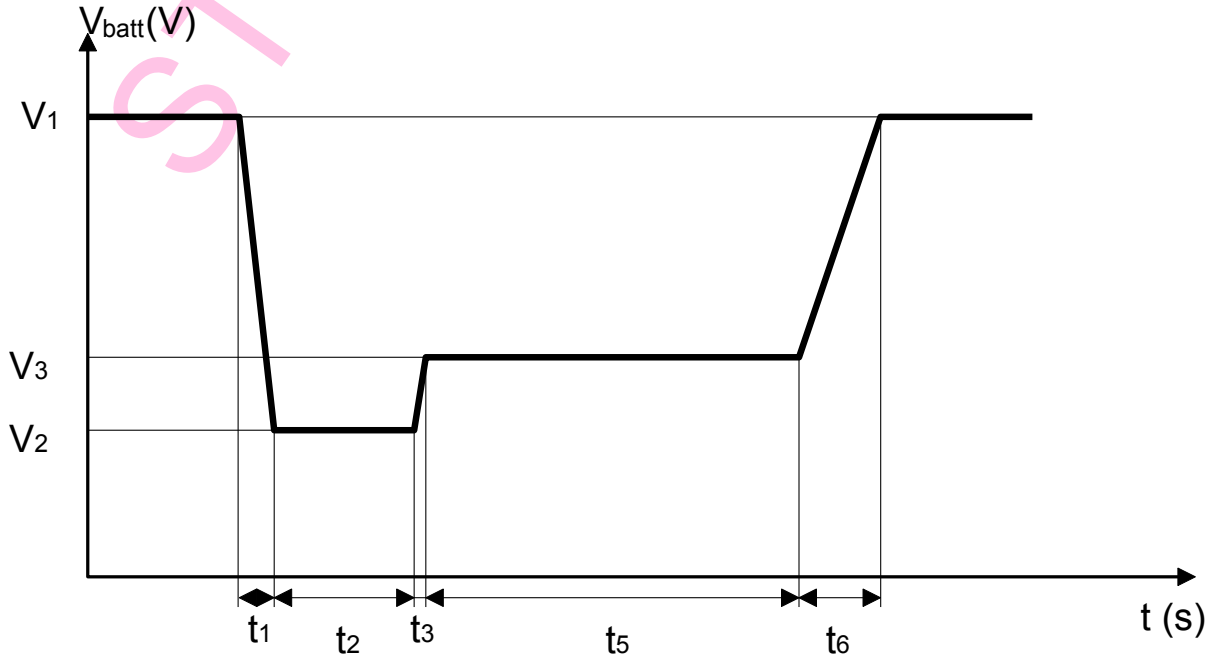
Battery cranking curves supported by HFDA801L are shown below, indicating the shape and durations of allowed battery transitions.

Figure 37. **“Start-stop” battery cranking curve example 1**



V1 = 12 V; V2 = 4.5 V; V3 = 7 V; V4 = 8 V
t1 = 2 ms; t2 = 50 ms; t3 = 5 ms; t4 = 300 ms; t5 =10 ms; t6 = 1 s; t7 = 2 ms

Figure 38. **“Start-stop” battery cranking curve example 2**



V1 = 12 V; V2 = 4.5 V; V3 = 7 V
t1 = 2 ms; t2 = 5 ms; t3 = 15 ms; t5 = 1 s; t6 = 50 ms

6.3 UVLO

HFDA801L presents an under voltage lock out threshold, (UVLO), to protect the device from malfunctions due to low supply voltage.

Once the V_{CC} is below the UVLO threshold the device moves in protection: device FSM automatically evolves to “UVLO” state, as described in Section 5.1 Finite state machine, shutting off the output PWM and power manager.

Once V_{CC} returns to a value above the UVLO threshold, the device automatically evolves starting the power manager start-up sequence, and following the retained I^2C registers settings previously set.

Under the UVLO threshold the device retains the I^2C register values down to I^2C_{Resth}, as reported in Table 4.

7 Muting architecture

The HFDA801L uses a mixed signal approach for muting function.

We can define a “mute command signal” as the system parameter which determines the mute function. The mute command signals are:

- “High voltage mute”: active when V_{CC} enters in a voltage window over the max voltage; the window is specified in the electrical parameters table.
- “Low battery mute”: active when V_{CC} enters in a voltage window under the max voltage; the window is specified in the electrical parameters table.
- “Hardware mute”: active when HWMute pin enters in the voltage window specified in the electrical parameters table.
- "Thermal mute”: active when temperature enters in the temperature window over the max temperature; the window is specified in the electrical parameters table.
- “PLL mute”: active when PLL gets unlocked
- “I^2C mute”: active when user selects mute/play I^2C bits

The mute is achieved by the combination of two separated actuators, “analog-mute” and “digital mute”.

7.1 Command dependence

Analog and digital mute actuators activation could be different based on the mute command signal. This is described in the following table:

Table 7. Command dependence

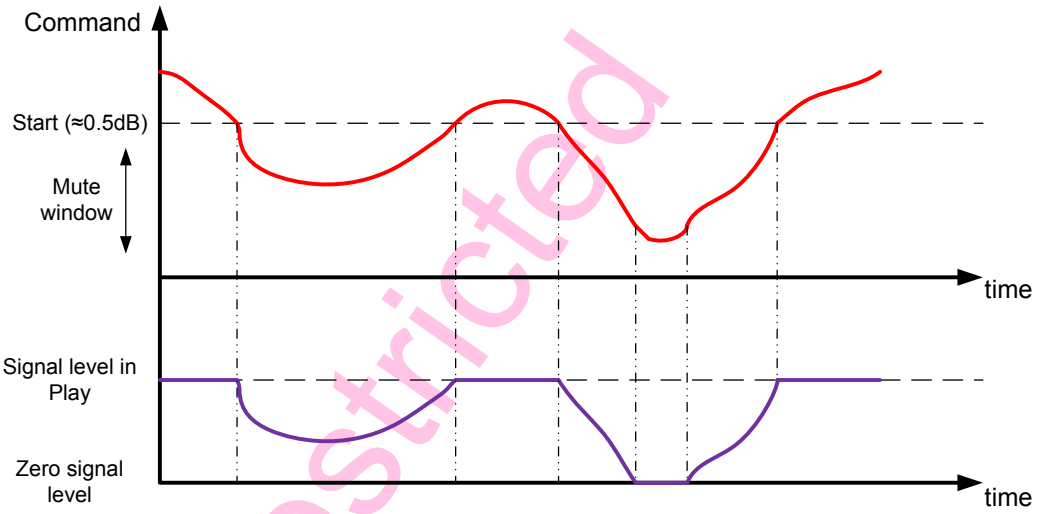
Command signal	When	Mute	Unmute
Low battery mute	When V_{CC} enters inside the low battery mute window	Mixed mute. Analog and digital, at the same time(1)	Digital(1)
High voltage mute	When V_{CC} enters inside the high voltage mute window	Mixed mute. Analog and digital, at the same time(1)	Digital(1)
PLL mute	When PLL gets unlocked	Mixed mute. Analog and digital, at the same time(1)	Digital(1)
Thermal mute	When temperature enters inside thermal mute window	Analog	Analog
Hardware mute	When hardware pin voltage enters inside its mute window	Mixed mute. Analog and digital, at the same time(1)	Digital(1)
I^2C mute	When I^2C mute bits are selected	Digital	Digital

1. *User can decide to disable digital-mute/unmute using bit I^2C, (IB12 d7); in this case in all the conditions, (except I^2C mute), the mute/unmute will be purely analog.*

7.2 Analog mute

Analog mute senses when the mute command signal transits across the muting-window and attenuates the output signal proportionally to the input level inside the muting-window.

Figure 39. Analog mute diagram



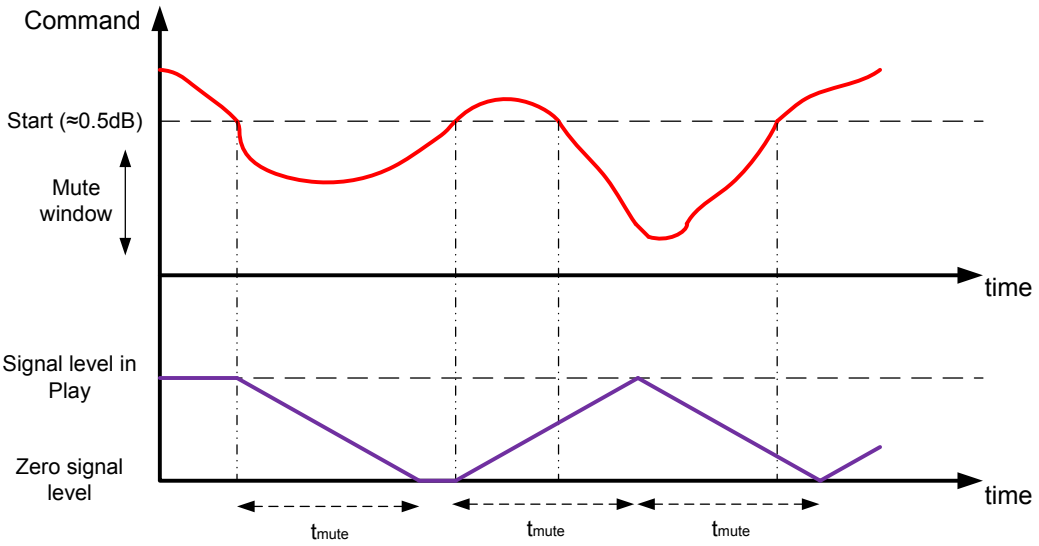
7.3 Digital mute

Digital mute acts on the digitally elaborated output signal attenuating it gradually to zero with digital steps in a pre-defined time frame (t_{mute}). The muting time, (t_{mute}), can be selected by I^2C, (IB5 d7-d6). There are two different actions performed by the digital-mute function:

Mute: it starts when analog mute attenuation becomes higher than 0.5 dB. It ends after t_{mute}.

UnMute: it starts when analog mute attenuation becomes lower than 0.5 dB. It ends after t_{mute}, regardless of analog mute attenuation. In case analog mute attenuation gets higher than 0.5 dB during the unmute ramp the system will start the mute from the signal level reached.

Figure 40. Digital mute diagram



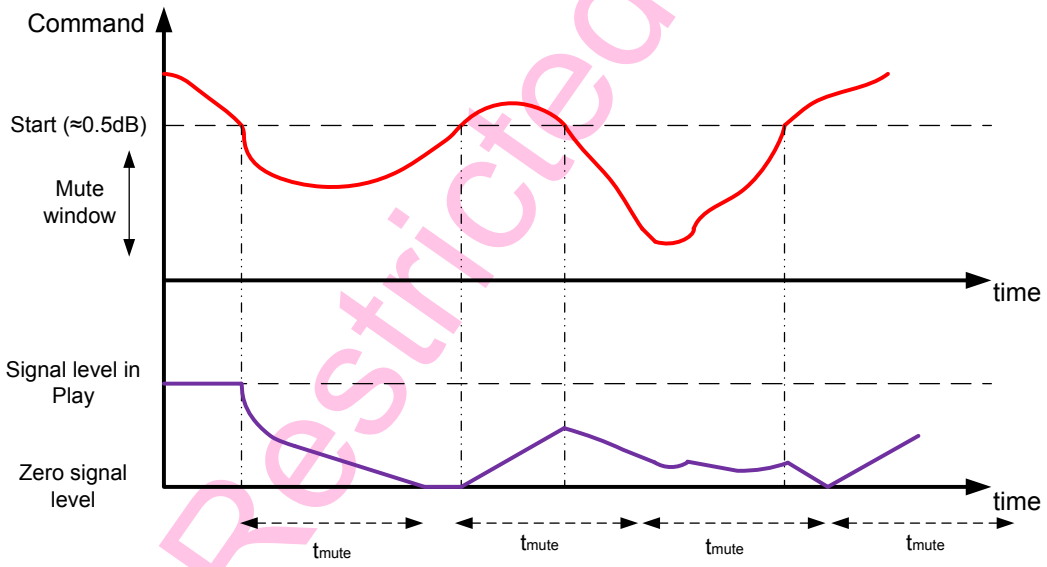
Note: In case of I²C mute the digital mute actuation does not follow the analog mute level but only the I²C command.

7.4 Mixed mute

The mixed mute approach is the superposition of the two mute actuators, analog mute and digital mute, at the same time.

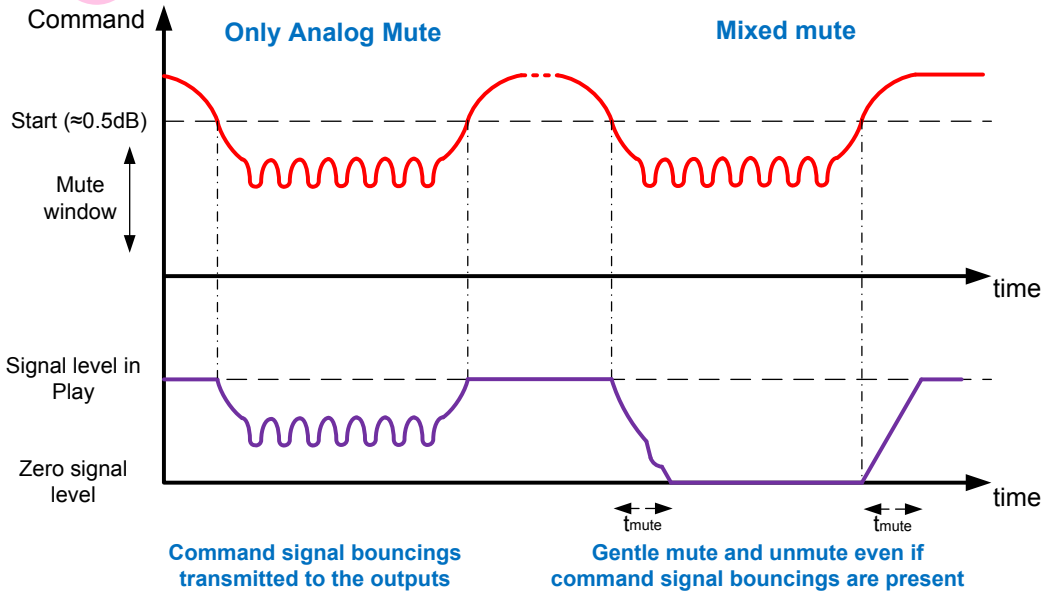
Here below the example of the previous pages with mixed mute:

Figure 41. Mixed mute diagram



The mixed mute approach is more robust than the analog mute approach. The effects are visible when the command signal variations inside the muting window last longer than the muting/unmuting time. An example is depicted in the figure below:

Figure 42. Analog mute vs mixed mute



In any moment the user can disable the digital mute, acting on the I^2C, (IB12-d7), obtaining the standard analog mute function.

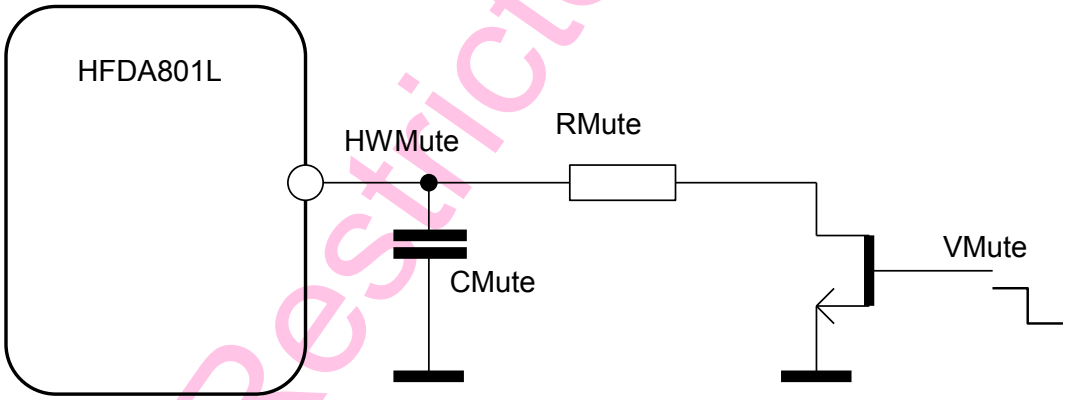
7.5 HW mute pin

The pin “HWMute” (pin 62) acts as mute command for the channel. It is an analog control of the output signal volume. The device is muted when this pin is low, while it is in play when this pin is high (low/high threshold in Table 4).

Inside the device, connected to this pin a pull-up current generator puts the device in play if left floating. An internal clamp limits the mute pin voltage. If not used, this pin should remain floating.

To drive the mute pin to get a hardware mute an external pull-down open drain is needed. (see Figure 43), RMute must be < 100 kΩ.

Figure 43. **HW mute pin schematic**



8 Diagnostic and protection function

The HFDA801L amplifiers family provides the diagnostic function for detecting several possible faults conditions. Any warning information will be stored in the I^2C interface and kept until the first I^2C bus reading operation. Here reported the HFDA801L's diagnostic features:

- Short to V_{CC}/GND faults
- Load detection, both DC and AC diagnostic
- Under/over voltage events
- Chip over temperature
- Digital input offset
- Output offset
- Output clipping

8.1 Load short detection

HFDA801L as the other device of the FDA family, implements a new concept of load diagnostic and it is specially designed for automotive applications. Advanced digital algorithms provide extremely reliable tests.

The FDA family diagnostic is performed in three phases and can be classified in:

- Short to V_{CC}/GND diagnostic
- DC load diagnostic
- AC load diagnostic

8.1.1 DC and AC internal diagnostic

In HFDA801L every channel could run its own DC or AC diagnostic independently from the other channels. This flexibility gives the system the possibility to analyze one single channel meanwhile the other channels are playing.

If DC diagnostic start commands are sent to all 4 channels in a single I^2C instruction, all the 4 diagnostics are performed simultaneously, while when AC diagnostic start commands are sent to all 4 channels the 4 diagnostics will be performed sequentially.

As described in Figure 34, the DC/AC diagnostic shall not be exectued when the V_{CC} supply voltage is lower than 6 V.

In case the diagnostic is executed with a V_{CC} supply voltage lower than 8 V two different situations can happen:

- Diagnostic result is not valid (DB2/3/4/5[d6] = "1", DATA NOT VALID).
- Diagnostic result is valid but not guaranteed to be inside the limit specified in Table 4.

Diagnostic enable

DC and AC diagnostic can be run independently by means of two I^2C bits for each channel: "start diag DC" and "start diag AC".

Once AC or DC diagnostic I^2C bits are set to "1" the amplifier channel performs the selected diagnostic. At the end of the diagnostic cycle the "start diag DC" or "start diag AC" instruction bits are set back to "0" by the device itself. If diagnostics are launched when the channel is in "PLAY" state it is necessary to set to "0" the play/mute bit in the I^2C register byte, one for channel. Otherwise if diagnostics are launched when the channel is in "MUTE" state the play/mute bit can be indifferently "0" or "1".

The idea is that the diagnostic can be performed only when the channel is in "MUTE" state: forcing the play/mute bit to "0" value we are forcing the finite state machine to mute the signal, if the channel was playing. Therefore the diagnostic on a specific channel starts only at the end of muting ramp.

Diagnostic sequencing and some special cases

If both "start diag DC" and "start diag AC" instruction bits are set to "1" the amplifier channel will perform first DC diagnostic and then AC diagnostic.

The DC diagnostics can be started at the same time on all 4 channels or separately; the AC diagnostics can be started at the same time on all 4 channels or separately.

However, the user should avoid these three special cases:

- DC diagnostic on channel "X" and AC diagnostic on channel "Y" at the same time, (with X different from Y).
- AC diagnostic with INTERNAL signal on channel "X" and AC diagnostic with EXTERNAL signal on channel "Y" at the same time, (with X different from Y).

- DC diagnostic on channel “X” and AC diagnostic with EXTERNAL signal on channel “Y” at the same time, (with X different from Y).

If the amplifier channel is in “eco-mode” and I^2C instructions for PWM ON + DIAG DC + DIAG AC + PLAY are given at the same time the channel will perform the following sequence automatically:

1. Turn on power stage
2. Perform DC diagnostic
3. Perform AC diagnostic
4. Enter PLAY mode

Internal Diagnostic start conditions

Diagnostic can be performed, only if:

- Channel is in MUTE state, (therefore with output PWM ON)
- DC or AC (or both) test enable bits are set from ‘0’ to ‘1’
- Overcurrent Protection level is set to OCP_0
- The PWM modulation is “in phase”
- Device is NOT kept in mute by means of the dedicated hardware pin

Relation with phase modulation

Diagnostic is performed only with PWM “in phase” modulation; “out of phase” modulation, if desired, must be selected after the AC-DC load diagnostic execution in order to avoid pop noise.

Setting of diagnostic “start diag DC” and “start diag AC” bits, for internal diagnostic

“Start diag DC” and “start diag AC” instruction bits should be set to “1” only in MUTE state.

8.1.2 Short to V_{CC}/GND diagnostic

The short to V_{CC}/GND diagnostic performs the sense of:

- “Hard” and “soft” short to V_{CC}
- “Hard” and “soft” short to GND

Timing

Short to V_{CC}/GND diagnostic cycle duration is the diagnostic time window duration, I^2C (IB6, d3-d2).

If a short to V_{CC}/GND is not stable during diagnostic cycle, the channel will remain in “short to V_{CC}/GND diagnostic” state until a fault or non-fault condition is stable for at least the diagnostic time window duration, I^2C (IB6, d3-d2). This special function avoids wrong communications in case of disturbs caused by mechanical stresses applied to the speaker (e.g. car door closing).

Short to V_{CC}/GND diagnostic automatic start:

Short to V_{CC}/GND diagnostic starts automatically after standby, and every time an overcurrent event occurs at the amplifier channel outputs.

Results communication and I^2C control:

After the diagnostic time window duration, I^2C (IB6, d3-d2), of diagnostic with stable fault/non-fault conditions there are two different situations:

- Fault is present: the channel will communicate the short presence by means of I^2C data bytes, (2 bits for each channel). The amplifier channel will remain in short to V_{CC}/GND diagnostic until the short is removed.
- Fault is not present: “short to V_{CC}/GND” diagnostic ends and the channel can actuate I^2C commands. After the short to V_{CC}/GND diagnostic ends without faults present, if the I^2C commands are already set, the amplifier will execute them immediately.

8.1.3 DC diagnostic

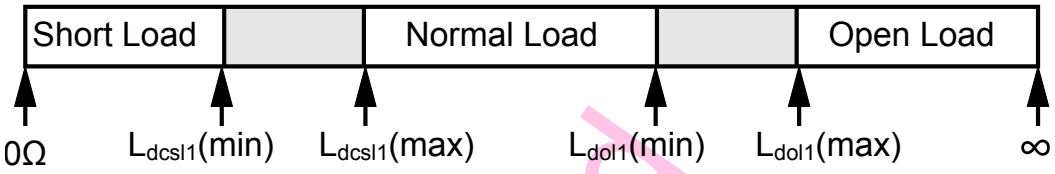
The load presence test is usually affected by noise, due for example to supply voltage variations or mechanical stress induced on the speaker (for example car door closing). The FDA amplifiers family provides a highly reliable and noise immune load diagnostic algorithm, with self-generated stimuli and widely programmable threshold ranges and time durations.

Load range can be configured based on some I^2C bits (IB11, d7-d6).

In the following figure it is shown the default configuration: IB11[7,6]=00.

Threshold windows for load diagnostic are fully programmable, by I²C. In default case, from L_{dcsl1} to L_{dol1} the load value is considered as normal load (see Figure 44).

Figure 44. Load detection precision and range in speaker mode, default I²C settings



Results: communication, as an example, in default case, for loads above L_{dol1} or below L_{dcsl1} an “open load” or “short load” message respectively will be displayed via I²C.

Timing: DC diagnostic pulse duration can be programmed via I²C. Typical values are shown in the Table 8 and Table 9. Duration can be calculated by:

$$Typical\ DC\ duration\ time = 4 \times DC\ diagnostic\ ramp\ time + 2\ DC\ diagnostic\ hold\ time \quad (1)$$

When default is used, the duration is 215 ms, pop-less.

Table 8. Diagnostic duration when IB6[D5-D4] = 00 and IB6[D7-D6] as reported in the table

Parameter	IB6[D7-D6]	Timing	Duration typ. [ms]	
			Fs = 44.1 kHz (IB0[D3-D2]=00)	Fs = 48 kHz, 96 kHz and 192 kHz (IB0[D3-D2]=01, 10, 11)
DC diagnostic ramp time selection	00	Normal	48	45
	01	X2	97	89
	10	X4	194	179
	11	/2	24	22

Table 9. Diagnostic duration when IB6[D7-D6] = 00 and IB6[D5-D4] as reported in the table

Parameter	IB6[D5-D4]	Timing	Duration typ. [ms]	
			Fs = 44.1 kHz (IB0[D3-D2]=00)	Fs = 48 kHz, 96 kHz and 192 kHz (IB0[D3-D2]=01, 10, 11)
DC diagnostic hold time selection	00	Normal	11.61	10.67
	01	X2	23.22	21.33
	10	X4	46.44	42.57
	11	/2	5.81	5.33

8.1.4 AC diagnostic

AC diagnostic checks the accidental disconnection of the tweeters in a 2-way speaker and, more in general, the presence of capacitive (AC) coupled loads.

HFDA801L provides an accurate AC diagnostic insensible to LC filter value thanks to a patented algorithm that is based on the measurement of both magnitude and phase of the load connected: this makes the AC diagnostic able to correctly detect even very small AC load impedance variations in the module after a tweeter disconnection.

As a basic description, the AC diagnostic uses a sinusoidal stimulus to verify if the tweeter is present measuring the impedance connected to the outputs and giving a result according to a threshold.

The tweeter is considered present if the load impedance is below lac ± 25% (when LC filter and other external component as specified in Section 9.4 External components guideline), while, if higher than this threshold the tweeter is considered not connected. The AC diagnostic can be performed both with internally generated signals and with externally generated signals. The result of the AC diagnostic test (AC load impedance and consequently the threshold for connected/disconnected tweeter) is influenced by normal or parallel operation setting (IB1[7-6]).

Since the overcurrent protection level affects the result of the diagnostic, the OCP_0 level must be set before running either internal or external AC diagnostic.

HFDA801L AC diagnostic creates an optimized signal for load analysis. The signal is a high frequency amplitude-modulated sine wave. During the AC diagnostic with internal signal the positive output is automatically fixed at half VCC in order to enhance diagnostic precision.

Voltage gains GV are directly managed by the internal logic when AC diagnostic test is executed by using the internally generated signal. The result is then independent from GV settings.

The internal generated signal has a frequency that varies according to the PWM switching frequency selected (22.050 KHz at Fs = 44.1 KHz, 24 Kz at Fs = 48, 96, 192 KHz) but always lies over audio band.

8.1.5 Diagnostic error code

Table 10. DC diagnostic error code

Error Code	What happened	When happened	Diagnostic Result
1000 0001	Overcurrent	First pulse unmuting ramp	Test not valid
1000 0010	Overcurrent	DC hold phase	Test not valid
1000 0011 1000 0100	Supply voltage went low causing current measurement clipping or voltage clipping	During whole DC pulse	Test not valid
1000 0101 1000 0110 1000 0111 1000 1000	Abnormal current injection	DC hold phase	Test not valid

Error code can be read in DB8-11-14-17 when the test is ended but invalid (DB2[7-6]/DB3[7-6]/DB4[7-6]/DB5[7-6] = ‘10’).

The first event in the table represents a particular case: error code can be read when the test is ended and valid (DB2[7-6-5-4]/DB3[7-6-5-4]/DB4[7-6-5-4]/DB5[7-6-5-4] = ‘1111’).

Table 11. AC diagnostic error code

Error Code	What happened	When happened	Diagnostic Result
1000 1001	Overcurrent	During whole AC pulse	Test Not Valid – Short Load
1000 1010 1000 1011	Supply voltage went low causing current measurement clipping or voltage clipping	During whole AC pulse	Test not valid
1000 1100 1000 1101	Abnormal current injection	Unmuting ramp	Test not valid
1000 1110 1000 1111	Abnormal current injection	During AC test	Test not valid
10010000	Short	Unmuting ramp	Test valid
10010001	Short	During AC test	Test valid

Error code can be read in DB10-13-16-19 when the test is ended but invalid (DB6[7-6]/DB7[7-6] = ‘10’).

The last 2 events in the table represent a particular case: error code can be read when the test is ended and valid (DB6[7-6-5-4]/DB7[7-6-5-4] = ‘1101’). The flag on bit DB6[4]/DB7[4] indicates that the information written in the registers DB10-13-16-19 is related to an error code and not to a phase value. Moreover, the load stored in DB9-12-15-18 is always 0 Ω.

8.1.6 Diagnostic timelines

Here below some examples of diagnostic timelines are reported.

Sequence and finite state machine relation:

After output bias and power manager start-up phases an automatic short to V_{CC}/GND diagnostic is managed by the device, following the finite state machine operation as reported in Section 5.1 Finite state machine. If no shorts are present the device moves to eco-mode state where the I^2C programming of DC and AC diagnostic is effective. DC and AC diagnostic can be started “on demand” in any moment, provided that the device is in MUTE state.

Diagnostics durations:

V_{CC}/GND diagnostic and DC diagnostic durations can be set acting on the I^2C IB6 byte. In this way the user can reduce the total diagnostic and, thus, start-up time, with a trade-off with diagnostic audibility that depends on the speaker used.

DC diagnostics can be started on all four channels in the same time frame.

AC diagnostics are launched sequentially with a fixed duration of 16ms per channel, (for the 4 Ω load case).

I^2C and I^2S relation:

For relation of diagnostic with I^2C and I^2S usage please refer to Section 11.5 Timing requirements.

Figure 45. DC diagnostic before turn on

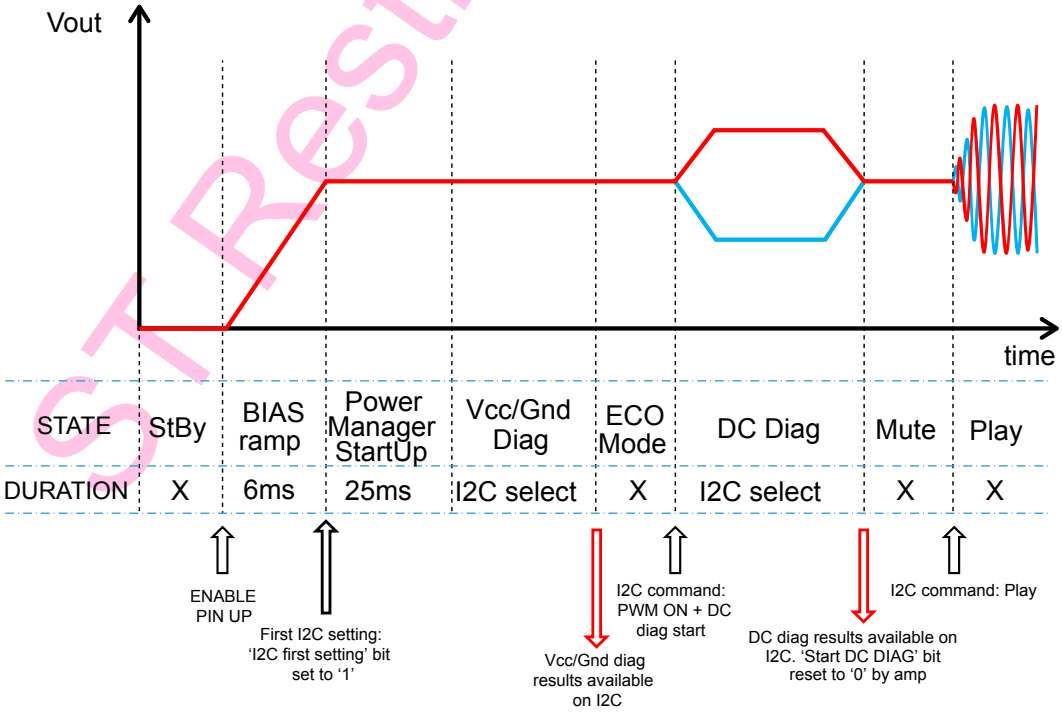


Figure 46. **AC diagnostic before turn on**

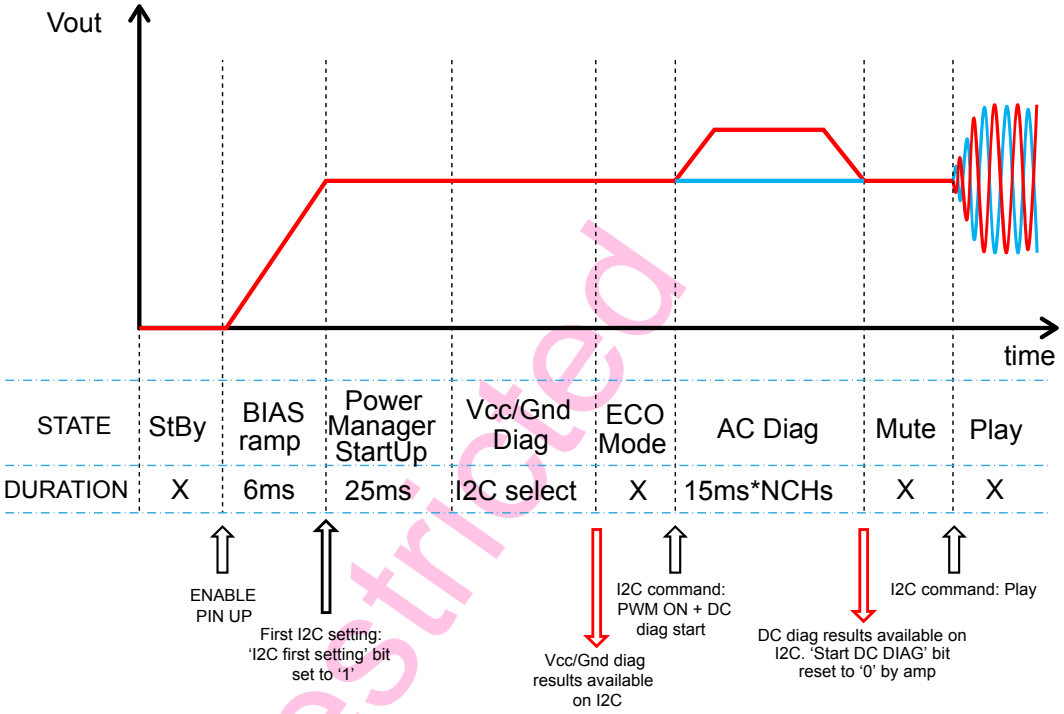


Figure 47. **DC diag + AC diag + play in a single I²C bus instruction**

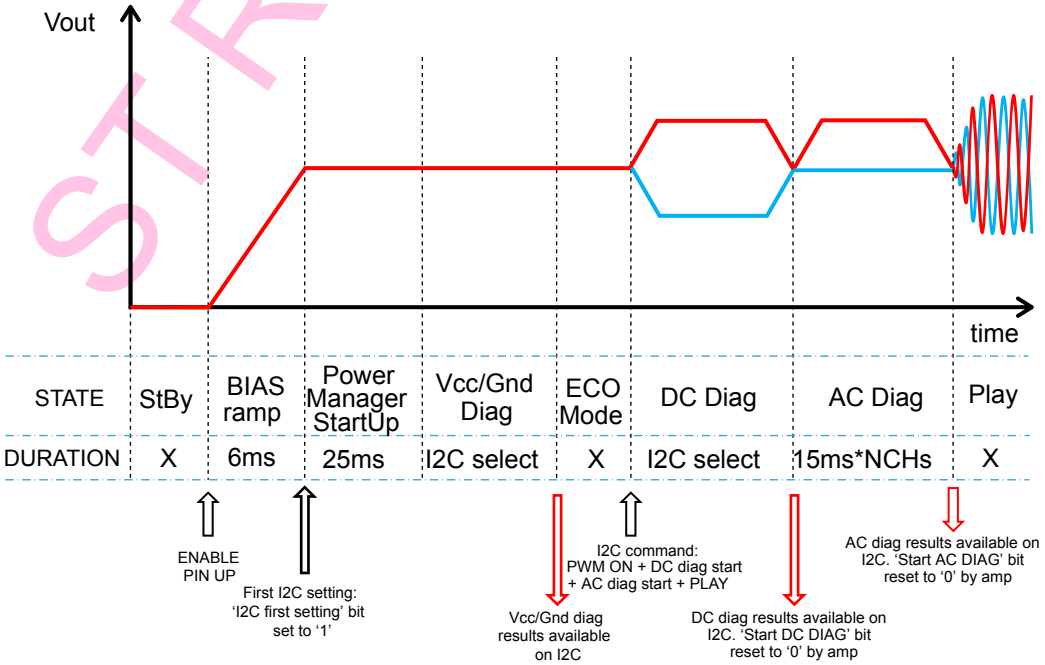


Figure 48. **Fast start-up (DC diag + AC diag + play)**

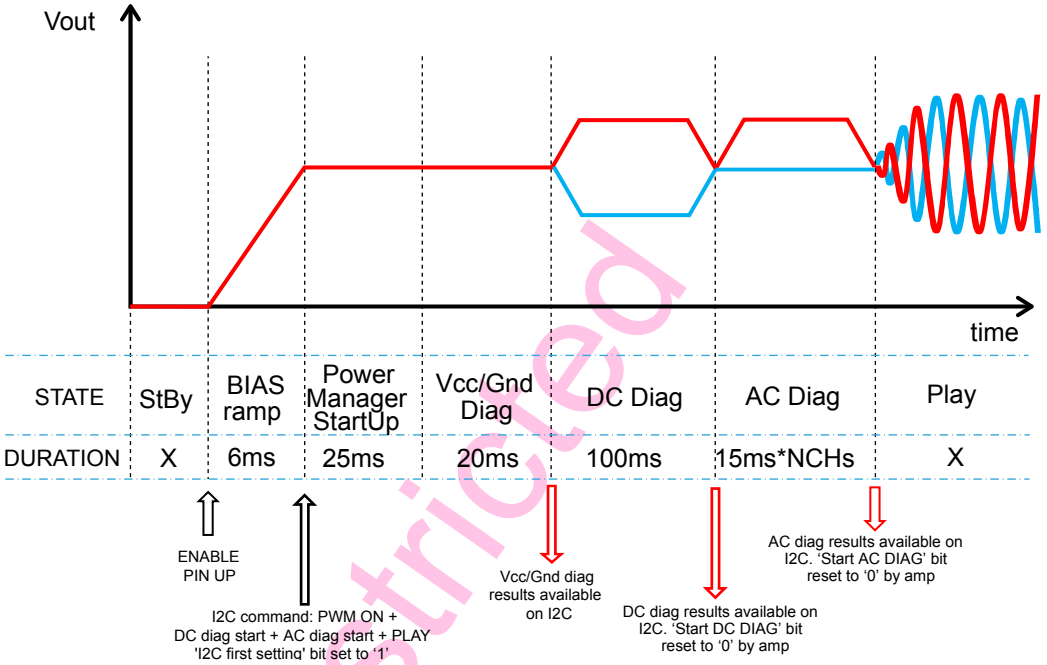


Figure 49. **DC and AC diag with separated commands before turn on**

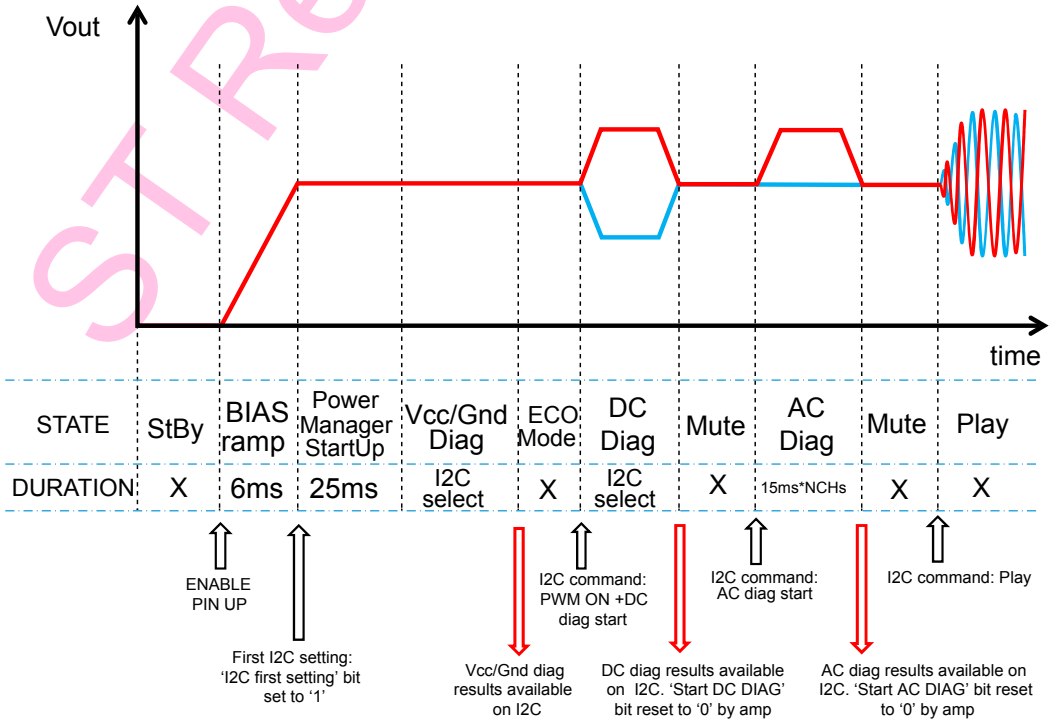


Figure 50. **Short to V_{CC} present at Turn ON**

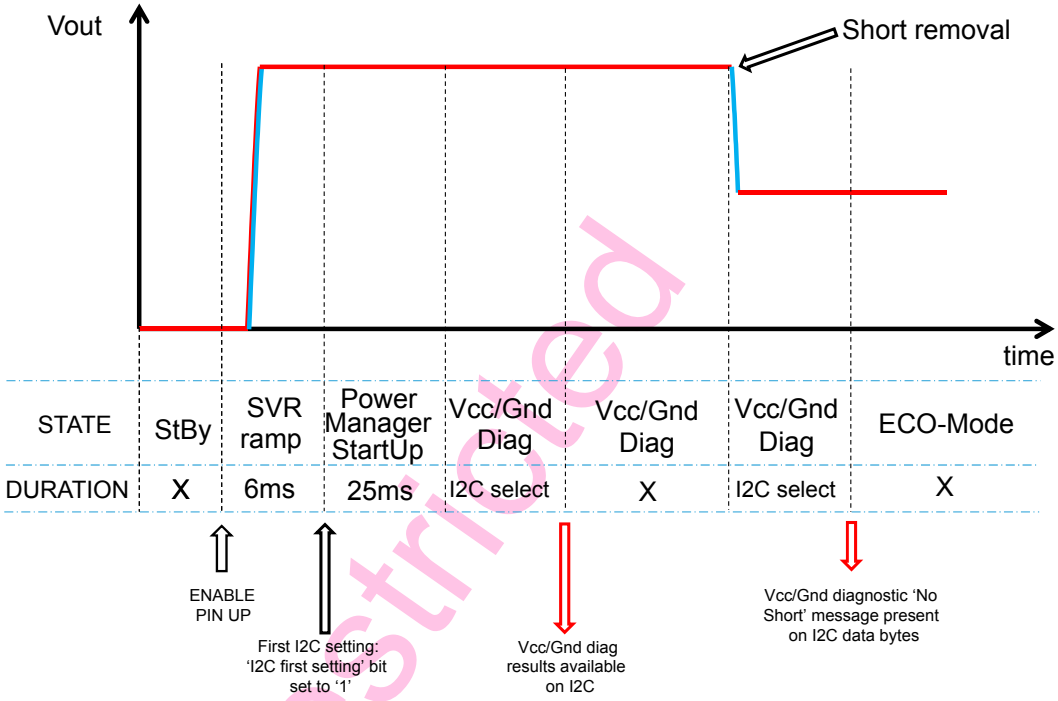


Figure 51. **DC and AC diagnostic in mute**

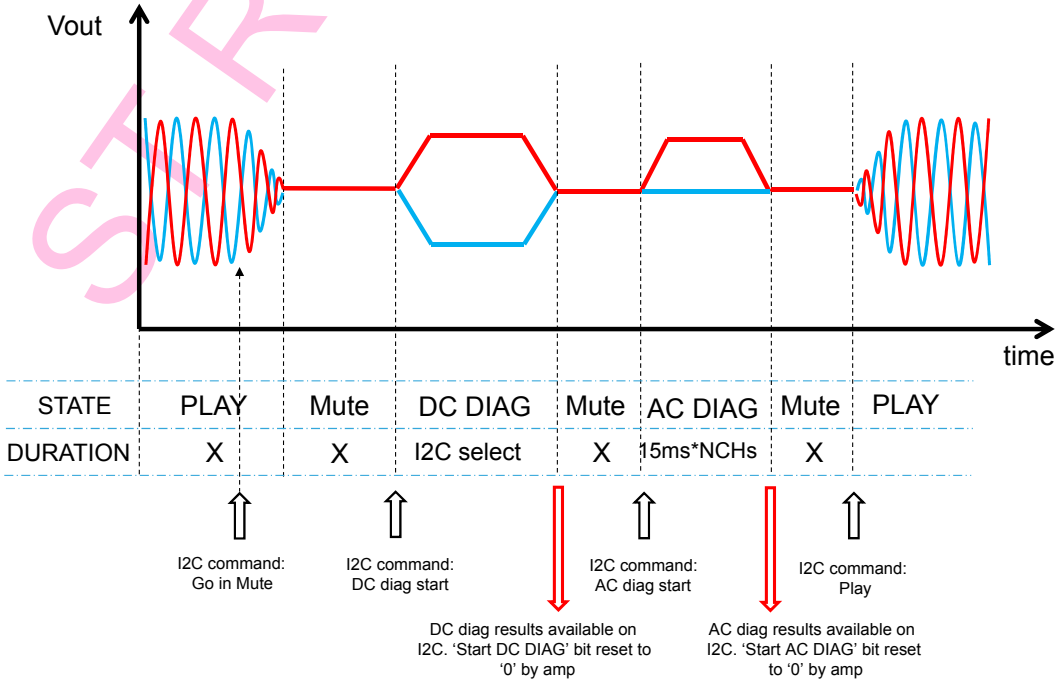
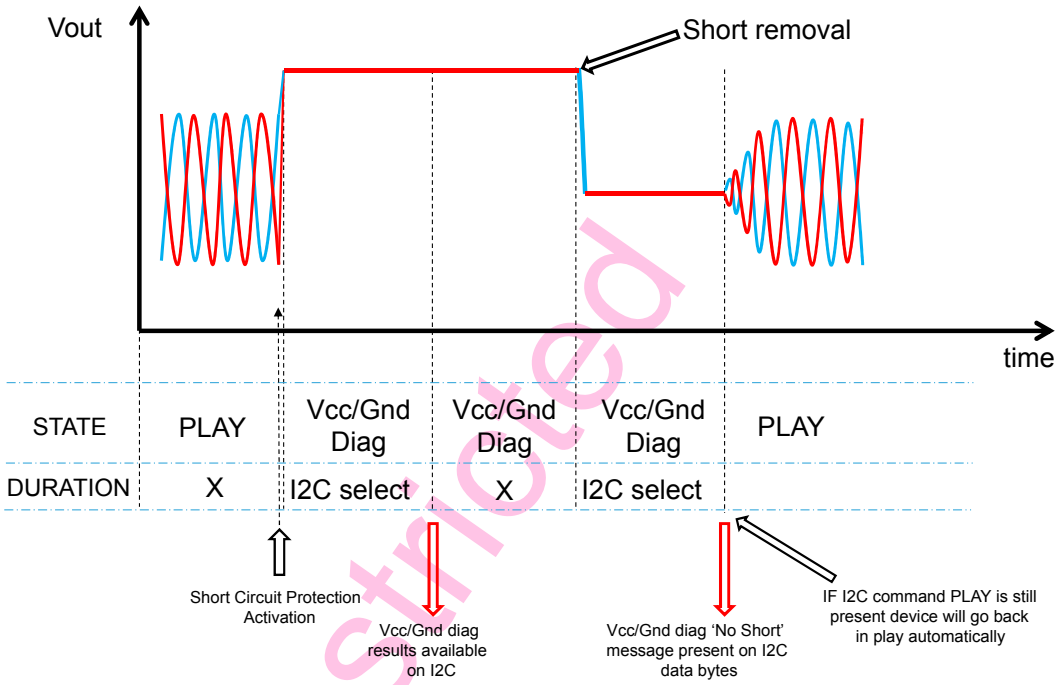


Figure 52. **Short circuit protection activation - Short to V_{CC} present**



8.1.7 Diagnostic in parallel mode

In case of parallel mode configuration, the short load and open load thresholds are halved, with respect to those in standard mode reported in Section 8.1.3 DC diagnostic and Section 8.1.4 AC diagnostic. Digital impedance meter (DIM) results change as well and the communicated load impedance value must be interpreted using an additional factor, as reported in Section 8.3.1 DIM result communication.

When in parallel mode, the diagnostic must be launched only on controller channels, as a consequence of the procedure reported in Section 4.3.1 Parallel mode control and recommendation and the results must be read referring to the controller channels.

8.1.8 AC diagnostic with external signal

This kind of diagnostic allows to check the impedance of the load using a user-defined signal. The algorithm is the same used for the AC diagnostic with internally generated signal and it permits to measure the load impedance magnitude and phase at a desired frequency.

It is needed to send a sinusoidal signal by I^2S, put the device in play selecting the channels to be tested and set the AC diagnostic I^2C bits to “1” keeping the play/mute bit set to “1”.

At the end of the diagnostic cycle the “start diag AC” instruction bits are set back to “0” by the device itself.

Since the algorithm works when the device is in “PLAY” state, any I^2C setting that influences audio signal also impacts on the results of the diagnostics. Therefore, it is important that the signal will not be subjected to modifications in amplitude and frequency, during the whole test.

The signal must have the following characteristics:

- - 30 dBfs < Amplitude < -13 dBfs
- - 500 Hz < Frequency < 5 KHz

External AC diagnostic thresholds are the same as the internal AC diagnostic.

Note: AC diagnostic with external signal - due to internal architecture - can be supported with the specified limits only up to 5 kHz. Above those frequencies (f > 5 kHz) the precision/ accuracy is no more guaranteed inside the mentioned limits. It is also possible to run diagnostic with external signal AC (f > 5 kHz) taking into account that the higher is the test signal frequency, the higher is the error.

8.1.9 DC and AC constraints

While running DC or AC diagnostics, some precautions, regarding the I^2C bits setting, must be adopted in order to guarantee that the algorithms work properly.

Particularly referring to the IBx registers:

- DC and AC diagnostic with internally generated signal can be executed only with voltage gain different from GV4.
- AC diagnostic with external signal can be executed with;
  - Voltage gain = GV4

About the results stored in the DBx registers:

- When the test is invalid, the user should not care of short/open load bits.

8.2 Open load in play detector

The open load in play detector aim is to detect the possible speaker detachment during PLAY state.

The innovative internal architecture allows to detect an open load condition taking advantage of the audio signal itself, guaranteeing high detection reliability without requiring a dedicated test signal.

8.2.1 Open load in play detector operation overview

The open load in play detection consists in one single shot test, which can be repeated according to the user's need.

The test firstly checks the audio signal characteristics. If the audio signal is judged good enough to provide a reliable result, the test result is valid. Otherwise, if the audio signal doesn't allow to perform a reliable detection, the test result is not valid, and the user needs to repeat the test.

During the same evaluation time window, an internal circuit measures the differential current flowing through the pins OUTP and OUTM. The test consequently evaluates both the digital input signal and the output current, monitoring the average load impedance over time.

If the test result is valid and the average load impedance exceeds the chosen impedance threshold, the device communicates that the load is not connected. Otherwise, if the test result is valid and the average load impedance is lower than the chosen threshold, the device communicates that the load is connected.

8.2.2 Processing bandwidth range

The feature requires an accurate measurement of the current flowing through the speaker.

The filter capacitors behave like an undesired load connected in parallel with the speaker, altering the current measurement. However, this undesired contribution is significant only in the high frequency range of the audio bandwidth.

On the other side, most of the audio signal energy is distributed in the middle-low frequency range of the audio bandwidth.

Due to the mentioned reasons, open load in play detector processes the audio bandwidth up to 2 kHz approximately, in order to guarantee a highly reliable solution without affecting the rate of valid tests.

Please note that the processing bandwidth limitation does not affect the main signal path from digital input signal to output voltage on FBP and FBM pins.

8.2.3 Audio signal evaluation

The audio signal is considered a good test signal if its amplitude allows the internal circuits to perform accurate measurements. open load in play detector processes the audio signal only if its amplitude exceeds the values expressed in Table 12:

Table 12. Open load in play detector impedance and validity thresholds

	Validity threshold vs input signal [dBFs]	Validity threshold vs output voltage [V]	Open load in PLAY in standard mode: HIGH threshold (IB11-d6 = 0)	Open load in PLAY in parallel mode: HIGH threshold (IB11-d6 = 0)	Open load in PLAY in standard mode: HIGH threshold (IB11-d6 = 1)	Open load in PLAY in parallel mode: HIGH threshold (IB11-d6 = 1)
GV1	> -25	> -1.46	LDOL1	0.5 x LDOL1	LDOL2	0.5 x LDOL2
GV2	> -25	> -1.07	0.75 x LDOL1	0.4 x LDOL1	0.75 x LDOL2	0.4 x LDOL2
GV3	> -25	> -0.62	0.45 x LDOL1	0.25 x LDOL1	0.45 x LDOL2	0.25 x LDOL2
GV4	> -25	> -0.45	0.35 x LDOL1	0.18 x LDOL1	0.35 x LDOL2	0.18 x LDOL2

The audio signal is unknown and not stationary, while the speaker has a complex impedance. Open load in play detector evaluates the audio signal for a time window lasting up to 1 s in order to properly average the data over time. The detection is considered valid if, during the evaluation time window, the input audio signal exceeds for 300 ms the thresholds reported in Table 12.

8.2.4 I²C control and timing

The user must set IB13[7-4] in order to start the open load in play detection for each channel.

Once the test is started, the internal circuits required for the detection are turned on, requiring a settling time lasting approximately 500 ms.

When the internal circuits are ready to work, both digital input signal and output current measurement start being evaluated, following the impedance threshold set through IB11[6]. Depending on the audio signal characteristics, the evaluation can last from 300ms to 1s approximately.

At the end of the evaluation, the device:

- Sets DB20[2] = '1' to communicate that the test ended successfully, and resets IB13[7] allowing the user to perform another test afterwards
- Sets DB20[1] = '1' to communicate that the test result is valid, otherwise sets DB20[1] = '0' to communicate that the test result is not valid.
- Sets DB20[0] = '1' to communicate that an open load has been detected, otherwise sets DB20[0] = '0' to communicate that an open load has not been detected.

Please note that the value on DB20[0] is significant only if the test result is valid.

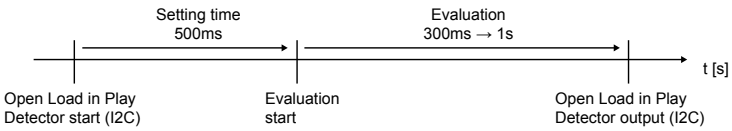
If the device FSM moves from PLAY to another state during the open load in play detection routine, the test ends unsuccessfully by keeping the flag DB20[2], clear. The device automatically resets IB13[7-4] allowing the user to repeat the test.

In the example above the DB20 refers to the information related to the channel #1, for the other channels DB21, DB22 or DB23 are the Data registers to be read.

If the test ends successfully but the result is not valid, the user must repeat the test. This condition happens when the audio signal is not good enough for a reliable detection.

The detection timings are represented in Figure 53:

Figure 53. Open load in play detector timing



If the device FSM moves from PLAY to another state during the open load in play detection routine, the test ends unsuccessfully by keeping the flag DB20[2], clear. The device automatically resets IB13[7-4] allowing the user to repeat the test.

8.3 DIM

HFDA801L implements a new powerful feature: a digital impedance-meter (DIM) embedded in the audio power amplifier. The DIM is activated while “DC diagnostic” and “AC diagnostic” are running and provides the user with the value of the load across the outputs.

More specifically it provides:

- The load resistance value after “DC diagnostic” state: DIM DC
- The phase value after “AC diagnostic", only if executed with external generated signal, state: DIM AC
- The magnitude value after “AC diagnostic” state: DIM AC

This feature goes beyond the standard failure present/not-present recognition of the diagnostic function. The user µC can elaborate the information provided and use them for implementing a large set of functions, (output equalization, speaker defects compensation, speaker sound enhancement…), without the need of dedicated external components.

8.3.1 DIM result communication

DIM results are communicated via I²C data register from DB8 to DB19. The DIM AC is activated running the AC diagnostic and the results are stored in module and phase, only when AC diagnostic executed with external signal.

- Magnitude is stored in: DB9 (CH1), DB12 (CH2), DB15 (CH3), DB18 (CH4)
- Phase is stored in: DB10 (CH1), DB13 (CH2), DB16 (CH3), DB19 (CH4), only when AC diagnostic executed with external signal

The DIM function is automatically activated running the DC diagnostic and the results are stored in:

- DC output load Resistance DB8 (CH1), DB11 (CH2), DB14 (CH3), DB17 (CH4)

The load resistance/AC-magnitude values written in the DBx register are represented by 7 significant bits and 1 bit as a multiplier, according to the following format representation:

Table 13. Load resistance/AC-magnitude values representation in DBx register

d7	d6	d5	d4	d3	d2	d1	d0
0 → M = 0.1 1 → M = 1.0	C[6]	C[5]	C[4]	C[3]	C[2]	C[1]	C[0]

The resistance could be calculated using this formula:

$$R = M \times D_P \times C[6 \div 0] \quad (2)$$

Where:

D_p is the factor to be applied for parallel mode operation:

- 1 in standard mode
- 0.5 in parallel mode

The load AC-phase value, stored in the DBx register, is represented by 8 bits in two complement formats and expressed in degrees in a range from -128 °C to +127 °C.

8.4 Overcurrent protection

When a short circuit is present on the amplifier outputs the over current protection is reached.

Once over current protection threshold is reached the amplifier immediately reacts interrupting the output signal and moving the system in protection. Amplifier will thus start automatically a V_{CC}/GND diagnostic phase, as described in Section 5.1 Finite state machine.

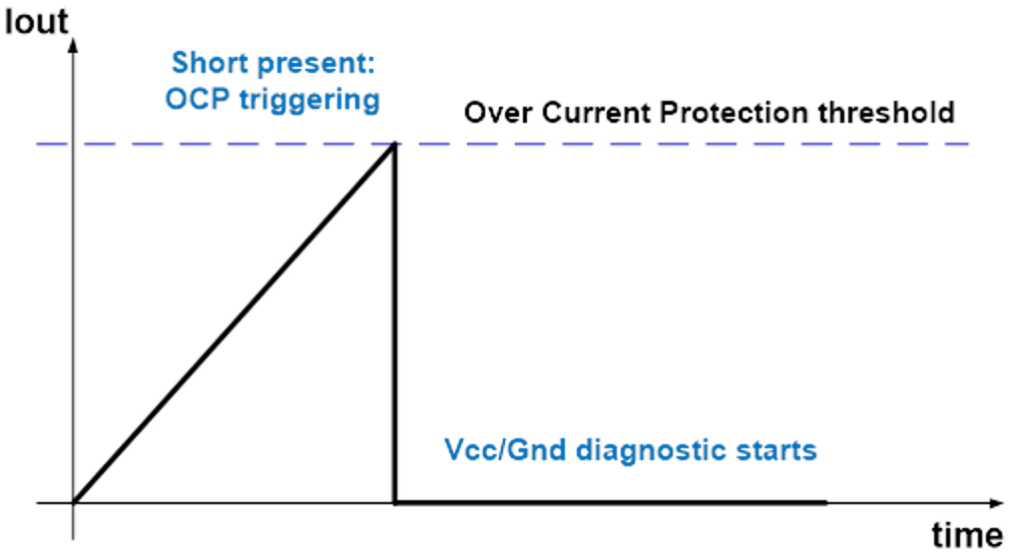
Different levels of OCP can be selected acting on I²C IB12-d4,d5,d6, as described in Table 14:

Table 14. Over current value I²C selection

IB12-d5	IB12-d4	IB12-d6 (+ 1A option)	OCP current level (typical)
0	0	0	OCP_0
0	1	0	OCP_1
1	0	0	OCP_2
1	1	0	OCP_3
0	0	1	OCP_0 (+1 A option not available)
0	1	1	OCP_1 + 1 A
1	0	1	OCP_2 + 1 A
1	1	1	OCP_3 + 1 A

Note:
- *OCP_0/1/2/3 values are reported in Table 4.*
- *The + 1 A option with IB12-d4,d5 = 00 is not permitted and thus automatically disabled by the device.*

Figure 54. **Overcurrent protection intervention example**



8.5 Input offset detection

The input offset detector aim is to avoid any possible offset that could come from µC through I^2S/TDM input stream. For this purpose, the HFDA801L input offset detector performs an evaluation of the input signal and calculates if an offset with values higher than -18 dBFs is present. If an input offset is sensed, the offset detector flag DB0-d7 goes to '1'. Moreover, if the high pass filter function is selected by means of IB1[d2], the HFDA801L will eliminate the input offset giving a complete robustness to any disturbance or malfunction coming from the previous audio chain blocks. The input offset detector and high-pass filtering are working during PLAY mode and MUTE state.

8.6 Output offset detection

8.6.1 Output voltage offset detection

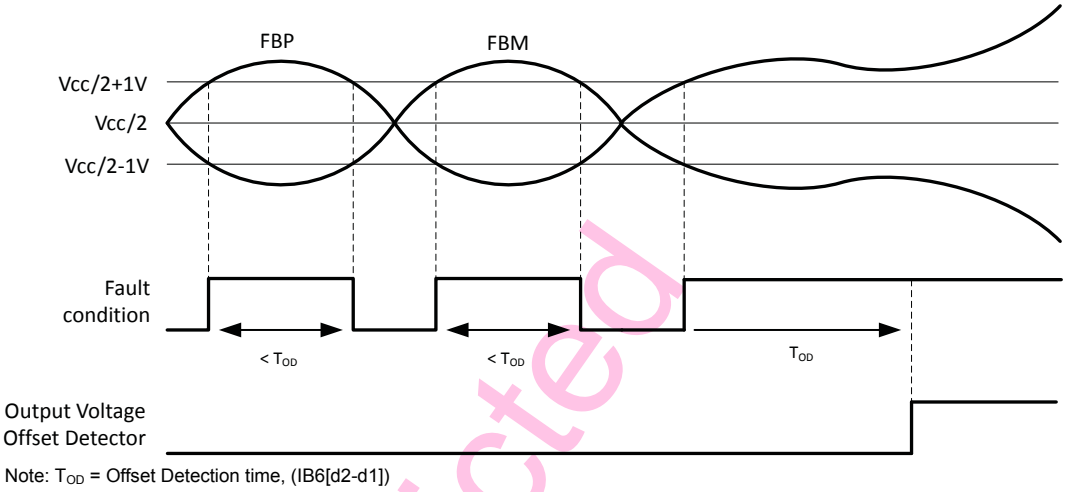
During play operation, the presence of an offset on the amplifier output can damage the speakers. For this purpose HFDA801L embeds the output offset detector function. Thanks to this function, HFDA801L is able to detect when the voltage difference between $V_{CC}/2$ and the voltage value on FBP pin, or between $V_{CC}/2$ and the voltage value on FBM pin, exceeds 1 V.

Its activation, IB1-d1 = "1", is necessary to avoid the presence of such failures at system level.

If the fault condition persists for the offset detection time, (IB6[d3-d2]), consecutively, the circuits set the flag on I^2C bit (DB20[5], DB21[5], DB22[5], DB23[5]). As soon as the fault condition is removed, both the flag and the Offset Detection time, (IB6[d3-d2]), counters are reset. The implemented logic avoids false detections in case of very low signal frequency.

The feature operation is showed in Figure 55:

Figure 55. **Output voltage offset detector operation**



Note: T_{OD} = Offset Detection time, (IB6[d2-d1])

When enabled, the feature is active both in MUTE and in PLAY states.

The offset detector output is provided in two forms:

- Enables the pull down on CDDiag pin, if IB3[1] = '1'
- Sets the flag DB20[5] = '1' for channel 1, DB21[5] = '1' for channel 2, DB22[5] = '1' for channel 3, DB23[5] = '1' for channel 4

8.7 Thermal protection

The device integrates different protection levels against over-temperature conditions.

The first protection level consists only in communicating if the temperature exceeds four different thresholds, from TW4 to TW1. The result is provided in two ways:

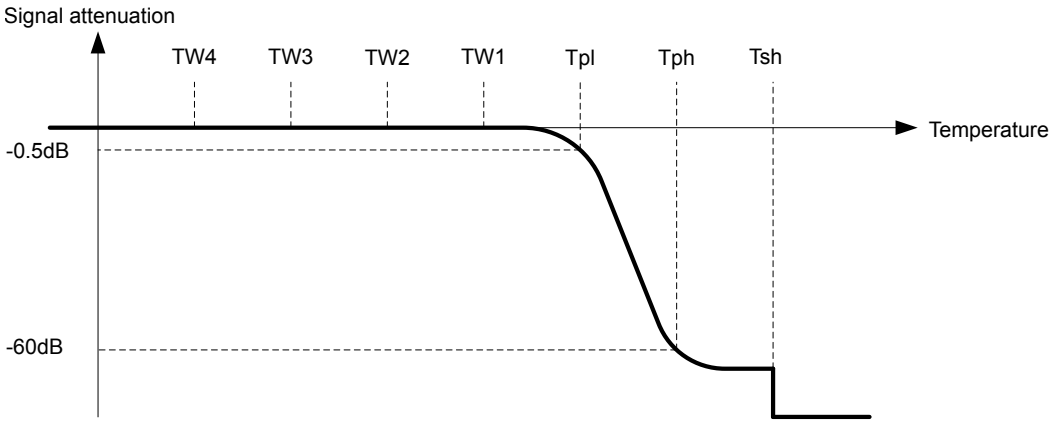
- Setting DB1[7-4];
- Pulling down the CDDiag pin, coherently with the setting of IB3[6-4].

If needed, the user should take proper actions to counteract the temperature rising.

The second protection level consists in the output signal attenuation as a function of the temperature, in order to reduce the power dissipation. The thermal attenuation occurs in the temperature range between Tpl and Tph, as shown in Figure 56.

The third level protection consists in switching off the power stage when the temperature overpasses the Tsh value. As shown in Figure 56, after thermal shutdown triggering, the device FSM enters in "Short to V_{CC}/GND diagnostic state", preventing subsequent power stage turn on in case of shorts to battery or ground.

Figure 56. **Thermal attenuation curve**



8.7.1 Temperature information

The HFDA801L embeds a thermal sensor for the communication of the average chip temperature via I²C bus.

The temperature is communicated on the I²C about register DB28-d0/d1 and DB29-d0/d7, by means of 10 bits expressed in 2- complements, in which each bit represents about 1 °C.

$$Die\ Temperature = K_{TADC} \times 2\ complement\ (DB28[1:0]\ DB29[7:0]) \quad (3)$$

Where:

K_{TADC} is the thermal reading correlation factor to be applied. Values can be found in Table 4.

This gives the user the possibility to easily read the average chip temperature in °C by simply reading the I²C.

Example:

DB28 = ”xxxxxx00”, DB29 = ”01000110” → Thermal reading=”0001000110” 10 bits-2complement → 75 °C

DB28 = ”xxxxxx00”, DB29 = ”00010111” → Thermal reading=”0000010111” 10 bits-2complement → 25 °C

DB28 = ”xxxxxx11”, DB29 = ”11101001” → Thermal reading=”1111101001” 10 bits-2complement → -25 °C

The information is updated every 1 ms.

8.7.2 Local thermal protection

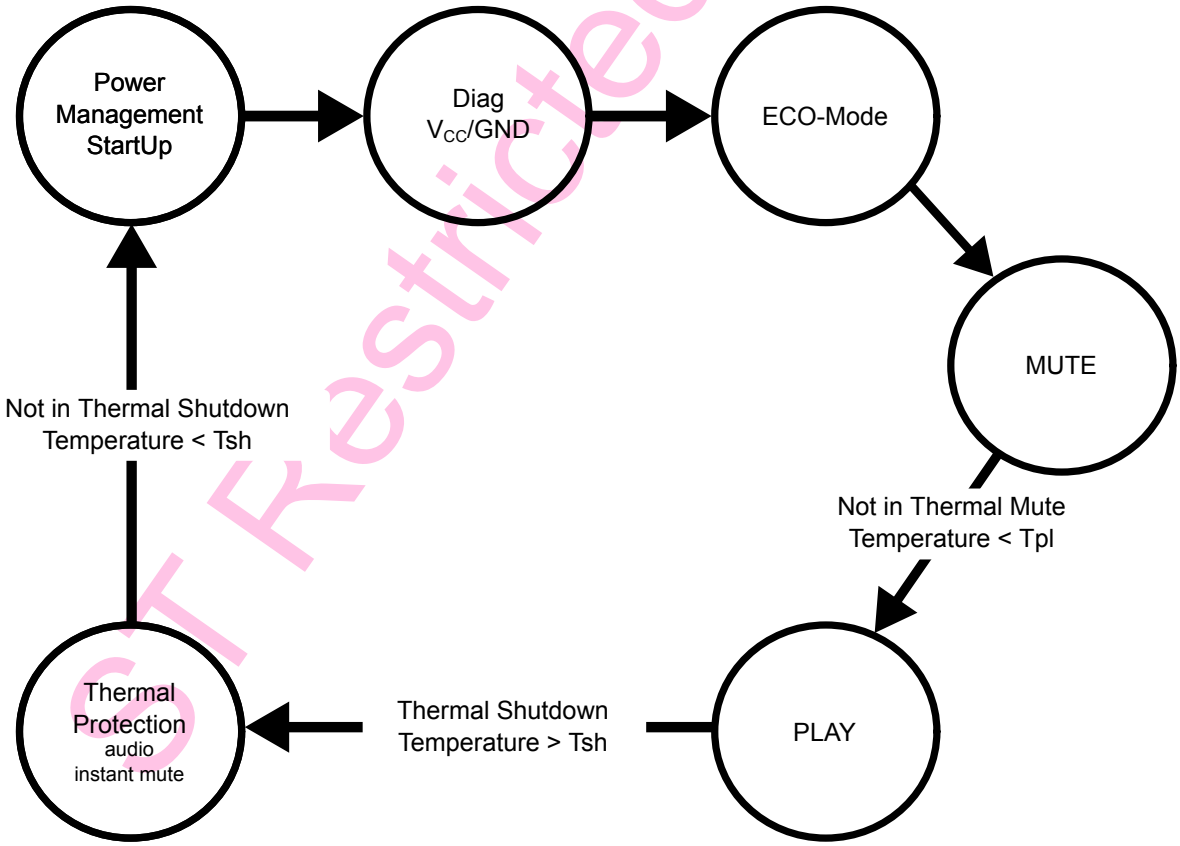
To protect the output stage of the device against local high temperature, a local thermal protection is embedded on each channel. Activation of the local thermal protection will cause the impacted channel to be muted and the related I²C data bit is set to ‘1’ (DB0[3] for channel 1, DB0[4] for channel 2, DB0[5] for channel 3, DB0[6] for channel 4).

Note: When the local thermal protection is activated on a channel, also the OCP flag is set. For example in case of thermal protection activation on channel 1, DB0[3] = 1, also DB2[5] = 1, OCP activated on channel 1.

8.7.3 Thermal shutdown

When the device temperature is over Tpl (see Table 4) the device is in Thermal Mute region and the output signal is attenuated proportionally to the temperature, as shown in Figure 56. When the device temperature reaches the shutdown threshold, over Tsh (see Table 4), the device moves into a thermal protection state in which all the outputs are instantly switched off and no PWM activity is present on the output. As soon as the temperature becomes lower than Tsh, the device exits from the thermal protection state and recovers to the normal operation. The device is then still in mute state until it does not exit from the Thermal mute region, and the temperature is between Tsh and Tpl. Once the device temperature becomes lower than Tpl the device automatically exits from Thermal Mute region and the PWM activity is restarted on the output.

Figure 57. Recover from thermal shutdown flow diagram



9 Application design high level guidelines

9.1 I²C settings

The I²C settings used for measurement present on the current data sheet, and suggested to be used as best settings, are shown in Table 15:

Table 15. I²C settings

IB name	IB address [hex]	Default value after reset		Suggested settings to be programmed	
		hex	bin	hex	bin
IB0	0x00	0x00	00000000	0x02	00000010
IB1	0x01	0x00	00000000	0x02	00000010
IB2	0x02	0x00	00000000	0x00	00000000
IB3	0x03	0x00	00000000	0x00	00000000
IB4	0x04	0x01	00000001	0x01	00000001
IB5	0x05	0x00	00000000	0x00	00000000
IB6	0x06	0x00	00000000	0x00	00000000
IB7	0x07	0x00	00000000	0x00	00000000
IB8	0x08	0x00	00000000	0x00	00000000
IB9	0x09	0x00	00000000	0x00	00000000
IB10	0x0	0x00	00000000	0x00	00000000
IB11	0x0B	0x10	00010000	0x10	00010000
IB12	0x0C	0x00	00000000	0x00	00000000
IB13	0x0D	0x00	00000000	0x00	00000000
IB14	0x0E	0x00	00000000	0x11	00010001
IB15	0x0F	0x00	00000000	0x11	00010001
IB16	0x10	0x00	00000000	0x11	0x00010001
IB17	0x11	0x00	00000000	0x11	0x00010001
IB18	0x12	0x01	00000001	0x01	00000001
IB19	0x13	0x98	10011000	0x9C	10011100
IB20	0x14	0x00	00000000	0x00	00000000
IB21	0x15	0x00	00000000	0x00	00000000
IB22	0x16	0x00	00000000	0x00	00000000
IB23	0x17	0x08	00001000	0x09	00001001
IB24	0x18	0x00	00000000	0x01	00000001

In case I²C suggested settings are used (see the Table 15), best THD performances can be obtained.

When the frequency hopping is set to mid frequency value (I²C register IB24[1-0] = 00), however, the THD can be up to 0.1% (f = 1 kHz, Po > 1 W).

9.2 Power supply

The device has two internal regulators to supply two internal floating rails. One voltage rail, suppling the analog circuitry, is 5 V between A5SVR and AGSVR. The other voltage rail, supplying the digital circuitry, is 1.8 V between D1V8SVR and DGSVR.

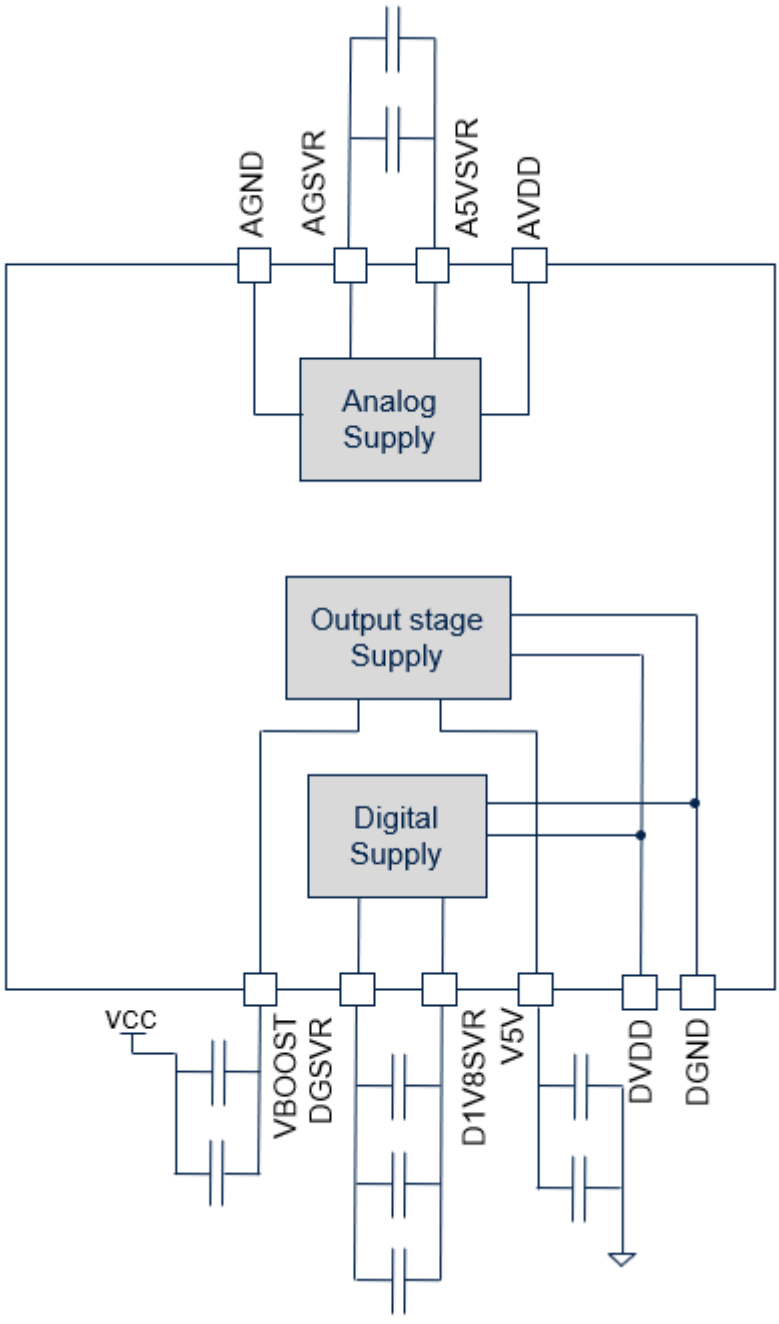
Other two internal supply lines are present to supply the output stages. The lowest one is 5 V between V5V and ground and the highest one is 7 V between Vboost and V_{CC}.

9.3 Internal power supply capacitor guideline

All these internal supplies need to be filtered by external capacitors. For each supply a couple of capacitors with different capacitance values must be applied. The biggest one acts as dominant pole for the supply and the smallest one acts to reduce the impact of the parasitic inductance of the former capacitors filtering high frequency noise.

The Figure 58 shows the internal power supplies with the related external capacitors.

Figure 58. Internal power supply



9.4 External components guideline

The external components have impact on the audio performances and on the EMC of the HFDA801L, especially the components related to the demodulator filter, power supply filter and the capacitors of the floating regulators. They should be designed according to the platform target.

In the Table 16, the parts used in the DEMO boards are reported, designed to provide 24 W on 4x4 Ω at battery level (14.4 V) with 1% of THD.

Table 16. External components example list for 4 Ω battery level applications

Quantity	Designator	Value	Description	Function	Tolerance [%]	Rated Current[A]/ Voltage[V]/ Power [W]	Package
1	C1	4.7 µF	SMD MLCC X7R capacitor	Floating regulators	10%	25 V	0805
3	C2, C29, C33	100 nF	SMD MLCC X7R capacitor	Floating regulators	10%	25 V	0603
8	C5, C8, C10, C15, C17, C20, C22, C27	220 nF	SMD MLCC X7R capacitor	Damping network	10%	50 V	0805
8	C7, C9, C11, C14, C19, C21, C23, C26 PN: C0805C154K5RACAUTO	150 nF	SMD MLCC X7R capacitor	Demodulator filter	10%	50 V	0805
11	C28, C42, C44, C48, C49, C58, C59, C62, C63, C64, C65	100 nF	SMD MLCC X7R capacitor	Floating regulators	10%	50 V	0603
2	C47, C61	2.2 µF	SMD MLCC X7R capacitor	Supply filter	10%	50 V	1210
2	C41, C43	1 µF	SMD MLCC X7R capacitor	Supply filter	10%	50 V	0805
1	C30	10 µF	SMD MLCC X7S capacitor	Floating regulators	10%	25 V	0805
1	C31	10 pF	SMD MLCC C0G/NP0 capacitor	Floating regulators	10%	25 V	0603
1	C32	10 µF	SMD MLCC X7R capacitor	Floating regulators	20%	50 V	1210
1	C36	2.2 µF	SMD MLCC X7R capacitor	Floating regulators	10%	25 V	0805
1	C38	47 pF	SMD MLCC C0G/NP0 capacitor	Floating regulators	5%	25 V	0603
8	L1, L2, L3, L4, L5, L6, L7, L8 PN: VCHA075D-3R3MS6CT	3.3 µH	SMD power inductor	Demodulator filter	20%	11.6 A	
1	L9	10 µH	SMD power inductor	Floating regulators	20%	2 A	
8	R4, R6, R9, R10, R12, R14, R17, R18	4.7 Ω	Surface mount chip resistor	Damping network	1%	200 V 0.25 W	1210
1	R21	10 Ω	Surface mount chip resistor	Floating regulators	1%	150 V 0.5 W	0805

Note: In case of 2 Ω loads application, it is suggested to add a snubber network to the output stage (ref. to the Figure 4)

9.5 Unused channel connection

In case one or more channels are not used, no external components are needed. The relative pins must be connected as:

- OUTM, FBM, OUTP, FBP shorted together
- V_{CC} connected to other V_{CC}, as if the channel is used
- GND connected to other GND, as if the channel is used

Additionally, the unused channel should remain in eco-mode by properly setting the related I^2C bits.

10 Additional features

10.1 Frequency hopping

It is possible to choose the PWM switching frequency by properly setting the I^2C register IB24[1-0].

The PWM frequency also depends on the WS frequency as reported in the table below:

Table 17. PWM switching frequency according to sample frequency

WS frequency [kHz]	Multiplication factor	PWM Mid frequency [MHz]	PWM Standard frequency [MHz]	PWM High frequency [MHz]
44.1	48	2.1168	1.9757	2.2796
48	48	2.304	2.1504	2.4812
96	24	2.304	2.1504	2.4812
192	12	2.304	2.1504	2.4812

The desired frequency hopping setting must be selected in eco-mode state (PWM off) to avoid any audible noise or PLL unlock event.

10.2 Noise gating

Noise gating is an automatic noise reduction feature that activates when output signal reaches not audible levels. When input signal levels fall below -120 dBFs the system activity is automatically optimized in order to limit the output noise level as much as possible and permits the full audio chain to exploit very low noise level on the output speakers. The noise gating process has a 500 ms watching time before turning on, in order to avoid spurious activations.

The feature is enabled by default and can be disabled selecting IB2-d7.

10.3 PWM pulse skipping detector

The pulse skipping detector aim is to detect the PWM stage saturation.

The feature detects pulse skipping when, for each output, at least six consecutive PWM commutations have been skipped. The operation is shown in Figure 59:

Figure 59. PWM pulse skipping detector set

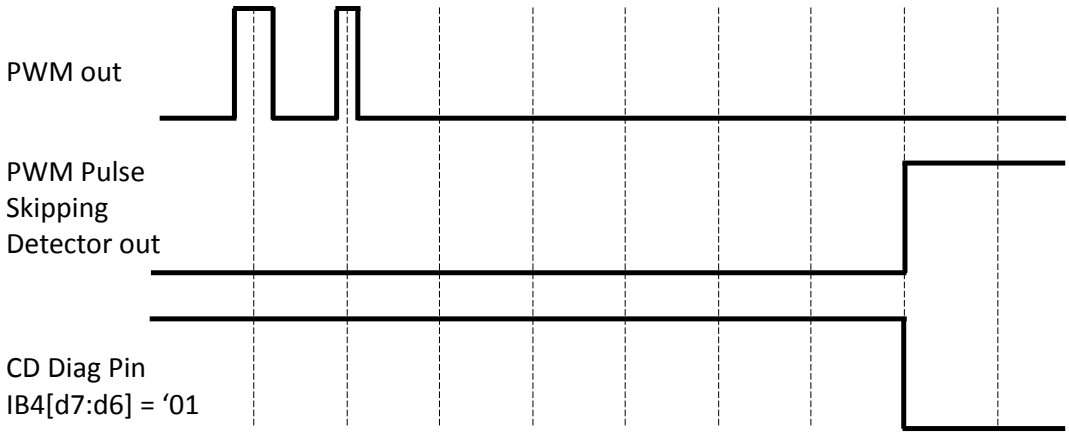
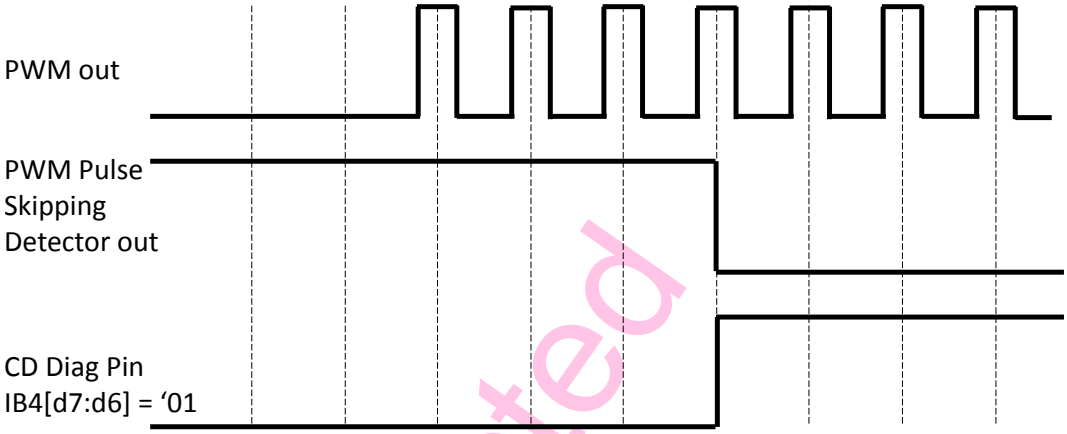


Figure 60. **PWM pulse skipping detector reset**



In order to enable the PWM pulse skipping detector on CD diag pin, the user must set IB4[d7:d6] = ‘01’.

The operation is shown in the Figure 60.

When at least four consecutive PWM commutations are present then PWM pulse skipping detector out is reset. The suggested utilization for this function is to connect a low-pass filter to CDDiag pin, therefore comparing the output with a voltage threshold. The lower is the CDDiag pin average voltage, the higher is the distortion.

10.4 Configurable clipping detector

This block implements an algorithm to detect the presence of the clipping on an output larger than a selectable percentage of distortion on a sinewave signal.

This is obtained by evaluating the time a clipping input is set compared to a voltage signal considered as a sine wave.

You can enable/disable this function and choose thresholds by I^2C bits IB11[2-1] according to this table:

Table 18. **Configurable clipping detector thresholds**

IB11 [D2-D1]	THD threshold
00	Clipping detector disabled
01	CD_1(1)
10	CD_2(1)
11	CD_3(1)

1. *Reference values can be found in Table 4.*

Selecting by I^2C bits IB4-d7/d6 = ”10”, the “configurable clipping detector” information on CD/Diag pin, the pin will go to low logic value, “0”, when the configurable clipping detector threshold selected is reached.

10.5 Watchdog

The function is based on a timer which is reset at each word select line rising edge, and which reaches the timeout in:

- 2.9 ms if fs = 44.1 kHz
- 2.7 ms if fs = 48 kHz, 96 kHz, 192 kHz

When the timer reaches the timeout, the function sends a muting command to the amplifier. In case of timeout, the muting command is released as soon as the timer is reset by a new word select line edge.

The user can disable the watch-dog function setting I2C IB12[0] = ‘1’.

10.6 Error frame check

The device integrates a function called “error frame check”, which is permanently enabled.

The function counts the number of rising edges received on the I²S Clock line, starting from each rising edge of the word select line. At the end of the data frame, marked by the subsequent rising edge on the word select line, the function checks that the reached count is coherent with the I²C configuration of the I²S protocol.

In case the function detects an error, the device sets a flag on DB20[7].

10.7 Input amplitude limiter function

An adjustable input amplitude limiting function has been integrated to protect “small speakers” applications: thanks to this feature, it’s possible to limit by configuration the max power delivered to load. Taking advantage of the digital input architecture, the output power limitation is obtained through the management of the input signal. It’s important to underline that the limitation is implemented independently of the supply voltage value.

The intervention threshold is configurable through I²C IB13[d3-d0] according to Table 19.

Table 19. Output voltage level threshold I²C configuration

I2C IB13[3-0]	Input amplitude limit [Fs]	Voltage output (V) with GV1	Voltage output (V) with GV2	Voltage output (V) with GV3	Voltage output (V) with GV4
0000	Disabled	-	-	-	-
0001	0.15	3.9	2.9	1.6	1.2
0010	0.20	5.2	3.8	2.2	1.6
0011	0.25	6.6	4.8	2.7	2.0
0100	0.30	7.9	5.7	3.3	2.4
0101	0.35	9.3	6.7	3.8	2.8
0110	0.40	10.5	7.6	4.4	3.2
0111	0.45	11.8	8.6	5.0	3.6
1000	0.50	13.1	9.5	5.5	4.1
1001	0.60	15.7	11.4	6.6	4.9
1010	0.70	18.4	13.3	7.7	5.7
1011	0.80	21	15.2	8.8	6.5
1100	not used	-	-	-	-
1101	not used	-	-	-	-
1110	not used	-	-	-	-
1111	not used	-	-	-	-

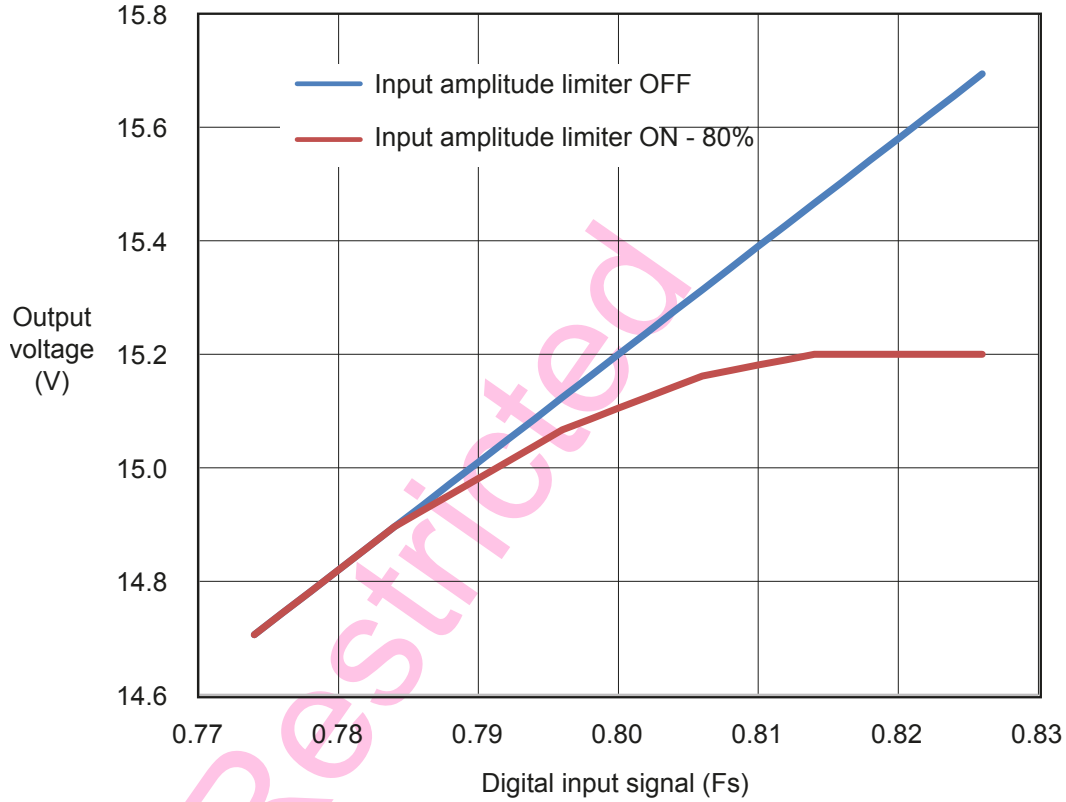
Note: The output voltage depends on the gain, as shown in the latest four columns. These typical values are sightly affected by gain spread (see Table 4) and frequency response.

The output voltage limit is independent from the Supply voltage range.

A gain compression is applied at 1.5 % FS before and 1.5 % FS after the selected amplitude limit in order to reduce the impact on the acoustic performance. When the input signal is further increased, the output amplitude is clipped for full protection of the application.

In Figure 61 there is an example of the response obtained with a limitation corresponding to 1011 setting of the full-scale: the blue line represents the signal when the input amplitude limiter is not enabled, while the red line is the result of the applied attenuation.

Figure 61. **Response obtained with a limitation corresponding to 80% of the full-scale with GV = GV2**



10.7.1 Input amplitude limiter control

The function can be controlled with the I²C bus, by properly setting the bits IB13[3-0]. The configuration of the input amplitude limiter threshold and the enable/disable is available only in MUTE state.

10.8 Legacy mode (backup mode)

HFDA801L provides a backup mode functionality called ‘legacy mode’ in which the device can work without the I²C bus.

To enter in legacy mode the address pin needs to be selected as reported in Section 5.2.1 Address selection.

Once the ENABLE is pulled up properly the device turns on as if it is programmed with the default I²C settings reported in the “default value” column of the I²C table in Section 13.1 Instruction bytes - "I00xxxxx".

In legacy mode the start-up sequence constraint (see Section 5.3.1 Startup sequence) is automatically respected.

10.9 SYNC pin

HFDA801L has the possibility to provide a PWM output frequency replica towards the application thanks to the SYNC pin. This feature is available in TDM mode only, where the I2Sdata2 pin is configured as SYNC pin.

For SYNC pin configuration and usage, the following steps should be followed:

1. Make sure that the device has completed the power management startup phase and TDM mode for the I²S input stream is selected, (see Section 11 I²S bus interface).
2. Select the I2Sdata2 pin in output mode: IB12-d2 = ’1’
3. Select the I2Sdata2 pin as SYNC pin: IB12-d3 = ’1’

SYNC pin provides a clock with the same frequency of the output PWM. The signal is referred to ground with a 1.8 V amplitude. The max output load capacitance for the pin is the same as for other I²Sdata2 configuration as output pin (see Section 11.8 Note about max output load capacitance of I2Sdata2 pin configured as output).

10.10 PWM switching slope control

HFDA801L provides the possibility to regulate the output PWM switching rising and falling slope, The I^2C bit IB19 controls the PWM slope.

11 I²S bus interface

HFDA801L accepts the I²S standard format that can be time division multiplexed.

I²S bus is made up of four lines: the clock line (I2Sclk), the word select line (I2Sws) and two serial data lines (I²Sdata1 and I2Sdata2) where 32 bits words are sent.

The word select line (I2Sws) frequency must be always equal to the audio sampling frequency fS. According to the I²C setting of IB0[3-2], the device supports the following standards for sampling frequency:

- 44.1 kHz;
- 48 kHz;
- 96 kHz;
- 192 kHz.

According to the I²C setting of IB0[7-6], the user can send the audio signal with the following data formats:

- I²S standard (max fs = 192 kHz);
- TDM 4 channels (max fs = 192 kHz);
- TDM 8 channels (max fs = 96 kHz);
- TDM 16 channels (max fs = 48 kHz).

For all mentioned data formats, the user must provide the data word following two complement representations, starting from the MSB. The data word is composed of 32 bits: the device processes only the first 24 most significant bits, while it does not care about the less significant 8 bits.

The internal PLL locks on the clock line signal. When the I²S clock (I2Sclk) is missing or corrupted the PLL consequently unlocks and the device forces the finite state machine in standby state. Furthermore, since the clock line frequency depends on the I²S bus configuration, it is strictly necessary to configure the I²C bits IB0[3-2] and IB0[7-6] accordingly.

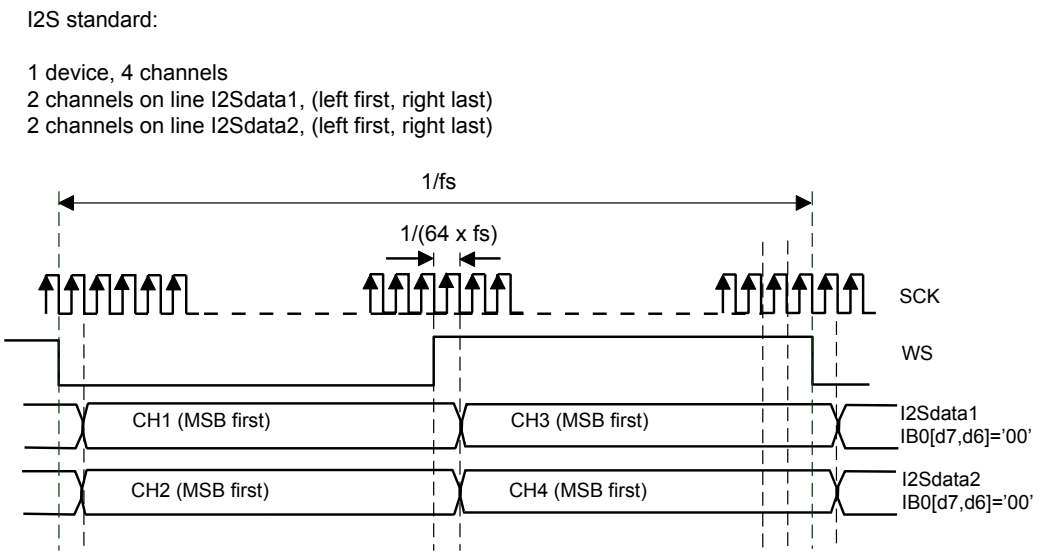
11.1 I²S standard description

With the I²S standard, the data are sent as shown in Figure 62, where the SCK frequency (f_{SCK}) is equal to $64 f_s$.

Data are mapped in slot with the following mapping:

- Data1, I^2S_{WS} = 0 → CH1
- Data1, $I2S_{WS}$ = 1 → CH3
- Data2, $I2S_{WS}$ = 0 → CH2
- Data2, $I2S_{WS}$ = 1 → CH4

Figure 62. I²S standard mode (channels mapping)



11.2 TDM 4 channels

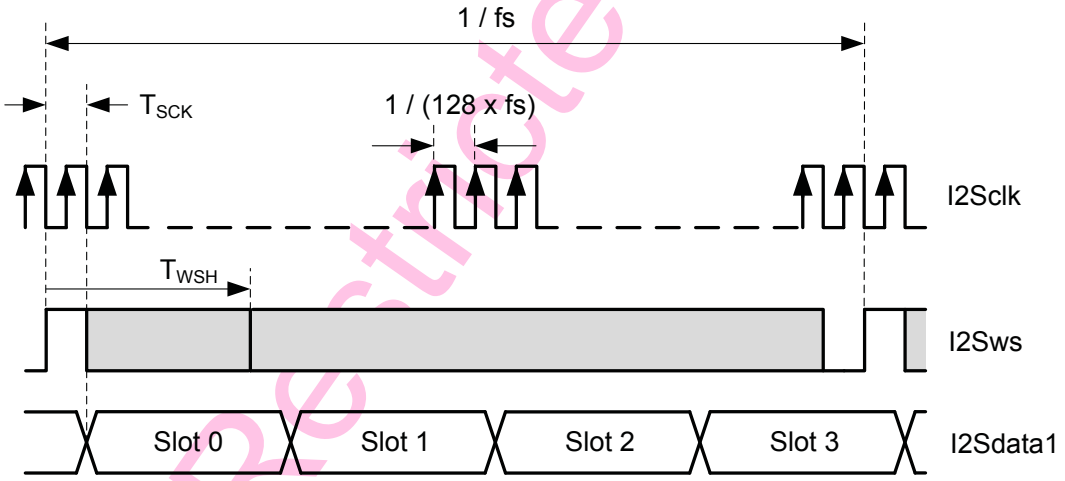
The TDM4 format uses only the $I2S_{data1}$ data line as shown in Figure 63.

The serial clock line frequency is equal to 128 fs.

The channels will be sent in the slot with the following mapping:

- Slot 0 → CH1
- Slot 1 → CH2
- Slot 2 → CH3
- Slot 3 → CH4

Figure 63. TDM4 mode



Note: In TDM-4, TDM-8 channels and TDM 16 channels the $I2S_{data2}$ line is not used. It should be connected to DGND.

11.3 TDM 8 channels

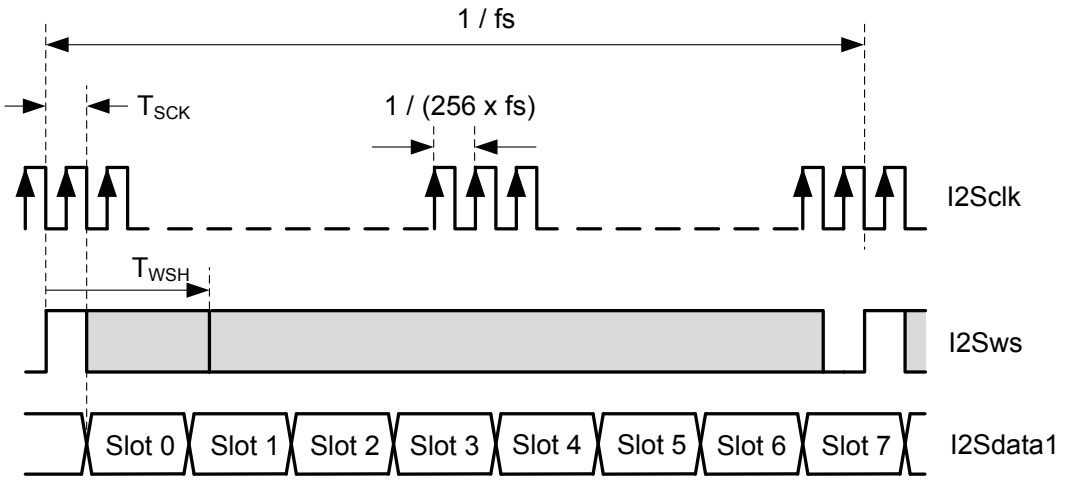
The TDM8 format uses only the $I2S_{data1}$ data line as shown in Figure 64.

The serial clock line frequency is equal to 256 fs.

With a proper I^2C configuration, the user can select the slot containing the data to be processed:

- IB0[5:4] = '00' → Slot0(CH1), Slot1(CH2), Slot2(CH3), Slot3(CH4)
- IB0[5:4] = '01' → Slot4(CH1), Slot5(CH2), Slot6(CH3), Slot7(CH4)

Figure 64. TDM8 mode



Note: In TDM-4, TDM-8 channels and TDM 16 channels the $I2S_{data2}$ line is not used. It should be connected to DGND.

11.4 TDM 16 channels

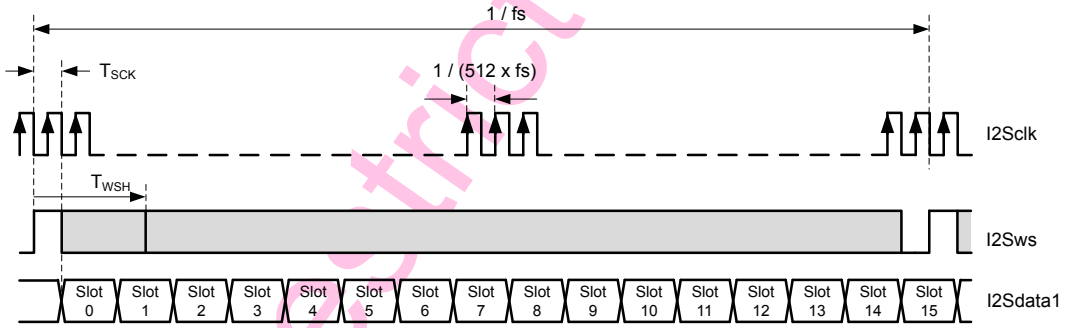
The TDM16 format uses only the $I2S_{data1}$ data line as shown in Figure 65.

The clock line frequency is equal to 512 fs.

With a proper I^2C configuration, the user can select the slot containing the data to be processed:

- IB0[5:4] = '00' → Slot0(CH1), Slot1(CH2), Slot2(CH3), Slot3(CH4)
- IB0[5:4] = '01' → Slot4(CH1), Slot5(CH2), Slot6(CH3), Slot7(CH4)
- IB0[5:4] = '10' → Slot8(CH1), Slot9(CH2), Slot10(CH3), Slot11(CH4)
- IB0[5:4] = '11' → Slot12(CH1), Slot13(CH2), Slot14(CH3), Slot15(CH4)

Figure 65. TDM16 mode



Note: In TDM-4, TDM-8 channels and TDM 16 channels the $I2S_{data2}$ line is not used. It should be connected to DGND.

11.5 Timing requirements

Figure 66. I^2S Interface timings

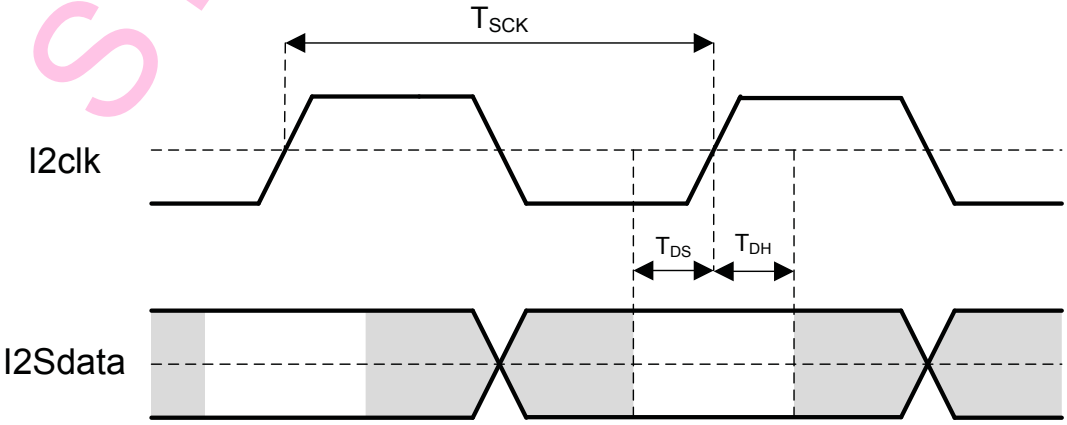


Figure 67. I²S clock transition timings

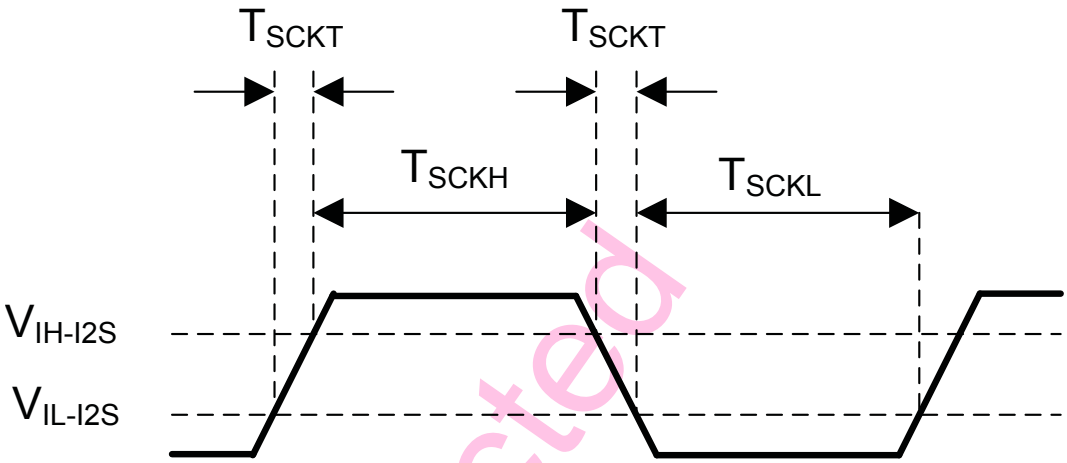


Table 20. I²S interface timings

Symbol	Parameter	Note	Min	Max	Unit
T_{sck}	I²S clock duty cycle	-	40	60	%
	I²S clock period tolerance	-	0.9 x T_{SCK}	1.1 x T_{SCK}	-
	I²S clock period	-	40.69	-	ns
T_{sckh}	I²S clock high time	-	15	-	ns
T_{sckl}	I²S clock low time	-	15	-	ns
T_{sckht}	I²S clock transition time	-	-	6	ns
T_{wsh}	I²S word select high time	I²S standard	1 x T_{SCK}	63 x T_{SCK}	ns
		TDM4 format	1 x T_{SCK}	127 x T_{SCK}	ns
		TDM8 format	1 x T_{SCK}	255 x T_{SCK}	ns
		TDM16 format	1 x T_{SCK}	511 x T_{SCK}	ns
T_{ds}	SD13 SD24 (data inputs) setup time before SCK rising edge	-	8	-	ns
T_{dh}	SD13 SD24 (data inputs) hold time after SCK rising edge	-	8	-	ns

11.6 Group delay

The group delay depends on the sampling frequency f_s, properly configured with the I²C bits IB0[3-2]. The typical value for all the configurations is reported in Table 21:

Table 21. Group delay dependency on input sampling frequency

Input sampling frequency fs	Group delay
44.1 kHz	505 µs
48 kHz	475 µs
96 kHz	190 µs
192 kHz	88 µs

11.7 I²S and system clock relationship

HFDA801L provides both I²C and I²S communication through two different digital interfaces.
In HFDA801L the digital part has different clock domains:

- The I²C programming block clock is the I²C clock.
- The I²S receiver clock which is the I²S clock.
- The system clock is generated by an internal PLL and derived from the I²S clock (see Table 22).

Table 22. System clock and I²S frequency relationship

		F sampling [kHz] (IB0(d3-d2))			
		44.1	48	96	192
PLL internal digital clock frequency [MHz]		59.27	64.51	64.51	64.51
I²S clock frequency[MHz] (IB0(d7-d6))	I²S standard	2.822	3.072	6.144	12.288
	TDM4	5.645	6.144	12.288	24.576
	TDM8	11.290	12.288	24.576	N.A.
	TDM16	22.579	24.576	N.A.	N.A.

The I²C commands are not effective if the I²S clock is not present. However, they will remain memorized inside the I²C registers. If the I²S clock is lost the digital machine goes in standby.

11.8 Note about max output load capacitance of I2Sdata2 pin configured as output

Once the I2Sdata2 pin is configured as output pin the max output load capacitance is 30 pF.

12 I²C bus interface

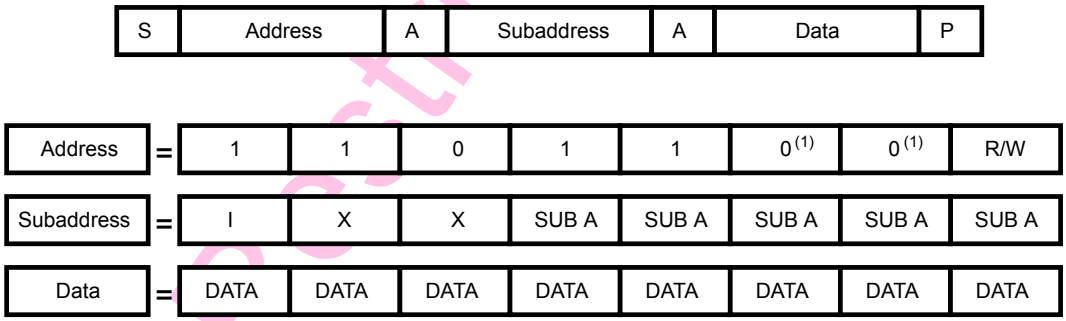
Data transmission from microprocessor to the HFDA801L and vice versa takes place through the 2 wires I²C bus interface, consisting of the two lines SDA and SCL (pull-up resistors to positive supply voltage must be connected).

When the I²C bus is active any operating mode of the IC may be modified, the diagnostic may be controlled and the results read back.

The protocol used for the bus is depicted in Figure 68 and comprises:

- A start condition (S)
- A chip address byte (the LSB bit determines read/write transmission)
- A sub address byte
- A sequence of data (N-bytes + acknowledge)
- A stop condition (P)

Figure 68. I²C bus protocol description



(1) The I²C addresses are:

- Address 0 = 1101100
- Address 1 = 1101101
- Address 2 = 1101110
- Address 3 = 1101111

Description:

- S = Start
- R/W = '0' → Receive-mode (chip could be programmed by µP)
- I = Auto increment; when 1, the address is automatically incremented for each byte transferred
- X = Not used
- A = Acknowledge
- P = Stop
- MAX CLOCK SPEED 400 kbit/sec

12.1 Writing procedure

There are two possible procedures:

- Without increment: the I bit is set to 0 and the register is addressed by the subaddress. Only this register is written by the data following the subaddress byte.
- With increment: the I bit is set to 1 and the first register write is the only one addressed by subaddress. The registers are written from this address up to stop bit or the reaching of the last register.

12.2 Reading procedure

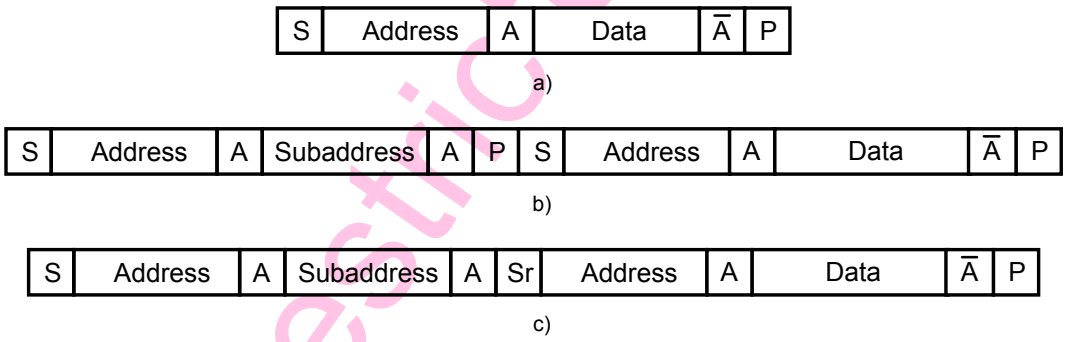
The reading procedure is made up only by the device address (sent by controller) and the data (sent by target) as reported in Figure 69 (a). In particular when a reading procedure is performed the first register read is the last addressed in a previous access to the I²C peripheral.

Hence, to read a particular register also a sort of write action (a write interrupted after the sub-address is sent) is needed to specify which register has to be read. Figure 69 (b) shows the complete procedure to read a specific register where:

- The controller performs a write action by sending just the device address and the subaddress; the transmission must be interrupted with the stop condition when the subaddress is sent.
- Now, the read procedure can be performed: the controller starts a new communication and sends the device address; then the target (HFDA) will respond by sending the data bits.
- The read communication is ended by the controller which sends a stop condition preceded by a not-acknowledge.

Instead, performing a start immediately after the stop condition could be possible to generate the repeated start condition (Sr) which also keeps busy the I²C bus until the stop is reached (Figure 69).

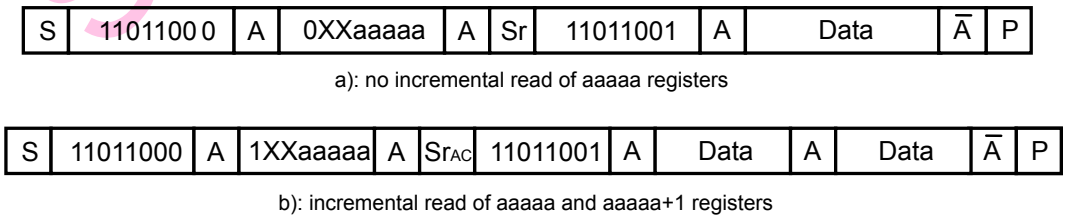
Figure 69. Reading procedure



There are two possible reading procedures:

1. Without auto-increment (Figure 70 (a)) if the “I” bit of the last I²C writing procedure has been set to 0: in this case only the register addressed by the sub-address sent in the previous writing procedure is read;
2. With auto-increment (Figure 70 (b)) if the “I” bit of the last I²C write procedure has been set to 1: in this case the first register read is the one addressed by the sub-address sent in the previous writing procedure. Only the registers from this address till the stop bit are read.

Figure 70. Without/with auto-increment reading procedure



If a microcontroller tries to read an undefined register, the FDA will return a “0xFF” data; for more details refer directly to the I²C specification.

12.3 Data validity

The data on the SDA line must be stable during the high period of the clock. The HIGH and LOW state of the data line can only change when the clock signal on the SCL line is LOW.

12.4 Start and stop conditions

The start condition is a HIGH to LOW transition of the SDA line while SCL is HIGH.

The stop condition is a LOW to HIGH transition of the SDA line while SCL is HIGH.

12.5 Byte format

Every byte transferred to the SDA line must contain 8 bits. Each byte must be followed by an acknowledge bit. The MSB is transferred first.

12.6 Acknowledge

The transmitter* puts a resistive HIGH level on the SDA line during the acknowledge clock pulse. The receiver** has to pull-down (LOW) the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during this clock pulse.

* Transmitter:

- Controller (µP) when it writes an address to the HFDA801L.
- Target (HFDA801L) when the µP reads a data byte from HFDA801L.

** Receiver:

- Target (HFDA801L) when the µP writes an address to the HFDA801L.
- Controller (µP) when it reads a data byte from HFDA801L.

12.7 I²C timing

This paragraph describes more in detail the I²C bus protocol used and its timings. Please refer to Table 23 and Figure 71 below.

Figure 71. I²C bus interface timing

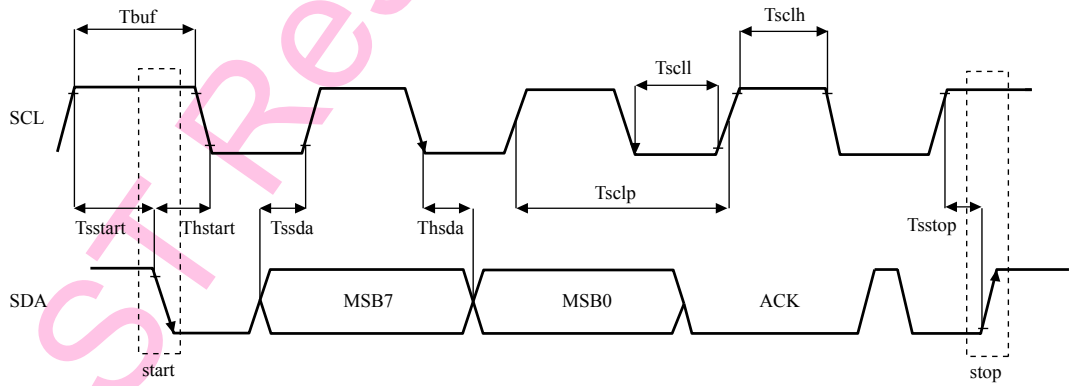


Table 23. I²C bus interface timing

Symbol	Parameter	Min	Max	Unit
F_{scl}	SCL (clock line) frequency	-	400	kHz
T_{scl}	SCL period	2500	-	ns
T_{sclh}	SCL high time	0.6	-	µs
T_{scll}	SCL low time	1.3	-	µs
T_{sstart}	Setup time for start condition	0.6	-	µs
T_{hstart}	Hold time for start condition	0.6	-	µs
T_{sstop}	Setup time for stop condition	0.6	-	µs
T_{buf}	Bus free time between a stop and a start condition	1.3	-	µs
T_{ssda}	Setup time for data line	100	-	ns
T_{hsda}	Hold time for data line	0(1)	-	ns
T_f	Fall time for SCL and SDA	-	300(2)	ns
T_r	Rise time for SCL and SDA	-	300(2)	ns

1. *The device must internally provide a hold time of at least 300 ns for the SDA signal to bridge the undefined region of the falling edge of SCL.*
2. *The value is referred from 30 % to 70 % of the I^2C bus pins voltage.*

12.8 Main I^2C functions

Several functions can be enabled/disabled through an I^2C serial communication bus. The main I^2C options are:

- Amplifier gain selection (high/low gain)
- Power stage ON/OFF control channel by channel
- Parallel outputs configuration (for 2 channel applications, 2.1 applications)
- Slow/fast play-mute transition
- High pass filtering for the digital input signal
- Woofer and tweeter misconnections test settings
- I^2S/TDM 4/8/16 channels
- 44.1 kHz, 48 kHz, 96 kHz, 192 kHz word frame clock selection
- Thermal warning selection
- Mute/unmute function
- Under voltage warning events

Any detected fault condition will be reported by means of the I^2C, included short events to V_{CC}, GND and mixed misconnections, over voltage, over-temperature, output offset warning.

13 I²C registers

13.1 Instruction bytes - "I00xxxxx"

Table 24. IB0-ADDR: "I0000000"

Data bit	Default value	Definition
D7-D6	00	Digital input settings: 00: I²S standard 01: TDM – 4 CHs 10: TDM – 8 CHs 11: TDM –16 CHs
D5-D4	00	Channel slotting: 00: 1-2-3-4 (TDM8 and TDM16) 01: 5-6-7-8 (TDM8 and TDM16) 10: 9-10-11-12 (only for TDM16) 11: 13-14-15-16 (only for TDM16)
D3-D2	00	Digital input frame sync frequency (Fs): 00: 44.1 kHz 01: 48 kHz 10: 96 kHz 11: 192 kHz
D1-D0	00	I²C register writing enable (for IB# > IB0): 00: I²C writing disable 01: I²C writing disable 10: I²C writing enable 11: I²C writing disable

Table 25. IB1-ADDR: "I0000001"

Data bit	Default value	Definition
D7	0	0 - CH1 and CH2 normal operation 1 - CH1 and CH2 parallel operation
D6	0	0 - CH3 and CH4 normal operation 1 - CH3 and CH4 parallel operation
D5-D4	00	Reserved
D3	0	0 - No highpass in the DAC 1 - Highpass in the DAC
D2	0	0 - Input offset detector disable 1 - Input offset detector enable
D1	0	0 - Output offset detector disable 1 - Output offset detector enable
D0	0	Reserved

Table 26. IB2-ADDR: "I0000010"

Data bit	Default value	Definition
D7	0	Reserved
D6	0	0 – PWM in phase 1 – PWM out of phase
D5-D0	000000	Reserved

Table 27. IB3-ADDR: "I0000011"

Data bit	Default value	Definition
D7	0	Reserved
D6	0	0 – Thermal warning on CD/DIAG pin 1 – No thermal warning on CD/DIAG pin
D5-D4	00	Temperature warning information on CD/DIAG pin(1) 00: TW1 01: TW2 10: TW3 11: TW4
D3	0	0 – No overcurrent information on CD/DIAG pin 1 – Overcurrent information on CD/DIAG pin
D2	0	0 – No input offset information on CD/DIAG pin 1 – Input offset information on CD/DIAG pin
D1	0	0 – No output offset information on CD/DIAG pin 1 – Output offset information on CD/DIAG pin
D0	0	Reserved

1. *Thermal warning on CD/DIAG pin depending on IB3[D6] setting*

Table 28. IB4-ADDR: "I0000100"

Data bit	Default value	Definition
D7-D6	00	Clipping information on CDDiag pin: 00: No clipping information 01: PWM pulse skipping detector 10: Configurable clipping detector 11: Not used
D5	0	0 - Fast TurnON boost disabled 1 - Fast TurnON boost enabled
D4-D0	00001	Reserved

Table 29. **IB5-ADDR: "I0000101**

Data bit	Default value	Definition
D7-D6	00	Mute timing setup, (values with fsample = 44.1KHz): 00: Very fast 3 ms 01: Fast 45 ms 10: Slow 90 ms 11: Very slow 185 ms
D5-D0	000000	Reserved

Table 30. **IB6-ADDR: "I0000110"**

Data bit	Default value	Definition
D7-D6	00	Diagnostic ramp time selection: 00: Timing normal 01: Timing x2 10: Timing x4 11: Timing /2
D5-D4	00	Diagnostic hold time selection: 00: Timing normal 01: Timing x2 10: Timing x4 11: Timing /2
D3-D2	00	“DiagShort2Supply” and "output offset detection" timing selection 00: 90 ms 01: 70 ms 10: 45 ms 11: 20 ms
D1- D0	00	Digital gain selection: 00: Normal 01: +6 dB 10: +12 dB 11: +18 dB

Table 31. **IB7-ADDR: "I0000111"**

Data bit	Default value	Definition
D7-D0	00000000	Reserved

Table 32. **IB8-ADDR: "I0001000"**

Data bit	Default value	Definition
D7-D0	00000000	Reserved

Table 33. **IB9-ADDR: "I0001001"**

Data bit	Default value	Definition
D7-D0	00000000	Reserved

Table 34. IB10-ADDR: "I0001010"

Data bit	Default value	Definition
D7-D0	0000000	Reserved

Table 35. IB11-ADDR: "I0001011"

Data bit	Default value	Definition
D7	0	Short load impedance threshold (DC Diagnostic): 0 - Ldcsl1 1 - Ldcsl2
D6	0	Open load impedance threshold (DC Diagnostic & Open load in play detector): 0 - Ldol1 1 - Ldol2
D5-D3	010	Reserved
D2-D1	00	Configurable clipping detector configuration: 00: Clipping detector disabled 01: CD_1 10: CD_2 11: CD_3
D0	0	Reserved

Table 36. IB12-ADDR: "I0001100"

Data bit	Default value	Definition
D7	0	0: Digital mute enabled in PLAY 1: Digital mute disabled in PLAY
D6	0	0: OCP protection to standard levels 1: OCP protection set at + 1 A (Do not use if IB12-d5,d4 = ”00”)
D5-D4	00	Over current protection level selection (for values please refer to Section 3.3 Electrical characteristics): 00: OCP_0 01: OCP_1 10: OCP_2 11: OCP_3
D3	0	0 - I2Sdata2 pin standard 1 - PWM clock on I2Sdata2 pin (only if IB0-d7,d6 <> ”00”)
D2-D1	00	Reserved
D0	0	0 - watchdog of I^2S WS signal enabled: device in Mute if I^2Sws is missing 1 - watchdog of I^2S WS signal disabled

Table 37. IB13-ADDR: "I0001101"

Data bit	Default value	Definition
D7	0	Open load in play on CH1: 0 - Disable

Data bit	Default value	Definition
		1 - Enable
D6	0	Open load in play on CH2: 0 - Disable 1 - Enable
D5	0	Open load in play on CH3: 0 - Disable 1 - Enable
D4	0	Open load in play on CH4: 0 - Disable 1 - Enable
D3-D0	0000	Power limiting function configuration: 0000: Power limiter disabled 0001: Power limited with maximum voltage scale at 15% 0010: Power limited with maximum voltage scale at 20% 0011: Power limited with maximum voltage scale at 25% 0100: Power limited with maximum voltage scale at 30% 0101: Power limited with maximum voltage scale at 35% 0110: Power limited with maximum voltage scale at 40% 0111: Power limited with maximum voltage scale at 45% 1000: Power limited with maximum voltage scale at 50% 1001: Power limited with maximum voltage scale at 60% 1010: Power limited with maximum voltage scale at 70% 1011: Power limited with maximum voltage scale at 80% 1100: Not used 1101: Not used 1110: Not used 1111: Not used

Table 38. IB14-ADDR: "I0001110"

Data bit	Default value	Definition
D7	0	Reserved
D6-D5	00	CH1 gain selection: 00: GV1 01: GV2 10: GV3 11; GV4
D4	0	0 - CH1 in eco-mode (PWM OFF) 1 - CH1 with PWM ON
D3	0	Reserved
D2	0	0 - CH1 DC diag disable 1 - CH1 DC diag start
D1	0	0 - CH1 AC diag disable 1 - CH1 AC diag start (both internal and external)
D0	0	0 - CH1 in MUTE

Data bit	Default value	Definition
		1 - CH1 in PLAY

Table 39. IB15- ADDR: "I0001111"

Data bit	Default value	Definition
D7	0	Reserved
D6-D5	00	CH2 gain selection: 00: GV1 01: GV2 10: GV3 11: GV4
D4	0	0 - CH2 in eco-mode (PWM OFF) 1 - CH2 with PWM ON
D3	0	Reserved
D2	0	0 - CH2 DC diag disable 1 - CH2 DC diag start
D1	0	0 - CH2 AC diag disable 1 - CH2 AC diag start
D0	0	0 - CH2 in MUTE 1 - CH2 in PLAY

Table 40. IB16-ADDR: "I0010000"

Data bit	Default value	Definition
D7	0	Reserved
D6-D5	00	CH3 gain selection: 00: GV1 01: GV2 10: GV3 11: GV4
D4	0	0 - CH3 in eco-mode (PWM OFF) 1 - CH3 with PWM ON
D3	0	Reserved
D2	0	0 - CH3 DC diag disable 1 - CH3 DC diag start
D1	0	0 - CH3 AC diag disable 1 - CH3 AC diag start
D0	0	0 - CH3 in MUTE 1 - CH3 in PLAY

Table 41. IB17-ADDR: "I0010001"

Data bit	Default value	Definition
D7	0	Reserved
D6-D5	00	CH4 gain selection:

Data bit	Default value	Definition
		00: GV1 01: GV2 10: GV3 11: GV4
D4	0	0 - CH4 in eco-mode (PWM OFF) 1 - CH4 with PWM ON
D3	0	Reserved
D2	0	0 - CH4 DC diag disable 1 - CH4 DC diag start
D1	0	0 - CH4 AC diag disable 1 - CH4 AC diag start
D0	0	0 - CH4 in MUTE 1 - CH4 in PLAY

Table 42. IB18-ADDR: "I0010010"

Data bit	Default value	Definition
D7-D0	00000001	Reserved

Table 43. IB19-ADDR: "I0010011"

Data bit	Default value	Definition
D7-D3	10011	Reserved
D2	0	0 - Slow slope 1 - Fast slope
D1-D0	00	Reserved

Table 44. IB20-ADDR: "I0010100"

Data bit	Default value	Definition
D7-D0	00000000	Reserved

Table 45. IB21-ADDR: "I0010101"

Data bit	Default value	Definition
D7-D0	00000000	Reserved

Table 46. IB22-ADDR: "I0010110"

Data bit	Default value	Definition
D7-D0	00000000	Reserved

Table 47. IB23-ADDR: "I0010111"

Data bit	Default value	Definition
D7-D1	0000100	Reserved
D0	0	0 - FIRST setup not programmed via I^2C

Data bit	Default value	Definition
		1 - FIRST setup programmed – ready to work

Table 48. **IB24-ADDR: "I0011000"**

Data bit	Default value	Definition
D7-D2	00000000	Reserved
D1-D0	00	00: PWM mid frequency 01: PWM standard frequency 10: PWM high frequency 11: Reserved

13.2 Data bytes - "I01xxxxx"

Legend:

- Type “S/C”: the hardware can only set the flag. An I^2C reading operation clears the flag;
- Type “SR/C”: the hardware can either set or reset the flag. An I^2C reading operation clears the flag;
- Type “SR”: the hardware can either set or reset the flag. An I^2C reading operation doesn’t affect the flag.

Table 49. DB0-ADDR:"I0100000"

Data bit	Type	Definition
D7	S/C	Input offset detector: 0 - No offset present at input 1 - Offset at input present
D6	S/C	0 - Thermal protection CH4 not detected 1 - Thermal protection CH4 detected
D5	S/C	0 - Thermal protection CH3 not detected 1 - Thermal protection CH3 detected
D4	S/C	0 - Thermal protection CH2 not detected 1 - Thermal protection CH2 detected
D3	S/C	0 - Thermal protection CH1 not detected 1 - Thermal protection CH1 detected
D2	S/C	0 - No dump pulses detected 1 - Dump detected
D1	S/C	0 - UVLO VCC not detected 1 - UVLO VCC detected *Note: after turn-on, the first reading of this flag will be always 0*
D0	SR/C	PLL lock: 0 - PLL not locked 1 - PLL locked

Table 50. DB1-ADDR:"I0100001"

Data bit	Type	Definition
D7	SR/C	0 – Thermal warning 1 not active 1 – Thermal warning 1 active
D6	SR/C	0 – Thermal warning 2 not active 1 – Thermal warning 2 active
D5	SR/C	0 – Thermal warning 3 not active 1 – Thermal warning 3 active
D4	SR/C	0 – Thermal warning 4 not active 1 – Thermal warning 4 active
D3	S/C	0 – Clipping not detected on channel 1 1 – Clipping detected on channel 1
D2	S/C	0 – Clipping not detected on channel 2 1 – Clipping detected on channel 2
D1	S/C	0 – Clipping not detected on channel 3 1 – Clipping detected on channel 3

Data bit	Type	Definition
D0	S/C	0 – Clipping not detected on channel 4 1 – Clipping detected on channel 4

Table 51. DB2-ADDR:"I0100010"

Data bit	Type	Definition
D7	SR/C	0 – CH1 normal operation 1 – CH1 DC diagnostic pulse ended
D6	SR/C	0 – CH1 DC diagnostic data not valid or diag not activated 1 – CH1 DC diagnostic data valid
D5	S/C	0 – CH1 No overcurrent, no thermal protection 1 – CH1 Overcurrent or local thermal protection triggered
D4	SR/C	0 – Normal load on CH1 1 – Short load on CH1
D3	SR	0 – No short to V_{CC} on CH1 1 – Short to V_{CC} on CH1
D2	SR	0 – No short to GND on CH1 1 – Short to GND on CH1
D1	SR/C	0 – Normal load on CH1 1 – Open load on CH1
D0	SR/C	0 – CH1 in mute 1 – CH1 in play

Table 52. DB3-ADDR:"I0100011"

Data bit	Type	Definition
D7	SR/C	0 – CH2 normal operation 1 – CH2 DC diagnostic pulse ended
D6	SR/C	0 – CH2 DC diagnostic data not valid or diag not activated 1 – CH2 DC diagnostic data valid
D5	S/C	0 – CH2 No overcurrent, no thermal protection 1 – CH2 Overcurrent or local thermal protection triggered
D4	SR/C	0 – Normal load on CH2 1 – Short load on CH2
D3	SR	0 – No short to V_{CC} on CH2 1 – Short to V_{CC} on CH2
D2	SR	0 – No short to GND on CH2 1 – Short to GND on CH2
D1	SR/C	0 – Normal load on CH2 1 – Open load on CH2
D0	SR/C	0 – CH2 in mute 1 – CH2 in play

Table 53. DB4-ADDR:"I0100100"

Data bit	Type	Definition
D7	SR/C	0 – CH3 normal operation 1 – CH3 DC diagnostic pulse ended
D6	SR/C	0 – CH3 DC diagnostic data not valid or diag not activated 1 – CH3 DC diagnostic data valid
D5	S/C	0 – CH3 No overcurrent, no thermal protection 1 – CH3 Overcurrent or local thermal protection triggered
D4	SR/C	0 – Normal load on CH3 1 – Short load on CH3
D3	SR	0 – No short to V_{CC} on CH3 1 – Short to V_{CC} on CH3
D2	SR	0 – No short to GND on CH3 1 – Short to GND on CH3
D1	SR/C	0 – Normal load on CH3 1 – Open load on CH3
D0	SR/C	0 – CH3 in mute 1 – CH3 in play

Table 54. DB5-ADDR:"I0100101"

Data bit	Type	Definition
D7	SR/C	0 – CH4 normal operation 1 – CH4 DC diagnostic pulse ended
D6	SR/C	0 – CH4 DC diagnostic data not valid or diag not activated 1 – CH4 DC diagnostic data valid
D5	S/C	0 – CH4 No overcurrent, no thermal protection 1 – CH4 Overcurrent or local thermal protection triggered
D4	SR/C	0 – Normal load on CH4 1 – Short load on CH4
D3	SR	0 – No short to V_{CC} on CH4 1 – Short to V_{CC} on CH4
D2	SR	0 – No short to GND on CH4 1 – Short to GND on CH4
D1	SR/C	0 – Normal load on CH4 1 – Open load on CH4
D0	SR/C	0 – CH4 in mute 1 – CH4 in play

Table 55. DB6-ADDR:"I0100110"

Data bit	Type	Definition
D7	SR/C	0 – CH1 normal operation 1 – CH1 AC diagnostic pulse ended
D6	SR/C	0 – CH1 AC diagnostic data not valid (error code available on DB10) or diag not executed

Data bit	Type	Definition
		1 – CH1 AC diagnostic data valid
D5	SR/C	0 – Tweeter present on CH1 1 – No tweeter present on CH1
D4	SR/C	When D6 = 1: 0 – CH1 no error-warning code 1 – CH1 error-warning code reported in DB10
D3	SR/C	0 – CH2 normal operation 1 – CH2 AC diagnostic pulse ended
D2	SR/C	0 – CH2 AC diagnostic data not valid (error code available on DB13) or diag not executed 1 – CH2 AC diagnostic data valid
D1	SR/C	0 – Tweeter present on CH2 1 – No tweeter present on CH2
D0	SR/C	When D2 = 1: 0 – CH2 no error-warning code 1 – CH2 error-warning code reported in DB13

Table 56. DB7-ADDR:"I0100111"

Data bit	Type	Definition
D7	SR/C	0 – CH3 normal operation 1 – CH3 AC diagnostic pulse ended
D6	SR/C	0 – CH3 AC diagnostic data not valid (error code available on DB16) or diag not executed 1 – CH1 AC diagnostic data valid
D5	SR/C	0 – Tweeter present on CH3 1 – No tweeter present on CH3
D4	SR/C	When D6 = 1: 0 – CH3 no error-warning code 1 – CH3 error-warning code reported in DB16
D3	SR/C	0 – CH4 normal operation 1 – CH4 AC diagnostic pulse ended
D2	SR/C	0 – CH4 AC diagnostic data not valid (error code available on DB19) or diag not executed 1 – CH4 AC diagnostic data valid
D1	SR/C	0 – Tweeter present on CH4 1 – No tweeter present on CH4
D0	SR/C	When D2 = 1: 0 – CH4 no error-warning code 1 – CH4 error-warning code reported in DB19

Table 57. DB8-ADDR:"I0101000"

Data bit	Type	Definition
D7-D0	SR/C	When DB2[6] = '0': CH1 DC diagnostic error code When DB2[6] = '1': CH1 output load resistance

Table 58. **DB9-ADDR:"I0101001"**

Data bit	Type	Definition
D7-D0	SR/C	CH1 diagnostic AC output load magnitude

Table 59. **DB10-ADDR:"I0101010"**

Data bit	Type	Definition
D7-D0	SR/C	CH1 AC diagnostic error code or AC output load phase (when AC diag with external signal)

Table 60. **DB11-ADDR:"I0101011"**

Data bit	Type	Definition
D7-D0	SR/C	When DB3[6] = '0': CH2 DC diagnostic error code When DB3[6] = '1': CH2 output load resistance

Table 61. **DB12-ADDR:"I0101100"**

Data bit	Type	Definition
D7-D0	SR/C	CH2 diagnostic AC output load magnitude

Table 62. **DB13-ADDR:"I0101101"**

Data bit	Type	Definition
D7-D0	SR/C	CH2 AC diagnostic error code or AC output load phase (when AC diag with external signal)

Table 63. **DB14-ADDR:"I0101110"**

Data bit	Type	Definition
D7-D0	SR/C	When DB4[6] = '0': CH3 DC diagnostic error code When DB4[6] = '1': CH3 output load resistance

Table 64. **DB15-ADDR:"I0101111"**

Data bit	Type	Definition
D7-D0	SR/C	CH3 diagnostic AC output load magnitude;

Table 65. **DB16-ADDR:"I0110000"**

Data bit	Type	Definition
D7-D0	SR/C	CH3 AC diagnostic error code or AC output load phase (when AC diag with external signal)

Table 66. **DB17-ADDR:"I0110001"**

Data bit	Type	Definition
D7-D0	SR/C	When DB5[6] = '0': CH4 DC diagnostic error code When DB5[6] = '1': CH4 output load resistance

Table 67. **DB18-ADDR:"I0110010"**

Data bit	Type	Definition
D7-D0	SR/C	CH4 diagnostic AC output load magnitude

Table 68. **DB19-ADDR:"I0110011"**

Data bit	Type	Definition
D7-D0	SR/C	CH4 AC diagnostic error code or AC output load phase (when AC diag with external signal)

Table 69. **DB20-ADDR:"I0110100"**

Data bit	Type	Definition
D7	S/C	0 – No error frame checked 1 – Error frame checked
D6	SR/C	Reserved
D5	S/C	0 – CH1 output voltage offset not present 1 – CH1 output voltage offset present
D4-D3	SR/C	Reserved
D2	SR/C	0 – CH1 open load test not ended 1 – CH1 open load test ended
D1	SR/C	0 – CH1 open load test input signal not valid 1 – CH1 open load test input signal valid
D0	SR/C	0 – CH1 open load not detected 1 – CH1 open load detected

Table 70. **DB21-ADDR:"I0110101"**

Data bit	Type	Definition
D7	SR/C	0 – DIM disabled 1 – DIM enabled
D6	SR/C	Reserved
D5	S/C	0 – CH2 output voltage offset not present 1 – CH2 output voltage offset present
D4-D3	SR/C	Reserved
D2	SR/C	0 – CH2 open load test not ended 1 – CH2 open load test ended
D1	SR/C	0 – CH2 open load test input signal not valid 1 – CH2 open load test input signal valid
D0	SR/C	0 – CH2 open load not detected 1 – CH2 open load detected

Table 71. **DB22-ADDR:"I0110110"**

Data bit	Type	Definition
D7-D6	SR/C	Reserved
D5	S/C	0 – CH3 output voltage offset not present

Data bit	Type	Definition
		1 – CH3 output voltage offset present
D4-D3	SR/C	Reserved
D2	SR/C	0 – CH3 open load test not ended 1 – CH3 open load test ended
D1	SR/C	0 – CH3 open load test input signal not valid 1 – CH3 open load test input signal valid
D0	SR/C	0 – CH3 open load not detected 1 – CH3 open load detected

Table 72. DB23-ADDR:"I0110111"

Data bit	Type	Definition
D7-D6	SR/C	Reserved
D5	S/C	0 – CH4 output voltage offset not present 1 – CH4 output voltage offset present
D4-D3	SR/C	Reserved
D2	SR/C	0 – CH4 open load test not ended 1 – CH4 open load test ended
D1	SR/C	0 – CH4 open load test input signal not valid 1 – CH4 open load test input signal valid
D0	SR/C	0 – CH4 open load not detected 1 – CH4 open load detected

Table 73. DB24-ADDR:"I0111000"

Data bit	Type	Definition
D7-D0	SR/C	Reserved

Table 74. DB25-ADDR:"I0111001"

Data bit	Type	Definition
D7-D0	SR/C	Reserved

Table 75. DB26-ADDR:"I0111010"

Data bit	Type	Definition
D7-D0	SR/C	Reserved

Table 76. DB27-ADDR:"I0111011"

Data bit	Type	Definition
D7-D0	SR/C	Reserved

Table 77. DB28-ADDR:"I0111100"

Data bit	Type	Definition
D7-D2	S/C	Reserved

Data bit	Type	Definition
D1-D0	SR/C	Device temperature output (9-8)

Table 78. **DB29-ADDR:"I0111101"**

Data bit	Type	Definition
D7-D0	SR/C	Device temperature output (7-0)

14 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

14.1 LQFP64 (10x10x1.4 mm exp. pad up) package information

Figure 72. **LQFP64 (10x10x1.4 mm exp. pad up) package outline**

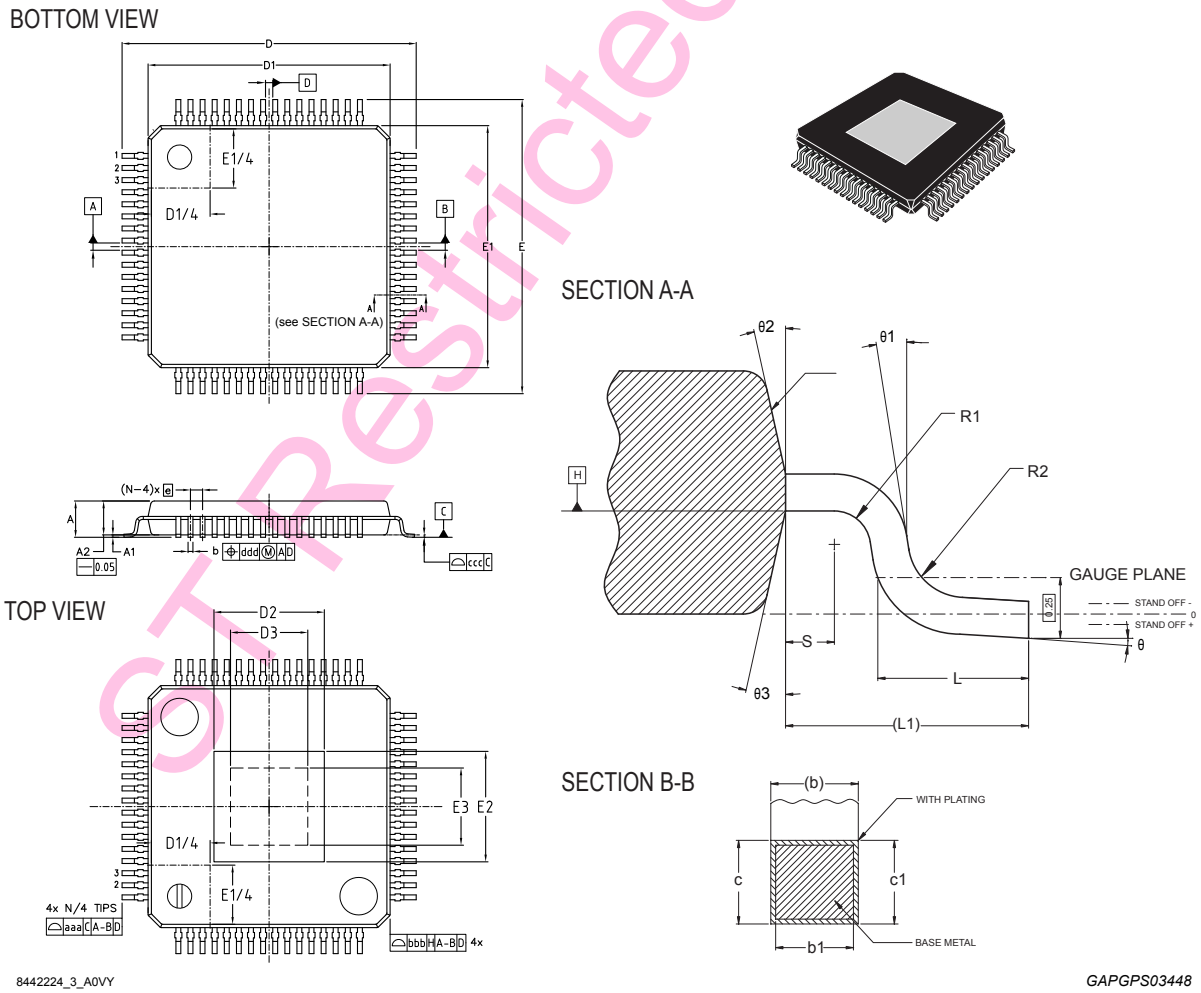


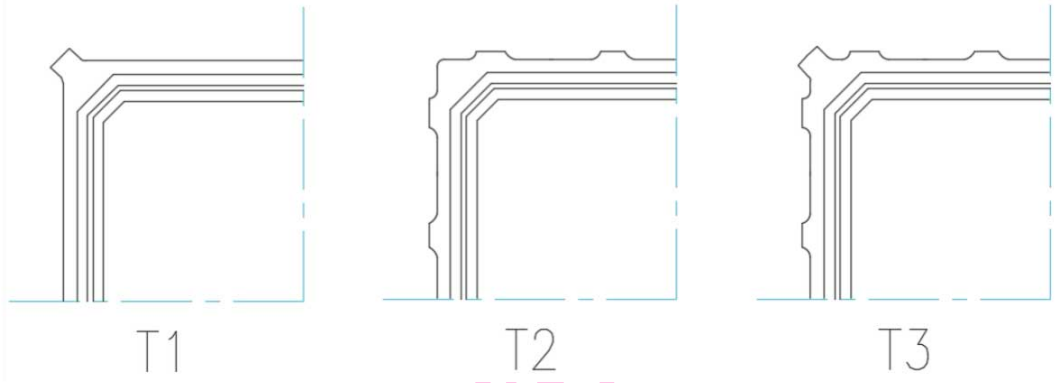
Table 79. **LQFP64 (10x10x1.4 mm exp. pad up) package mechanical data**

Symbol	Dimension in mm		
	Min.	Typ.	Max.
Θ	0°	3.5°	6°
Θ1	0°	9°	12°
Θ2	11°	12°	13°
Θ3	11°	12°	13°
A	-	-	1.49
A1	-0.04	-	0.04

Symbol	Dimension in mm		
	Min.	Typ.	Max.
A2	1.35	1.4	1.45
b	-	-	0.27
b1	0.17	0.2	0.23
c	0.09	-	0.2
c1	0.09	0.127	0.16
D		12.00 BSC	
D1(1)(2)		10.00 BSC	
D2		**See VARIATIONS**	
D3		**See VARIATIONS**	
e		0.50 BSC	
E		12.00 BSC	
E1(1)(2)		10.00 BSC	
E2		**See VARIATIONS**	
E3		**See VARIATIONS**	
L	0.45	0.6	0.75
L1	1.00 REF		
N	-	64	-
R1	0.08	-	-
R2	0.08	-	0.2
S	0.2	-	-
Tolerance of form and position			
aaa	-	0.2	-
bbb	-	0.2	-
ccc	-	0.08	-
ddd	-	0.08	-
VARIATIONS			
Pad option 6.0x6.0 (T1-T3)(3)			
D2	-	-	6.61
E2	-	-	6.61
D3	4.8	-	-
E3	4.8	-	-

1. *Dimensions D1 and E1 do not include mold flash or protrusions. Allowable mold flash or protrusion is “0.25 mm” per side.*
2. *The Top package body size may be smaller than the bottom package size by as much as 0.15 mm.*
3. *Number, dimension and position of groves shown in Figure 73 are for reference only.*

Figure 73. **Exposed-pad groove's shapes**



Revision history

Table 80. **Document revision history**

Date	Version	Changes
03-May-2021	1	Initial release.
05-Oct-2021	2	Updated: • *Section 3.4 Typical curves of the main electrical parameters*; • *Section 9.1 I2C settings*; • *Section 10.3 PWM pulse skipping detector*; • *Table 4. Electrical Characteristics*; • *Table 36. IB12-ADDR: "I0001100"*; • *Table 69. DB20-ADDR:"I0110100"*; • *Table 70. DB21-ADDR:"I0110101"*; • *Table 71. DB22-ADDR:"I0110110"*; • *Table 72. DB23-ADDR:"I0110111"*; • *Figure 34. Operation vs battery charge*. Minor text changes in: • *Section 8.3.1 DIM result communication*; • *Section 8.7.1 Temperature information*; • *Section 10.3 PWM pulse skipping detector*.
29-Apr-2022	3	Added: • *Table 73. DB24-ADDR:"I0111000"*; • *Table 74. DB25-ADDR:"I0111001"*; • *Table 75. DB26-ADDR:"I0111010"*; • *Table 76. DB27-ADDR:"I0111011"*. Updated: • *Section 8.3 DIM*; • *Table 50. DB1-ADDR:"I0100001"*; • *Table 51. DB2-ADDR:"I0100010"*; • *Table 52. DB3-ADDR:"I0100011"*; • *Table 53. DB4-ADDR:"I0100100"*; • *Table 54. DB5-ADDR:"I0100101"*; • *Table 59. DB10-ADDR:"I0101010"*; • *Table 62. DB13-ADDR:"I0101101"*; • *Table 65. DB16-ADDR:"I0110000"*; • *Table 68. DB19-ADDR:"I0110011"*; • *Figure 34. Operation vs battery charge*. Minor text changes in: • *Section 8.1.1 DC and AC internal diagnostic*; • *Section 8.3.1 DIM result communication*; • *Section 8.7.1 Temperature information*.
08-Aug-2023	4	Updated: • Figure 67. I^2S clock transition timings; • Table 70. DB21-ADDR:"I0110101"; • Section 9.4 External components guideline. Minor text changes in: • Table 36. IB12-ADDR: "I0001100"; • Section 4.3 Load possibilities; • Section 8.6.1 Output voltage offset detection. Minor text changes to improve readability.

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