Operational Amplifier Stability
Part 10 of 15: Cap Load Stability: Riso w/Dual Feedback

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Part 10 of this series is the sixth and final verse of our familiar electrical engineering tune "There must be six ways to leave your capacitive load stable". The six ways are Riso, High Gain & CF, Noise Gain, Noise Gain & CF, Output Pin Compensation, and Riso w/Dual Feedback. In part 10 we will cover Riso w/Dual Feedback.

This topology is very often used to buffer a precision reference integrated circuit. As a voltage buffer the op amp circuit provides higher source and sink currents than can be originally driven from the precision reference. Although we will look specifically at the gain of 1, voltage follower configuration the Riso w/Dual Feedback can be used with gains greater than one with slight modifications to the formulae provided. We will look at the two dominant type of op amp topologies, bipolar emitter-follower and CMOS RRO. The analytical and synthesis steps and techniques will be similar but there are subtle differences - enough to warrant looking at each respective output topology. As an added bonus we will purposely violate our rule-of-thumb guide and create the BIG NOT to see the effects of improper stability compensation.

From our stability analysis tool kit the Riso w/Dual Feedback technique will be presented by first order analysis, confirmed through Tina SPICE loop stability simulation, checked by the Vout/Vin AC transfer function analysis in Tina SPICE and finally sanity-checked by the Transient Real World Stability Test run in Tina SPICE. This Cload stability technique has been confirmed to work as predicted in real-world, actually-built circuits at some time over the last 25 years. However, due to resource limitations, each circuit specifically presented here has not been built, but rather is left to the reader as an exercise or the application of each technique to his/her own individual application (i.e. analyze, synthesize, simulate, build and test).

Bipolar Emitter-Follower: Riso w/Dual Feedback

The bipolar emitter-follower we will choose to analyze the Riso w/Dual Feedback technique is the OPA177, as detailed in Fig.10.1. The OPA177 is a low drift, low input offset voltage op amp capable of being powered from +/-3V to +/-15V.

OPA177
Precision Operational Amplifier

Parameter	**Specification**
Supply Voltage	+/-3V to +/-15V
Quiescent Current	1.3mA typical
Offset Voltage	10uV typical
Offset Drift	0.1uV/C typical
Input Bias Current	+/-0.5nA typical
Input Voltage Noise	85nVrms (1Hz to 100Hz)
Input Voltage Range	(V-)+2V to (V+)-2V
Gain-Bandwidth Product	600kHz
Open Loop Gain	140dB
Open Loop Output Resistance	60 ohms
Slew Rate	0.3V/us
Voltage Output Swing from Rail	2V typical (RL=2k)
Package	DIP-8, SO-8

Fig. 10.1: Bipolar Emitter-Follower Op Amp Specifications

A typical bipolar emitter-follower topology is shown in Fig.10.2. Note that both the positive and negative output drives to Vo are bipolar emitter-followers. Very few op amp data sheets today include “equivalent schematics” that would tell us the topology of the output stage used inside of the op amp. As such it is only through “Factory Only” information that we are assured of the topology.

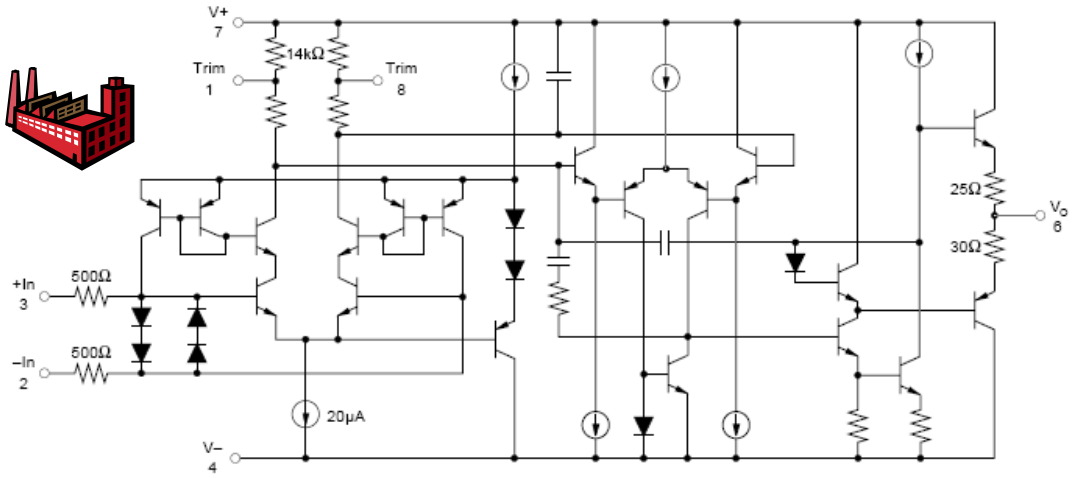
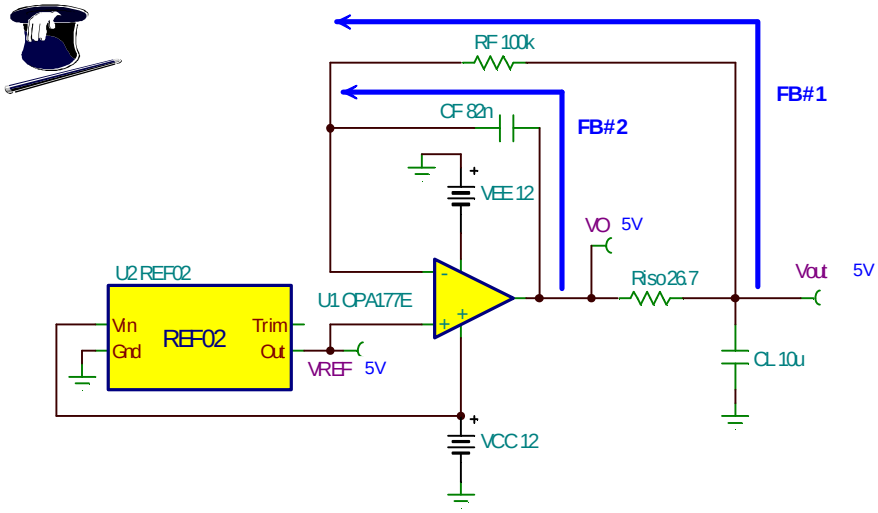


Fig. 10.2: Typical Bipolar Emitter-Follower Op Amp Topology

The Riso w/Dual Feedback circuit we will analyze for Bipolar Emitter-Follower op amps is shown in Fig.10.3. FB#1, through RF, provides direct feedback across the load, CL, and thereby forces Vout to equal VREF. FB#2, through CF, provides a second feedback path, which dominates at high frequency, to guarantee stable operation. Riso creates the isolation between FB#1 and FB#2. Notice than in many of our previous techniques for stabilizing capacitive loads we used the modified Aol approach where the output impedance of the op amp and capacitive load modified the op amp’s Aol curve. On the modified Aol curve we plotted a 1/β which would make the circuit stable. When using the Riso w/Dual Feedback technique we will find it easier to leave the op amp Aol curve unmodified and to plot FB#1 1/β and FB#2 1/β. We will then use superposition to arrive at a net 1/Βετα curve which, when plotted on the op amp Aol curve, will allow us to easily synthesize a solution to this capacitive load stability problem.



Dual Feedback:
FB#1 through RF forces accurate Vout across CL
FB#2 through CF dominates at high frequency for stability
Riso provides isolation between FB#1 and FB#2

Fig. 10.3: Riso w/Dual Feedback: Emitter-Follower

The Aol Test Circuit in Fig.10.4 will give us the starting point for stability analysis once we have chosen our op amp. The Aol curve can be gotten from the data sheet or measured in our Tina SPICE simulation as shown here. This circuit, using dual power supplies, allows us to measure the unloaded Aol curve since Vout is nearly zero volts and our input common mode voltage specification is easily met. R2 and R1 together with LT provide an AC path for the low pass filter function which allows us DC short circuit and AC open circuit in the feedback path. Remember SPICE must perform a closed loop DC analysis to find the operating point of the circuit before it can perform an AC analysis. R2 and R1 together with CT provide an AC path for the high pass filter function which allows us DC open circuit and AC short circuit into the input. LT and CT are chosen as large values to ensure their respective operations of shorts and opens at any AC frequency of interest..

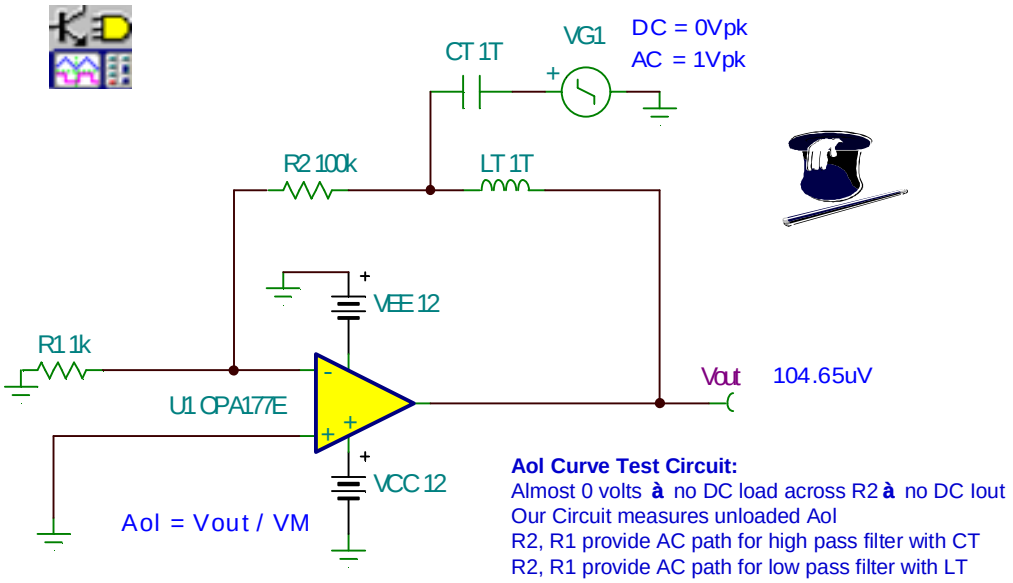


Fig. 10.4: Aol Test Schematic: Emitter-Follower

The OPA177 Aol Curve as a result of our Tina SPICE simulation is shown in Fig. 10.5. The unity gain bandwidth is measured to be 607.2kHz.

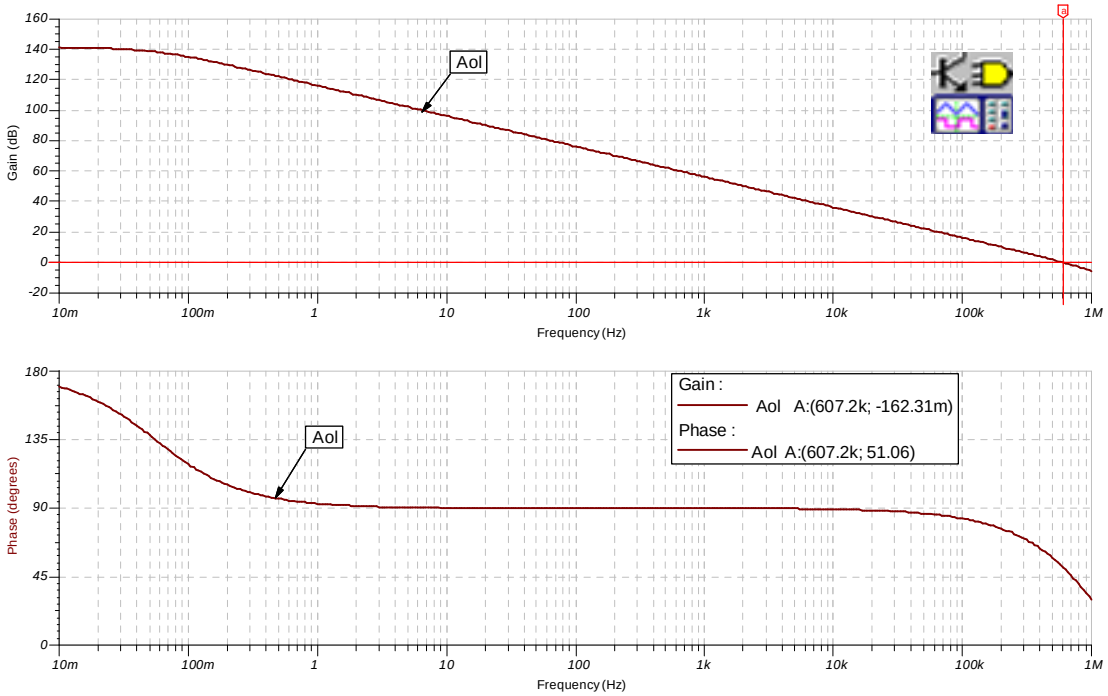


Fig.10.5: Aol Test Results: Emitter-Follower

We must now measure Zo (small signal AC open loop output impedance) as shown in Fig.10.6. This Tina SPICE test circuit will test the unloaded Zo of the OPA177. R2 and R1 together with LT provide an AC path for the low pass filter function which allows us DC short circuit and AC open circuit in the feedback path. The DC operating point is shown to be nearly zero volts at the output which means no current is flowing into or out of the OPA177. Zo is now easily measured by our application of a 1Apk AC current generator which we will sweep over the AC frequency range of 10mHz to 1MHz. Zo = Vout and if we convert the results from dB to linear or logarithmic Vout will be Zo in ohms.

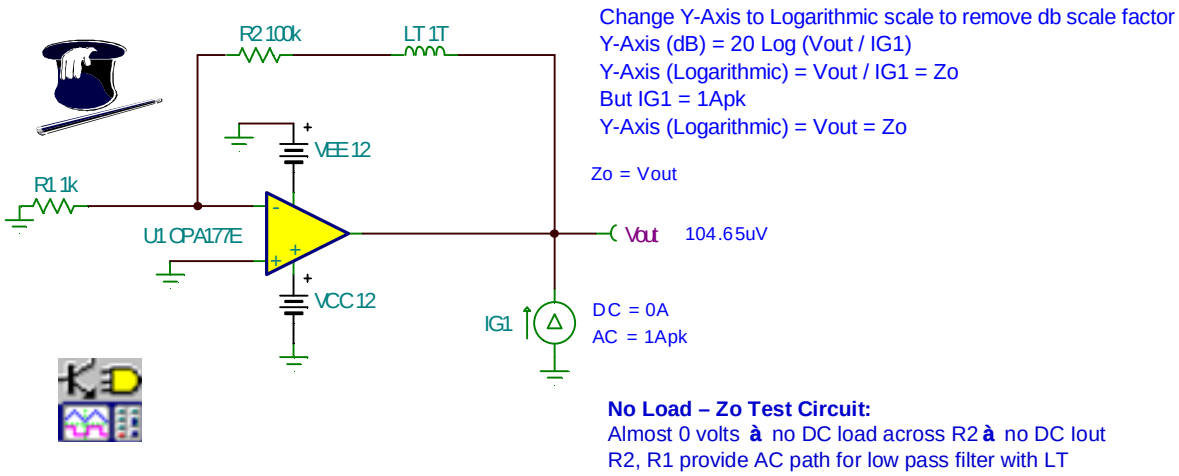


Fig.10.6: No Load Zo Test Circuit: Emitter-Follower

From Fig.10.7 the OPA177 Zo is seen to be characteristic of bipolar emitter-follower output stages with Ro dominating the only component of output impedance within the unity gain bandwidth of the OPA177. Ro for the OPA177 is 60 ohms.

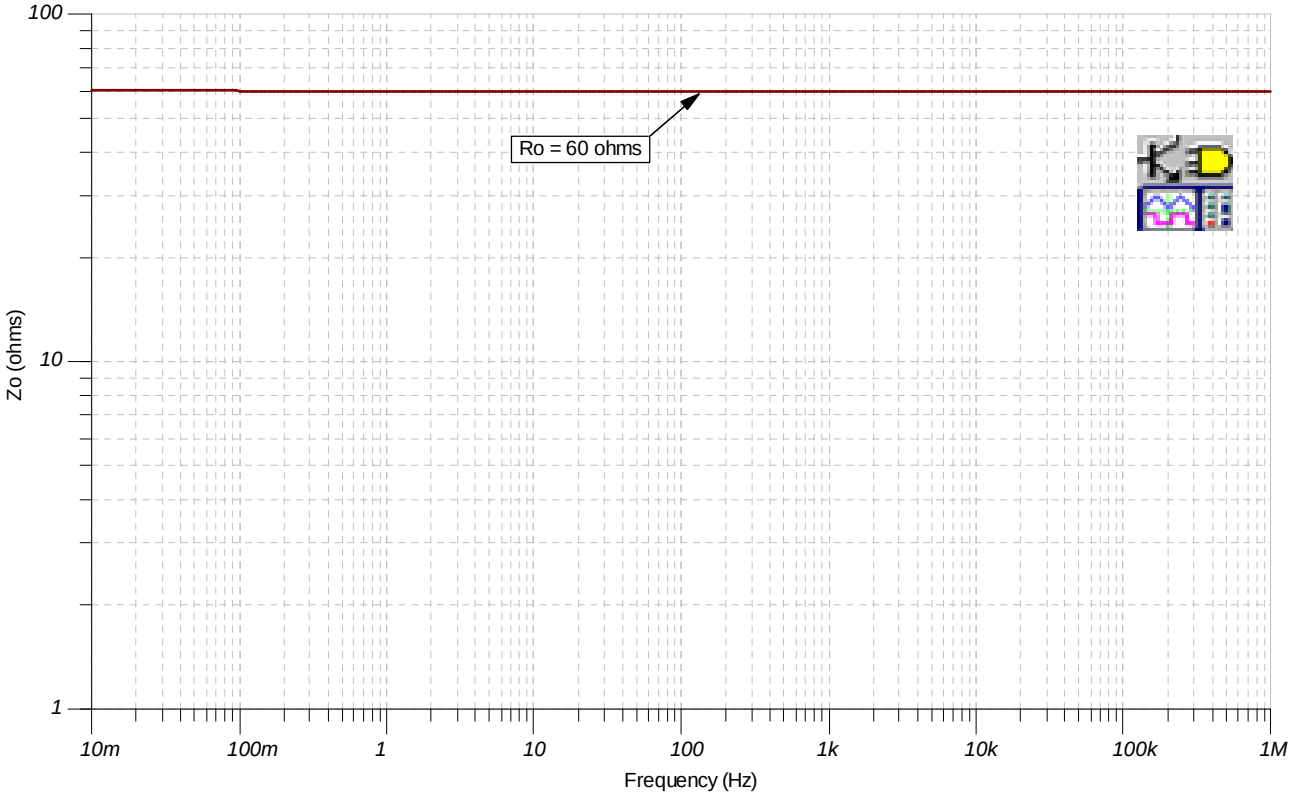
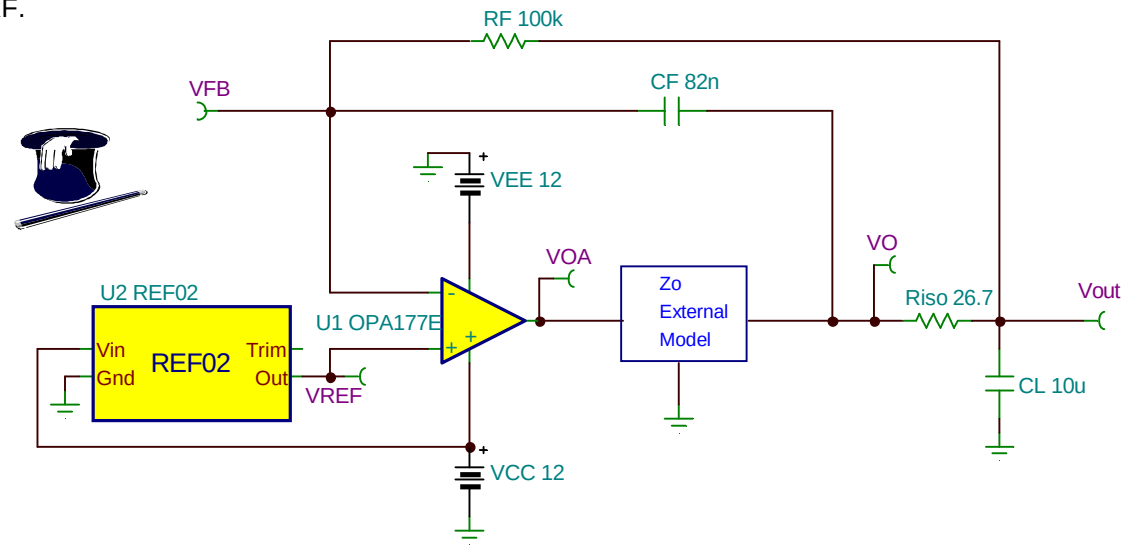


Fig. 10.7: Zo, Open Loop Output Impedance: Emitter-Follower

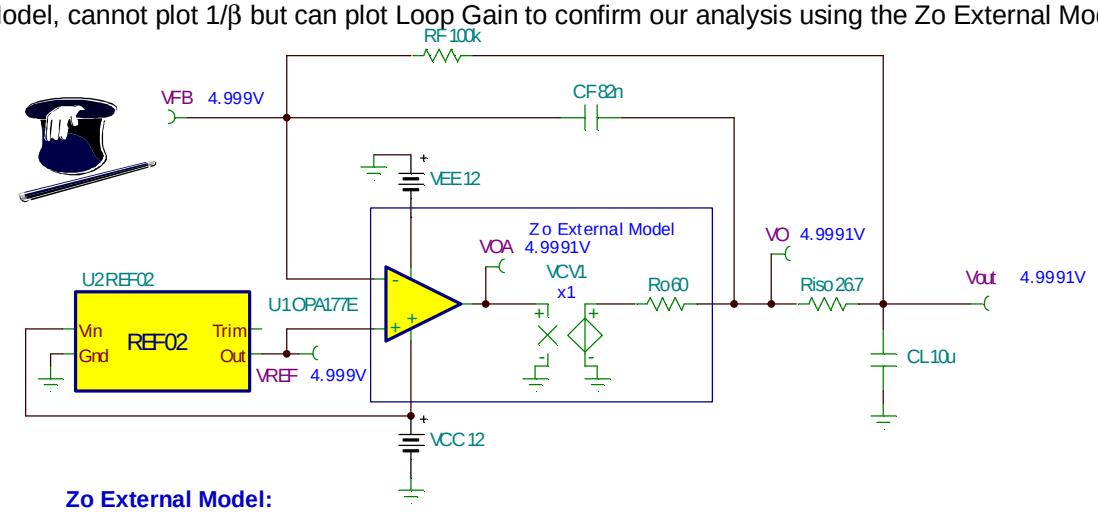
In order for our 1/β analysis to include the effects of Zo interacting with Riso, CL, CF, and RF we need to move Zo outside of our op amp macromodel so we can probe the necessary nodes in our circuit. This concept is shown in Fig. 10.8. U1 will provide the data sheet Aol curve and be buffered from any effects of Riso, CL, CF, and RF.



Zo External Model:
U1 is complete SPICE macromodel of OPA177 with data sheet Aol curve and Zo
Zo is moved outside of the op amp macromodel to form a new macromodel
Allows for simulation of 1/β with effects of Zo and external loads

Fig. 10.8: Zo External Model: Emitter-Follower

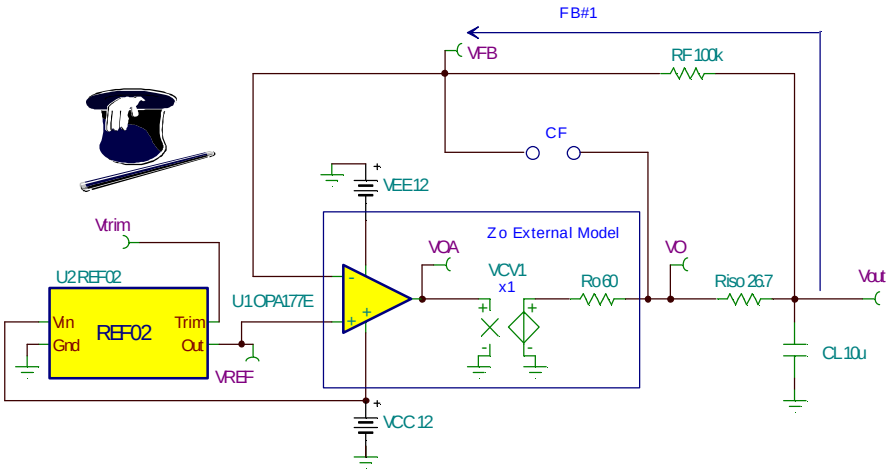
The Zo External Model shown in Fig. 10.9 allows for us to measure the effects of Zo interacting with Riso, CL, RF, and CF on 1/β. In our Zo External Model set Ro = Ro OPA177, measured to be 60 ohms. The voltage-controlled-voltage-source, VCV1 isolated our op amp macromodel, U1, from Ro, Riso, CL, CF, and RF. VCV1 is set to x1 to keep the data sheet Aol gain the same. Remove any large DC load since we want to analyze this circuit under worst case stability conditions which will be with CL only and our calculated unloaded Zo (Ro=60 ohms for this case). VOA is an internal node to the op amp which in the real world cannot be measured. It is also not easy to access this internal node on many SPICE macromodels. 1/β is analyzed relative to VOA to include the effects of Ro, Riso, CL, CF, and RF. Final stability simulation in SPICE, without using the Zo External Model, cannot plot 1/β but can plot Loop Gain to confirm our analysis using the Zo External Model.



Zo External Model:
VCV1 ideally isolates U1 so U1 only provides data sheet Aol with no effects of Zo and external loads
Set Ro to match measured Ro
Remove any large DC load **à** Analyze with unloaded Ro (largest Ro) which creates worst instability

Fig. 10.9: Zo External Model Details: Emitter-Follower

First we will analyze FB#1 as shown in Fig.10.10. Notice that CF is treated as an open since we are only going to analyze FB#1. Later we will analyze FB#2 and then, using superposition, combine the two feedback paths for the net 1/β. The results of our analysis are shown above with the derivations and details shown in the next slide. We see a zero in the FB#1 1/β plot at fzx=183.57Hz. The low frequency 1/β value is 1. If this had gain the low frequency 1/β value would be greater than 1.



FB#1 1/β:

$$\text{Zero: } fzx = \frac{1}{2\cdot\pi\cdot(Ro+Riso)\cdot CL}$$

$$fzx = \frac{1}{2\cdot\pi\cdot(60+26.7)\cdot 10u}$$

$$fzx = 183.57\text{Hz}$$

$1/\beta = 1$ (f=0) for Low-f 1β

FB#1 Analysis:

1/β zero due to combination of CL interacting with RO + Riso
Low frequency 1/β set by open CL and feedback through RF
CF is treated as an open since we are using superposition and analyzing FB#1 only

Fig. 10.10: FB#1 Analysis: Emitter-Follower

The derivation for FB#1 β is shown on the left in Fig. 10.11. Since the 1/β is the reciprocal of β, FB#1 1/β calculation is easily derived as shown on the right in Fig. 10.11. We see that the pole, fpx, in the β derivation becomes the zero, fzx, in the 1/β derivation.

FB#1 β Derivation:

$$\beta = \frac{VFB}{VOA}$$

$$\beta = \frac{XCL}{Ro+Riso+XCL}$$

$$\beta = \frac{\frac{1}{SCL}}{Ro+Riso+\frac{1}{SCL}}$$

$$\beta = \frac{1}{(Ro+Riso)\cdot SCL+1}$$

$$\beta = \frac{\frac{1}{(Ro+Riso)\cdot CL}}{S+\frac{1}{(Ro+Riso)\cdot CL}}$$

$$\text{Pole: } fpx = \frac{1}{2\cdot\pi\cdot(Ro+Riso)\cdot CL}$$

$\beta = 1$ (f=0) for Low-fβ

FB#1 1/β Derivation:

$$1/\beta = \frac{VOA}{VFB}$$

$$1/\beta = \frac{Ro+Riso+XCL}{XCL}$$

$$1/\beta = \frac{Ro+Riso+\frac{1}{SCL}}{\frac{1}{SCL}}$$

$$1/\beta = \frac{(Ro+Riso)\cdot SCL+1}{1}$$

$$1/\beta = \frac{S+\frac{1}{(Ro+Riso)\cdot CL}}{\frac{1}{(Ro+Riso)\cdot CL}}$$

$$\text{Zero: } fzx = \frac{1}{2\cdot\pi\cdot(Ro+Riso)\cdot CL}$$

$1/\beta = 1$ (f=0) for Low-f 1β

Fig. 10.11: FB#1 1/β Derivation: Emitter-Follower

We will use the circuit in Fig. 10.12 to perform AC analysis, using Tina SPICE, to find 1/β for FB#1, Aol for the OPA177, and Loop Gain for this circuit using only FB#1. Because of this we eliminate CF from the schematic.

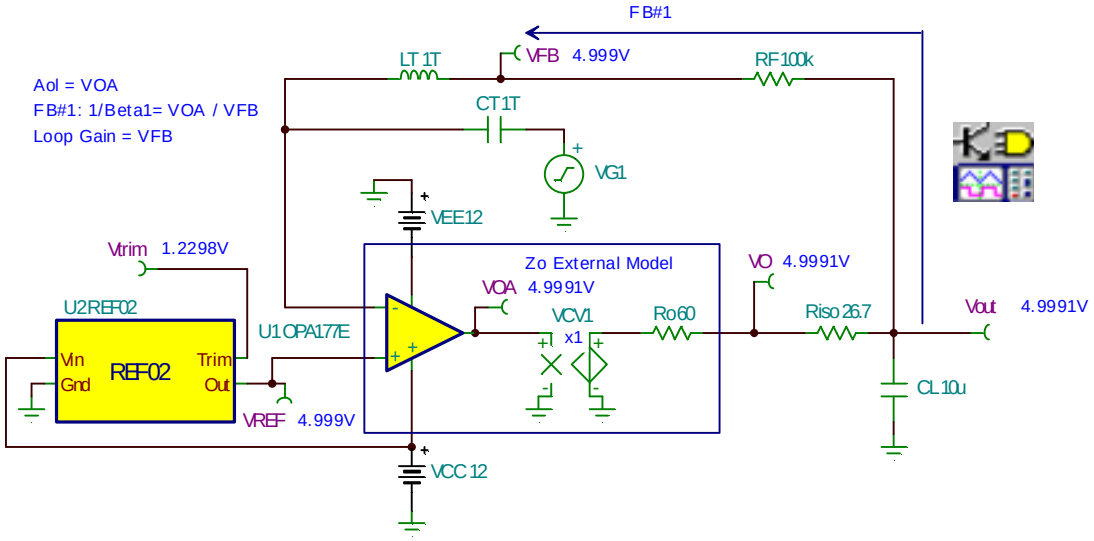


Fig. 10.12: FB#1 Analysis AC Circuit: Emitter-Follower

FB#1 1/β results are plotted on the OPA177 Aol curve in Fig. 10.13. At fcl, where Loop Gain goes to zero we see that the rate-of-closure is 40dB/decade:
[(-20dB/decade from Aol) – (+20dB/decade from FB#1 1/β) = -40dB/decade rate-of-closure]
which, from our rate-of-closure rule-of-thumb indicates instability. Our analysis of FB#1 was low frequency 1/β = 1, with a zero, fzx, at 183.57Hz. As can be seen in Fig. 10.13 our first order analysis predicted accurately FB#1 1/β.

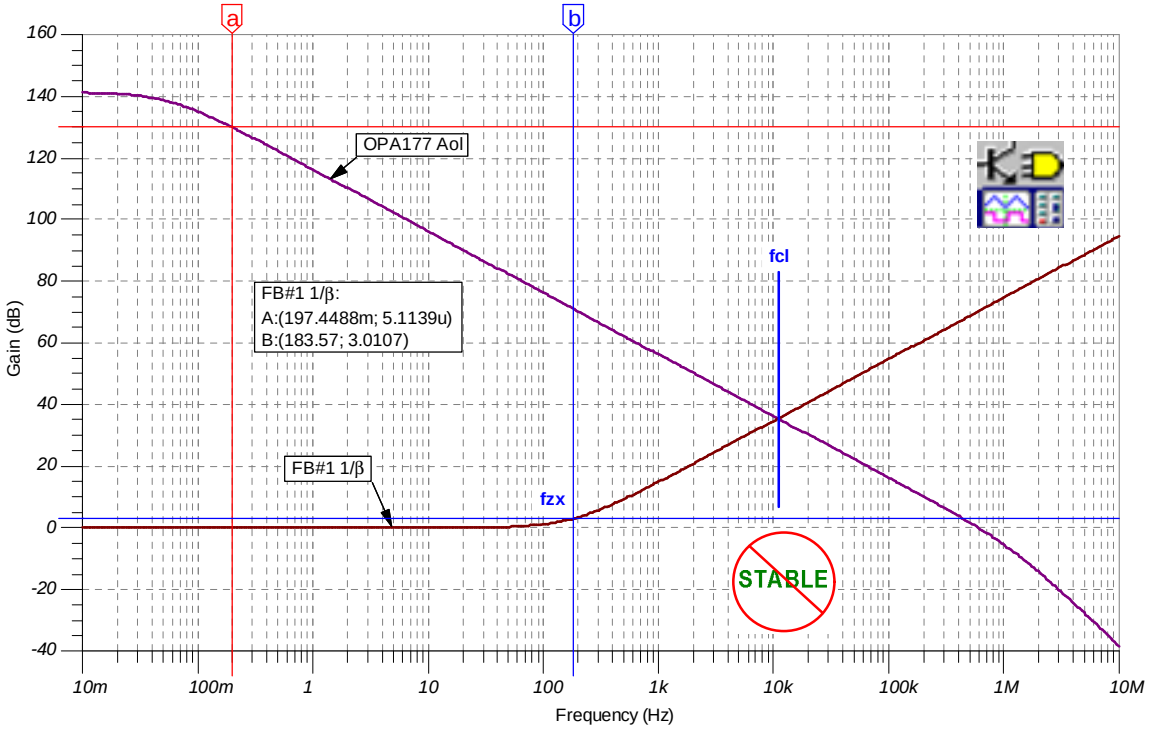


Fig. 10.13: FB#1 1/β Plot: Emitter-Follower

In Fig. 10.14 we see loop gain analysis of our circuit using only FB#1 shows that we have close to zero phase margin at fcl where loop goes to zero. This is definite confirmation that we have an unstable circuit. The poles and zeros in the loop gain plot can be predicted, by inspection, from the FB#1 1/β plot on the Aol curve in Fig. 10.13.

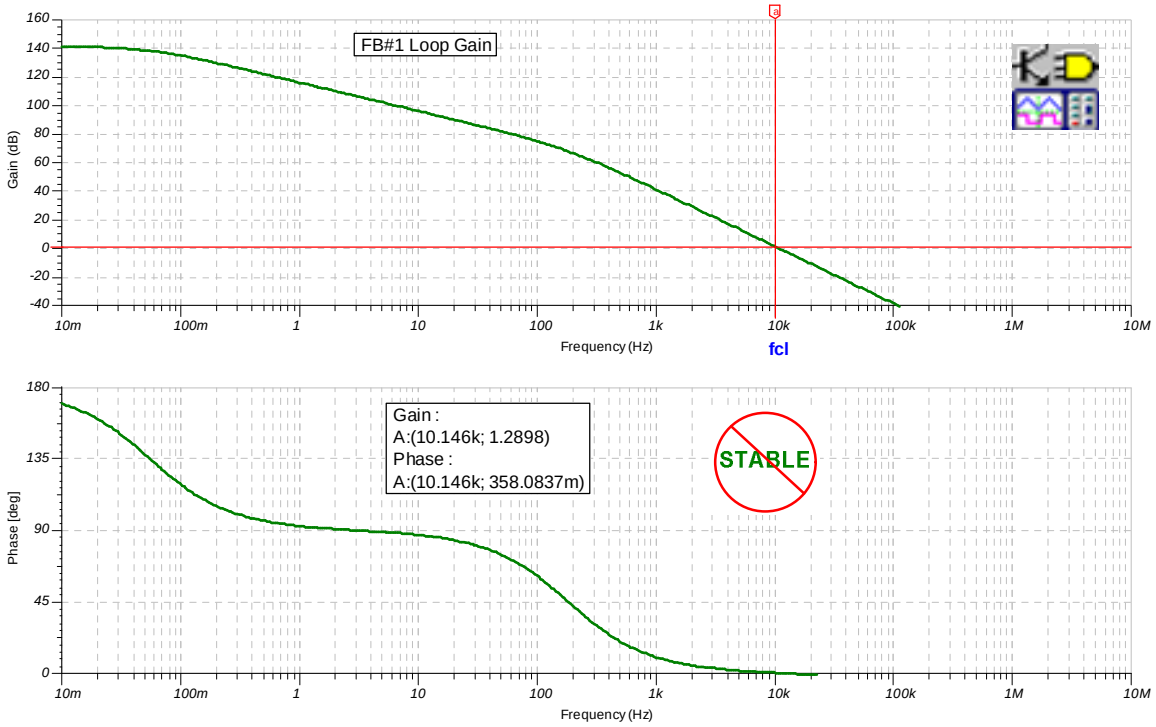


Fig. 10.14: FB#1 Loop Gain Analysis: Emitter-Follower

In case we had any doubt, or if we built our reference buffer circuit with only FB#1 we could use our real world Transient Stability Test using the circuit in Fig. 10.15.

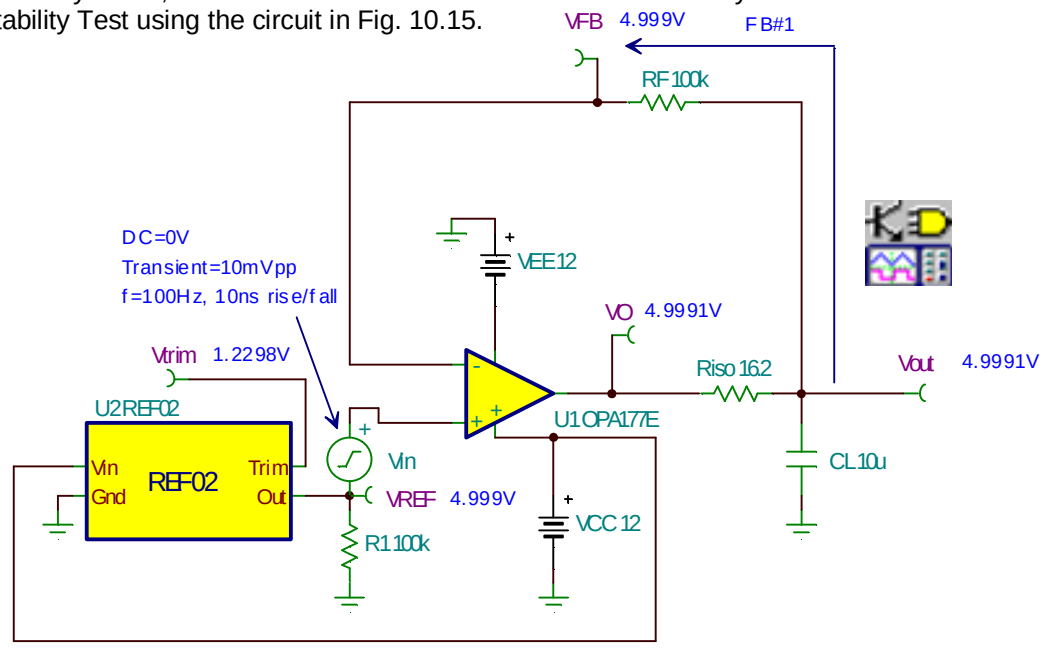


Fig. 10.15: FB#1 Transient Stability Test Circuit: Emitter-Follower

The Transient Stability Test results in Fig. 10.16 coincide with both the 1/β on Aol Pot and Loop Gain plot in confirming we have an unstable circuit by using only FB#1 in our reference buffer configuration

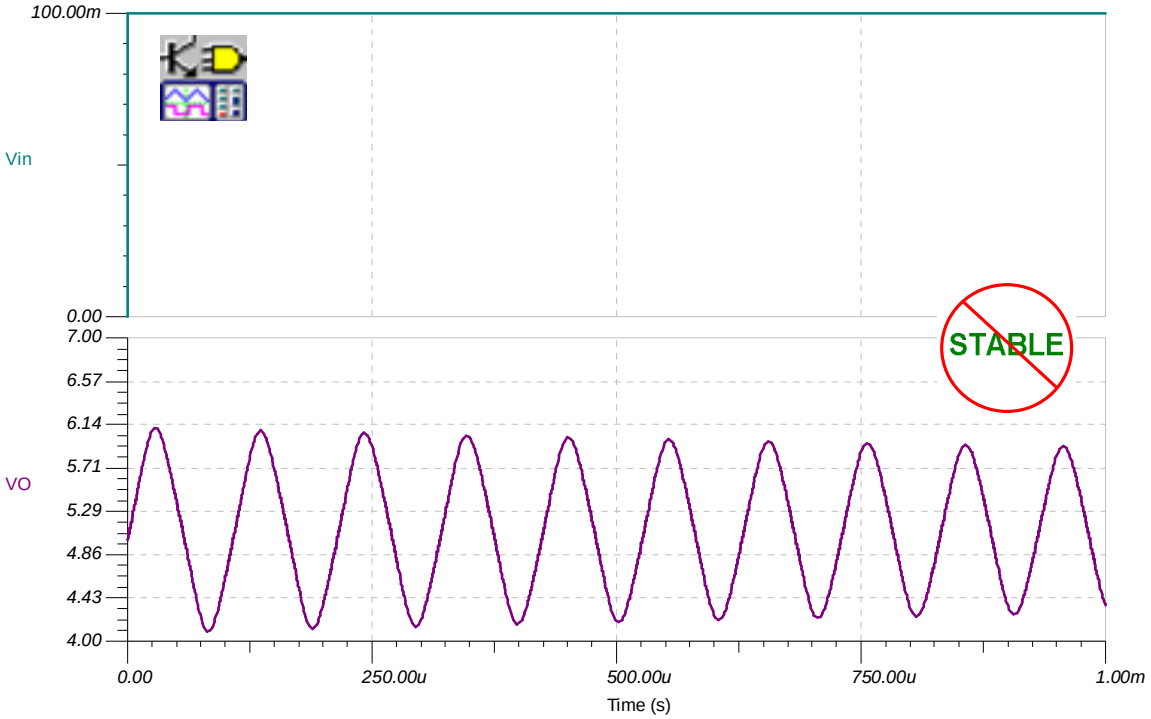


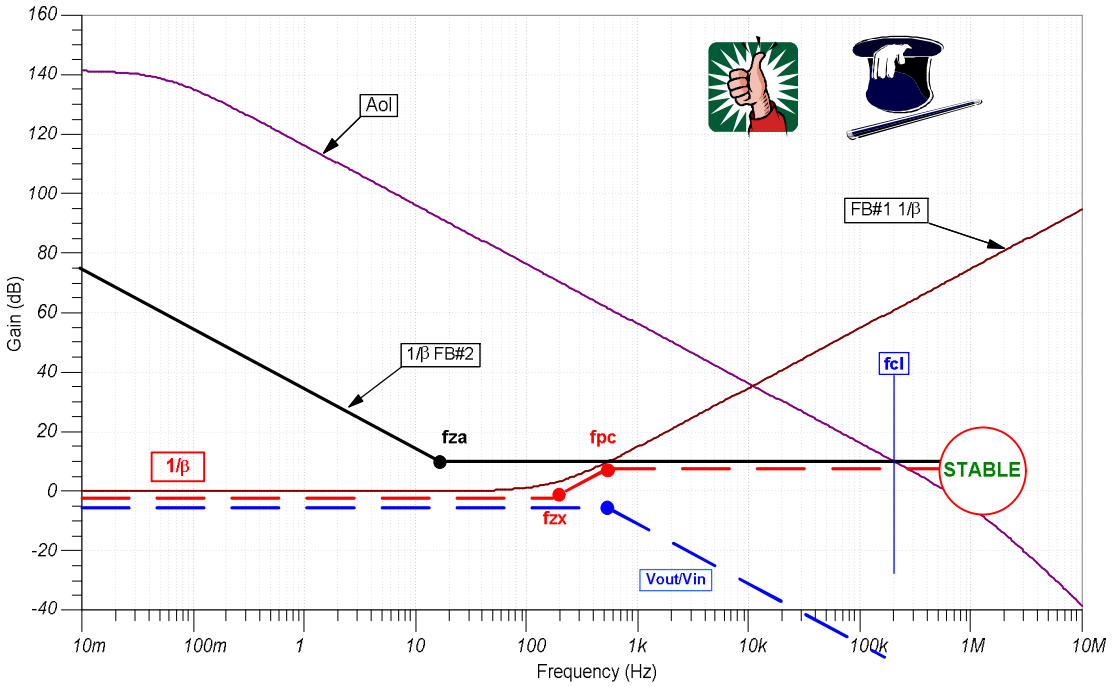
Fig. 10.16: FB#1 Transient Stability Test: Emitter-Follower

Now we must figure out how to synthesize a solution to make our reference buffer with capacitive load stable. At this point we know the Aol curve and the FB#1 1/β as shown in Fig. 10.17. If we add FB#2 1/β as shown in Fig. 10.17 we can see a net 1/β which will be a stable circuit from our stability rule-of thumb for rate-of-closure at fcl.

In addition we will force fpc to be less than a decade from fzx in the 1/β curve to ensure phase margin will be better than 45 degrees for frequencies less than fcl. This is done by setting the high frequency portion of FB#2 1/β only +10dB greater than the low frequency 1/β of FB#1. fza is set to be at least one decade less than fpc to guarantee that as parameters shift in the real world we can avoid the BIG NOT. By inspection the net 1/β curve is formed from FB#1 1/β and FB#2 1/β by choosing the path with lowest 1/β.

Remember in dual feedback paths the largest voltage fed back from the op amp output to the negative input will dominate the feedback. The largest feedback voltage implies the largest β or the smallest 1/β. Fig. 10.18 reminds us of this key trick.

As a final point we see that the Vout/Vin transfer function is predicted to follow FB#1 until FB#2 dominates at which point Vout/Vin will roll off at -20dB/decade until FB#2 intersects with the Aol curve where it would then follow the Aol curve on down.



Adding FB#2 for Stability:
Set FB#2 High-f 1/β = +10db greater than FB#1 Low-f 1/β: best phase margin within loop gain bandwidth
Set fza in FB#2 1/β = 0.1fzx in FB#1 1/β

Fig. 10.17: FB#2 Graphical Analysis: Emitter-Follower

Fig. 10.18 reminds us when using dual feedback paths around op amp circuits the largest β path will dominate. An easy analogy to remember is that if two people are talking to you in one ear which person do you hear the easiest? – The one talking the loudest! So the op amp will "listen" to the feedback path with the largest β or smallest 1/β. The net 1/β plot the op amp sees is the lower one at any frequency of FB#1 1/β or FB#2 1/β.
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Question:
How will the two feedbacks combine?

Answer:
The largest β (smallest 1/β) will dominate!

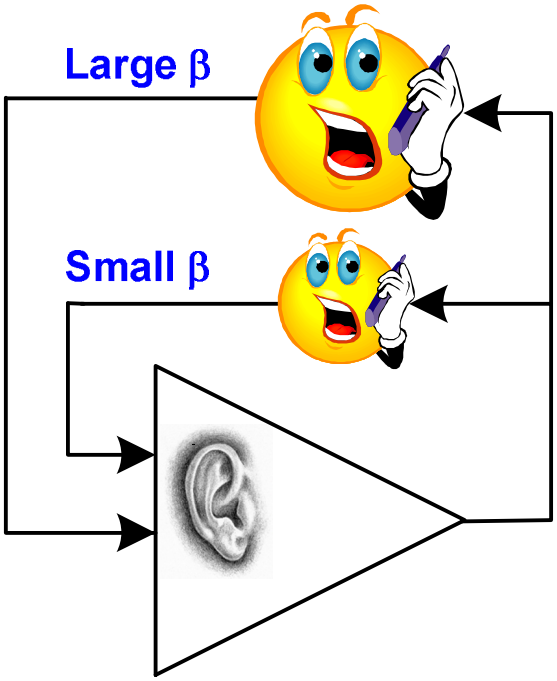
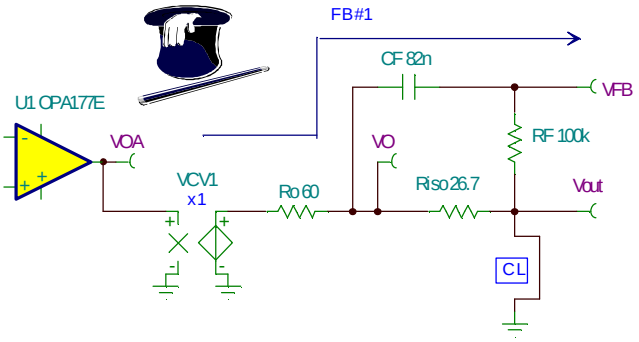


Fig. 10.18: Dual Feedback, Superposition & 1/β: Emitter-Follower

As shown in Fig. 10.19 there are some key assumptions we will make that apply to almost all Riso w/Dual Feedback circuits. First we will assume that CL>10* CF which means that CL will become a short at high frequencies long before CF does. We will therefore short CL to eliminate FB#1 so as to analyze FB#2 independently. In addition we will assume that RF>10*Riso which implies that that RF has little to no effect as a load across Riso. From Fig. 10.19 and the detailed derivations in the Fig. 10.20 we see FB#2 will have a pole at the origin with a zero, fza, at 19.41Hz caused by RF and CF. The high frequency 1/β portion of FB#2 is a ratio of Ro+Riso to Riso since CF and CL are both a short at high frequency. The derivation of FB#2 1/β is shown in the next slides with the results computed in the slide here. The high frequency 1/β for FB#2 is set to be 3.25 or 10.24dB with a pole at the origin and a zero at 19.41Hz.



FB#2 Analysis:
1/β pole at the origin
1/β zero set by RF and CF
High-f 1/β set by RO and Riso
CL = zero since we are using superposition and only analyzing FB#2

Assume:
CL > 10CF
RF > 10Riso

$$\beta = \frac{VFB}{VOA}$$

$$1/\beta = \frac{VOA}{VFB}$$

FB#2 1/β Calculation:

Pole: At Origin

$$\text{Zero: } \frac{1}{2 \cdot \pi \cdot RF \cdot CF}$$

$$\text{Zero: } \frac{1}{2 \cdot \pi \cdot 100k \cdot 82nF}$$

Zero: fza = 19.41Hz

High Frequency β:
CL = short
By Inspection:

$$1/\beta = \frac{Ro+Riso}{Riso} \text{ for High-f } 1/\beta$$

$$1/\beta = \frac{60+26.7}{26.7} \text{ for High-f } 1/\beta$$

1/β = 3.25 or 10.24dB for High-f 1β

Fig. 10.19: FB#2 Analysis: Emitter-Follower

The derivation for FB#2 β is shown on the left in Fig. 10.20. Since the 1/β is the reciprocal of β, FB#1 1/β calculation is easily derived as shown on the right in Fig. 10.20. We see that the pole, fpa, in the β derivation becomes the zero, fza, in the 1/β derivation.

FB#2 b Derivation:

FB#2 β Calculation:

$$VFB = \frac{VOA \cdot RF}{XCF + RF}$$

$$\frac{VFB}{VOA} = \frac{RF}{RF + \frac{1}{SCF}}$$

$$\frac{VFB}{VOA} = \frac{SCF \cdot RF}{SCF \cdot RF + 1}$$

$$\frac{VFB}{VOA} = \frac{S}{\frac{1}{S + CF \cdot RF}}$$

This Implies:
Zero: At Origin

$$\text{Pole: fpa} = \frac{1}{2 \cdot \pi \cdot RF \cdot CF}$$

Assume:
CL > 10CF
RF > 10Riso

$$\beta = \frac{VFB}{VOA}$$

$$1/\beta = \frac{VOA}{VFB}$$

High Frequency β:
CL = short
By Inspection:

$$\beta = \frac{Riso}{Ro + Riso} : \beta \text{ High-f}$$

$$1/\beta = \frac{Ro + Riso}{Riso} : 1/\beta \text{ High-f}$$

FB#2 1/b Derivation:

FB#2 1/β Calculation:

$$VFB = \frac{VOA \cdot RF}{XCF + RF}$$

$$\frac{VOA}{VFB} = \frac{RF + \frac{1}{SCF}}{RF}$$

$$\frac{VOA}{VFB} = \frac{SCF \cdot RF + 1}{SCF \cdot RF}$$

$$\frac{VOA}{VFB} = \frac{\frac{1}{S + CF \cdot RF}}{S}$$

This Implies:
Pole: At Origin

$$\text{Zero:fza} = \frac{1}{2 \cdot \pi \cdot RF \cdot CF}$$

Fig. 10.20: FB#2 1/β Derivation: Emitter-Follower

To check our first order analysis of FB#2 we can use the Tina SPICE circuit shown in Fig. 10.21. For ease of analysis we set CL to 10GF so it will be a short for any frequencies of interest but will still allow a proper DC operating point to be found by SPICE before the AC Analysis is performed.

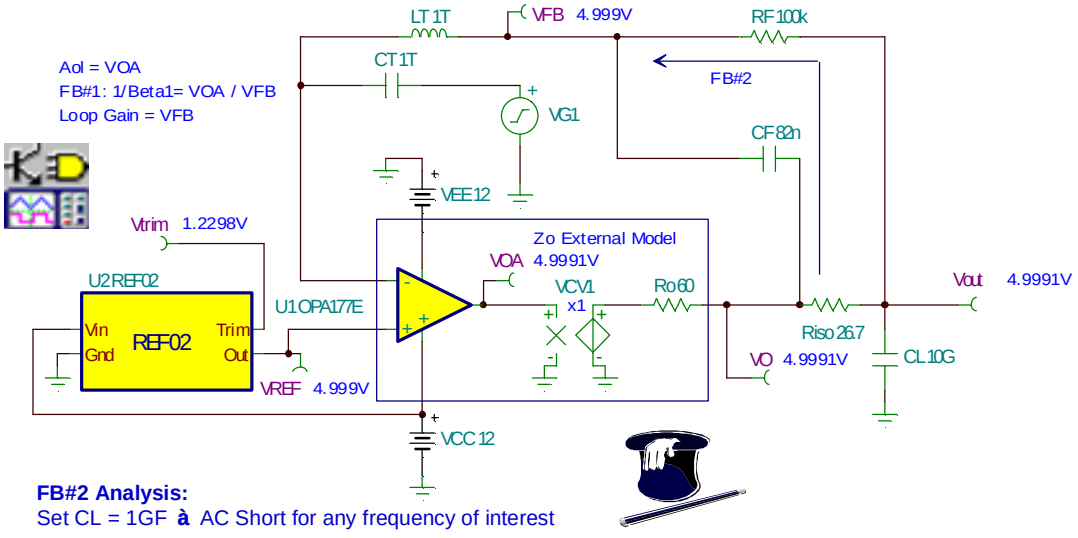


Fig. 10.21: FB#2 Analysis AC Circuit: Emitter-Follower

The results of our Tina SPICE simulation are shown in Fig. 10.22. The FB#2 1/β plot is as predicted by our first order analysis with fza= 19.41Hz and a high frequency 1/β of 10.235dB. We also plot the OPA177 Aol curve to see how FB#2 will intersect with it at high frequency.

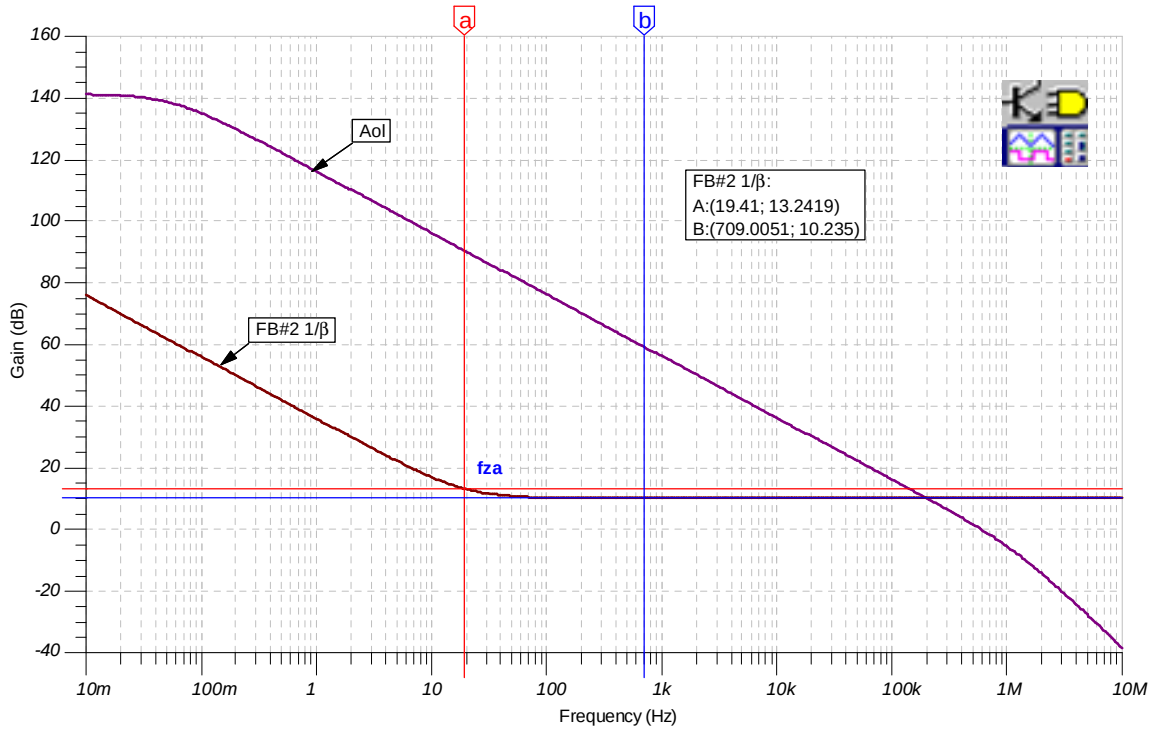


Fig. 10.22: FB#2 1/β Plot: Emitter-Follower

We will analyze if the predicted superposition results of FB#1 and FB#2 will produce the desired net 1/β by using the Tina SPICE circuit shown in Fig. 10.23. This same circuit will allow us to plot Aol, net 1/β and Loop Gain.

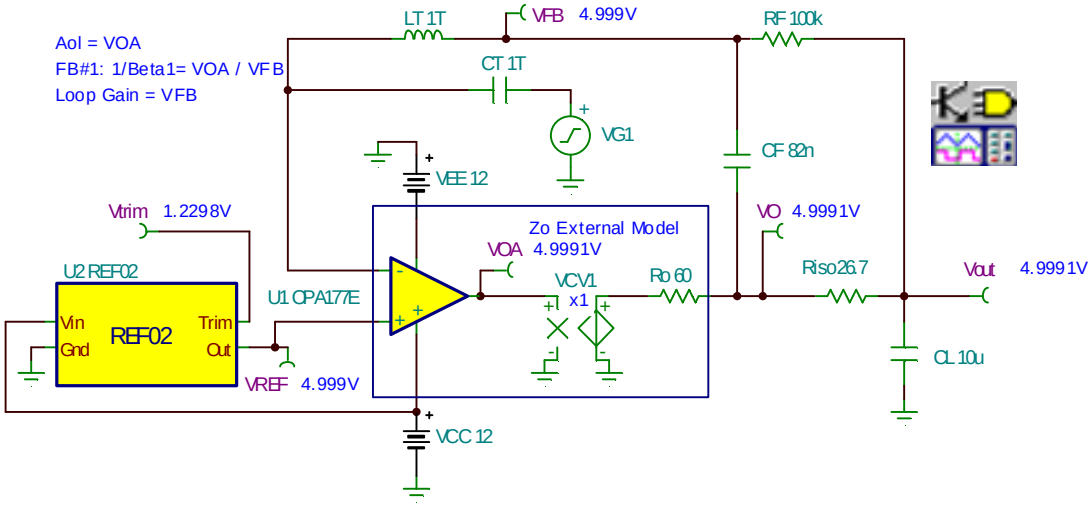


Fig. 10.23: Final Loop Gain Analysis Circuit: Emitter-Follower

In Fig. 10.24 we see our analysis results confirm our predicted net 1/β plot. At fcl, where loop gain goes to zero, we see our expected 20dB/decade rate-of-closure.

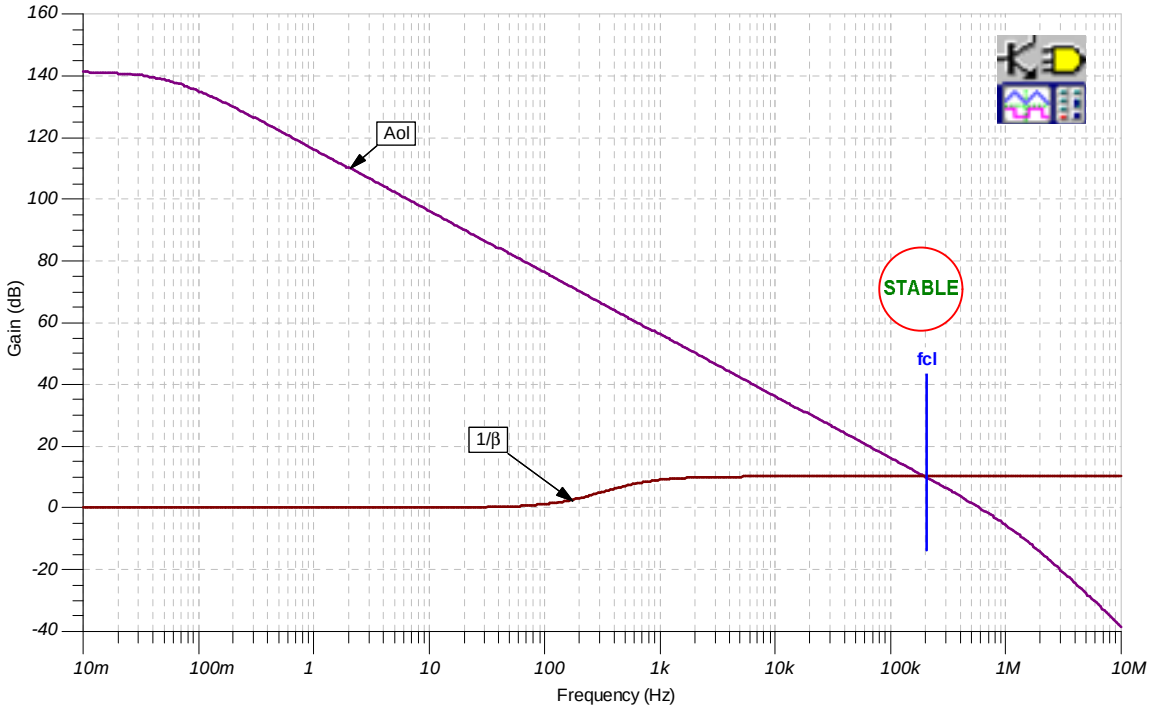


Fig. 10.24: Final Net 1/β: Emitter-Follower

The loop gain phase plot for our final circuit, which uses FB#1 and FB#2, is shown in Fig. 10.25. Phase shift never dips to less than 58.77 degrees (as seen at 199.57kHz) and at fcl, 199.57kHz, the phase margin is 76.59 degrees.

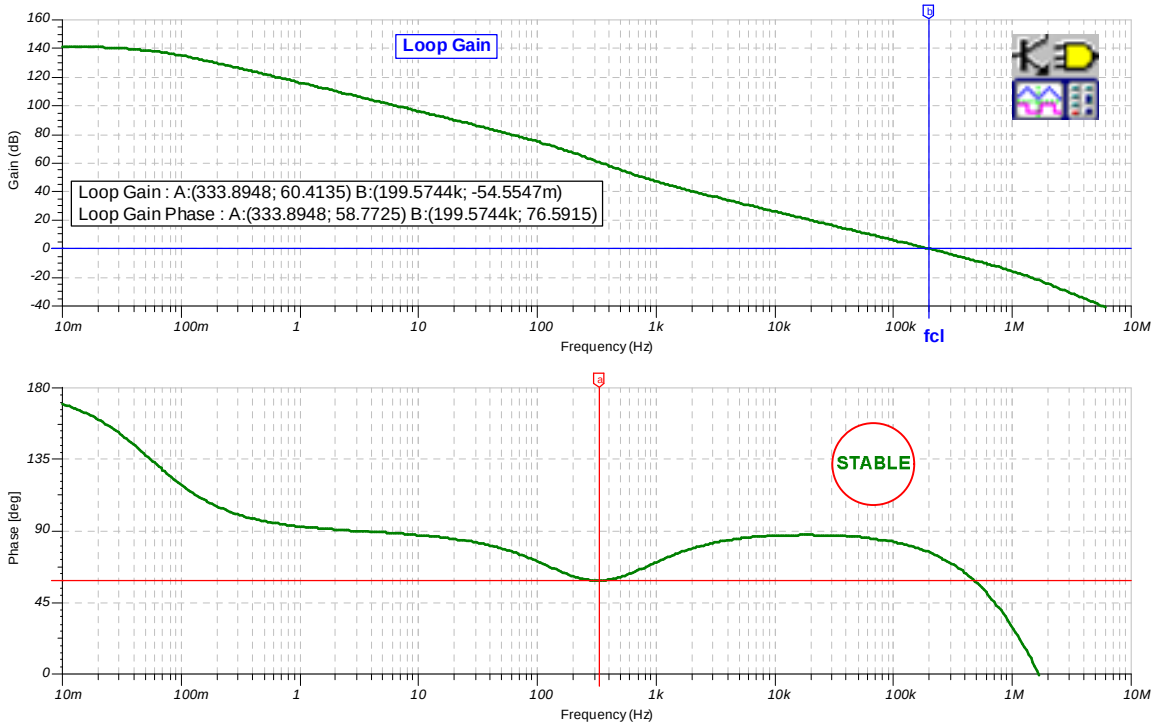


Fig. 10.25: Final Loop Gain Analysis: Emitter-Follower

We will do our final check on our stabilized circuit by running a Transient Stability Test using the Tina SPICE circuit in Fig. 10.26.

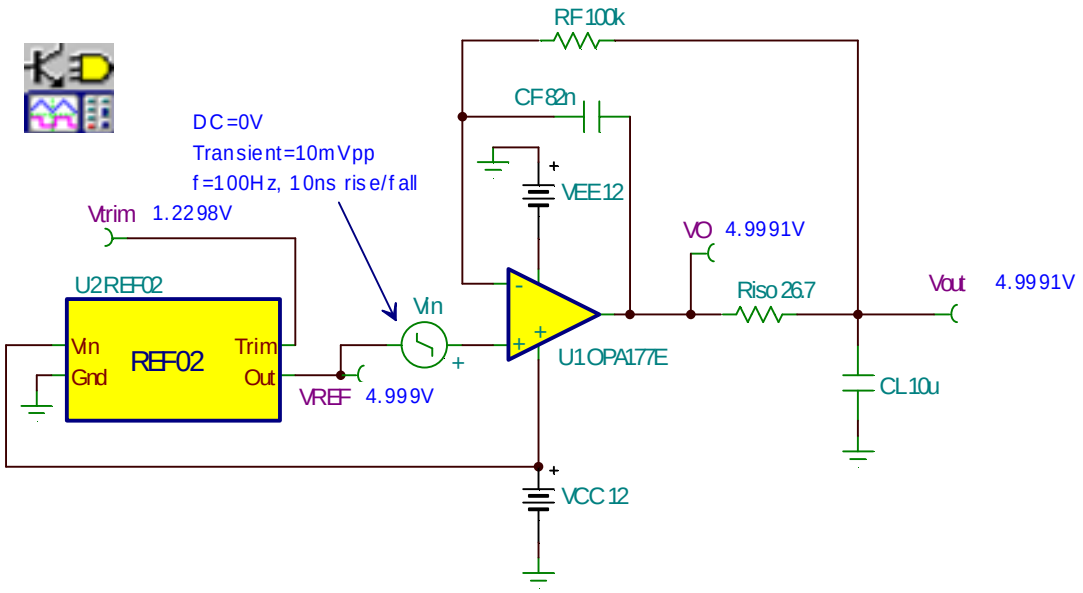


Fig. 10.26: Final Transient Stability Test Circuit: Emitter-Follower

The results of our Transient Stability Test on our final circuit in Fig. 10.27 agrees with all of our other predictions resulting in a good, stable circuit we can put into production with confidence that we will not have any failures or real world operation anomalies.

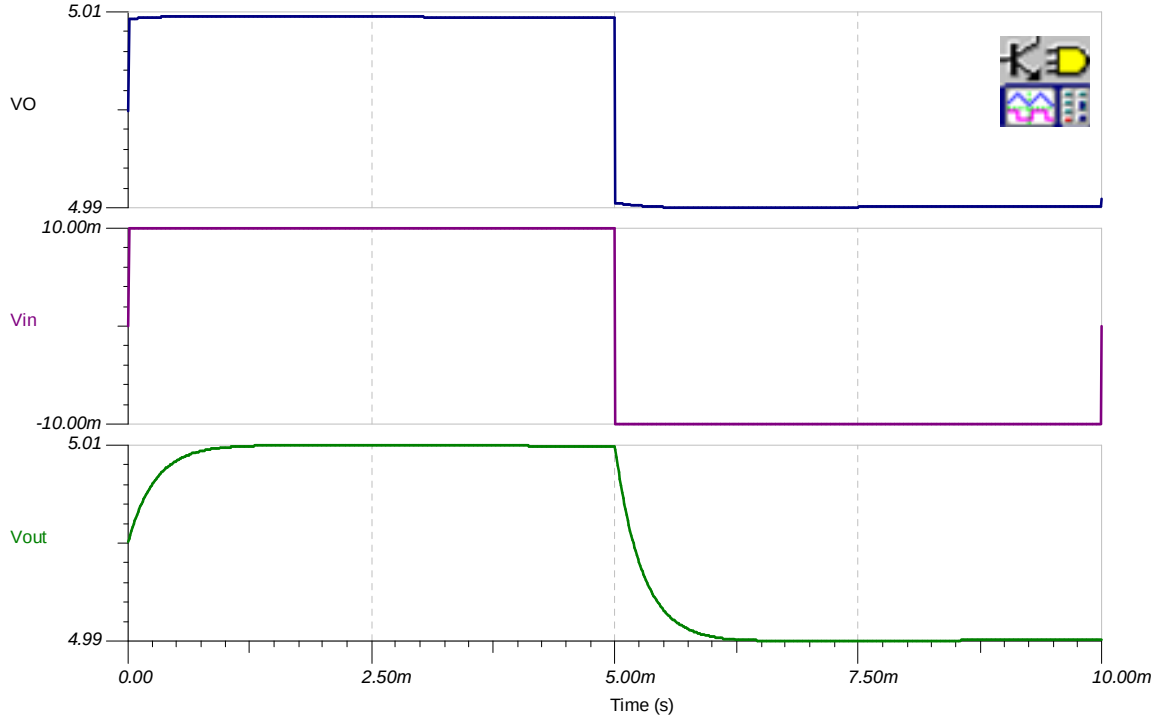


Fig. 10.27: Final Transient Stability Test: Emitter-Follower

The Tina SPICE circuit in Fig. 10.28 will allow us to confirm if our prediction of Vout/Vin is correct.

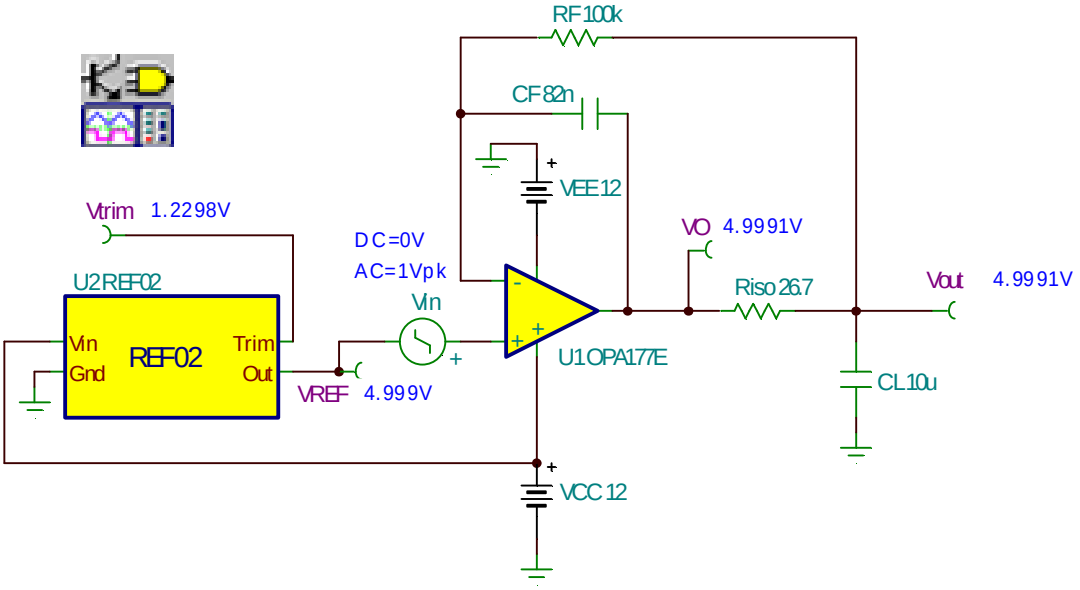


Fig. 10.28: Final Vout/Vin Transfer Function Circuit: Emitter-Follower

In Fig. 10.29 we see that the results of our Vout/Vin test match our predicted first order results with a single pole roll off at 625.53Hz and a second pole appearing at about 200kHz where FB#2 intersects the OPA177 Aol curve.

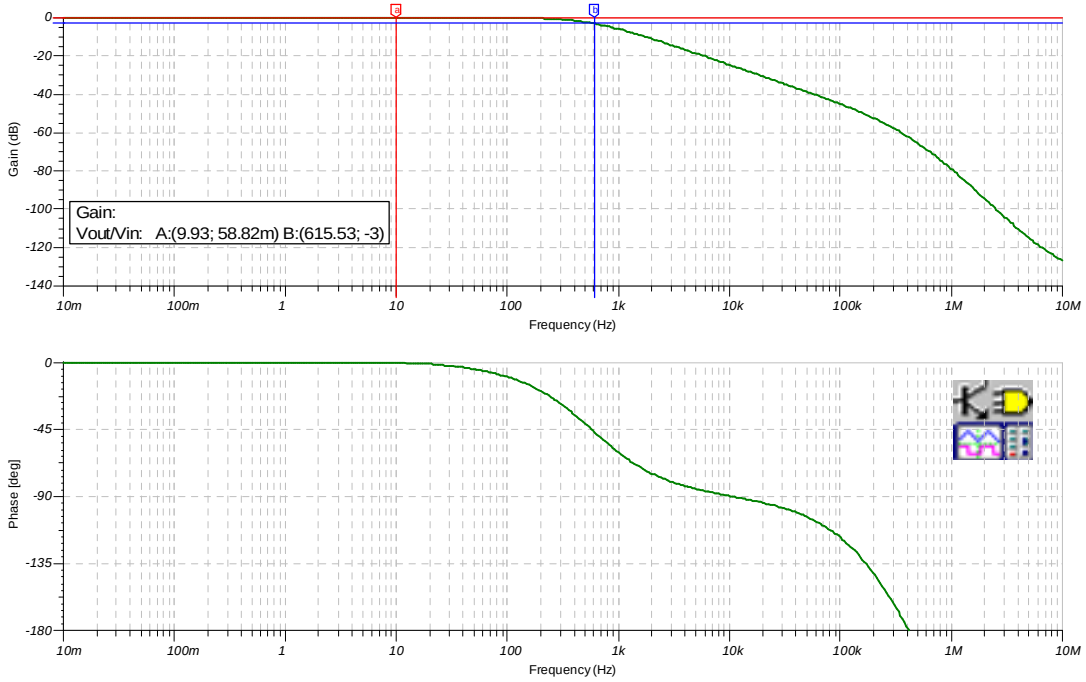


Fig. 10.29: Final Vout/Vin Transfer Function: Emitter-Follower

Fig. 10.30 summarizes an easy to use step-by-step procedure to easily use the Riso w/Dual Feedback capacitive load stability technique on Bipolar Emitter-Follower output op amps.

FB#1 1/β Formulae:

Zero: $fzx = \frac{1}{2 \cdot \pi \cdot (Ro + Riso) \cdot CL}$

$1/\beta = 1$ (f=0) for Low-f 1/β

FB#2 1/β Formulae:

Assume:
CL > 10CF
RF > 10Riso

Pole: At Origin

Zero: $fza = \frac{1}{2 \cdot \pi \cdot RF \cdot CF}$

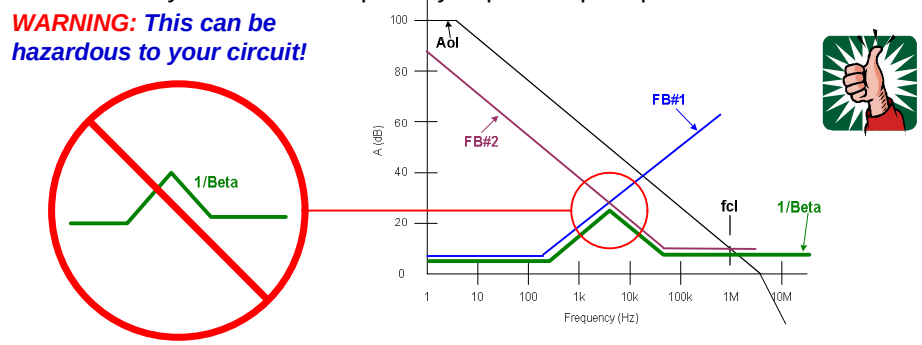
High Frequency 1/β:
CL = short
By Inspection:

$1/\beta = \frac{Ro + Riso}{Riso}$ for High-f 1/β

1) Measure Aol of Op Amp
2) Measure & Plot Zo of Op Amp
3) Determine RO
4) Create Zo External Model
5) Compute FB#1 Low-f 1/b: Equals 1 for unity gain voltage buffer
6) Set FB#2 High-f 1/b = +10dB higher than FB#1 Low-f 1/b
   (For best Vout/Vin transient response and least amount of phase shift within loop gain bandwidth)
7) Choose Riso from FB#2 High-f 1/b and RO
8) Compute FB#1 1/b fzx from CL, Riso, RO
9) Set FB#2 1/b fza = 1/10 fzx
10) Choose RF and CF with practical values to yield fza
11) Run simulation with final values for Aol, 1/b, Loop Gain, Vout/Vin, Transient Analysis to confirm design
12) Check for Loop Gain Phase shift NOT to dip more than 135 degrees (>45 degrees phase margin)
13) For low noise applications:
    Check for flat Vout/Vin response to avoid gain peaking **à** noise peaking in Vout/Vin

Fig. 10.30: Riso w/Dual Feedback Compensation Procedure: Emitter-Follower

When using dual feedback paths around an op amp there is one extremely important case to avoid – the "BIG NOT". As demonstrated in Fig. 10.31 there are op amp circuits which can result in feedback paths that create the BIG NOT, which is seen in the net 1/β plot that contains a net 1/β slope which changes from +20db/decade to -20dB/decade abruptly. This rapid change implies a complex conjugate pole in the 1/β plot which is therefore a complex conjugate zero in the Loop Gain plot. Complex zeros and poles create a +/-90 degree phase shift at the frequency of the complex zero/complex pole. In addition the phase slope around a complex zero/complex pole can range from +/-90 degrees to +/-180 degrees in a narrow frequency band around the frequency location of the occurrence. Complex zero/complex pole occurrences can cause severe gain peaking in the closed loop op amp response. This can be very undesirable especially in power op amp circuits.



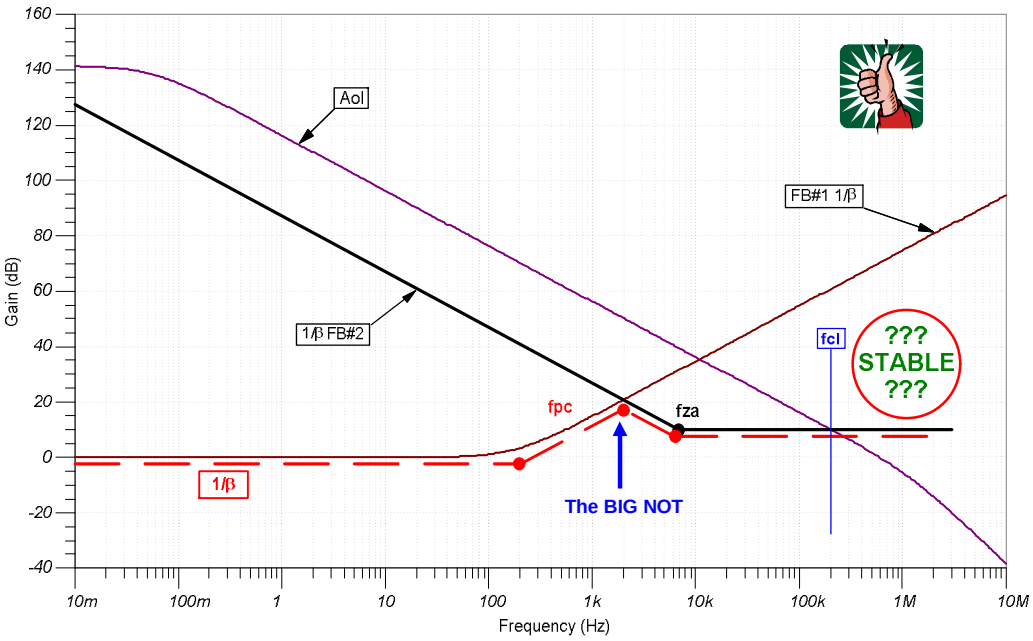
Dual Feedback and the *BIG NOT*:

1/β Slope changes from +20db/decade to -20dB/decade

- **Implies a "complex conjugate pole " in the 1/β Plot.**
- **Implies a "complex conjugate zero" in the Aolβ (Loop Gain Plot).**
- **+/-90° phase shift at frequency of complex zero/complex pole.**
- **Phase slope from +/-90°/decade slope to +/-180° in narrow band near frequency of complex zero/complex pole depending upon damping factor.**
- **Complex zero/complex pole can cause *severe* gain peaking in closed loop response.**

Fig. 10.31: Dual Feedback and the *BIG NOT*

Let's return to our plot of FB#1 and FB#2 on the OPA177 Aol curve from Fig. 10.17. We can easily create the BIG NOT by simply changing the location of fza as shown in Fig. 10.32. At fcl our rate-of-closure rule-of-thumb would indicate that this circuit is stable – but is it?



Create the BIG NOT: Change CF to 220pF which moves fza to 7.23kHz

Fig. 10.32: Create the *BIG NOT* Gaphically

In Fig. 10.33 we modify our Tina SPICE circuit used to analyze FB#1 and FB#2 together to create the BIG NOT as described in Fig. 10.32. CF is changed from 82nF to 220pF to move fza to the desired BIG NOT creation location.

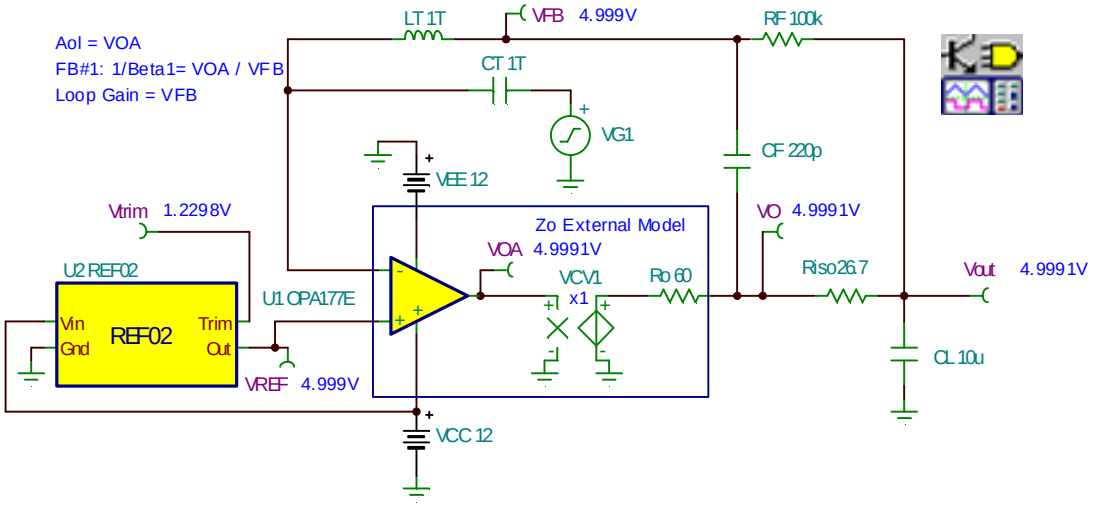
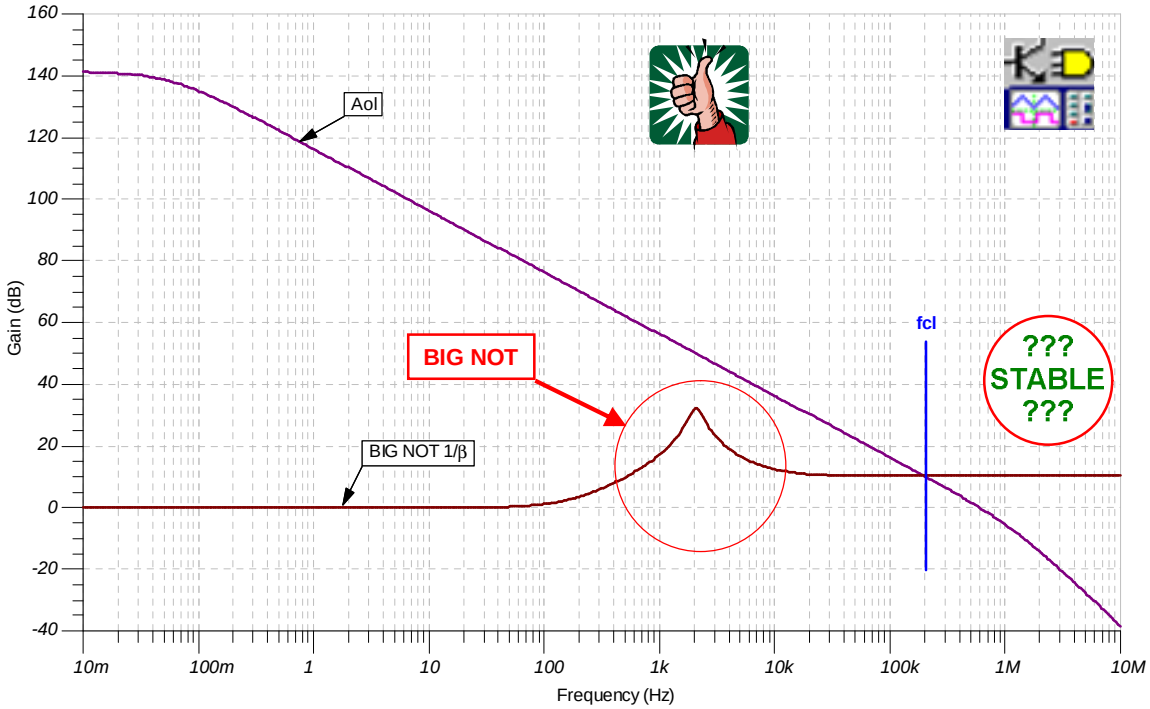


Fig. 10.33: Loop Gain Analysis Circuit: *BIG NOT*

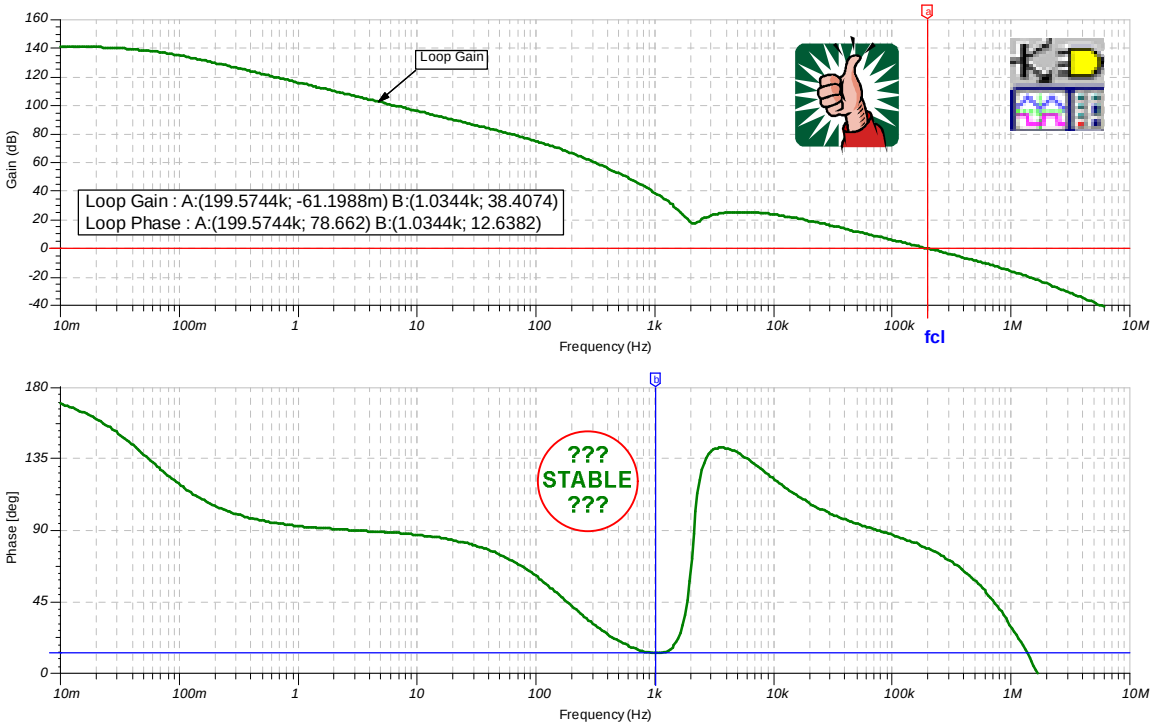
The 1/β plot of the BIG NOT is shown along with the OPA177 Aol curve in Fig. 10.34. At fcl there is 20dB/decade rate of closure but notice the quick turn-around from +20dB/decade to –20dB/decade slope in the BIG NOT 1/β plot. This 1/β peaking is not a good thing and we should question if this circuit will be stable.



BIG NOT1/b: At fcl rate-of-closure rule-of-thumb says circuit is stable but is it?

Fig. 10.34: 1/β: *BIG NOT*

A Loop Gain plot of our BIG NOT circuit in Fig. 10.35 shows phase shift to be almost 180 degrees (>167 degrees at 1.034kHz) which means we are only about 13 degrees away from a 180 degree phase shift at 1.034kHz. Also note how loop gain is sharply spiking downwards toward zero loop gain in this same region. Again at fcl there is plenty of phase margin but are we stable?



BIG NOT Loop Gain: Loop Gain phase shift >135 degrees (<45 degrees from 180 degree phase shift) for frequencies <fcl which violates the loop gain phase shift rule-of-thumb. But is it stable?

Fig. 10.35: Loop Gain Analysis: *BIG NOT*

So assume we are inexperienced in the wisdom of stability analysis (which we are not) and build this BIG NOT circuit. What can we expect a real-world Transient Stability test to look like? The Tina SPICE circuit in Fig. 10.36 will allow us to see what would result should we put this BIG NOT circuit into production and then out into the real world.

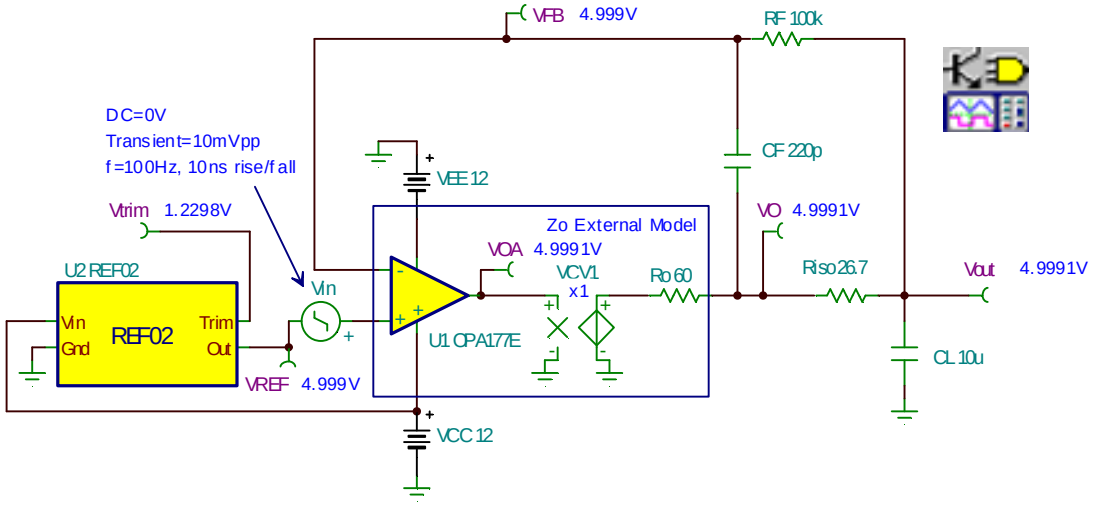
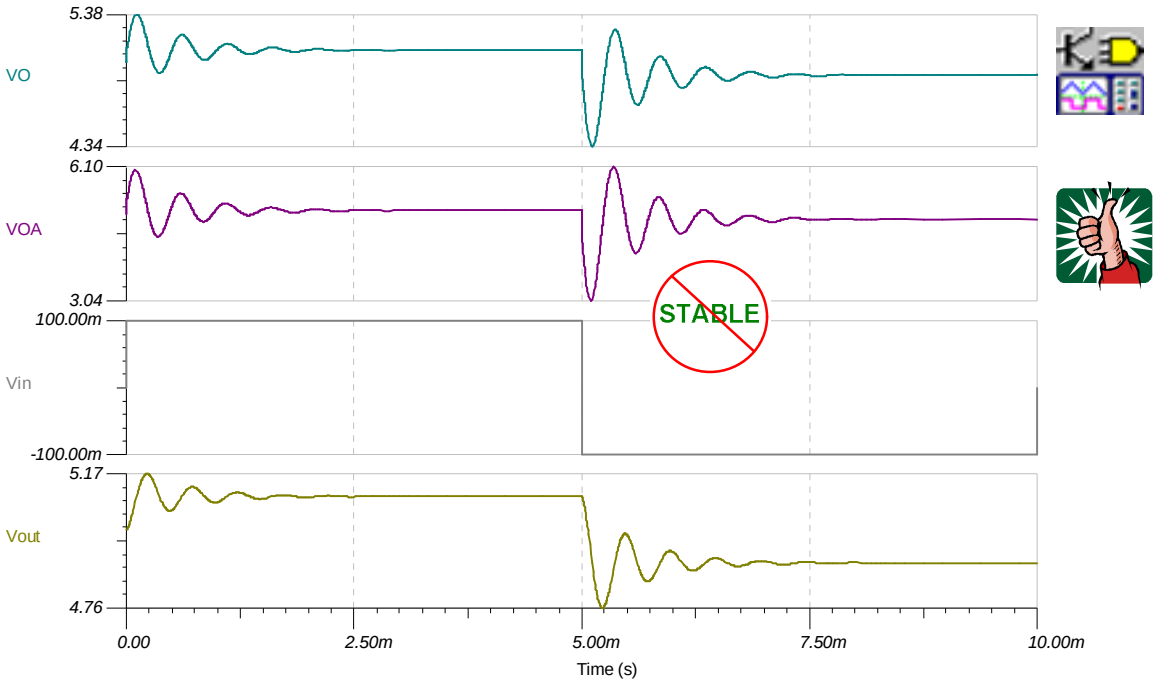


Fig. 10.36: Transient Stability Test Circuit: *BIG NOT*

Don't tell your boss we put this circuit into production or worse yet the customer who received the equipment you shipped with this circuit down inside which causes weird and intermittent problems when powered-up sometimes or when something else abruptly loads this reference buffer. Time to update our resumes? Despite the fact that this is not an oscillator the excessive ringing and long settling time from our Transient Stability Test shown in Fig. 10.37 indicate an extremely marginally stable circuit. Depending upon where the BIG NOT occurs the duration and amplitude of the oscillatory ringing can easily be worse than this example. From our board and system level view we call this circuit "unstable" especially since our analysis does not account for real world parasitics in our PCB layout, component tolerances, op amp parameter tolerances, and temperature variances of both component and op amp parameters. Fortunately we only put this into "virtual" production and can apply our Riso w/Dual Feedback technique properly to the circuit which will go into real production.



BIG NOT Transient Stability Test: Excessive ringing and marginal stability are apparent. Real world implementation and use may cause even more severe oscillations. We do not want this in production!

Fig. 10.37: Transient Stability Test: *BIG NOT*

CMOS RRO: Riso w/Dual Feedback

The CMOS RRO we will choose to analyze the Riso w/Dual Feedback technique is the OPA734, as detailed in Fig. 10.38. The OPA734 is a Zero-Drift, low input offset voltage op amp capable of being powered from +2.7V to +12V. The extremely low drift of 0.05uV/C plus its super low initial input offset voltage of 1uV make this an ideal reference buffer amplifier for single supply applications. Since this is not a rail to rail input CMOS amplifier we need to observe the Input Voltage Range specifications of (V-)-0.1V to (V+)-1.5V.

OPA734
0.05uV/C Max, Single-Supply, CMOS Operational Amplifier, Zero-Drift Series

Parameter	**Specification**
Supply Voltage (Vs)	+2.7V to +12V
Quiescent Current	600uA typical
Offset Voltage	1uV max
Offset Drift	0.05uV/C max
Input Bias Current	+/-100pA typical
Input Voltage Noise	0.8uVp-p (0.1Hz to 10Hz)
Input Voltage Noise Density	135nV/rt-Hz
Input Voltage Range	(V-)-0.1V to (V+)-1.5V
Gain-Bandwidth Product	1.6MHz
Open Loop Gain	130dB (RL=10k)
Open Loop Output Resistance	125 ohms @ f=1MHz, Io=0A
Slew Rate	1.5V/us
Voltage Output Swing from Rail	20mV max (RL=10k to Vs/2)
Package	SOT23-5, MSOP-8, SO-8

Fig. 10.38: CMOS RRO Op Amp Specifications

A typical CMOS RRO equivalent schematic is shown in Fig. 10.39. As can be seen the output of the op amp is connected to the drains of MOSFETs. This type of drain output op amp will exhibit a Zo which is both resistive and capacitive and will require us to apply some slightly different techniques for analysis then those in our bipolar emitter-follower, Riso w/Dual Feedback circuit example.

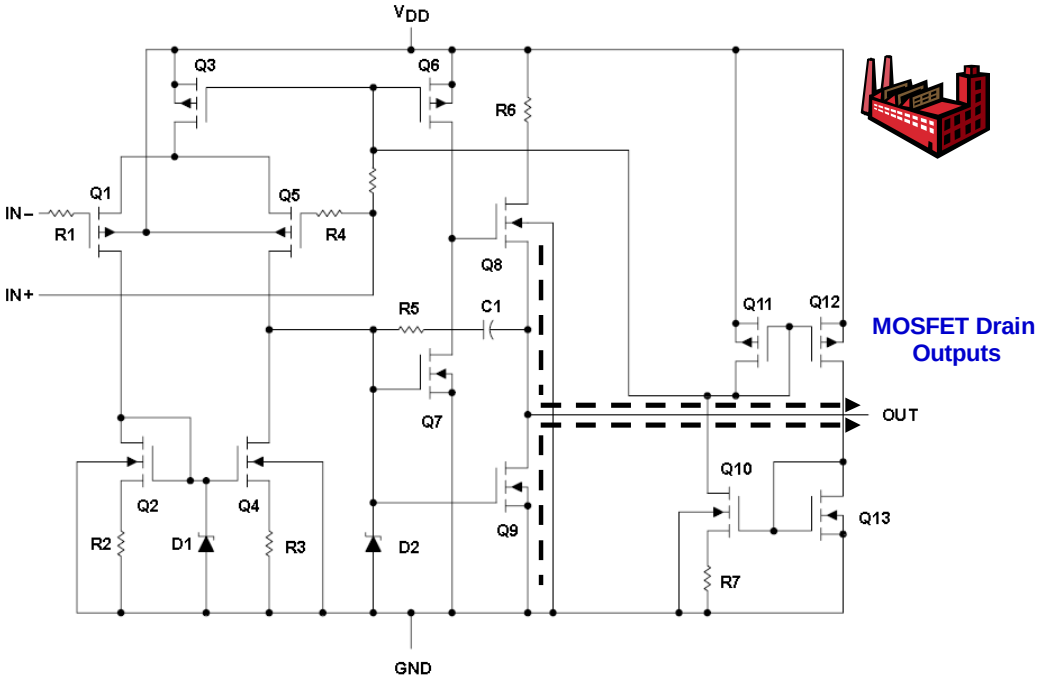
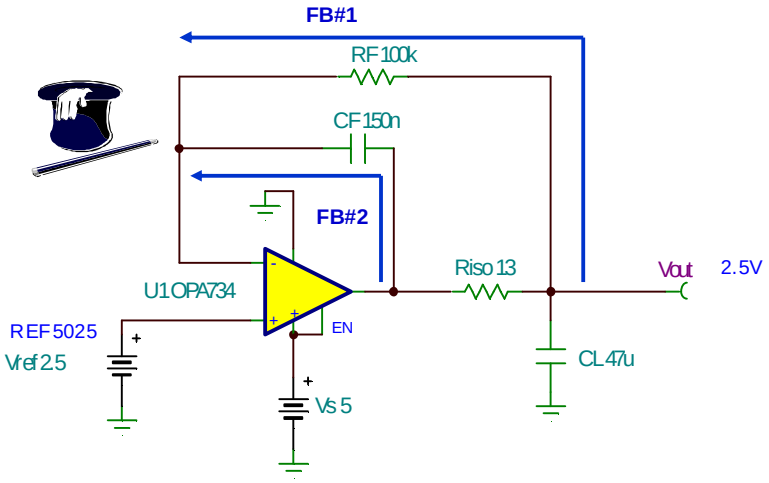


Fig. 10.39: Typical CMOS RRO Op Amp Topology

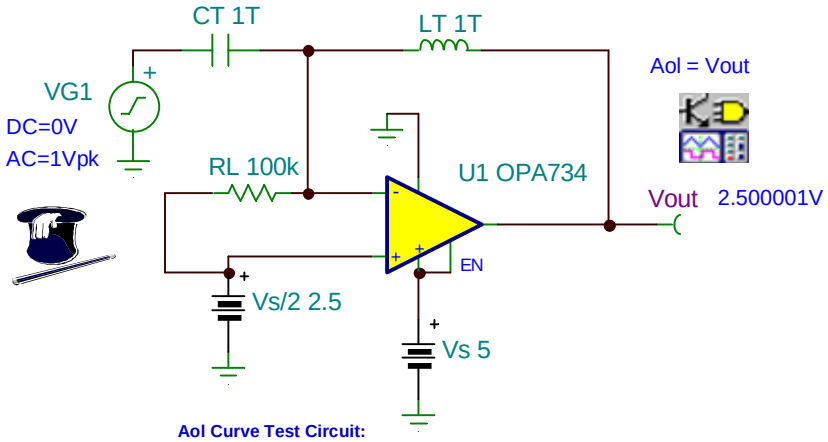
As seen in Fig. 10.40, from the outside our CMOS RRO reference buffer looks the same as the bipolar emitter-follower example. This application uses a single 5V supply and we will be buffering a 2.5V reference which is under our input voltage range specification (Input Voltage Range: 5V-1.5V =3.5V). An accurate reference voltage will be provided at Vout due to FB#1. FB#2 will provide the required feedback at high frequency for good stability. Riso will provide the needed isolation between the two feedbacks.



Dual Feedback:
FB#1 through RF forces accurate Vout across CL
FB#2 through CF dominates at high frequency for stability
Riso provides isolation between FB#1 and FB#2

Fig. 10.40: Riso w/Dual Feedback: CMOS RRO

Since we are on a single supply for this application we will use a few new tricks to get the unloaded Aol curve as shown in Fig. 10.41. First we need to ensure the OPA734 output after a DC operating point analysis is in the linear region of operation. Typically saturated outputs of op amps do not give correct AC performance since they are no in the linear region of operation. This is true for most op amp macromodels too. At DC LT is a short and CT is an open. The non-inverting input of the OPA734 is tied to Vs/2 (2.5V) and so the output will be at Vs/2 (2.5V). With RL connected as shown there is no DC load on the output of the op amp. RL together with LT provides an AC path for the low pass filter function which allows us DC short circuit and AC open circuit in the feedback path. Remember SPICE must perform a closed loop DC analysis to find the operating point of the circuit before it can perform an AC analysis. RL together with CT provide an AC path for the high pass filter function which allows us DC open circuit and AC short circuit into the input. LT and CT are chosen as large values to ensure their respective operations of shorts and opens at any AC frequency of interest.



Aol Curve Test Circuit:
RL tied to Vs/2 with Vout = Vs/2 yield No DC Iout
RL provides AC path for high pass filter with C T
RL provides AC path for low pass filter with LT

Fig. 10.41: Aol Test Schematic: CMOS RRO

The OPA734 Aol Curve as a result of our Tina SPICE simulation is shown in Fig. 10.42. The unity gain bandwidth is measured to be 1.77MHz.

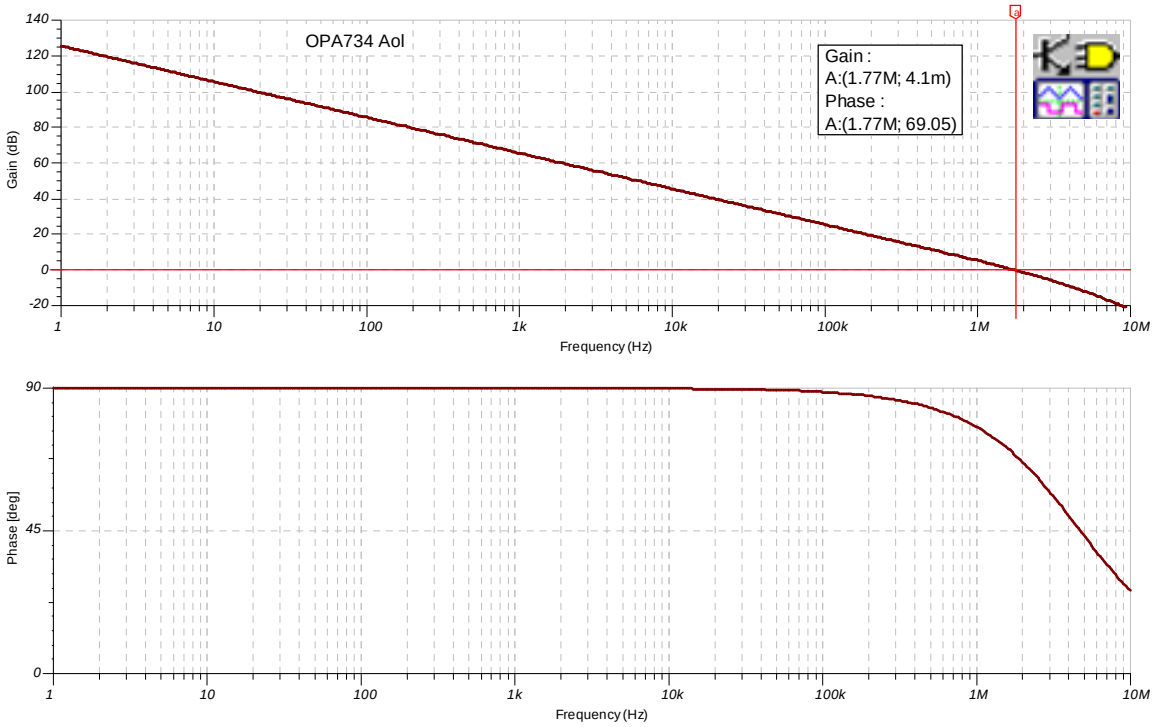
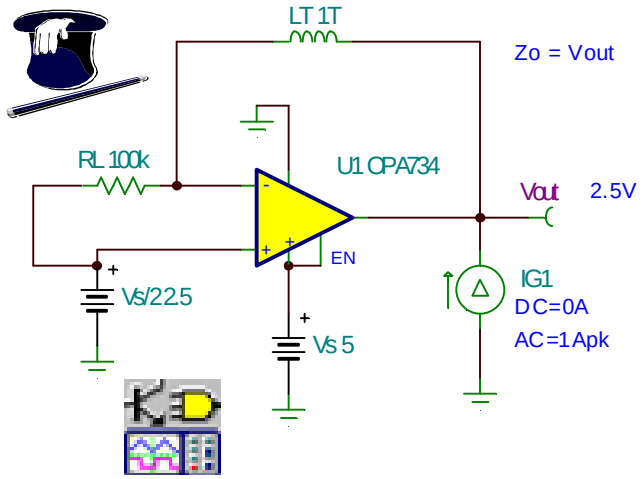


Fig. 10.42: Aol Test Results: CMOS RRO

We must now measure Zo (small signal AC open loop output impedance) as shown in Fig. 10.43. This Tina SPICE test circuit will test the unloaded Zo of the OPA734. Note that since we are testing this on single supply we choose to put the output at Vs/2 (2.5V) to ensure the op amp output I sin the linear region of operation. RL together with LT provide an AC path for the low pass filter function which allows us DC short circuit and AC open circuit in the feedback path. The DC operating point is shown to be 2.5V or Vs/2 volts at the output which means no current is flowing into or out of the OPA734 since RL is tied between Vout (2.5V) and Vs/2 (2.5V). Zo is now easily measured by our application of a 1Apk AC current generator which we will sweep over the AC frequency range of 10mHz to 1MHz. Zo = Vout and if we convert the results from dB to linear or logarithmic Vout will be Zo in ohms.



No Load – Zo Test Circuit:
RL tied to Vs/2 with Vout = Vs/2 yield No DC Iout
RL provides AC path for low pass filter with LT

Change Y-Axis to Logarithmic scale to remove db scale factor
Y-Axis (dB) = 20 Log (Vout / IG1)
Y-Axis (Logarithmic) = Vout / IG1 = Zo
But IG1 = 1Apk
Y-Axis (Logarithmic) = Vout = Zo

Fig. 10.43: TINA Circuit for Modified Aol Effects by Zo, CCO, RCO, CL

The OPA734 Zo shown in Fig. 10.44 is seen to be characteristic of CMOS RRO op amp output stages with Ro dominating at high frequency and the capacitive effect represented by Co dominating at frequencies less than 92Hz.

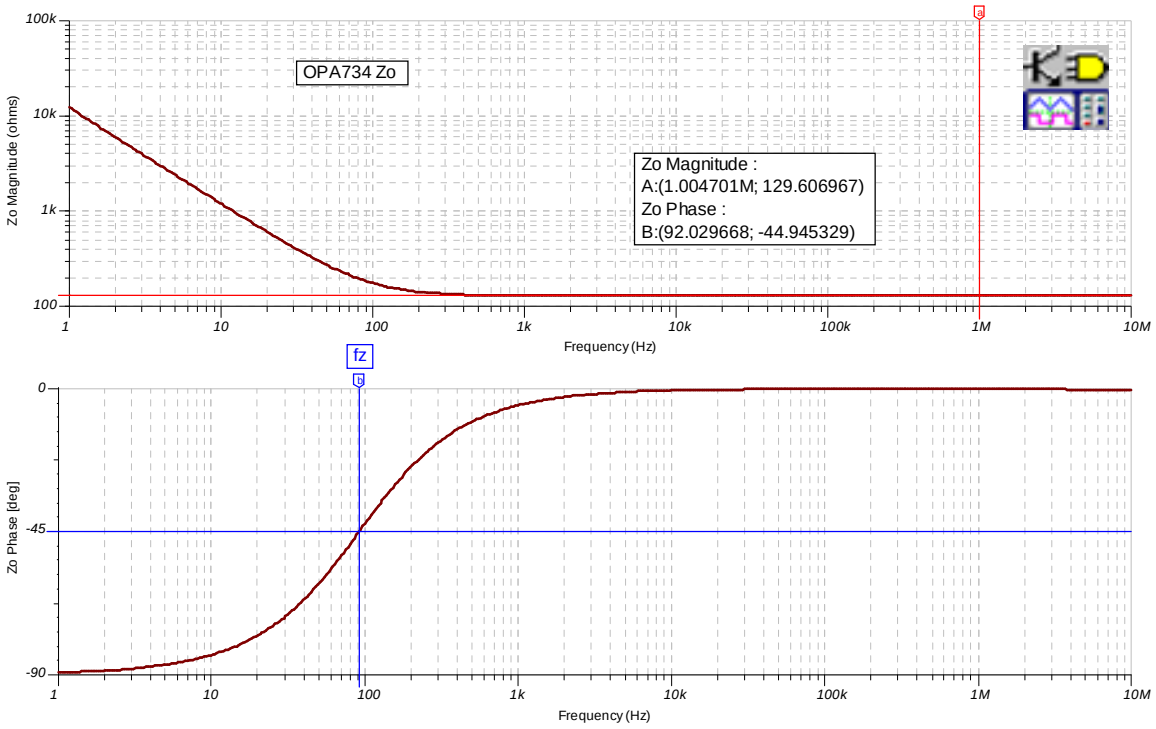
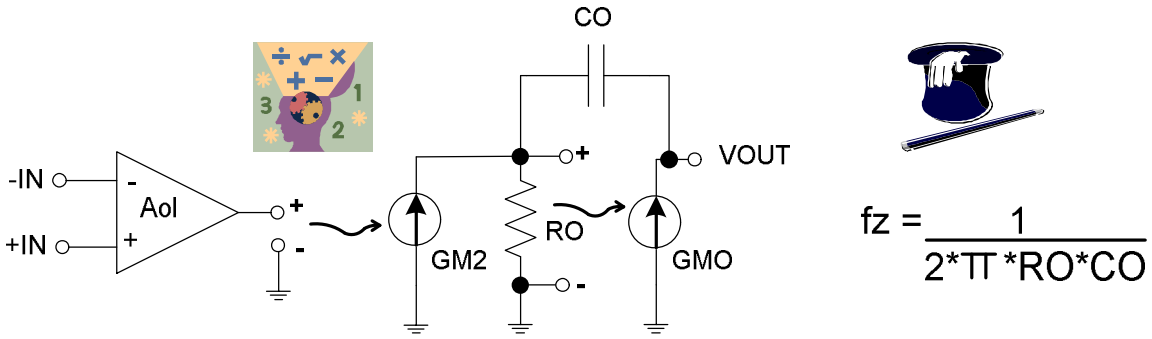


Fig. 10.44: Zo, Open Loop Output Impedance: CMOS RRO

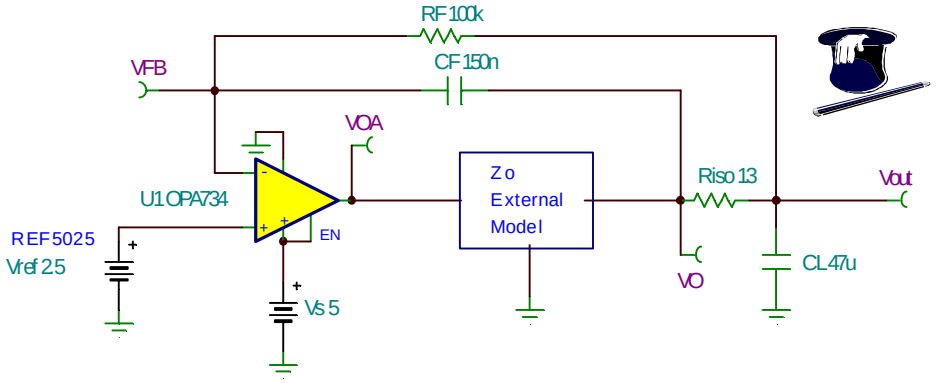
In Fig. 10.45 we build our Zo model of the OPA734 based on simulation test results from the previous slide. RO was measured directly to be 129 ohms and fz was measured directly to be 92Hz. From fz and RO we can easily compute CO to be 13.4uF and our Zo model is complete as shown.



	fz	RO	CO
No Load	92Hz	129Ω	13.4μF

Fig. 10.45: Zo Model: CMOS RRO

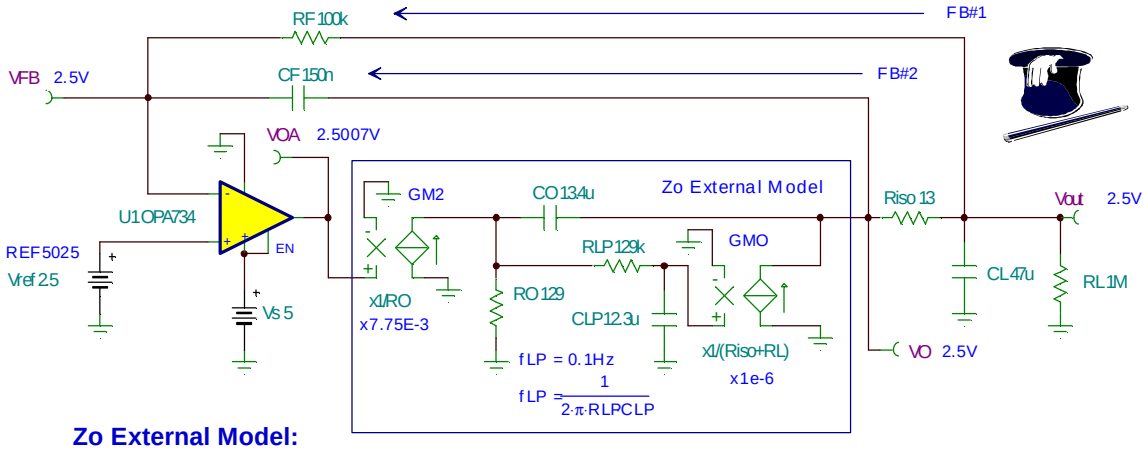
In order for our 1/β analysis to include the effects of Zo interacting with Riso, CL, CF, and RF we need to move Zo outside of our op amp macromodel so we can probe the necessary nodes in our circuit. This concept is shown in Fig. 10.46. U1 will provide the data sheet Aol curve and be buffered from any effects of Riso, CL, CF, and RF.



Zo External Model:
U1 is complete SPICE macromodel of OPA734 with data sheet Aol curve and Zo
Zo is moved outside of the op amp macromodel to form a new macromodel
Allows for simulation of 1/β with effects of Zo and external loads

Fig. 10.46: Zo External Model: CMOS RRO

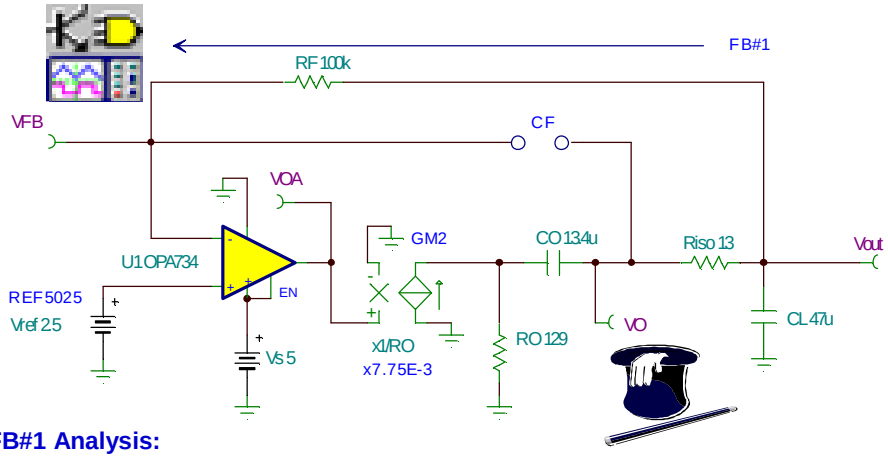
The Zo External Model shown in Fig. 10.47 allows for us to measure the effects of Zo interacting with Riso, CL, RF, and CF on 1/β. RO and CO are parameters we measured in an earlier slide. GM2 isolates U1, the OPA734 Op Amp macromodel, from our Zo External Model. GM2 is set to 1/RO to preserve the proper Aol gain to match the original OPA734 op amp macromodel and data sheet Aol. SPICE must perform a DC Analysis before it can perform and AC Analysis and so we need to make sure our expanded op amp model will have the correct DC operating point without saturation U1. To do this we add a low frequency path around CO to VO. GMO will be controlled by the voltage across RO which matches VOA. GMO is set to 1/RL to preserve the overall gain at DC to match the original OPA734 Aol. A low pass filter is formed by RLP and CLP and set to be 0.1*fLOW where fLOW is our lowest frequency of interest. RLP is set to 1000*RO to prevent any loading on RO or interaction to cause the Zo transfer function to be wrong.



Zo External Model:
GM2 ideally isolates U1 so U1 only provides data sheet Aol with no effects of Zo and external loads
Set GM2 = x1/RO to maintain data sheet Aol gain characteristic
RLP, CLP, GMO provide a path for DC Analysis
Set RLP = 1000 * RO to avoid loading RO to any level of concern
Set CLP to yield fLP = 0.1*fLOW, where fLOW is the lowest frequency of interest
Set GMO = 1/(Riso+RL) to maintain proper data sheet Aol DC gain

Fig. 10.47: Zo External Model Details: CMOS RRO

First we will analyze FB#1 as shown in Fig. 10.48. Notice that CF is treated as an open since we are only going to analyze FB#1. Later we will analyze FB#2 and then, using superposition, combine the two feedback paths for the net 1/β. The results of our analysis are shown Fig, 10.48 with the derivations and details shown in Fig. 10.49. We see a zero in the FB#1 1/β plot at fzx=107.49Hz. The low frequency 1/β value is 4.5 or 13dB and is determined by a capacitor divider between CO and CL. If this circuit were changed to have gain the low frequency 1/β value would be greater than 1.



FB#1 Analysis:
1/β zero due to series combination of CO and CL interacting with RO + Riso
Low frequency 1/β set by capacitive divider between CO and CL
CF is treated as an open since we are using superposition an analyzing FB#1 only

FB#1 1/β:

$$fzx = \frac{1}{2\cdot\pi\cdot\left(\frac{CO\cdot CL}{CL+CO}\right)\cdot(Riso+RO)}$$

$$fzx = \frac{1}{2\cdot\pi\cdot\left(\frac{13.4u\cdot 47u}{47u+13.4u}\right)\cdot(13+129)}$$

$$fzx = 107.49Hz$$

$$\frac{1}{\beta} = \frac{CL+CO}{CO} \text{ for Low-f}$$

$$\frac{1}{\beta} = \frac{47u+13.4u}{13.4u} \text{ for Low-f}$$

$$\frac{1}{\beta} = 4.5 \text{ or } 13dB \text{ for for Low-f}$$

Fig. 10.48: FB#1 Analysis: CMOS RRO

The derivation for FB#1 β is shown on the left in Fig. 10.49. Since the 1/β is the reciprocal of β, FB#1 1/β calculation is easily derived as shown on the right in Fig. 10.49. We see that the pole, fpx, in the β derivation becomes the zero, fzx, in the 1/β derivation.

FB#1 β Derivation:

$$\beta = \frac{VFB}{VOA}$$

$$\beta = \frac{XCL}{RO+XCO+Riso+XCL}$$

After Algebraic Manipulation:

$$\beta = \frac{\frac{1}{CL\cdot(Riso+RO)}}{S+\frac{1}{\left(\frac{CO\cdot CL}{CL+CO}\right)\cdot(Riso+RO)}}$$

Note: $\frac{CO\cdot CL}{CL+CO}$ is series combination of CO and CL

$$\text{Pole: } fpx = \frac{1}{2\cdot\pi\cdot\left(\frac{CO\cdot CL}{CL+CO}\right)\cdot(Riso+RO)}$$

$\beta = \frac{CO}{CL+CO}$ for f = 0 (Low-fβ)
CO and CL form a Capacitive Divider

FB#1 1/β Derivation:

$$\frac{1}{\beta} = \frac{Vout}{VOA}$$

$$\frac{1}{\beta} = \frac{RO+XCO+Riso+XCL}{XCL}$$

After Algebraic Manipulation:

$$\frac{1}{\beta} = \frac{S+\frac{1}{\left(\frac{CO\cdot CL}{CL+CO}\right)\cdot(Riso+RO)}}{\frac{1}{CL\cdot(Riso+RO)}}$$

Note: $\frac{CO\cdot CL}{CL+CO}$ is series combination of CO and CL

$$\text{Zero: } fzx = \frac{1}{2\cdot\pi\cdot\left(\frac{CO\cdot CL}{CL+CO}\right)\cdot(Riso+RO)}$$

$\frac{1}{\beta} = \frac{CL+CO}{CO}$ for f = 0 (Low-f 1β)
CO and CL form a Capacitive Divider

Fig. 10.49: FB#1 1/β Derivation: CMOS RRO

We will use the circuit in Fig 10.50 to perform AC analysis, using Tina SPICE, to find 1/β for FB#1, Aol for the OPA734, and Loop Gain for this circuit using only FB#1.

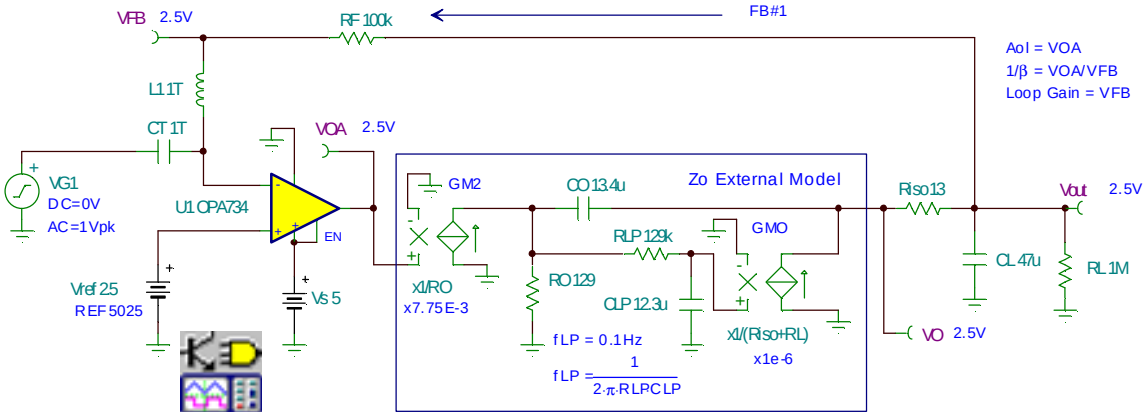


Fig. 10.50: FB#1 Analysis AC Circuit: CMOS RRO

FB#1 1/β results are plotted on the OPA734 Aol curve in Fig. 10.51. At fcl, where Loop Gain goes to zero we see that the rate-of-closure is 40dB/decade:
[(-20dB/decade from Aol) – (+20dB/decade from FB#1 1/β) = -40dB/decade rate-of-closure]
which, from our rate-of-closure rule-of-thumb indicates instability. Our analysis of FB#1 was low frequency 1/β = 13.09dB with a zero, fzx, at 183.57Hz. As can be seen in Fig. 10.51 our first order analysis predicted accurately FB#1 1/β.

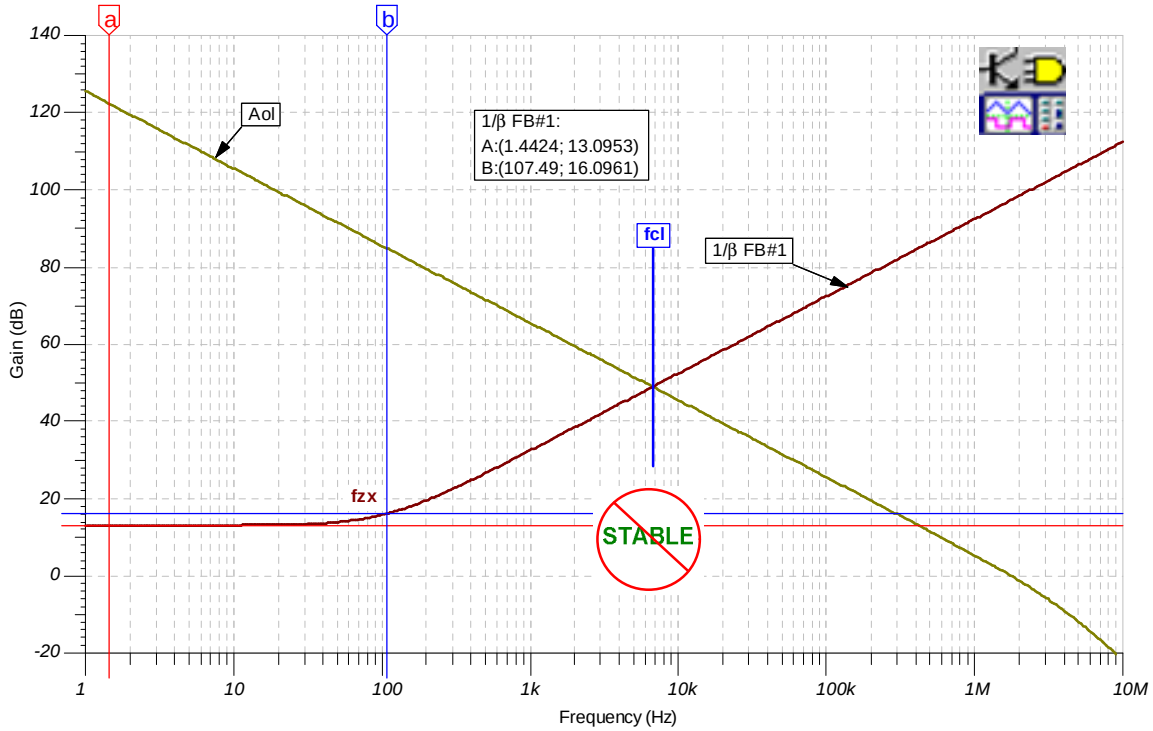


Fig. 10.51: FB#1 1/β Plot: CMOS RRO

In Fig. 10.52 we see loop gain analysis of our circuit using only FB#1 shows that we have close to zero phase margin at fcl where loop goes to zero. This is definite confirmation that we have an unstable circuit. The poles and zeros in the loop gain plot can be predicted, by inspection, from the FB#1 1/β plot on the Aol curve in Fig. 10.51.

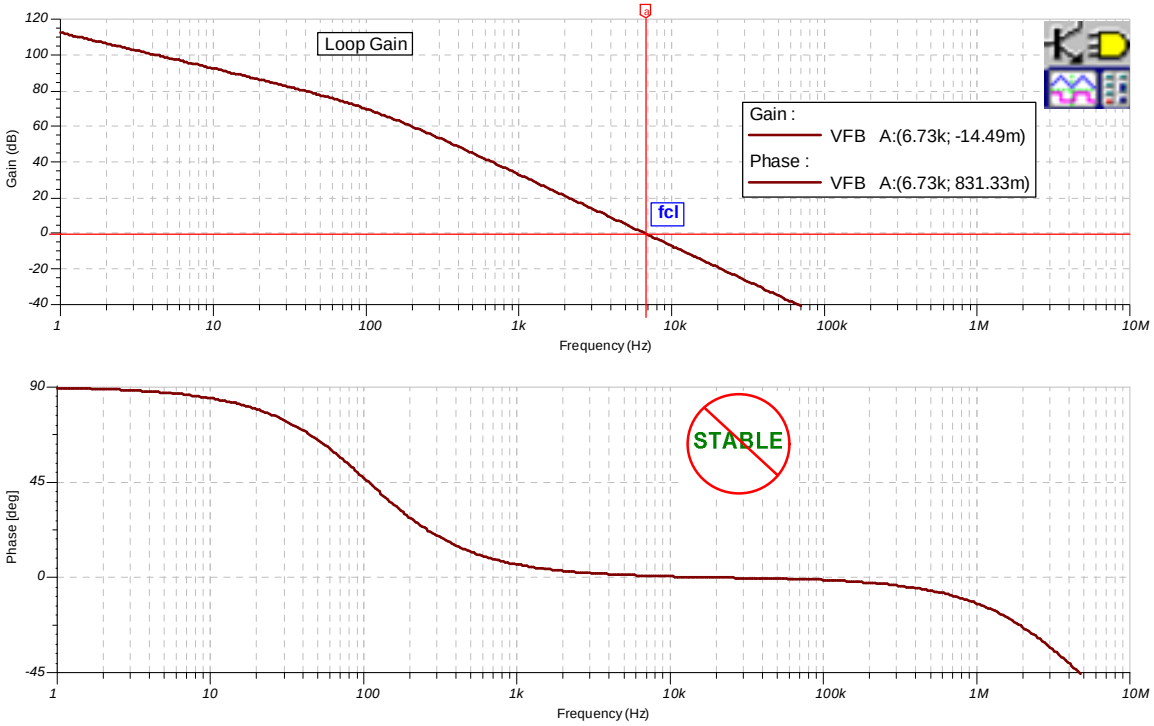


Fig. 10.52: FB#1 Loop Gain Analysis: CMOS RRO

In case we had any doubt, or if we built our reference buffer circuit with only FB#1 we could use our real world Transient Stability Test using the circuit in Fig. 10.53.

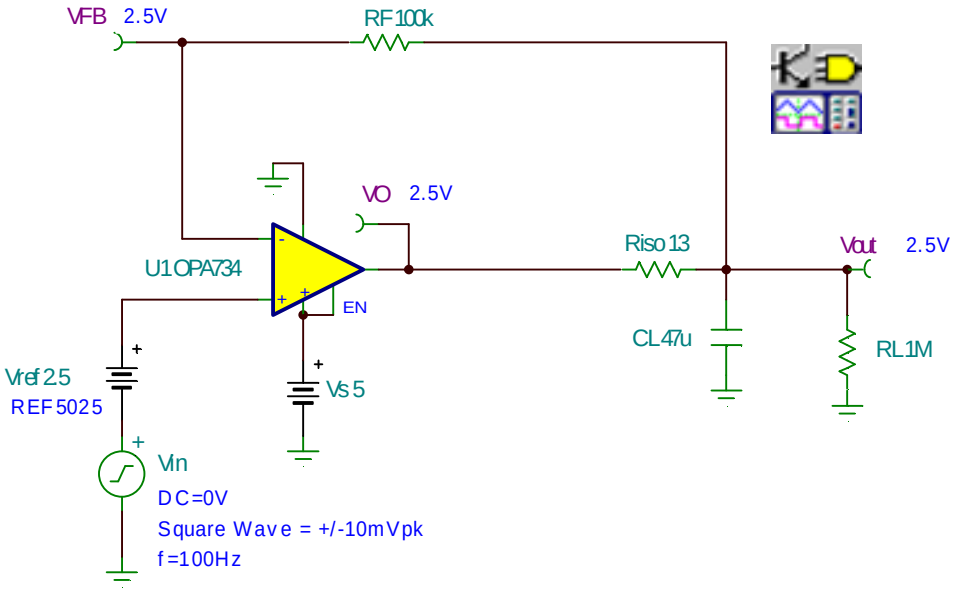


Fig. 10.53: FB#1 Transient Stability Test Circuit: CMOS RRO

The Transient Stability Test results in Fig. 10.54 coincide with both the 1/β on Aol Plot and Loop Gain plot in confirming we have an unstable circuit by using only FB#1 in our reference buffer configuration.

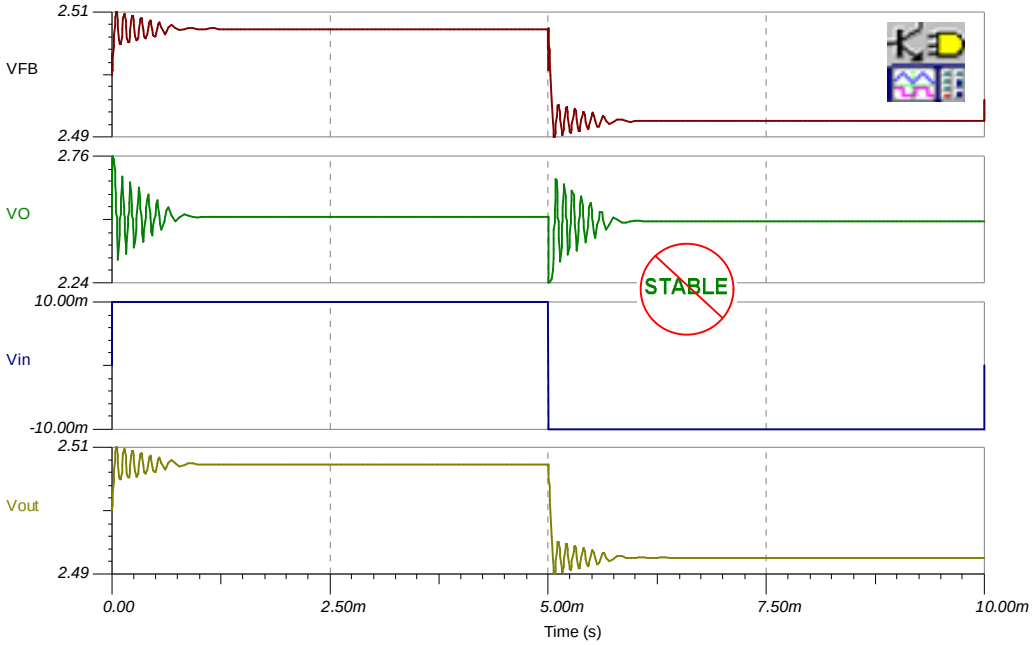


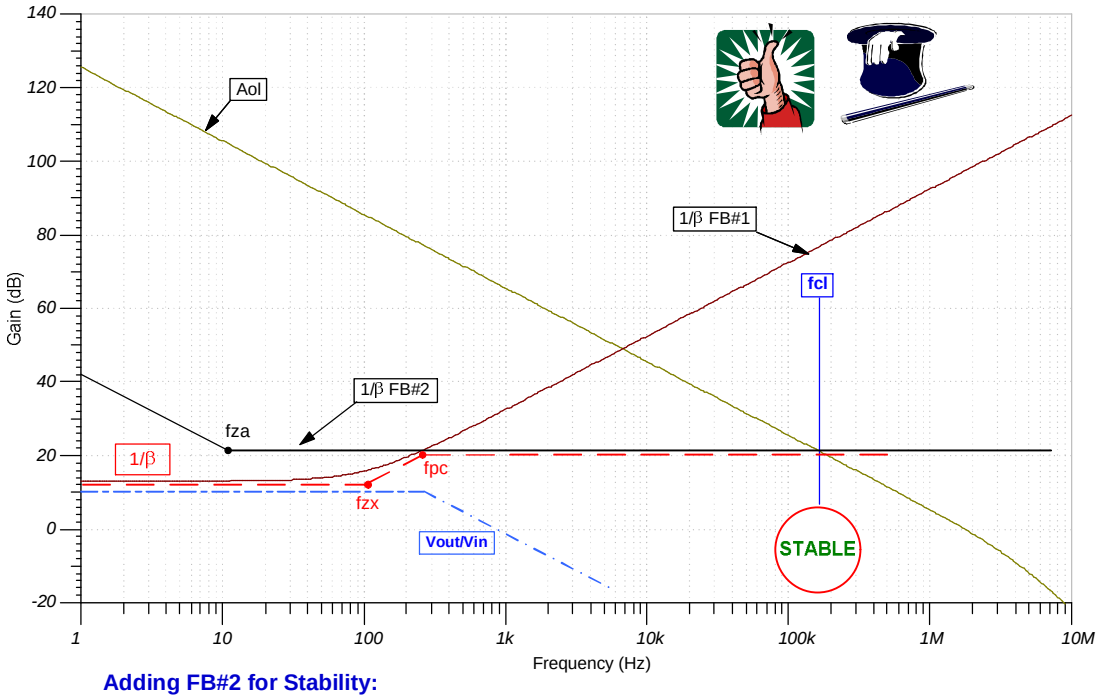
Fig. 10.54: FB#1 Transient Stability Test: CMOS RRO

Now we must figure out how to synthesize a solution to make our reference buffer with capacitive load stable. At this point we know the Aol curve and the FB#1 1/β as shown in Fig. 10.55. If we add FB#2 1/β as shown in Fig. 10.55 we can see a net 1/β which will be a stable circuit from our stability rule-of thumb for rate-of-closure at fcl.

In addition we will force fpc to be less than a decade from fzx in the 1/β curve to ensure phase margin will be better than 45 degrees for frequencies less than fcl. This is done by setting the high frequency portion of FB#2 1/β only +10dB greater than the low frequency 1/β of FB#1. fza is set to be at least one decade less than fpc to guarantee that as parameters shift in the real world we can avoid the BIG NOT. By inspection the net 1/β curve is formed from FB#1 1/β and FB#2 1/β by choosing the path with lowest 1/β.

Remember in dual feedback paths the largest voltage fed back from the op amp output to the negative input will dominate the feedback. The largest feedback voltage implies the largest β or the smallest 1/β.

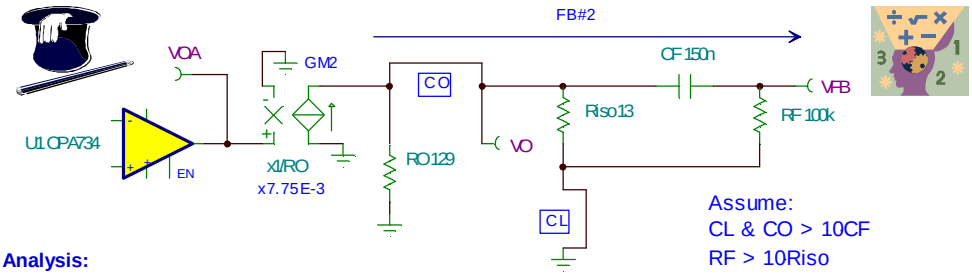
As a final point we see that the Vout/Vin transfer function is predicted to follow FB#1 until FB#2 dominates at which point Vout/Vin will roll off at -20dB/decade until FB#2 intersects with the Aol curve where it would then follow the Aol curve on down.



Adding FB#2 for Stability:
Set FB#2 High-f 1/β = +10db greater than FB#1 Low-f 1/β: best phase margin within loop gain bandwidth
Set fza in FB#2 1/β = 0.1fzx in FB#1 1/β

Fig. 10.55: FB#2 Graphical Analysis: CMOS RRO

As shown in Fig. 10.56 there are some key assumptions we will make that apply to almost all Riso w/Dual Feedback circuits. First we will assume that CL>10*CF which means that CL will become a short at high frequencies long before CF does. We will therefore short CL to eliminate FB#1 so as to analyze FB#2 independently. In addition we will assume that RF>10*Riso which implies that that RF has little to no effect as a load across Riso. From Fig. 10.56 and the detailed derivations in Fig. 10.57 we see FB#2 will have a pole at the origin with a zero, fza, at 19.41Hz caused by RF and CF. The high frequency 1/β portion of FB#2 is a ratio of Ro+Riso to Riso since CF and CL are both a short at high frequency. The derivation of FB#2 1/β is shown in the next slides with the results computer in the slide here. The high frequency 1/β for FB#2 is set to be 10.92 or 20.76dB with a pole at the origin and a zero at 10.6Hz.



FB#2 Analysis:
1/β pole at the origin
1/β zero set by RF and CF
High-f 1/β set by RO and Riso
CL = zero since we are using superposition
and only analyzing FB#2

Assume:
CL & CO > 10CF
RF > 10Riso

FB#2 1/β Calculation:

$$\beta = \frac{VFB}{VOA}$$

Pole: At Origin

$$1/\beta = \frac{VOA}{VFB}$$

Zero: $\frac{1}{2 \cdot \pi \cdot RF \cdot CF}$

Zero: $\frac{1}{2 \cdot \pi \cdot 100k \cdot 150n}$

Zero: fza = 10.6Hz

High Frequency β:
CO & CL = short
By Inspection:

$$1/\beta = \frac{RO+Riso}{Riso}$$ for High-f 1/β

$$1/\beta = \frac{129+13}{13}$$ for High-f 1/β

1/β = 10.92 or 20.76dB for High-f 1β

Fig. 10.56: FB#2 Analysis: CMOS RRO

The derivation for FB#2 β is shown on the left in Fig. 10.57. Since the 1/β is the reciprocal of β, FB#1 1/β calculation is easily derived as shown on the right in Fig. 10.57. We see that the pole, fpa, in the β derivation becomes the zero, fza, in the 1/β derivation.

FB#2 b Derivation:

FB#2 β Calculation:

$$VFB = \frac{VOA \cdot RF}{XCF + RF}$$

$$\frac{VFB}{VOA} = \frac{RF}{RF + \frac{1}{SCF}}$$

$$\frac{VFB}{VOA} = \frac{SCF \cdot RF}{SCF \cdot RF + 1}$$

$$\frac{VFB}{VOA} = \frac{S}{S + CF \cdot RF}$$

This Implies:
Zero: At Origin

$$\text{Pole: } fpa = \frac{1}{2 \cdot \pi \cdot RF \cdot CF}$$

Assume:
CL & CO > 10CF
RF > 10Riso

$$\beta = \frac{VFB}{VOA}$$

$$1/\beta = \frac{VOA}{VFB}$$

High Frequency β:
CO & CL = short
By Inspection:

$$\beta = \frac{Riso}{RO + Riso} : \beta \text{ High-f}$$

$$1/\beta = \frac{RO + Riso}{Riso} : 1/\beta \text{ High-f}$$

FB#2 1/b Derivation:

FB#2 1/β Calculation:

$$VFB = \frac{VOA \cdot RF}{XCF + RF}$$

$$\frac{VOA}{VFB} = \frac{RF + \frac{1}{SCF}}{RF}$$

$$\frac{VOA}{VFB} = \frac{SCF \cdot RF + 1}{SCF \cdot RF}$$

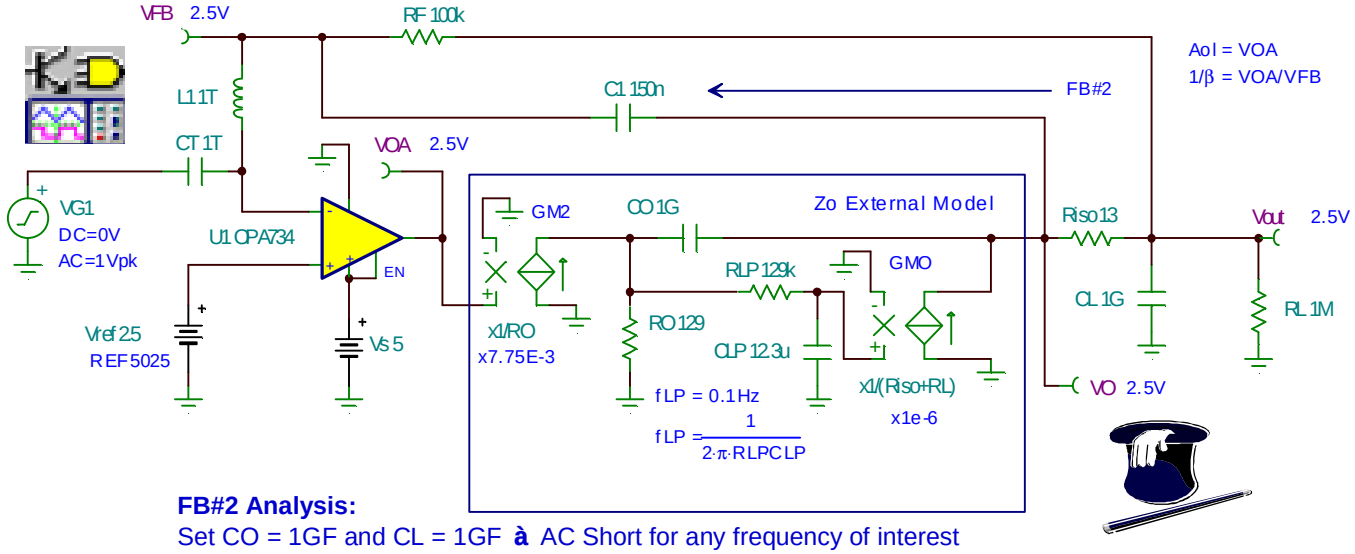
$$\frac{VOA}{VFB} = \frac{\frac{1}{S + CF \cdot RF}}{S}$$

This Implies:
Pole: At Origin

$$\text{Zero: } fza = \frac{1}{2 \cdot \pi \cdot RF \cdot CF}$$

Fig. 10.57: FB#2 Analysis: CMOS RRO

To check our first order analysis of FB#2 we can use the Tina SPICE circuit in Fig. 10.58. For ease of analysis we set CL to 10GF so it will be a short for any frequencies of interest but will still allow a proper DC operating point to be found by SPICE before the AC Analysis is performed.



FB#2 Analysis:
Set CO = 1GF and CL = 1GF **à** AC Short for any frequency of interest
Allows for GM2 and GMO to remain unchanged for this analysis

Fig. 10.58: FB#2 Analysis AC Circuit: CMOS RRO

The results of our Tina SPICE simulation are shown in Fig. 10. 59. The FB#2 1/β plot is as predicted by our first order analysis with fza= 10.6Hz and a high frequency 1/β of 23.78dB. We also plot the OP734 Aol curve to see how FB#2 will intersect with it at high frequency.

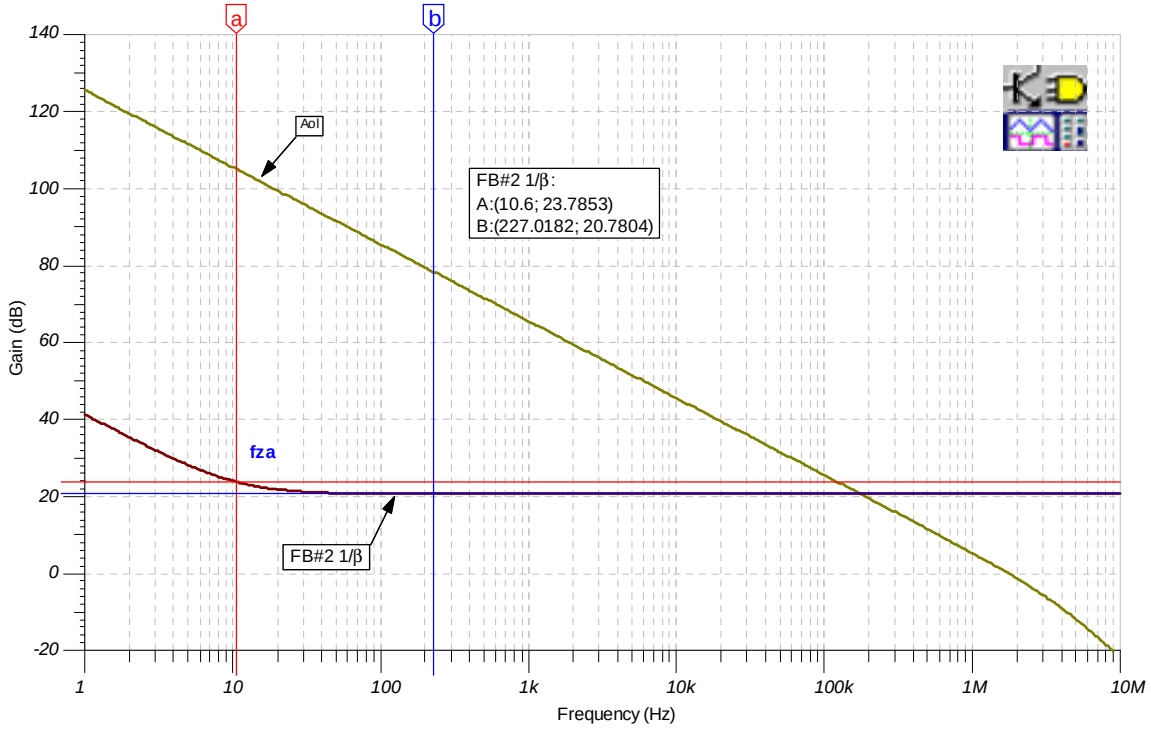


Fig. 10.59: FB#2 1/β Plot: CMOS RRO

We will analyze if the predicted superposition results of FB#1 and FB#2 will produce the desired net 1/β by using the Tina SPICE circuit shown in Fig. 10.60. This same circuit will allow us to plot Aol, net 1/β and Loop Gain.

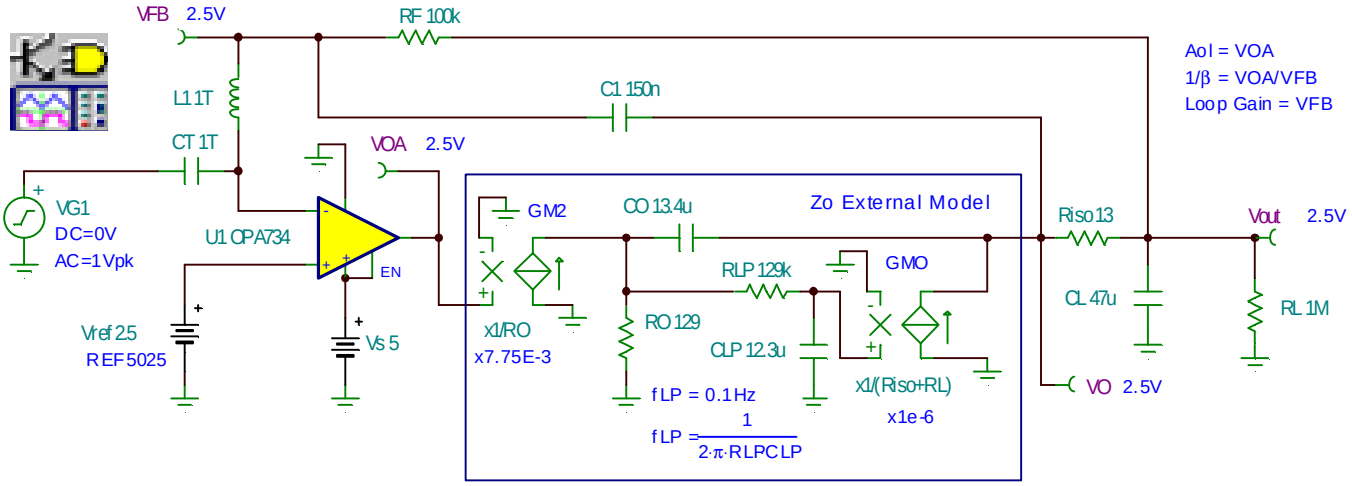


Fig. 10.60: Final Loop Gain Analysis Circuit: CMOS RRO

In Fig. 10.61 we see our analysis results confirm our predicted net 1/β plot. At fcl, where loop gain goes to zero, we see our expected 20dB/decade rate-of-closure.

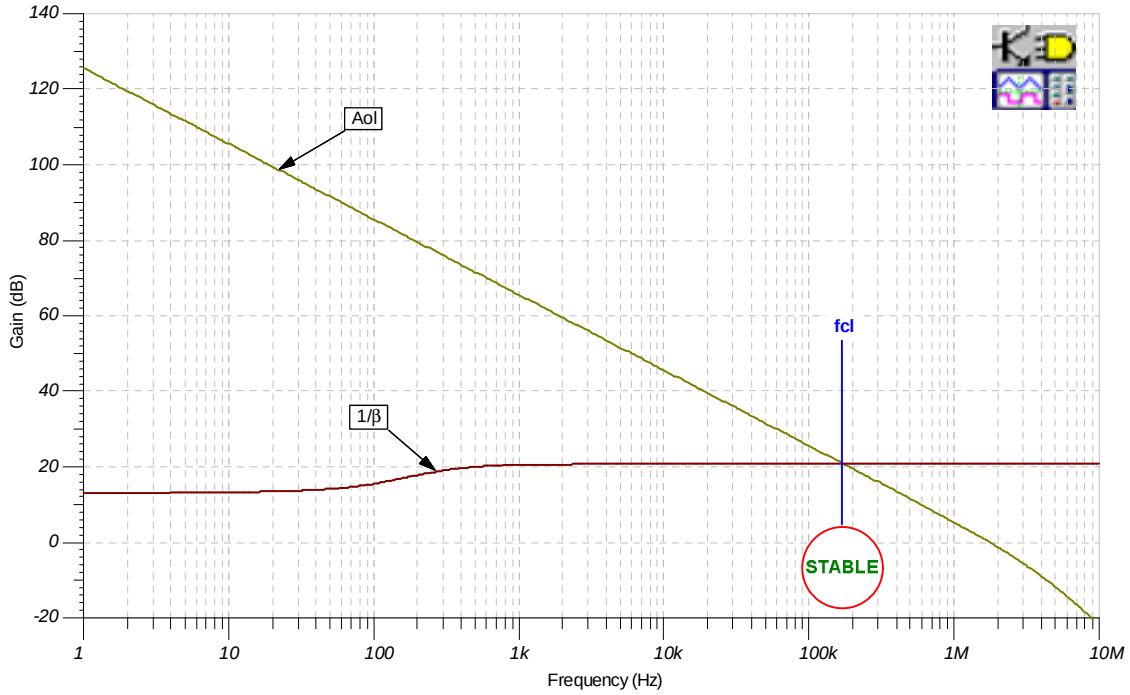


Fig. 10.61: Final Net 1/β: CMOS RRO

The loop gain phase plot for our final circuit, which uses FB#1 and FB#2, is shown in Fig. 10.62. Phase shift never dips to less than 66.54 degrees (as seen at 146.43Hz) for frequencies and at fcl, 172.64kHz, the phase margin is 87.79 degrees.

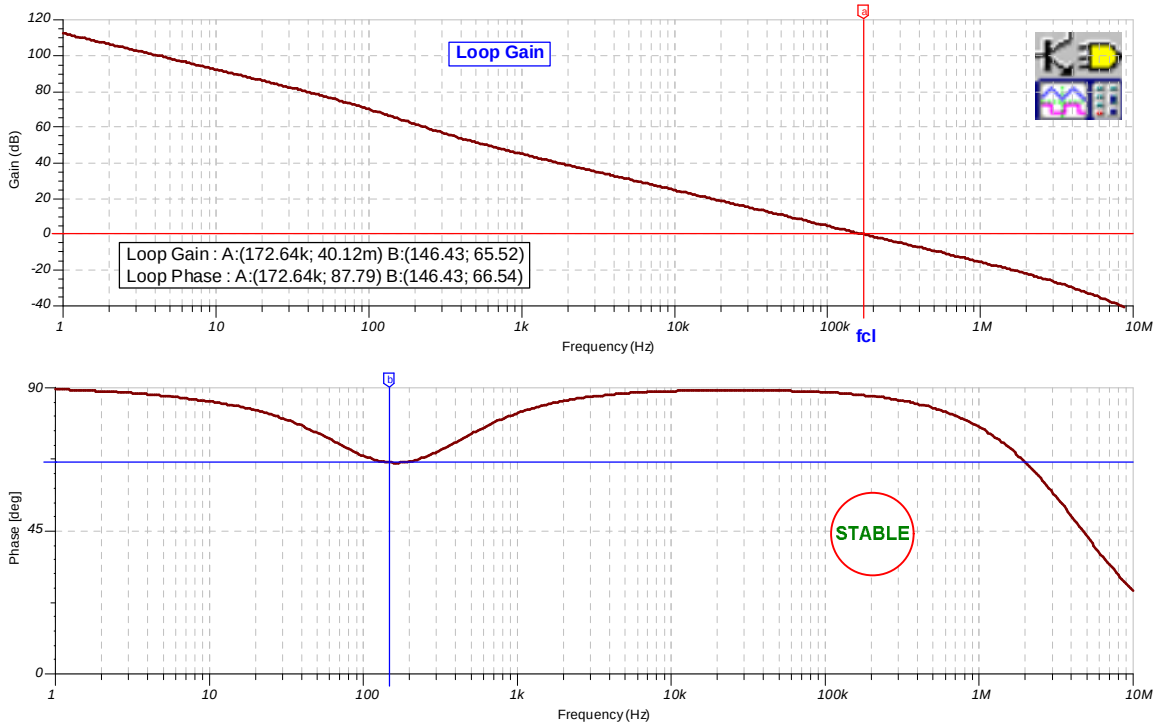


Fig. 10.62: Final Loop Gain Analysis: CMOS RRO

We will do our final check on our stabilized circuit by running a Transient Stability Test using the Tina SPICE circuit in Fig. 10.63.

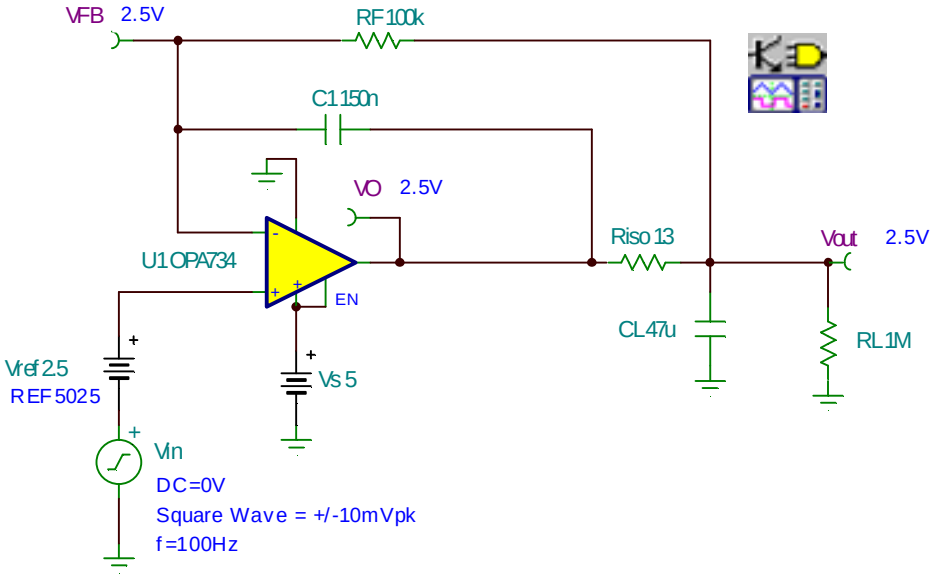


Fig. 10.63: Final Transient Stability Test Circuit: CMOS RRO

The results of our Transient Stability Test on our final circuit in Fig. 10.64 agrees with all of our other predictions resulting in a good, stable circuit we can put into production with confidence that we will not have any failures or real world operation anomalies.

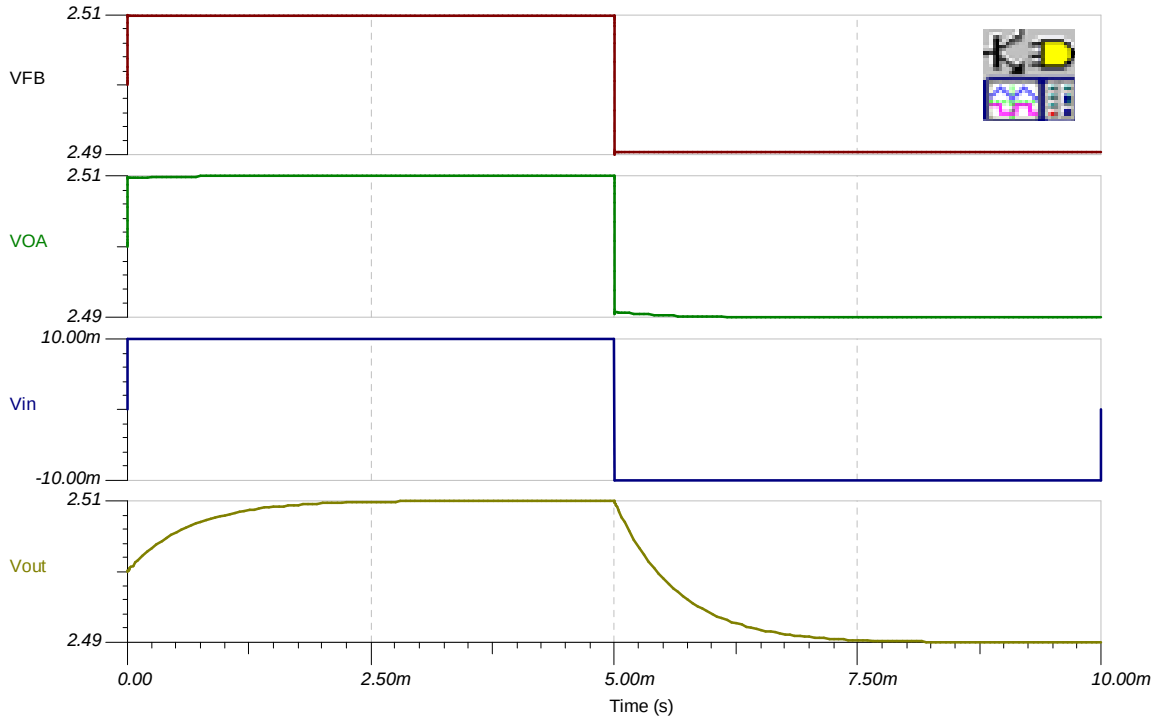


Fig. 10.64: Final Transient Stability Test: CMOS RRO

The Tina SPICE circuit in Fig. 10.65 will allow us to confirm if our prediction of Vout/Vin is correct.

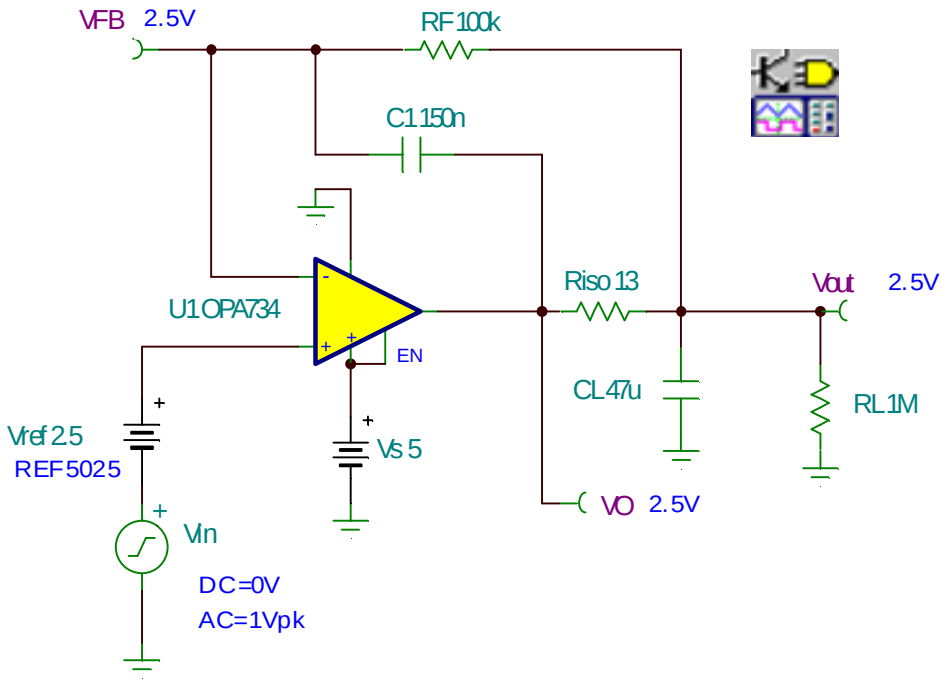


Fig. 10.65: Final Vout/Vin Transfer Function Circuit: CMOS RRO

In Fig. 10.66 we see that the results of our Vout/Vin test match our predicted first order results with a single pole roll off at 253.88Hz and a second pole appearing at about 167kHz where FB#2 intersects the OPA734 Aol curve.

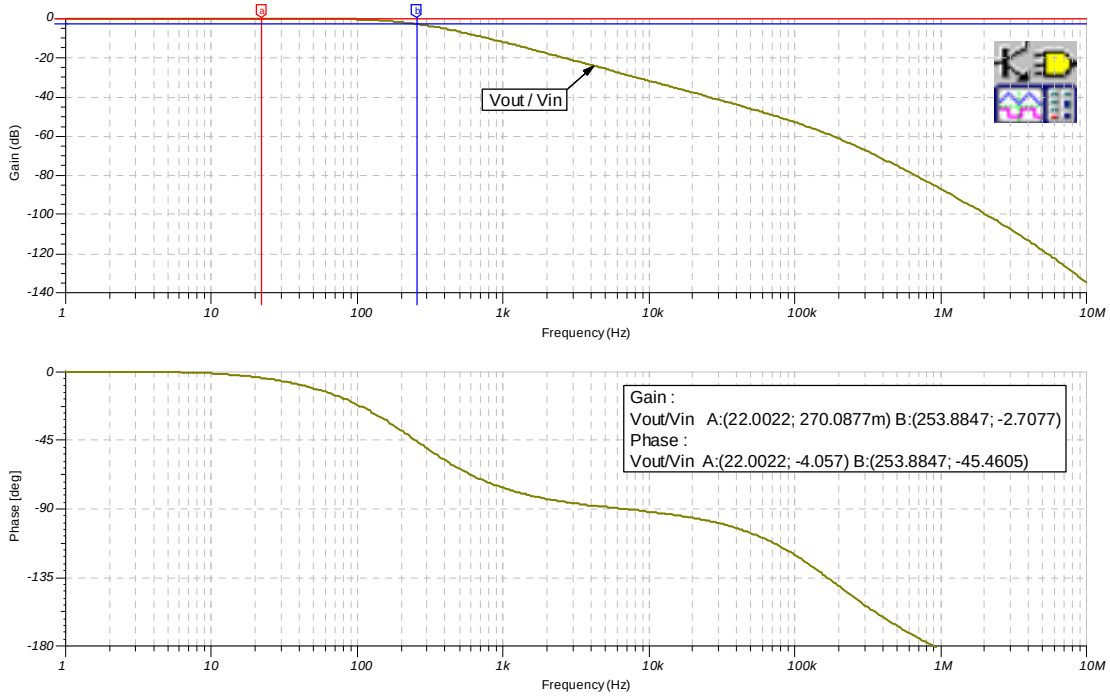


Fig. 10.66: Final Vout/Vin Transfer Function: CMOS RRO

Fig. 10.67 summarizes an easy to use step-by-step procedure to easily use the Riso w/Dual Feedback capacitive load stability technique on CMOS RRO output op amps.

FB#1 1/β Formulae:

$$\text{Zero: } fzx = \frac{1}{2\cdot\pi\cdot\left(\frac{CO\cdot CL}{CL+CO}\right)\cdot(Riso+RO)}$$

Note: $\frac{CO\cdot CL}{CL+CO}$ is series combination of CO and CL

$\frac{1}{\beta} = \frac{CL+CO}{CO}$ for Low-f 1/β

CO and CL form a Capacitive Divider

FB#2 1/β Formulae:

Assume:
CL & CO > 10CF
RF > 10Riso

Pole: At Origin

$$\text{Zero: } fza = \frac{1}{2\cdot\pi\cdot RF\cdot CF}$$

High Frequency 1/β:
CO & CL = short
By Inspection:

$1/\beta = \frac{RO+Riso}{Riso}$ for High-f 1/β

1) Measure Aol of Op Amp
2) Measure & Plot Zo of Op Amp
3) Determine CO and RO
4) Create Zo External Model
5) Compute FB#1 Low-f 1/b due to CO & CL
6) Set FB#2 High-f 1/b = +10dB higher than FB#1 Low-f 1/b
   (For best Vout/Vin transient response and least amount of phase shift within loop gain bandwidth)
7) Choose Riso from FB#2 High-f 1/b and RO
8) Compute FB#1 1/b fzx from CO, CL, Riso, RO
9) Set FB#2 1/b fza = 1/10 fzx
10) Choose RF and CF with practical values to yield fza
11) Run simulation with final values for Aol, 1/β, Loop Gain, Vout/Vin, Transient Analysis to confirm design
12) Check for Loop Gain Phase shift NOT to dip more than 135 degrees (>45 degrees phase margin)
13) For low noise applications:
    Check for flat Vout/Vin response to avoid gain peaking **à** noise peaking in Vout/Vin

Fig. 10.67: Riso w/Dual Feedback Compensation Procedure: CMOS RRO

About the Author:
After earning a BSEE from the University of Arizona in 1981, Tim Green has worked as an analog and mixed signal board/system level design engineer for over 24 years, including brushless motor control, aircraft jet engine control, missile systems, power op amps, data acquisition systems, and CCD cameras. Tim's recent experience includes analog & mixed-signal semiconductor strategic marketing. He is currently the Linear Applications Engineering Manager at Burr-Brown, a division of Texas Instruments, in Tucson, AZ. Tim can be reached at green_tim @ti.com