Operational Amplifier Stability
Part 4 of 15: Loop Stability Key Tricks and Rules-of-Thumb

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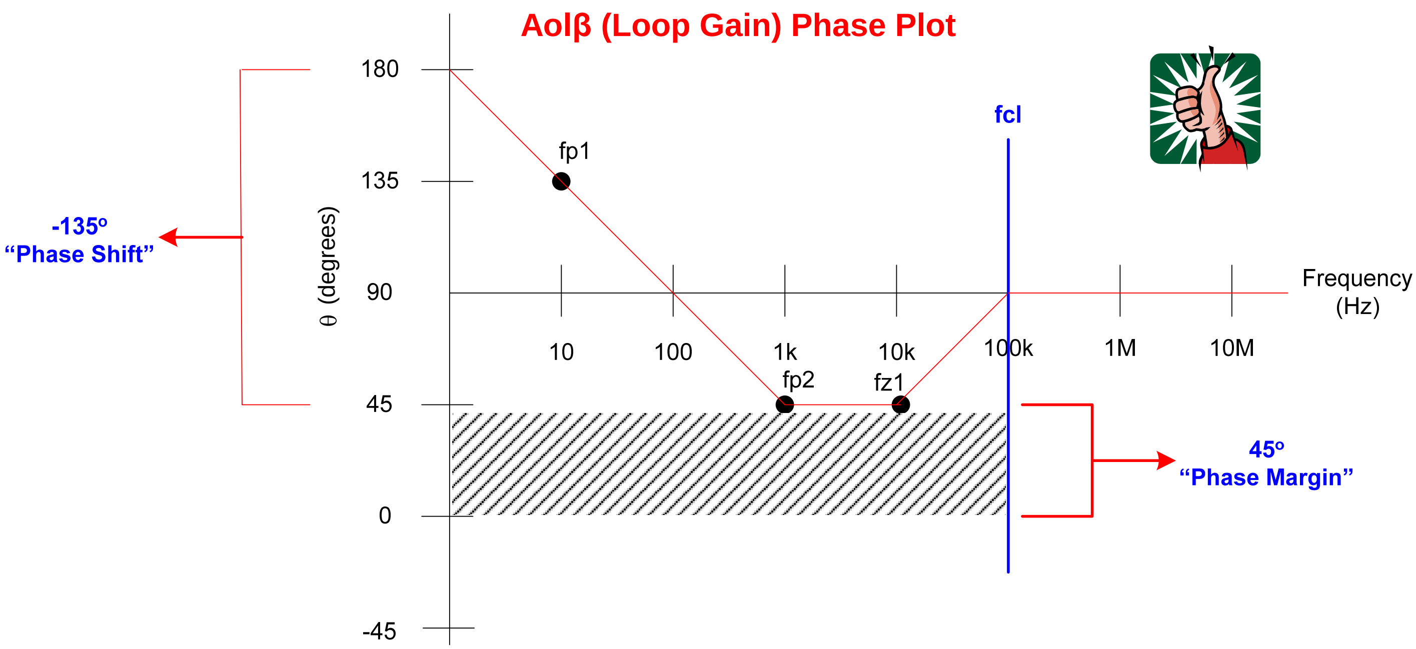
Part 4 of this series focuses on loop stability key tricks and rules-of-thumb. First we will discuss the 45 degree phase, loop gain bandwidth rule. The translation between poles and zeros in the Aol plot and 1/β plots to the loop gain plot, Aolβ, will be reviewed. Frequency "decade rules" will be discussed for loop gain stability. These decade frequency rules will be used for poles and zeros in 1/β, Aol, and Aolβ plots. We will present the magnitude "decade rule" for the op amp input network, ZI, and the feedback network, ZF. A technique will be developed for plotting dual feedback paths on a 1/β plot. A special case, the "BIG NOT", to avoid when using dual feedback paths will be explained. Finally an easy-to-use real world stability test will be presented. A combination of these key tools will allow us to methodically and easily stabilize a useful real world op amp application, with a complex feedback circuit, in Part 5 of this series.

Loop Gain Bandwidth Rule

The established loop stability criteria is less than a 180 degree phase shift at fcl, the frequency at which loop gain goes to zero. How close the phase shift is to a full 180 degrees phase shift at fcl is defined as phase margin. As detailed in Fig. 4.0 the recommended rule-of-thumb for real world circuits is to design for 135 degree phase shift (45 degree phase margin) throughout the loop gain bandwidth (f ≤ fcl). This allows for the real world cases of power-up, power-down and power-transient conditions where the op amp can have changes in its Aol curve which may result in transient oscillations. This is especially undesirable in power op amp circuits. This rule-of-thumb also allows for extra phase margin in the loop gain bandwidth to account for additional real world phase shifts due to parasitic capacitances and PCB layout parasitics. Also, phase margins less than 45 degrees within the loop gain bandwidth can result in undesired peaking in the closed loop transfer function. The lower the phase margin dip and the closer it is to fcl, the more pronounced the closed loop peaking will be.



Loop Stability Criteria: <-180 degree phase shift at fcl
Design for: ≤-135 degree phase shift at all frequencies <fcl
Why?:
Because Aol is not always "Typical"
Power-up, Power-down, Power-transient à Undefined "Typical" Aol
Allows for phase shift due to real world Layout & Component Parasitics

Fig. 4.0: Loop Gain Bandwidth Rule

Poles and Zeros Transfer Technique

Fig. 4.1 reminds us of the relationship between the Loop Gain plot and the Aol plot, with a 1/β plot included on it. This relationship allows us to use the manufacturer's Aol curve from an op amp data sheet and plot our feedback curve, 1/β, on it. From these two plots it is easy to infer what is going on in the Loop Gain plot and therefore easy to synthesize what we need to modify in our feedback for good stability. Think of the Loop Gain plot as a "open loop" plot. The Aol plot is already an open loop plot and therefore poles in the Aol plot are poles in the Loop Gain plot, and zeros in the Aol are zeros in the Loop Gain plot. The 1/β plot is a plot of small-signal AC closed loop gain. If we want to open the loop and look at the effects of the feedback network we will see an inverse relationship as we analyze the network. A simpler way to remember the translation between the 1/β plot and Loop Gain plot is that the Loop Gain plot is Aolβ and the closed loop feedback plot is 1/β. Therefore, since β, is the reciprocal of 1/β, poles in the 1/β plot will become zeros in the Loop Gain (Aolβ) plot and zeros in the 1/β plot will become poles in the Loop Gain plot (Aolβ).

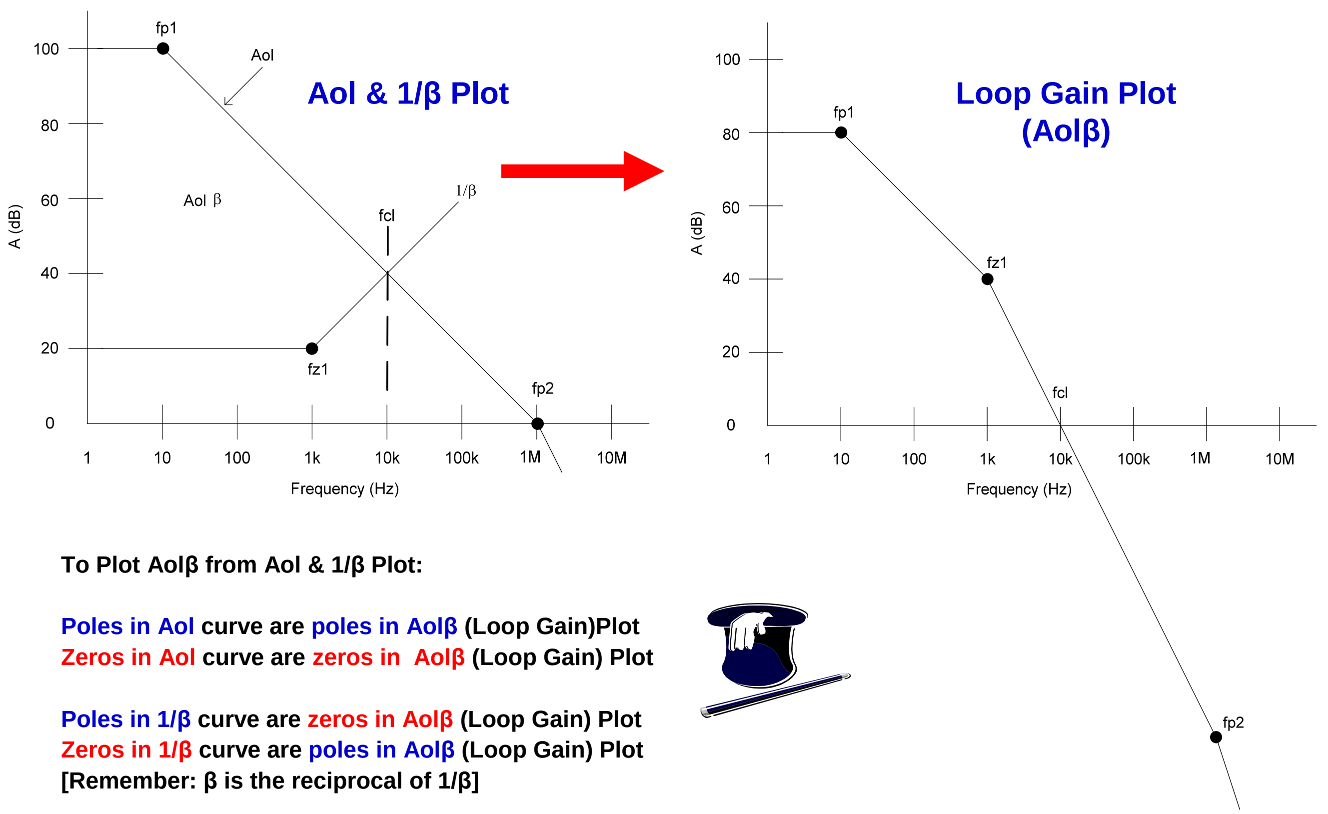


Fig. 4.1: Poles and Zeros Transfer Technique

Frequency Decade Rule

The "decade rules" for frequency in the Loop Gain plot are detailed in Fig. 4.2. These frequency decade rules will be used for 1/β plots and Aol plots as well as Aolβ, loop gain plots, which we can predict directly from the Aol and 1/β plots. For the circuit shown in this slide the Aol curve contains a second pole, fp2, around 100kHz due to the capacitive load, CL, and the op amp's R_O, the details of which will be presented in Part 6 of this series. We will create a feedback network that will meet our Loop Gain Bandwidth rule of 45 degrees margin for f≤ fcl. We will analyze and synthesize the feedback network using the 1/β plot and Aol plot with the knowledge of what we are doing to the Loop Gain plot, Aolβ. fp1 gives us a first pole at 10Hz in the Loop Gain plot which implies a -45 degree phase shift at 10Hz with phase shifting by -90 degrees at 100Hz. At 1kHz, fz1, a zero in the 1/β plot, we add a pole in the Loop Gain plot and another -45 degree phase shift at 1kHz. Our total phase shift now is -135 degrees at 1kHz. But if we continue on in frequency with just fz1 we will reach -180 phase shift at 10kHz!! So we add fp3, a pole in the 1/β plot, which is a zero in the Loop Gain plot at 10kHz (+45 Degre phase shift at 10kHz, with a +45 degree/decade slope above and below 10kHz). This keeps the phase shift at 1kHz to -135 degrees and flattens the phase plot to -135 degrees phase shift from 1kHz to 10kHz (remember poles and zeros have an effect a decade above and a decade below their actual frequency location). fp2 adds another pole in the Loop Gain plot at 100kHz since fp2 is from the Aol plot. Between 10kHz, where fp3 is, and 100kHz, where fp2 is, we expect no change in phase shift since fp3 is a Loop Gain plot zero and fp2 is a Loop Gain plot pole.

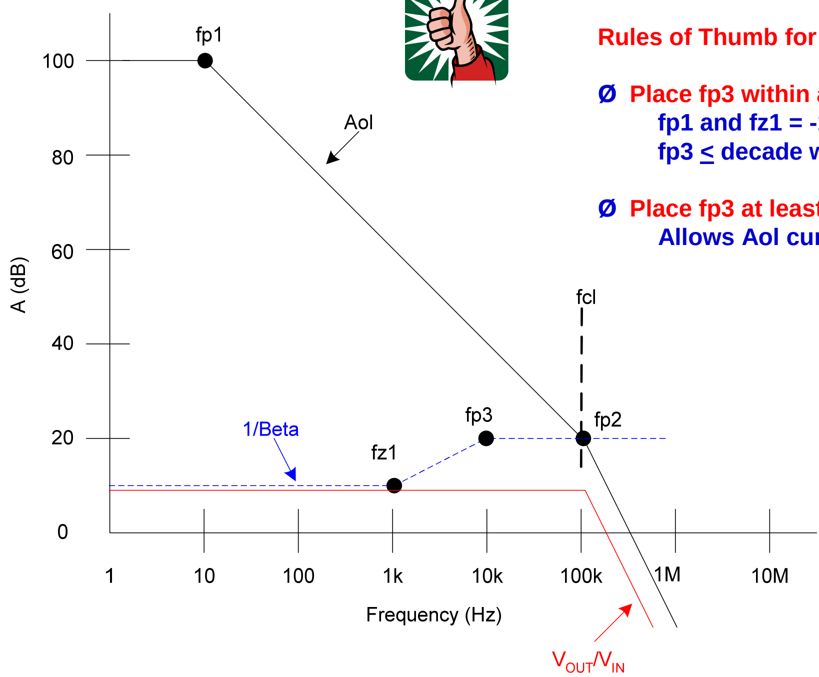
So if we keep poles and zeros spaced a decade away from each other they will keep the phase shift from dipping between them since each has an effect on one another a decade above and a decade below their location. The final key part of the Frequency Decade Rules for Loop Gain is to place fp3 no closer than a decade away from fcl. This allows for a decade shift in Aol towards the lower frequency range before we would be in a marginal stability condition. When pressed for a worst case Aol shift over process and temperature many IC Designers will sight a number of 2 to 1 (i.e. a 1MHz Unity Gain Bandwidth Op Amp may have that frequency shift from 500kHz to 2MHz). We prefer our decade rule because it is easy to remember and readily seen on a Bode plot. Extra phase margin design never got anyone in trouble. However, if one is pushed for bandwidth, stability, and performance the 2 to 1 rule is a good fallback.

The V_{OUT}/V_{IN} for this circuit is predicted to be flat until loop gain goes away at 100kHz, at which point it will then follow the Aol curve on down.

Loop Gain View: Poles: fp1, fp2, fz1; Zero: fp3

Rules of Thumb for Good Loop Stability:

- **Place fp3 within a decade of fz1**
  - **fp1 and fz1 = -135° phase shift at fz1**
  - **fp3 ≤ decade will keep phase from dipping further**
- **Place fp3 at least a decade below fcl**
  - **Allows Aol curve to shift to the left by one decade**



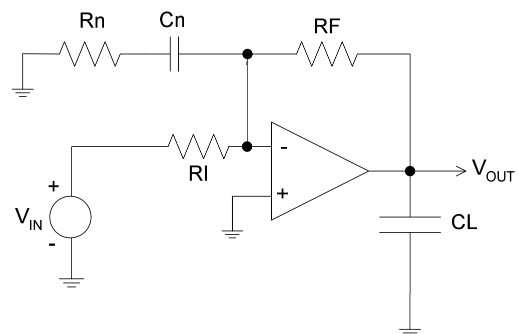


Fig. 4.2: Poles and Zeros Transfer Technique

Fig. 4.3 shows the first order hand analysis prediction for the Loop Gain phase plot of the circuit described in the Fig. 4.2. We add another pole, fp4, to our analysis at 1MHz to simulate a typical real world two pole op amp.

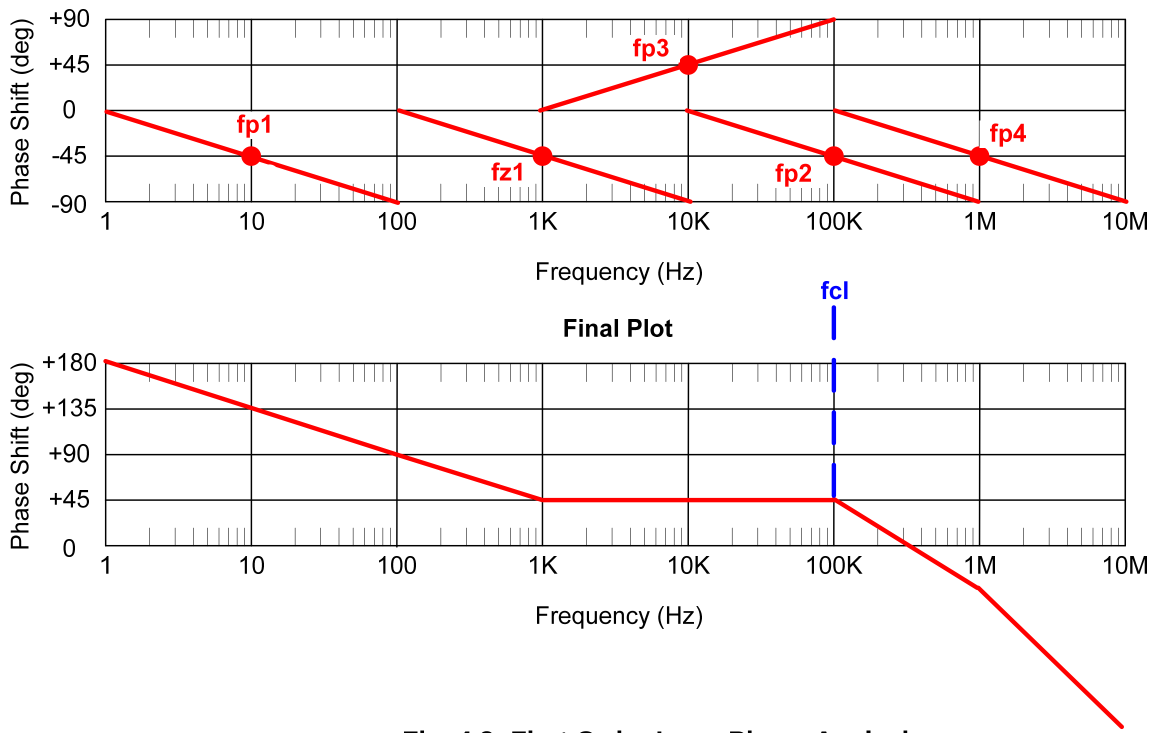


Fig. 4.3: First Order Loop Phase Analysis

To check our first order loop phase analysis we build our op amp circuit in Tina SPICE, as shown in Fig 4.4, and use the SPICE Loop Gain Test to measure the Aol plot and 1/β plot.

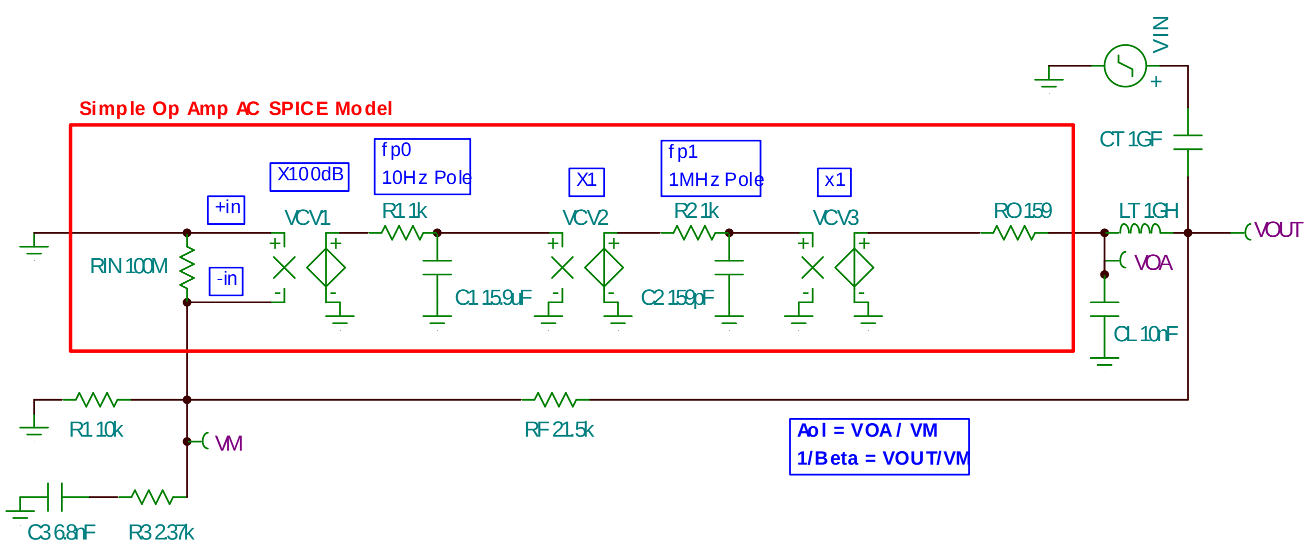


Fig. 4.4: Tina SPICE Circuit: SPICE Loop Gain Test

The Tina SPICE results for Aol and 1/β are shown in Fig 4.5 and correlate closely to our first order hand analysis.

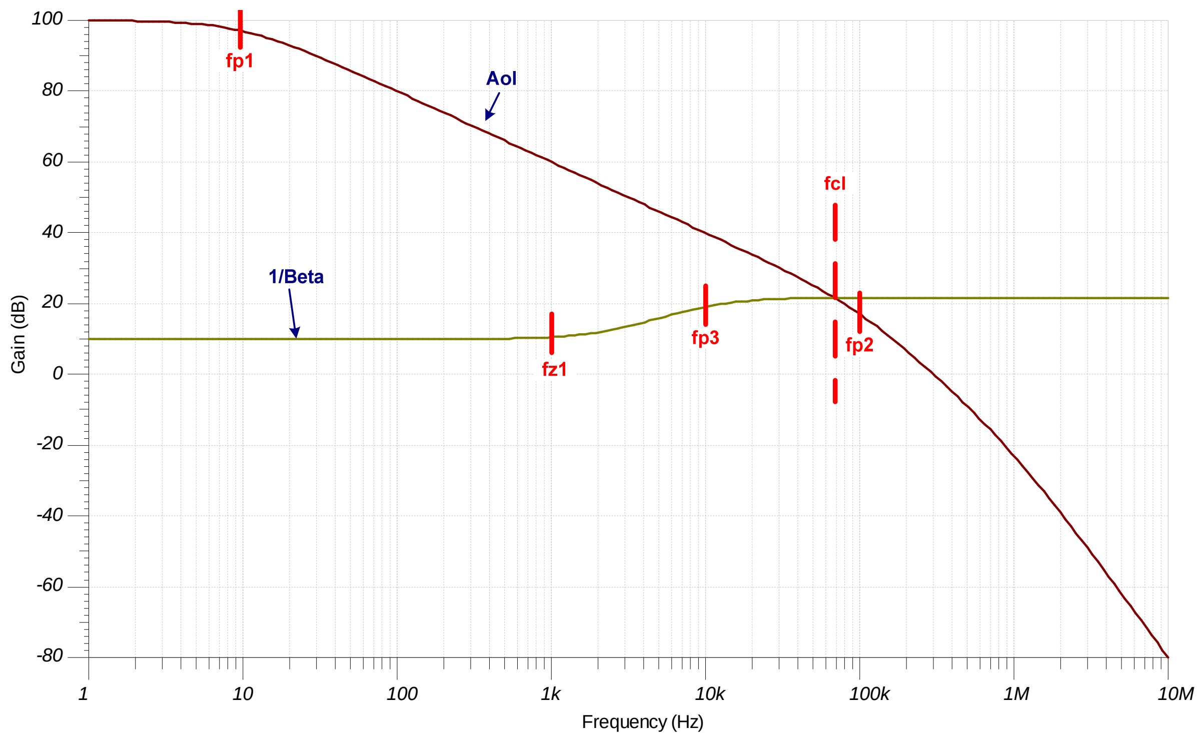


Fig. 4.5: Tina SPICE Circuit: Aolβ and 1/β

Our Tina SPICE simulation was also used to plot Loop Gain and Loop Phase. The Loop Phase plot is shown in Fig. 4.6 and is what we expected, based on our first order hand analysis.

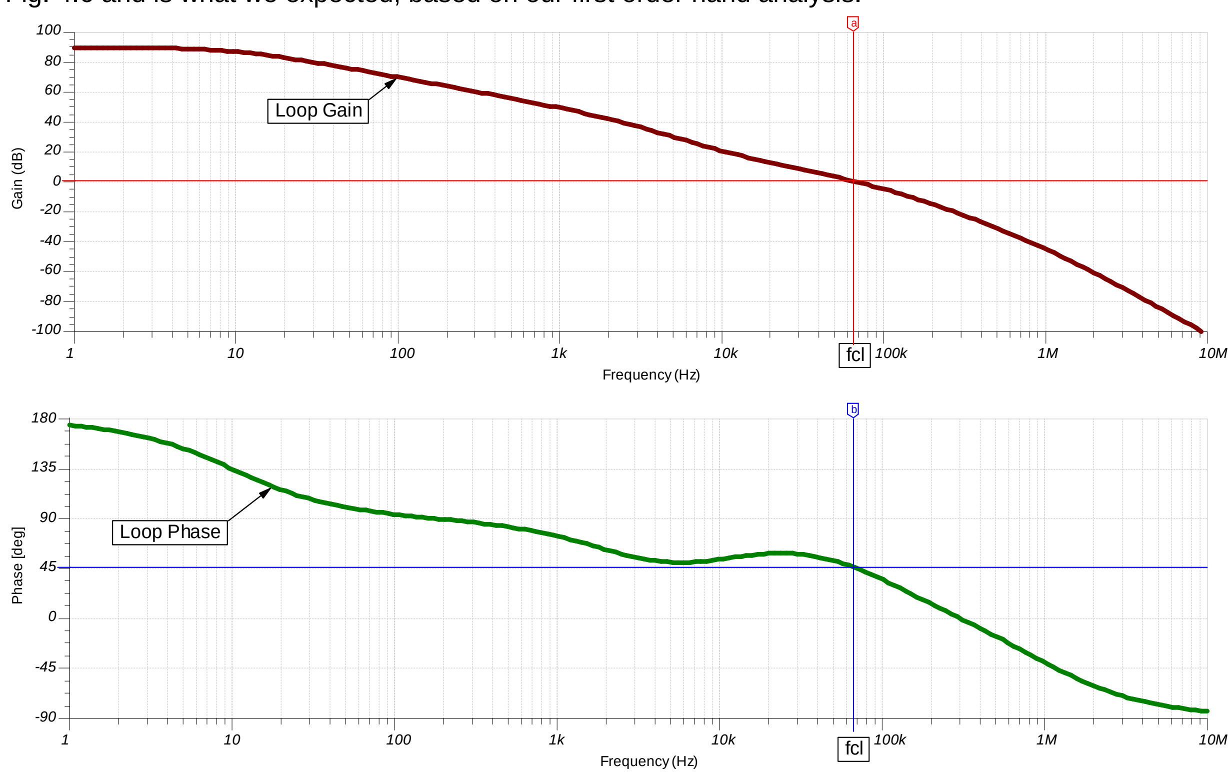


Fig. 4.6: Tina SPICE Circuit: Loop Gain and Loop Phase

To check if our V_{OUT}/V_{IN} predictions were correct we modify our Tina SPICE circuit to the one in Fig. 4.7 and simulate.

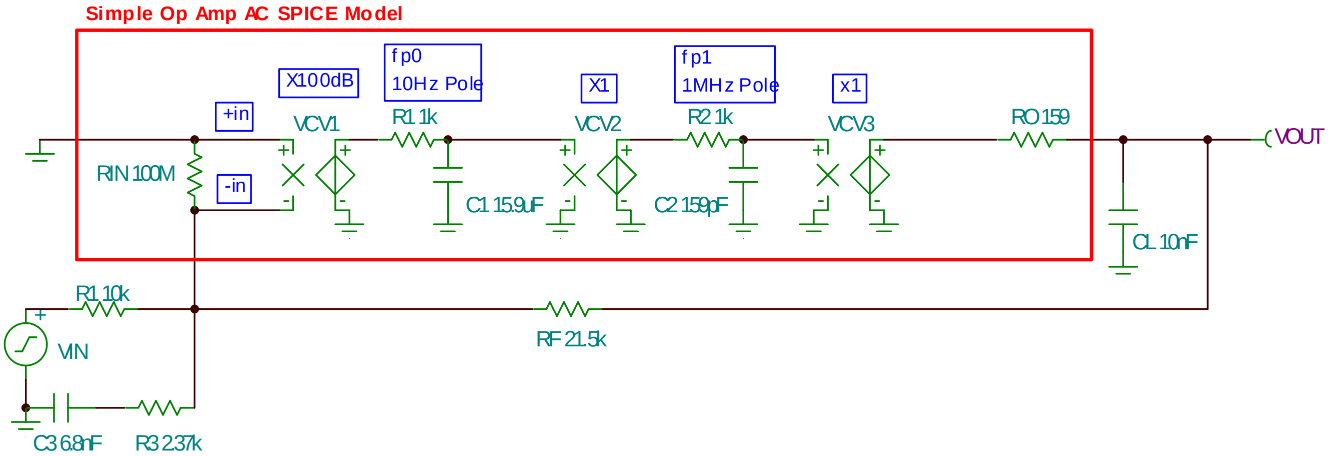


Fig. 4.7: Tina SPICE Circuit: V_{OUT}/V_{IN}

The Tina SPICE simulation results for V_{OUT}/V_{IN} are shown in Fig. 4.8. We see a slight rise in the V_{OUT}/V_{IN} transfer function starting at about 10kHz. This is due to the fact that the loop gain is beginning to be significantly reduced due to the Rn-Cn network. However, we are not far off from our first order, hand analysis prediction. A key point to note again is that V_{OUT}/V_{IN} is not always the same as 1/β.

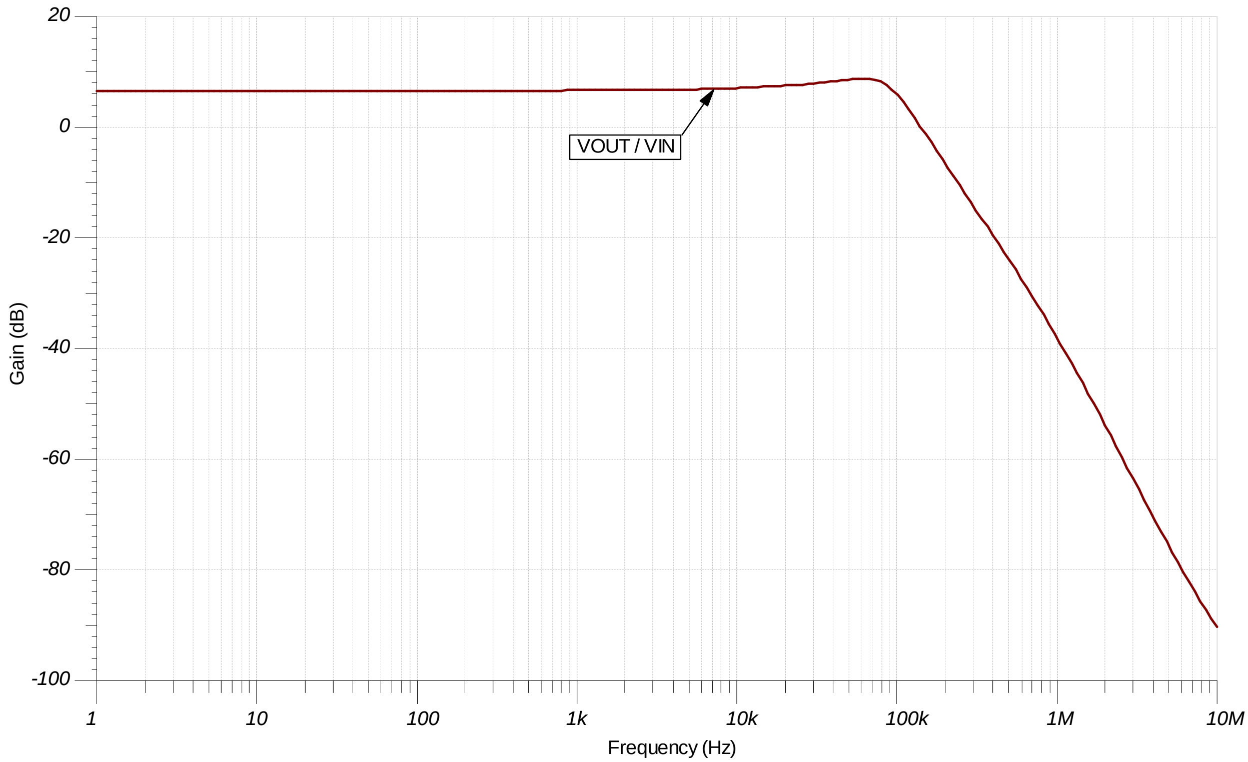


Fig. 4.8: Tina SPICE Circuit: V_{OUT}/V_{IN} Transfer Function

ZI and ZF Magnitude Decade Rule

We learned about the ZI and ZF networks in Part 2 of this series. The “decade rule” for magnitudes in the ZI, input network, is detailed in Fig. 4.9. If we scale Rn = RI/10 (Rn a “decade” in value less than RI) we can be assured that at high frequencies, when the impedance of Cn is a short, Rn will set the high frequency as RF/Rn. Scaling this way allows us to easily plot the dominant first order results for a 1/β plot. The other advantage to our decade rule for magnitudes is that it forces the pole/zero pair, fp and fz, we are adding to be within one decade of each other and therefore between fp and fz the phase shift will remain flat.

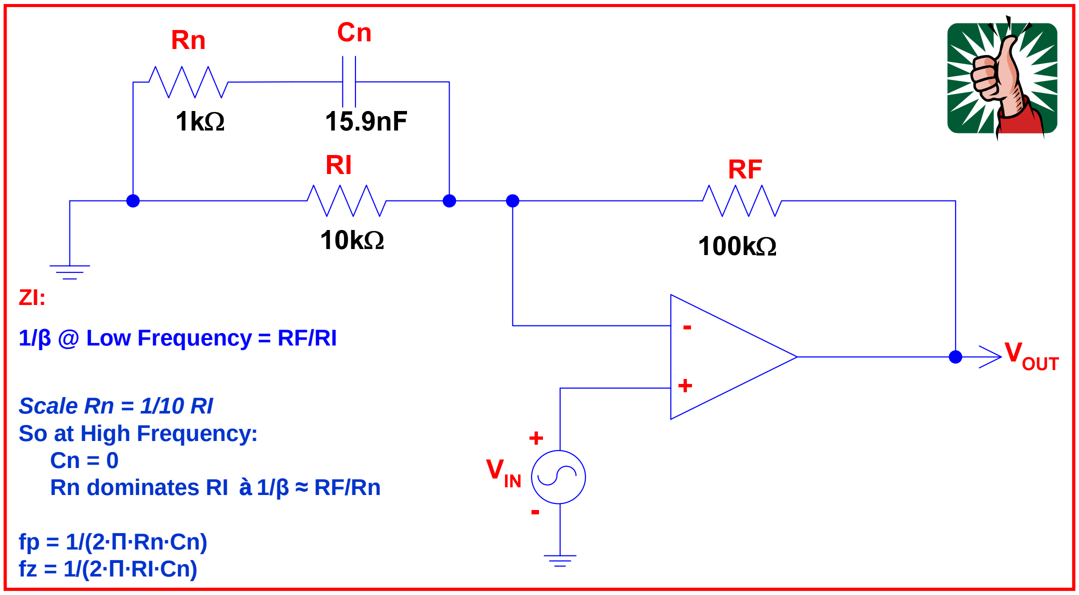


Fig. 4.9: ZI Magnitude Decade Rule

The “decade rule” for magnitudes in the ZF, feedback network, is detailed in Fig. 4.10. If we scale Rp = RF/10 (Rp a “decade” in value less than RF) we can be assured that at high frequencies, when the impedance of Cp is a short, Rp will set the high frequency as Rp/RI. Scaling this way allows us to easily plot the dominant first order results for a 1/β plot. As with the input network, ZI, the other advantage to our decade rule for magnitudes in ZF is that it forces the pole/zero pair, fp and fz, we are adding to be within one decade of each other and therefore between fp and fz the phase shift will remain flat.

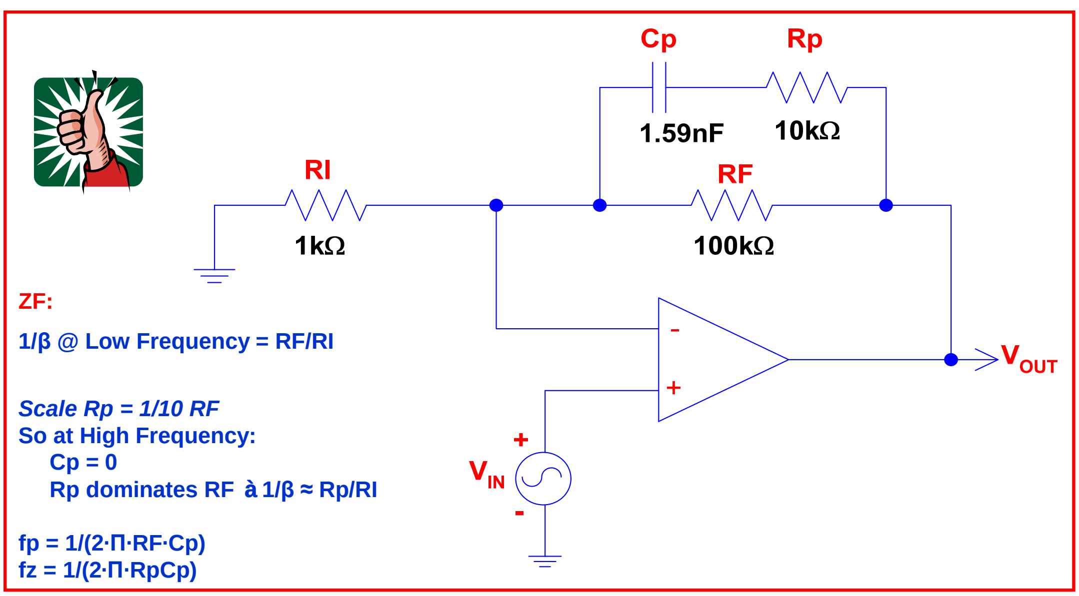


Fig. 4.10: ZF Magnitude Decade Rule

Dual Feedback Paths

We will see as we go forward in this series that often times the feedback circuits around op amps to guarantee good stability will require the use of more than one feedback path. To easily analyze and synthesize these types of multiple feedbacks we will call upon the superposition rule. Fig. 4.11 defines superposition. In our case we will analyze each effect independently and then use the dominant effect as the final one for our feedback.

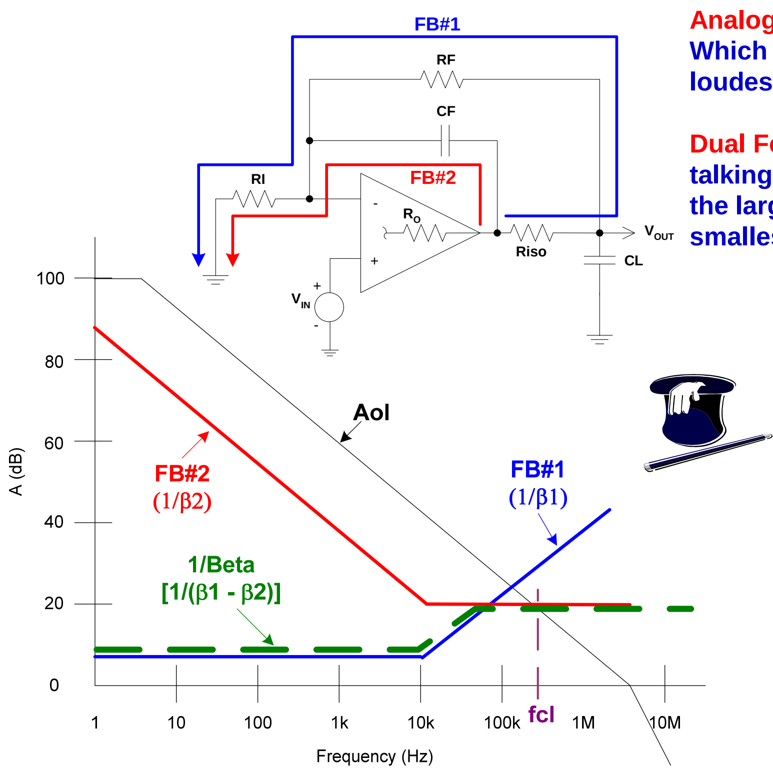
Superposition:

If cause & and effect are linearly related, the total effect of several causes acting simultaneously is equal to the sum of the effects of the individual causes acting one at a time.

From: Smith, Ralph J. Circuits, Devices, And Systems. John Wiley & Sons, Inc. New York. Third Edition, 1973.

Fig. 4.11: The Superposition Principle

In Fig. 4.12 we see an op amp circuit which uses two feedback paths. The first feedback path, FB#1, is out of the op amp, through Riso and CL back through RF and RI to the –input of the op amp. The second feedback, FB#2, is out of the op amp, through CF and back to the –input of the op amp. The equivalent 1/β plots for each of these feedbacks are plotted separately. The details of this derivation will presented later in a later part of this series. When more than one feedback path is used around an op amp the feedback path which feeds back the largest voltage to the op amp's input will become the dominant feedback path. This implies that if 1/β is plotted for each feedback that the feedback with the lowest 1/β at a given frequency will dominate at that point. Remember that the smallest 1/β implies the largest β and since $\beta = V_{FB}/V_{OUT}$, the largest β implies the most voltage fed back to the input of the op amp. An easy analogy to remember is that if two people are talking to you in one ear which person do you hear the easiest – the one talking the loudest! So the op amp will "listen" to the feedback path with the largest β or smallest 1/β. The net 1/β plot the op amp sees is the lower one at any frequency of FB#1 or FB#2.



Analogy: Two people are talking in your ear. Which one do you hear? The one talking the loudest!

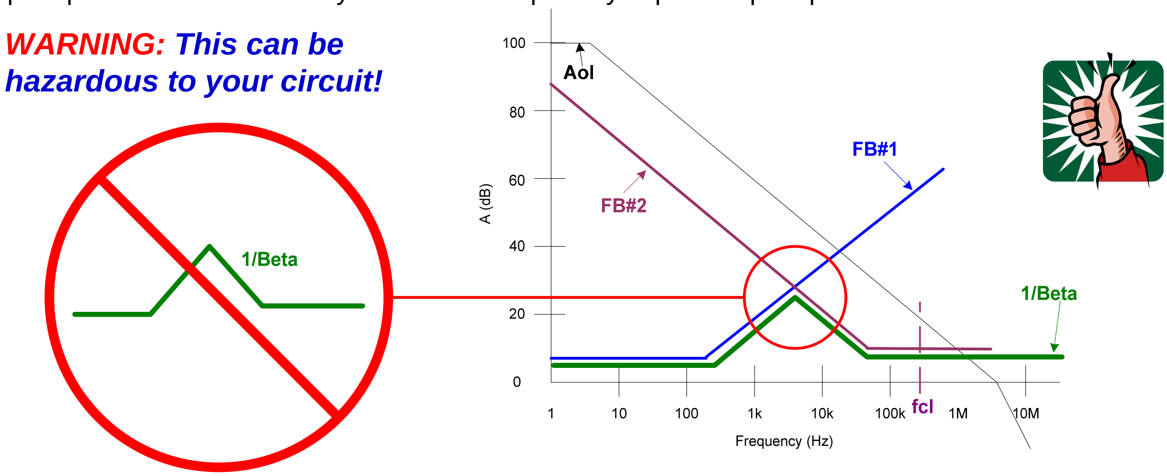
Dual Feedback: Op amp has two feedback paths talking to it. It listens to the one that feeds back the largest voltage ($\beta = V_{FB}/V_{OUT}$). This implies the smallest 1/β!

Dual Feedback Networks:

- **Use Superposition**
- **Analyze & Plot each FB# 1/β**
- **Smallest FB# dominates 1/β**
- **1/β = 1/(β1 – β2)**

Fig. 4.12: Dual Feedback Networks

When using dual feedback paths around an op amp there is one extremely important case to avoid – the "BIG NOT". As demonstrated in Fig. 4.13 there op amp circuits which can result in feedback paths that create the BIG NOT, which is seen in the net 1/β plot that contains a net 1/β slope which changes from +20db/decade to -20dB/decade abruptly. This rapid change implies a complex conjugate pole in the 1/β plot which is therefore a complex conjugate zero in the Loop Gain plot. Complex zeros and poles create a +/-90 degree phase shift at the frequency of the complex zero/complex pole. In addition the phase slope around a complex zero/complex pole can range from +/-90 degrees to +/-180 degrees in a narrow frequency band around the frequency location of the occurrence. Complex zero/complex pole occurrences can cause severe gain peaking in the closed loop op amp response. This can be very undesirable especially in power op amp circuits.



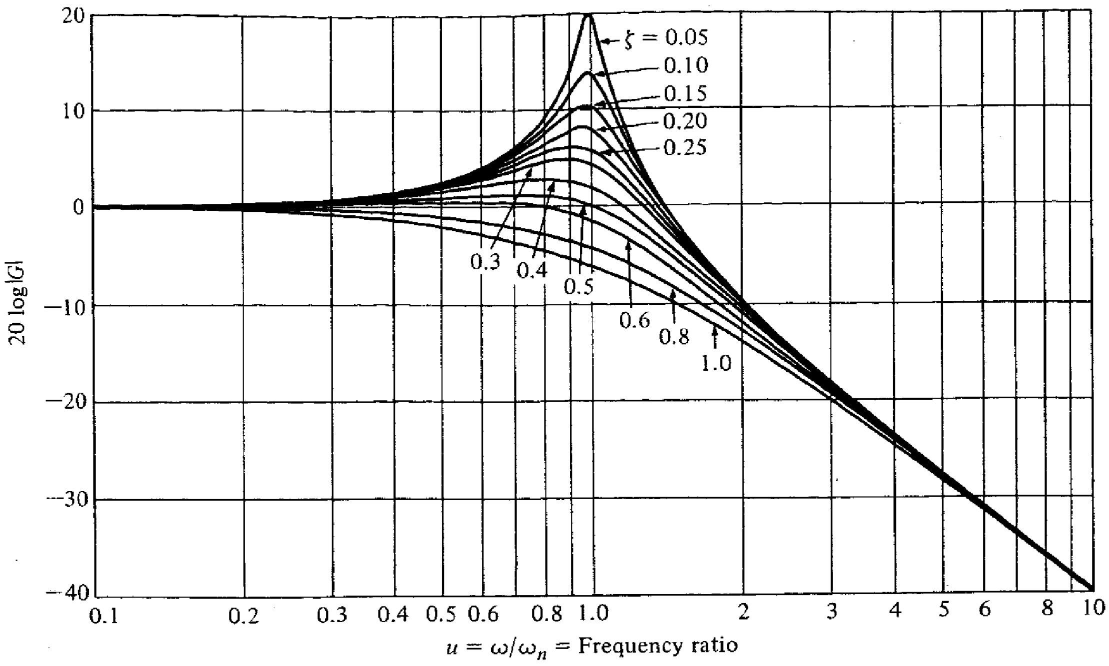
Dual Feedback and the *BIG NOT*:

1/β Slope changes from +20db/decade to -20dB/decade

- **Implies a "complex conjugate pole " in the 1/β Plot.**
- **Implies a "complex conjugate zero" in the Aolβ (Loop Gain Plot).**
- **+/-90° phase shift at frequency of complex zero/complex pole.**
- **Phase slope from +/-90°/decade slope to +/-180° in narrow band near frequency of complex zero/complex pole depending upon damping factor.**
- **Complex zero/complex pole can cause *severe* gain peaking in closed loop response.**

Fig. 4.13: Dual Feedback and the BIG NOT

The magnitude plot for a complex conjugate pole is shown in Fig. 4.14. for different damping factors. Irrespective of the damping factor the pole appears to be two-pole with a -40dB/decade slope. However, the phase will show a different story.

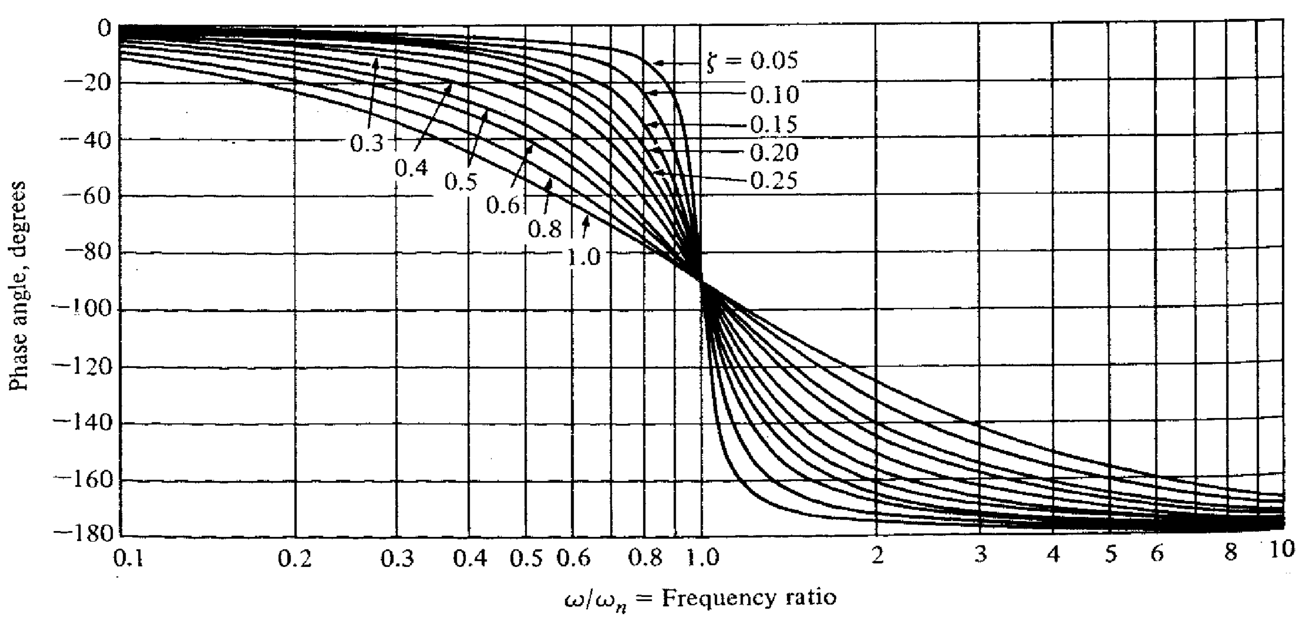


(a)

From: Dorf, Richard C. Modern Control Systems. Addison-Wesley Publishing Company. Reading, Massachusetts. Third Edition, 1981.

Fig. 4.14: Complex Conjugate Pole Magnitude Example

The phase plot for a complex conjugate pole is shown in Fig. 4.15. It is clear that, depending upon the damping factor, the phase shift can be dramatically different than one for a simple double pole which we would expect to be -90 degree shift at the frequency and a -90 degree/decade slope (damping factor=1).



(b)

From: Dorf, Richard C. Modern Control Systems. Addison-Wesley Publishing Company. Reading, Massachusetts. Third Edition, 1981.

Fig. 4.15: Complex Conjugate Pole Phase Example

Real World Stability Test

Once we complete our first order hand analysis and then do a SPICE simulation as a sanity check we will build our op amp circuit. It would be convenient to have an easy way to confirm if our real world phase margin is what we predicted by analysis. Most real world op amp circuits are dominated by a two pole, second order, system response. Refer to Fig. 4.16. A typical op amp Aol has a low frequency pole in the 10Hz to 100Hz region and another high frequency pole at its unity gain crossover frequency or soon after that in frequency. If pure resistive feedback is used we can see that the loop phase plot would demonstrate the effects of a two pole system. For more complicated op amp circuits the resultant loop gain and loop phase plots are usually dominated by a two pole response. Closed loop behavior of a second order system is well defined and offers us a powerful technique for a real world stability check.

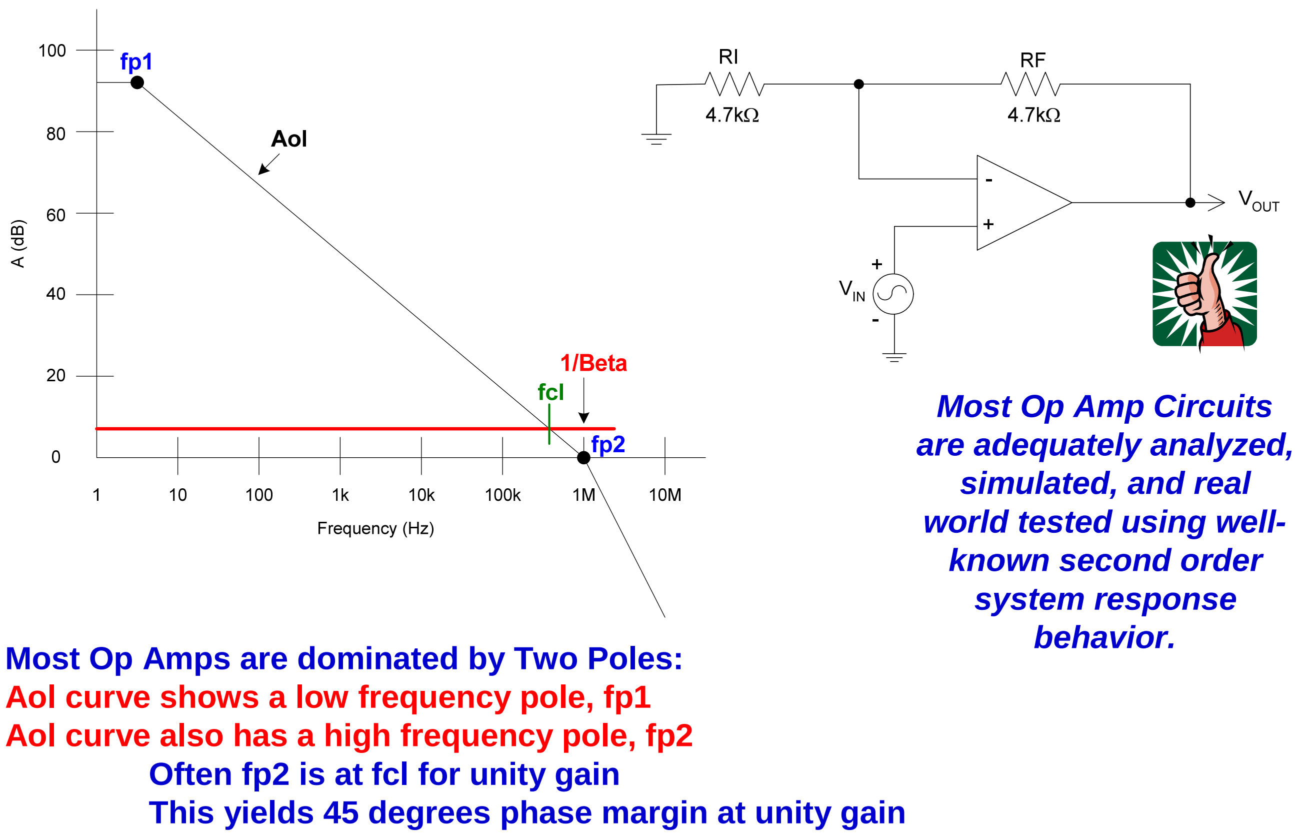
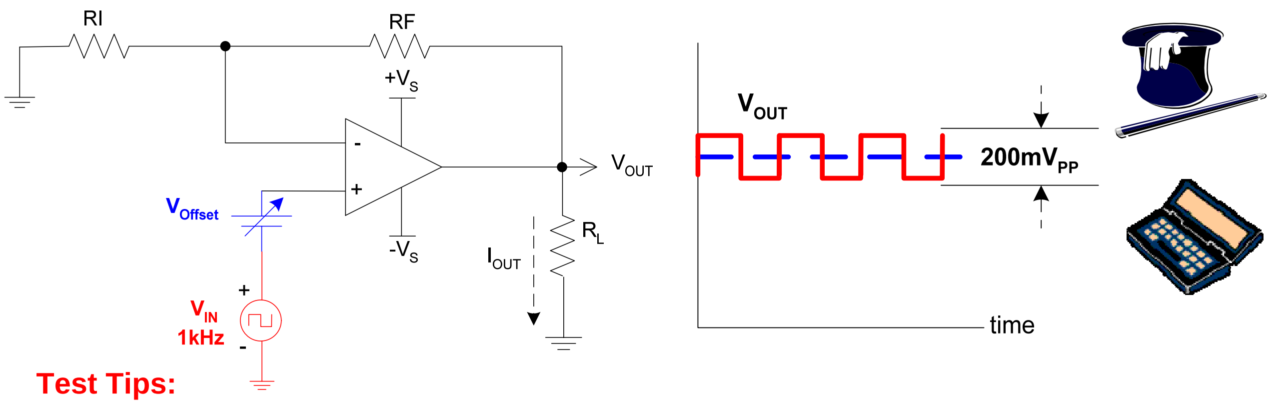


Fig. 4.16: Op Amp Circuits' AC Behavior

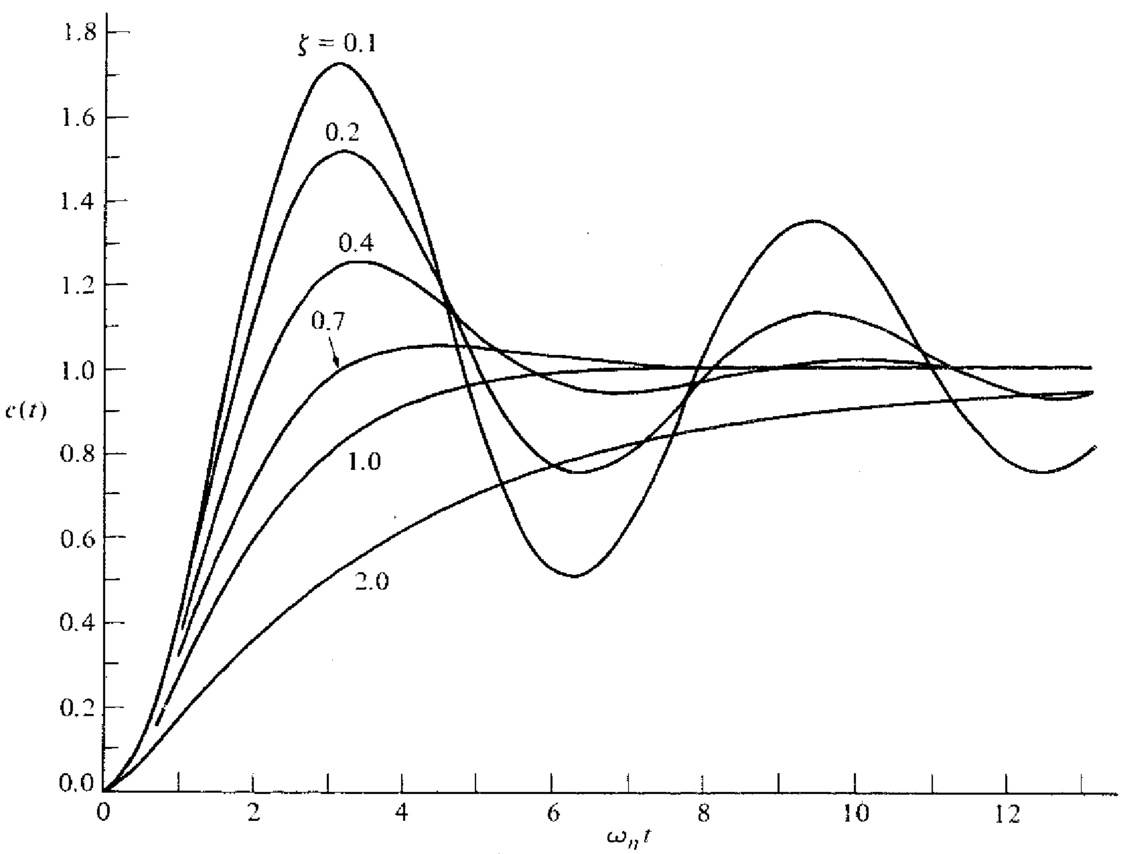
Fig. 4.17 details the Transient Real World Stability Test. A small amplitude square wave is injected into the closed loop op amp circuit as the VIN source. A frequency is chosen well within the loop gain bandwidth but also high enough to make triggering with an oscilloscope easy. 1kHz is a good test frequency for most applications. V_{IN} is adjusted such that V_{OUT} is 200mVpp or less. We are interested in the small signal AC behavior of the circuit to look for AC stability. To that end we do not want a large signal swing on the output which could also contain large signal limitations such as slew rate or output current limitations or output stage voltage saturation. V_{offset} provides a mechanism to move the output voltage up and down through its entire output voltage range to look for AC stability under all operating point conditions. For many circuits, especially those that drive capacitive loads, the worst case for stability is when the output is near zero (for a dual supply op amp application) and there is little or no DC load current since this results in the highest value of R_O, the op amp's open loop small signal resistance. Record the amount of overshoot and ringing on the square wave output and compare it to the 2nd Order Transient Curves in Fig. 4.18. From the curve that matches your measured circuit the closest note the respective damping ratio. Find this respective damping ratio in y-axis of the 2nd Order Damping Ratio vs Phase Margin curve in Fig. 4.19. The x-axis contains the phase margin of the second order circuit.



Test Tips:

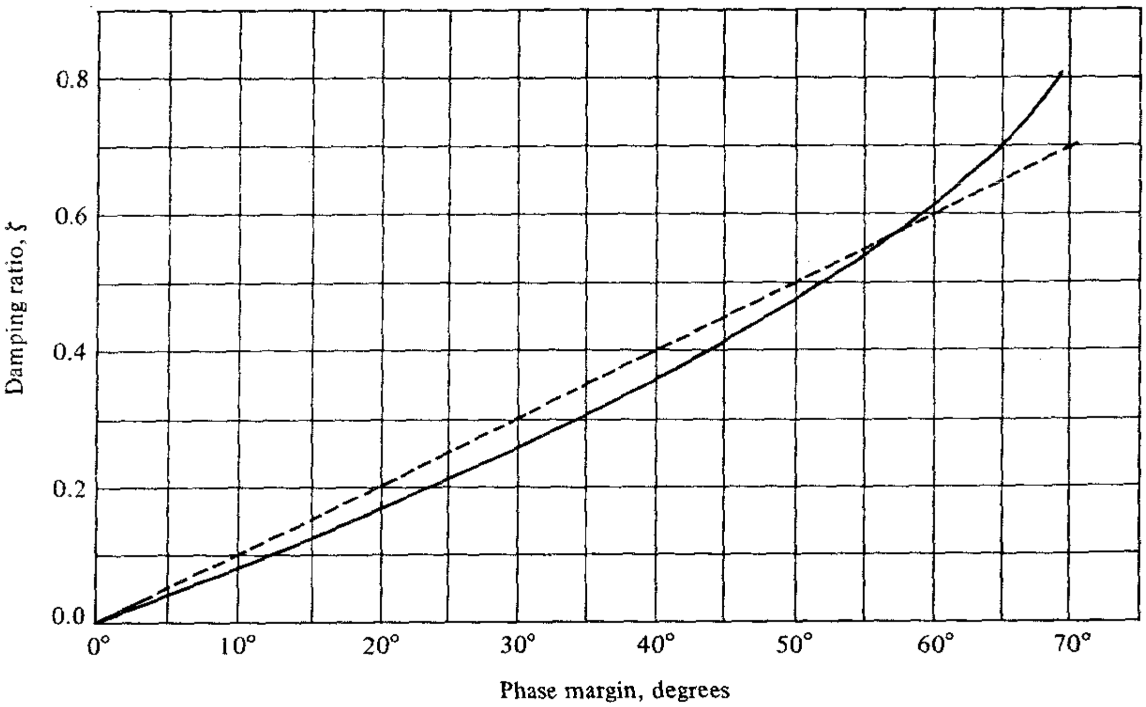
- Ø Choose test frequency << fcl
- Ø Adjust V_{IN} amplitude to yield "Small Signal" AC Output Square Wave
- Ø Worst case is usually when $V_{Offset} = 0$ à Largest Op Amp R_O ($I_{OUT} = 0$)
- Ø Use V_{Offset} as desired to check all output operating points for stability
- Ø Set scope = AC Couple & expand vertical scope scale to look for amount of overshoot, undershoot, ringing on V_{OUT} small signal square wave

Fig. 4.17: Transient Real World Stability Test



From: Dorf, Richard C. Modern Control Systems. Addison-Wesley Publishing Company. Reading, Massachusetts. Third Edition, 1981.

Fig. 4.18: 2nd Order Transient Curves



From: Dorf, Richard C. Modern Control Systems. Addison-Wesley Publishing Company. Reading, Massachusetts. Third Edition, 1981.

Fig. 4.19: 2nd Order Damping Ratio versus Phase Margin

References:
Frederiksen, Thomas M. *Intuitive Operational Amplifiers*, From Basics to Useful Applications, Revised Edition. McGraw-Hill Book Company. New York, New York. 1988

Dorf, Richard C. Modern Control Systems. Addison-Wesley Publishing Company. Reading, Massachusetts. Third Edition, 1981

Smith, Ralph J. Circuits, Devices, And Systems. John Wiley & Sons, Inc. New York. Third Edition, 1973.