CHIP MSP430F5419A

QUESTION:

Test Condition:
MSP430F5419A HAVE 4 UART module.
The XT2 as the clock source.

1>UART0123 work good when DCOCLKDIV as clock source.
2> Only the UART1 can not working when select XT2 as clock source.

When the UART1 enable will cause SMCLK(P11.2) output 1MHz,
The other UART fail the same time.

3> Only 3 UART port can be used when select XT2 as clock source.

	STATUS	Clock source	P11.2= SMCLK	baudrate	Communication function
			1.034MHZ		
UART0	enable	DCOCLKDIV		115200	OK
UART1	enable	DCOCLKDIV		115200	OK
UART2	enable	DCOCLKDIV		115200	OK
UART3	enable	DCOCLKDIV		115200	OK

	STATUS	Clock source	P11.2= SMCLK	baudrate	Communication function
UART0	enable	XT2=8MHZ	8MHZ	115200	OK
UART1	disable				
UART2	disable				
UART3	disable				

	STATUS	Clock source	P11.2= SMCLK	baudrate	Communication function
UART0	disable				
UART1	enable	XT2=8MHZ	1MHZ	115200	fail
UART2	disable				
UART3	disable				

	STATUS	Clock source	P11.2= SMCLK	baudrate	Communication function
UART0	disable				
UART1	disable				
UART2	enable	XT2=8MHZ	8MHZ	115200	OK
UART3	disable				

	STATUS	Clock source	P11.2= SMCLK	baudrate	Communication function
UART0	disable				
UART1	disable				
UART2	disable				
UART3	enable	XT2=8MHZ	8MHZ	115200	OK

	STATUS	Clock source	P11.2= SMCLK	baudrate	Communication function
UART0	enable	XT2=8MHZ	1MHZ	115200	fail
UART1	enable	XT2=8MHZ	1MHZ	115200	fail
UART2	enable	XT2=8MHZ	1MHZ	115200	fail
UART3	enable	XT2=8MHZ	1MHZ	115200	fail

	STATUS	Clock source	P11.2= SMCLK	baudrate	Communication function
UART0	enable	XT2=8MHZ	8MHZ	115200	OK
UART1	disable				
UART2	enable	XT2=8MHZ	8MHZ	115200	OK
UART3	enable	XT2=8MHZ	MHZ	115200	OK