MSP430 Advanced Technical Conference 2006

Leveraging MSP430 for Robust System Design

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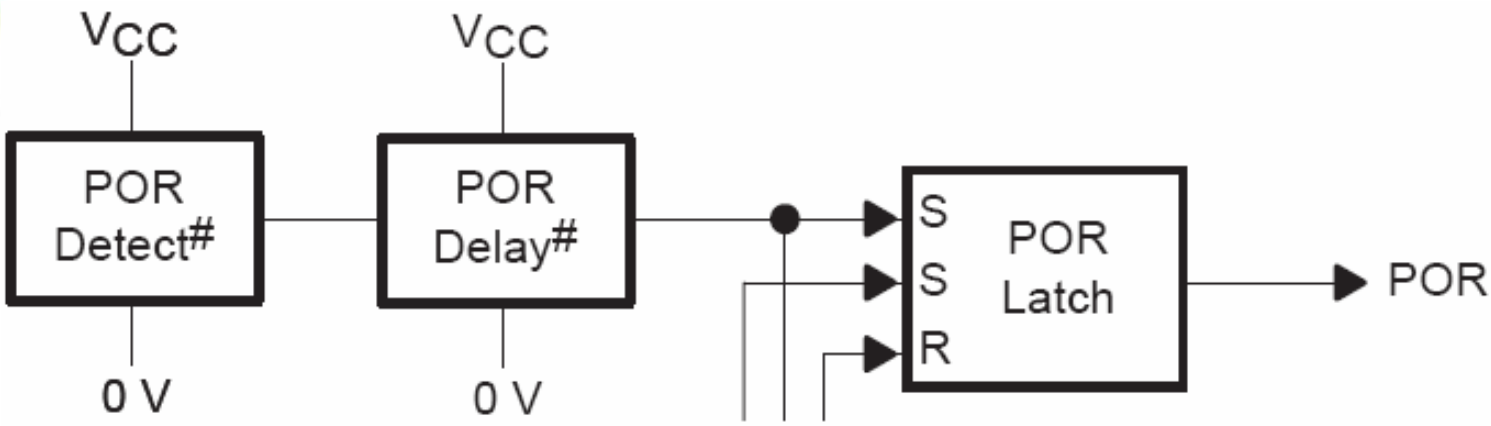
Agenda

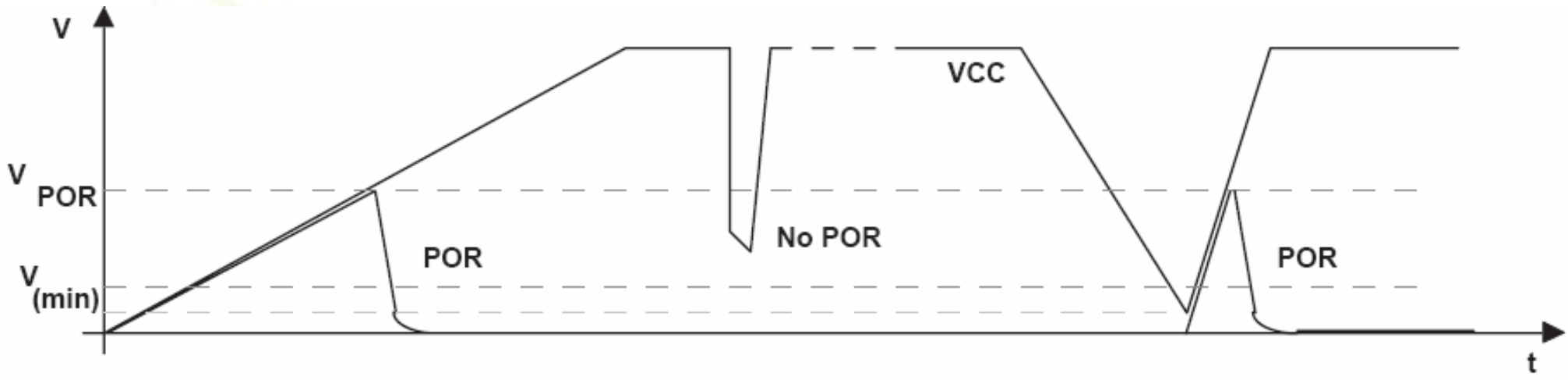
- Startup and Power Supply
- ESD
- Board Design
- Crystal Considerations
- Built-in Protection
- Software Considerations

Power On Reset (POR)



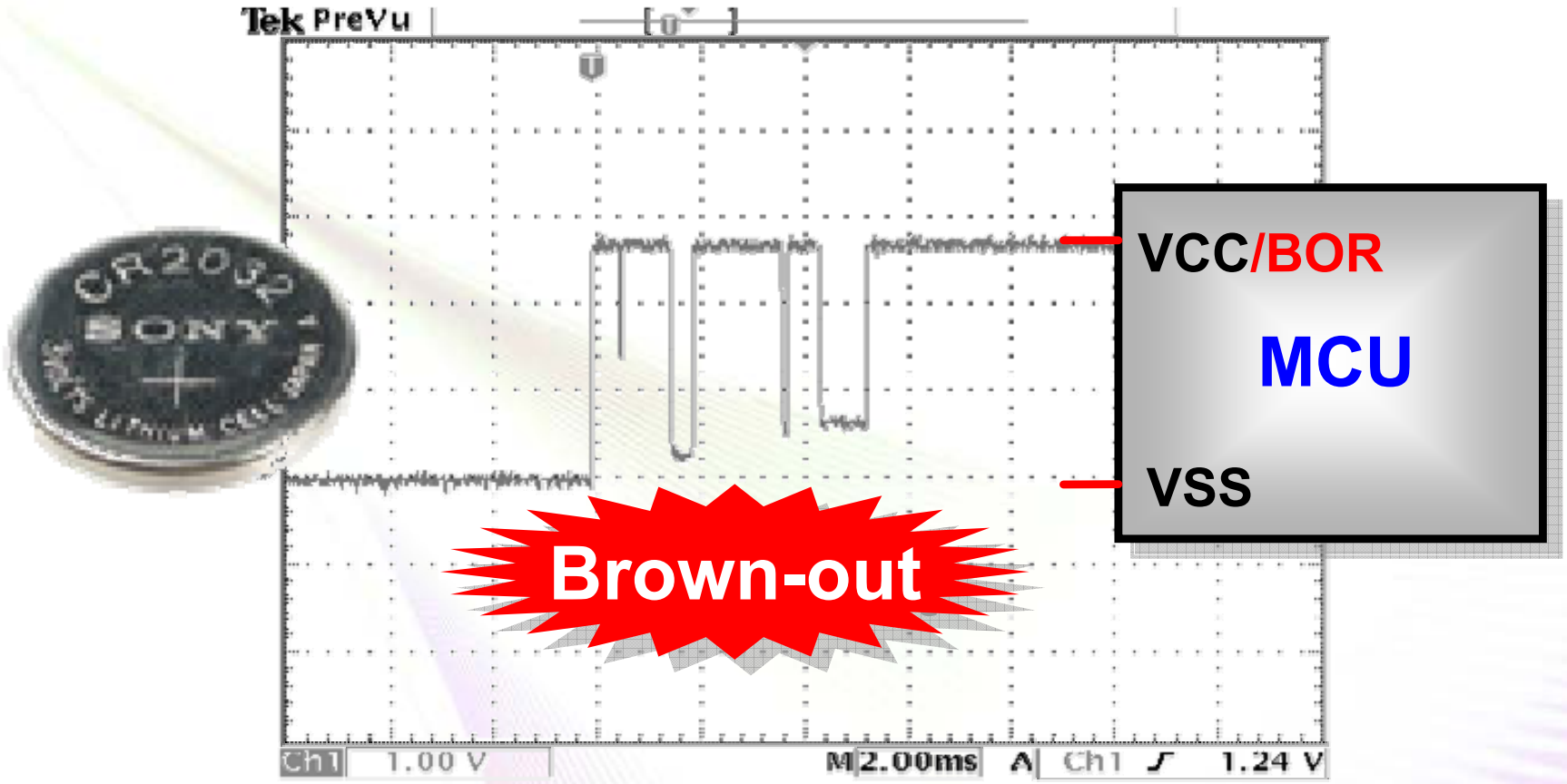
- **Built-into MSP430s w/o brownout reset**
- **Consists of two parts:**
  - Power-on reset detection
  - Power-on reset delay
- **Guaranteed POR if VCC ≤ 0.2V and |dV/dt| ≥ 1V/ms**
- ***POR is not a voltage supervising circuit!***

POR Operation



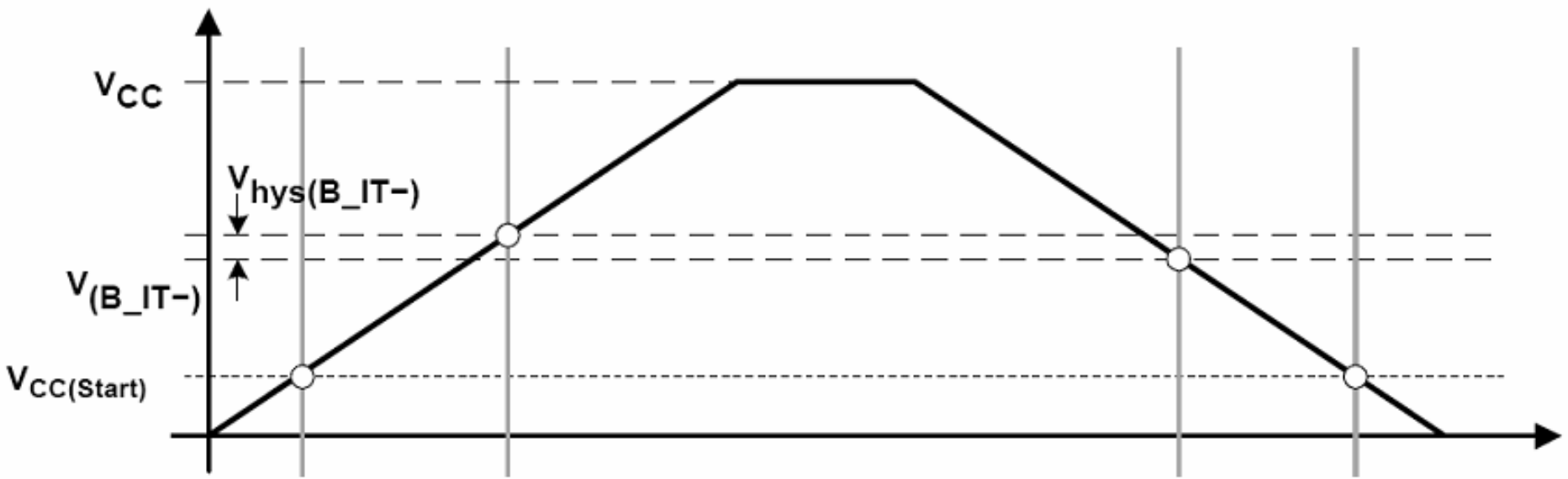
- Code execution can start with V_{CC} as low as 0.8V
- V_{POR} is temperature dependent!
- Remember: V_{CCmin} = 1.8V
- *Always obey max. MCLK vs. V_{CC}!*

Brown Out Reset (BOR)



- **Built-in BOR: all MSP430 devices (Except: x11x1, x12x, x13x, x14x)**
- **Always on, *zero-power* *(included in LPMx data)***

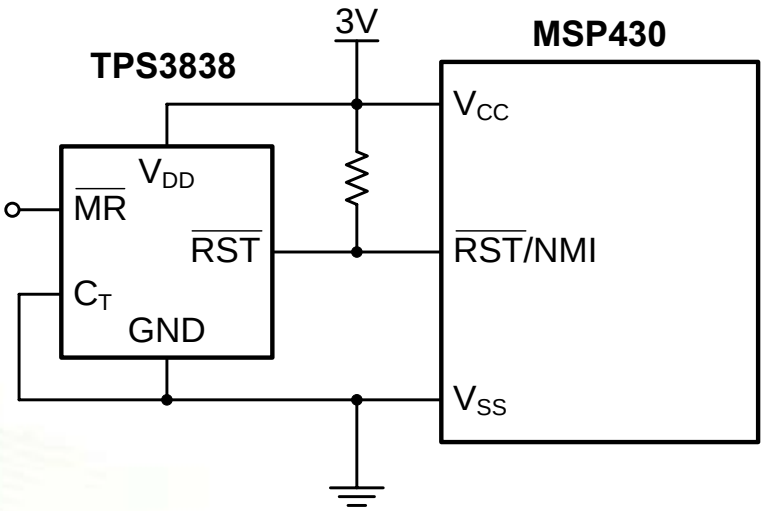
BOR Operation

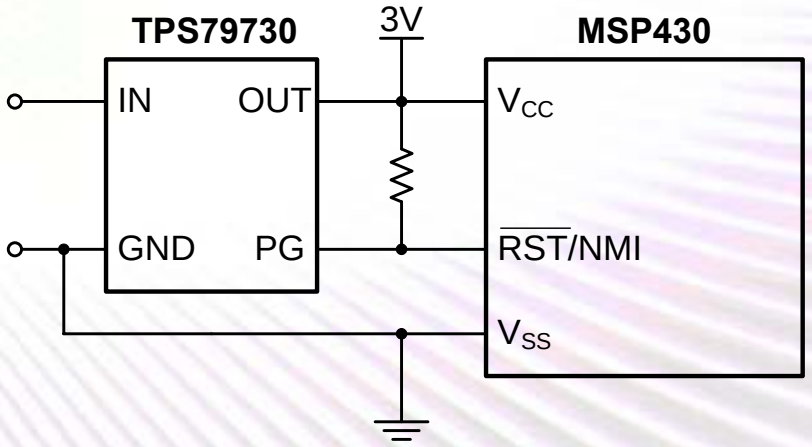


- RESET when V_{CC} crosses $V_{CC(Start)}$
- BOR releases device after $V_{CC} = V_{(B\_IT-)} + V_{hys(B\_IT-)}$ and $t_{d(BOR)}$ = 2000µs max.
- $V_{(B\_IT-)} + V_{hys(B\_IT-)}$ is ≤ 1.8 V
- ***Again, always obey max. MCLK vs. V_{CC}!***

Supply Voltage Supervisor (SVS)

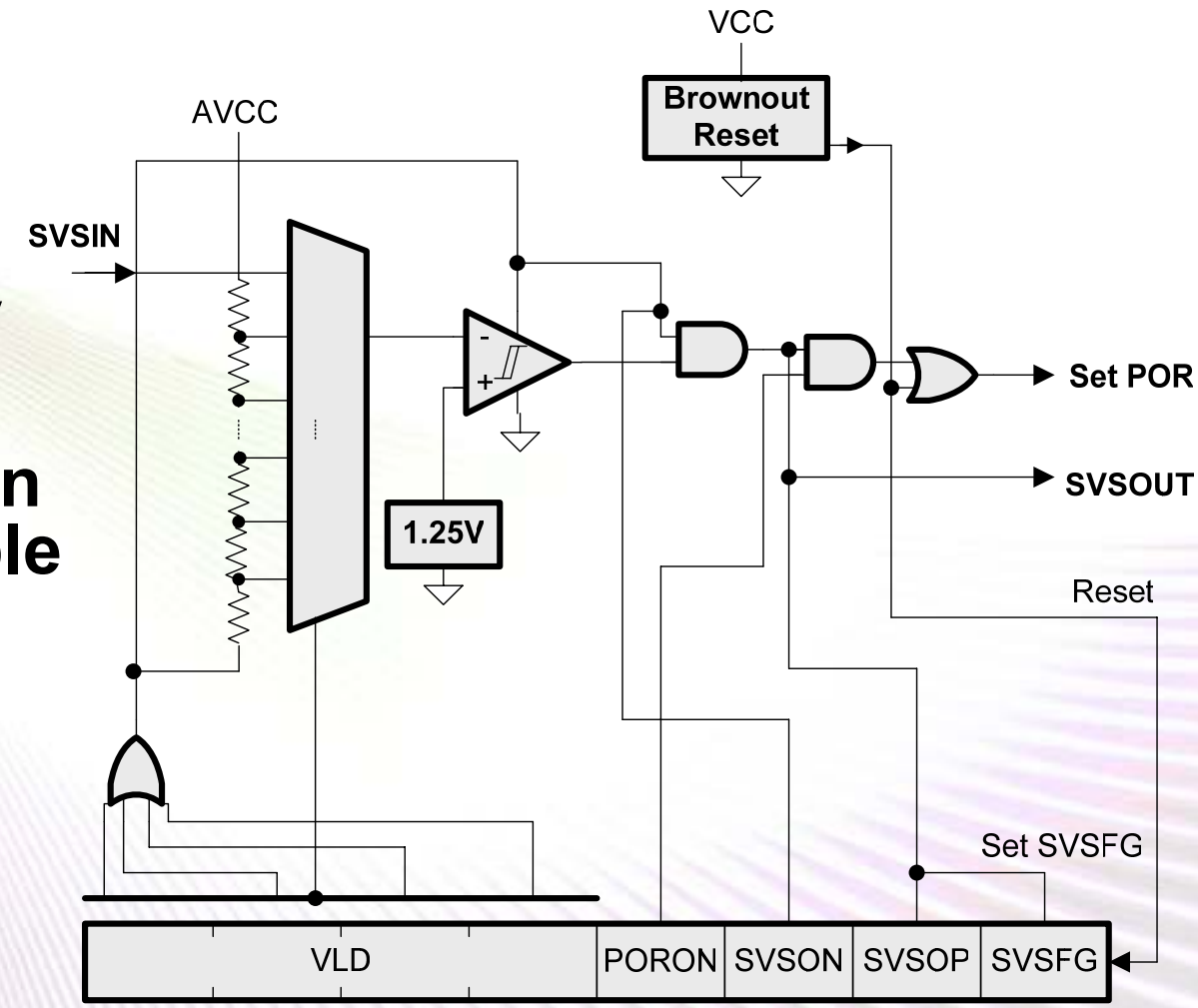
- **Can indicate & limit device operation to certain V_{CC} conditions**
- **MSP430s with built-in SVS:**
  - ‘F15x, ‘F16x(x)
  - ‘F4xx (excl. ‘F42x0)
- **Other MSP430 devices:**
  - Nano-power SVS connected to RST/NMI pin, e.g.: TI part # TPS3836/7/8xx ***I_{DD} = 200nA***
  - Voltage regulator with power good signal, e.g.: TI part # TPS797xx ***I_Q = 1.2uA***



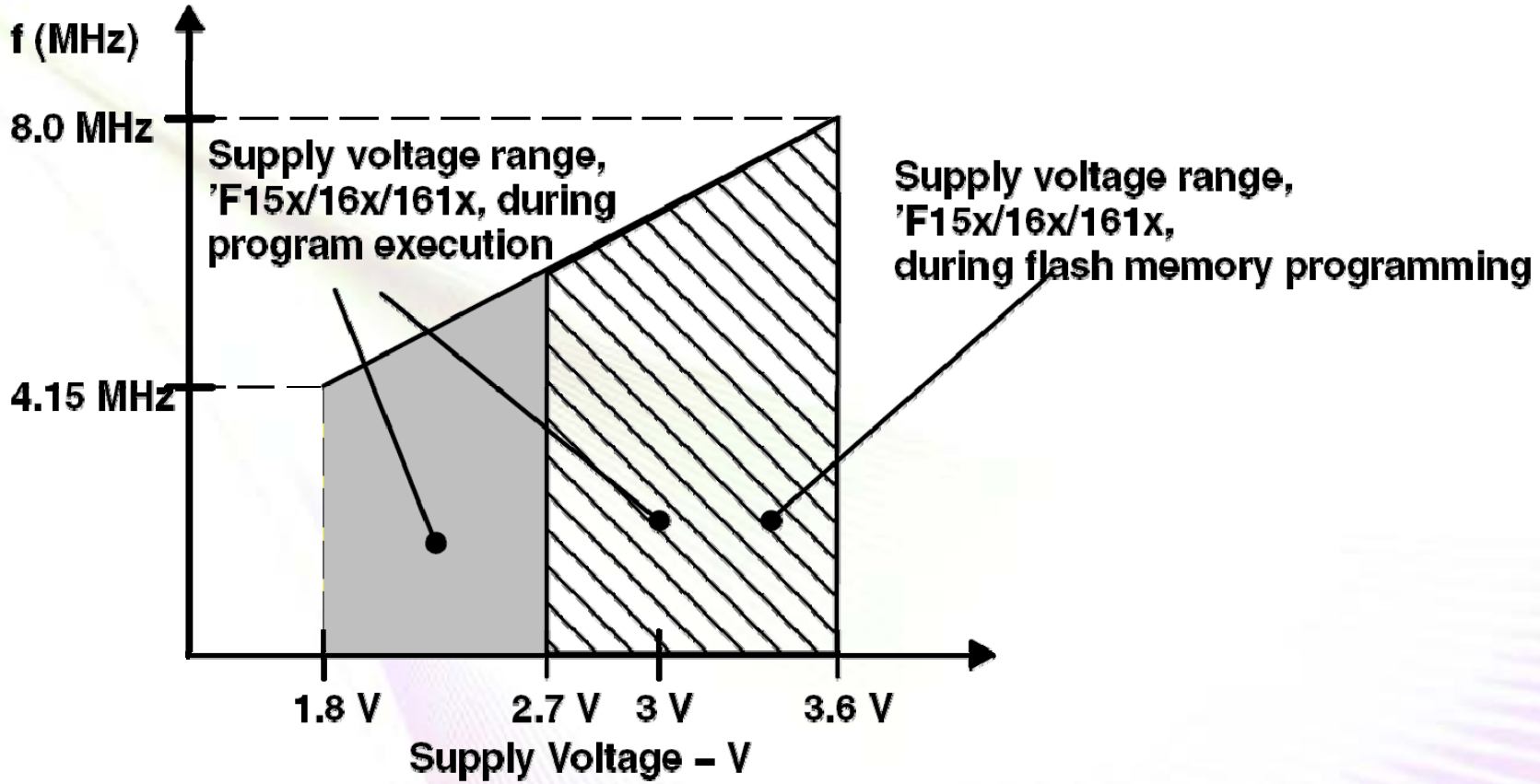


MSP430 Built-In SVS

- V_{CC} monitoring
- Selectable POR
  - Reset
  - Flag
- Output accessible by software
- Low-voltage condition latched and accessible by software
- 14 selectable levels
- External voltage monitor
- Output can be used externally



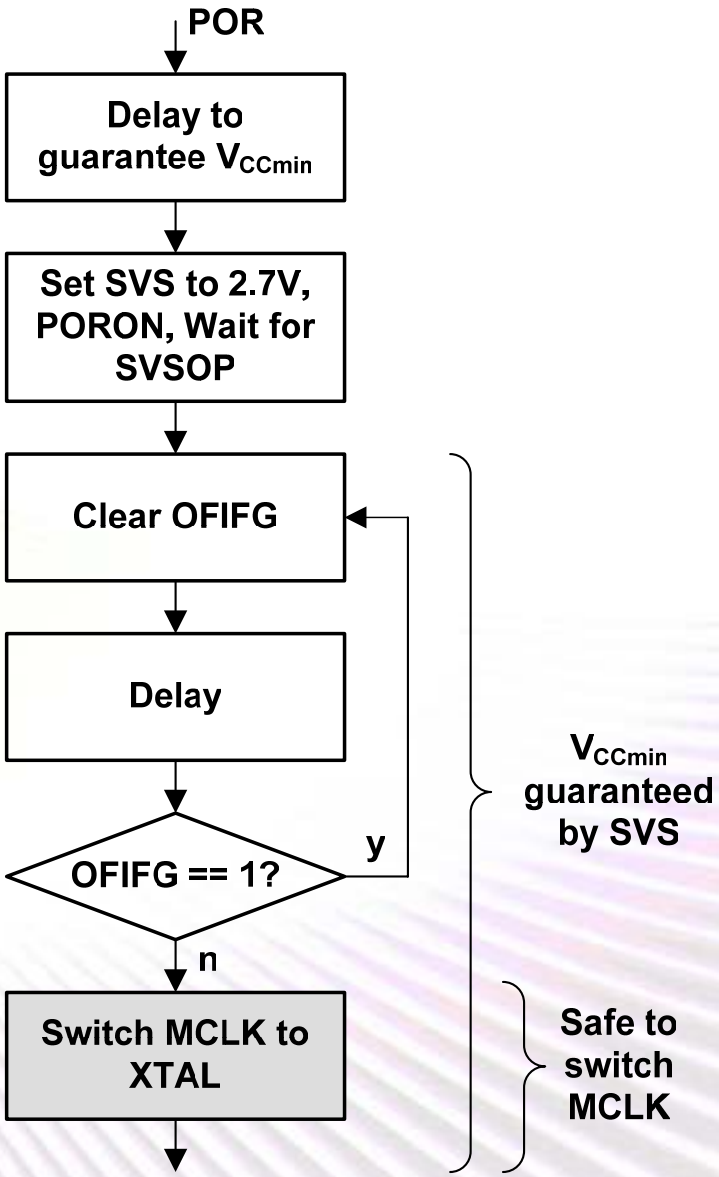
SVS Application Ideas



- Minimum V_{CC} for MLCK, Flash ISP, and analog peripherals
- Always see device-specific datasheet (2xx = 2.2V)

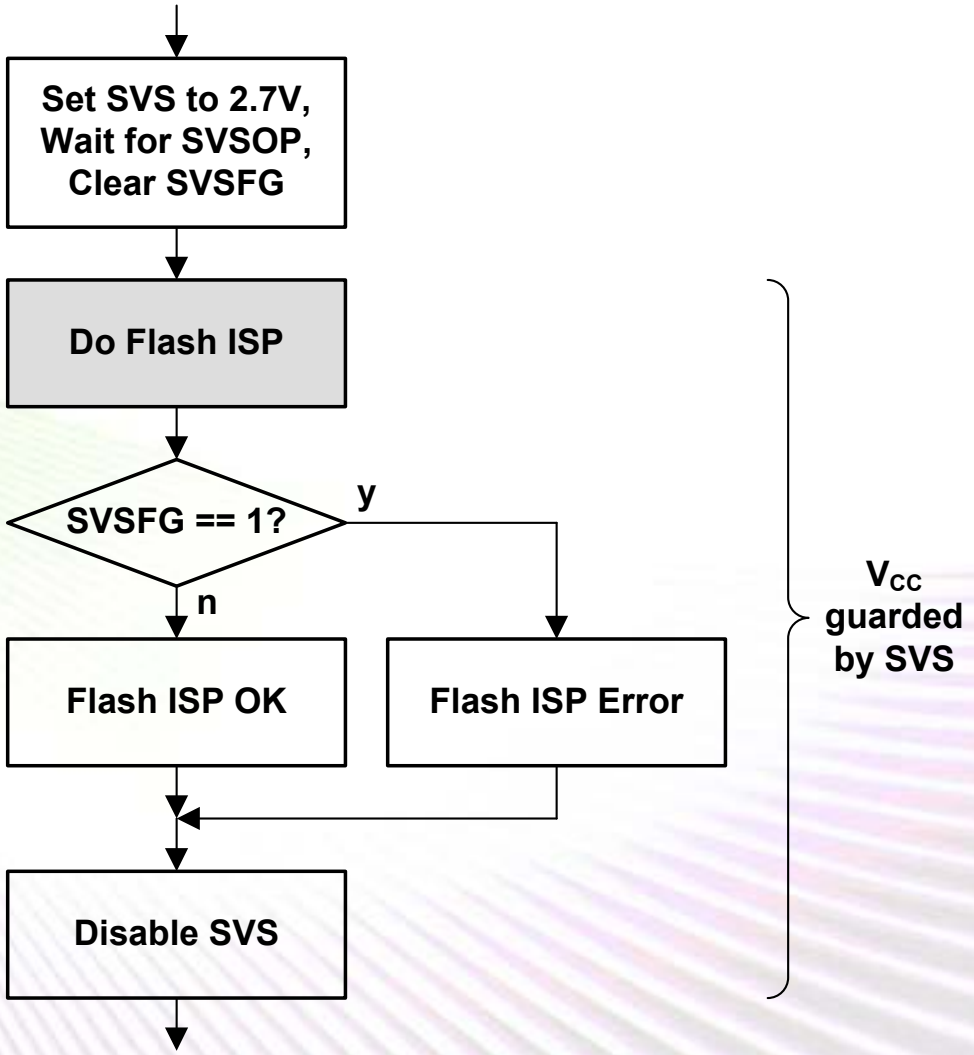
Safe High-Speed Operation Example

- Design goal: run ‘F155 CPU at 6MHz
- $V_{CCmin}(f) = -0.142V + f \times 0.468\ mV/MHz$
- $V_{CCmin}(6MHz) = 2.67V$
- System V_{CC} is 3.3V
- SVS threshold selection per device data sheet: $V_{(SVS\_IT-)} = 2.7V$
- SVS will keep device in reset while V_{CC} not met



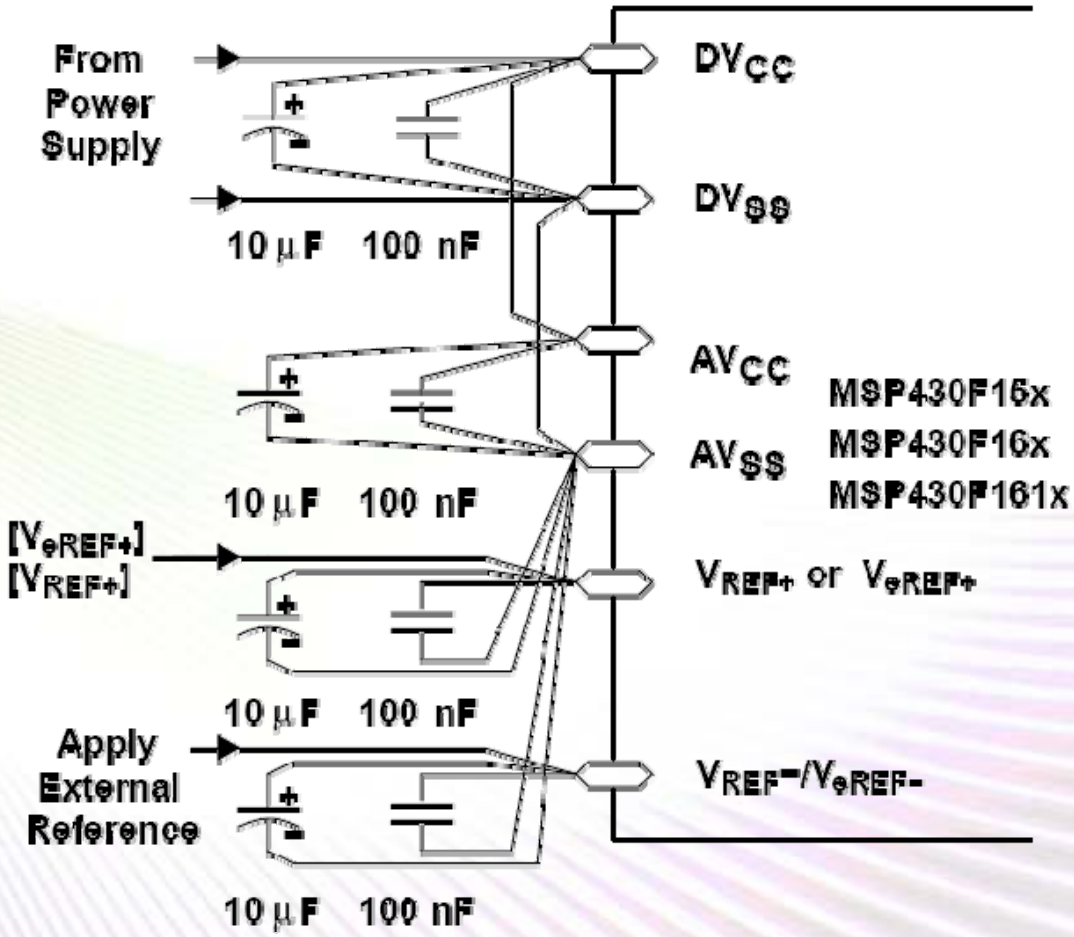
Safe Flash ISP Example

- **Requirement: $V_{CC\ min}$ = 2.7V during Flash ISP for ’F155**
- **System V_{CC} is 3.3V**
- **SVS threshold selection per device data sheet: $V_{(SVS\_IT-)}$ = 2.7V**
- **SVS will set SVSFG in case of low-voltage condition**
- **Enable/disable SVS to conserve power**



Power Supply Considerations

- AV_{CC} and DV_{CC} connected internally by diodes
- *$DV_{CC} - AV_{CC} << 0.3V$*
- DO NOT power down DV_{CC} and AV_{CC} separately
- AV_{CC} must not come up before DV_{CC}
- AV_{SS} and DV_{SS} connected internally - always connect them on your board



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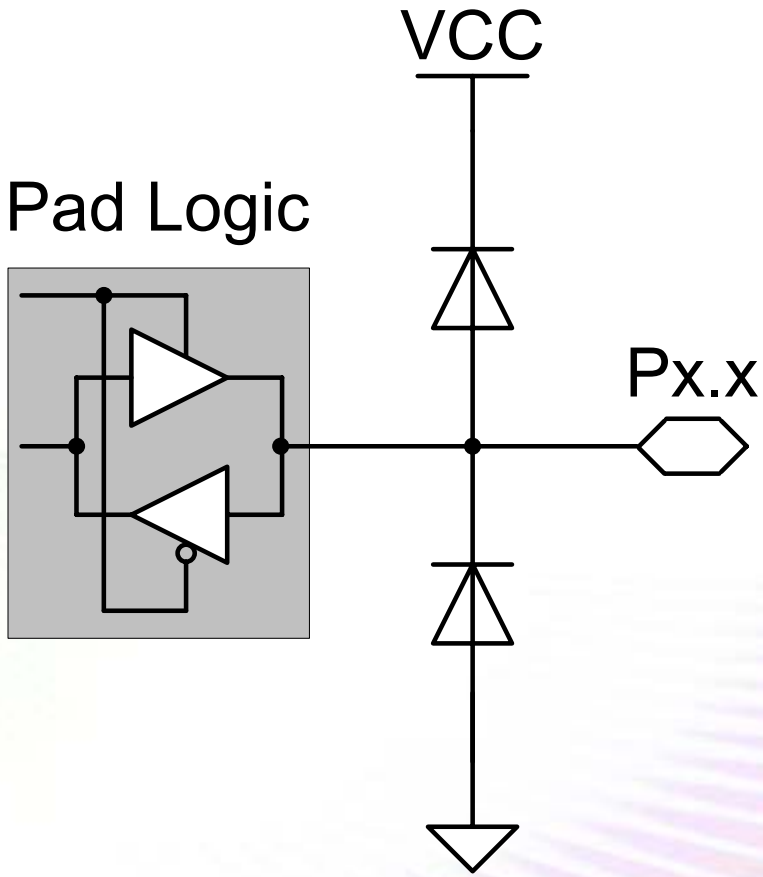
ESD Considerations

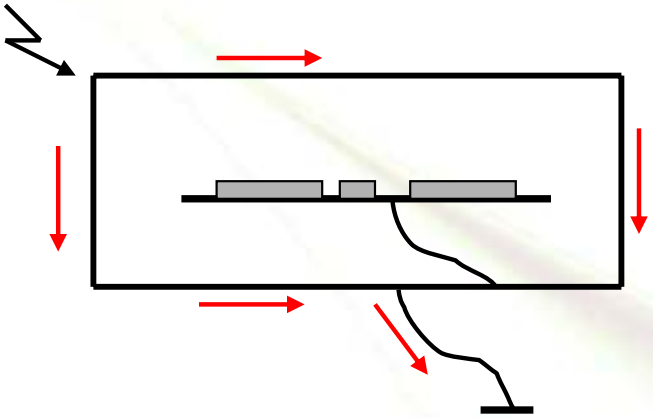
- **MSP430s comply with standard TI ESD specs:**
  - HBM = 1.5KV
  - CDM = 500V
  - MM = 200V
- **System level spec – robust design is a must**
- ***TI testing does not substitute robust system design***



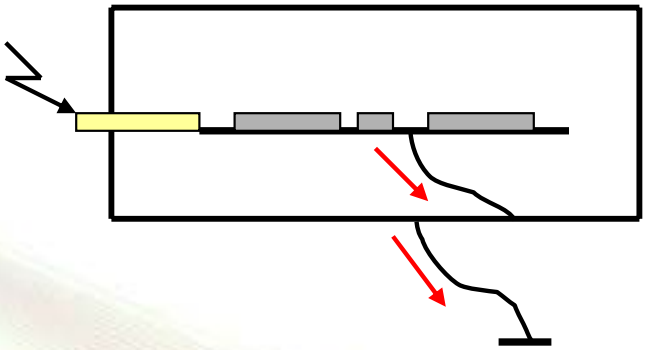
ESD Protection Design Ideas

- **Use proper MSP430 supply decoupling, with caps placed closely**
- **Interface ICs with high level of built-in ESD protection**
- **Transient voltage suppressors (e.g.: SN75240)**
- **External series-Rs on I/O lines**
- **Additional clamping diodes**
- **Keep traces short, lead length is critical because of inductance:**
  - V = L x di / dt
  - L for leads and PCB = 20nH / inch
  - ESD hits can induce di / dt of 10A / 500ps
  - V = 400 V/inch

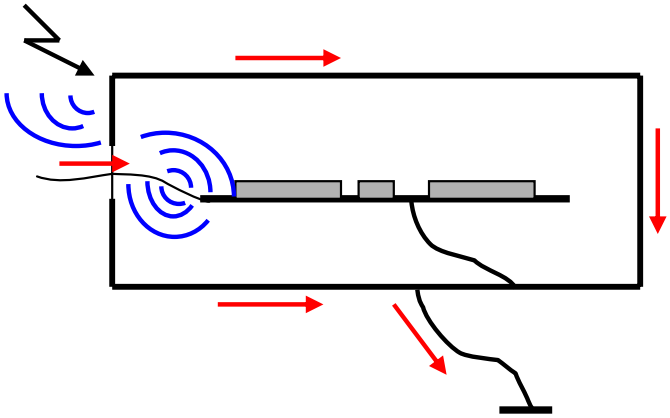
ESD Effects Through Enclosures



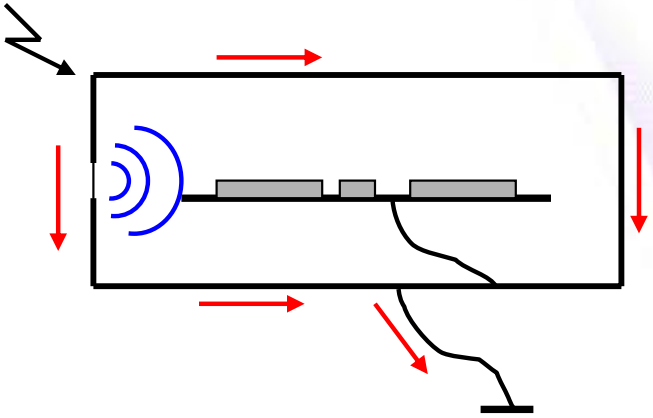
No influence, ideal



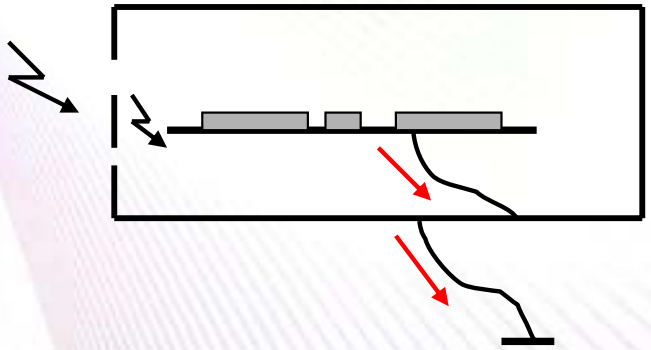
Direct discharge



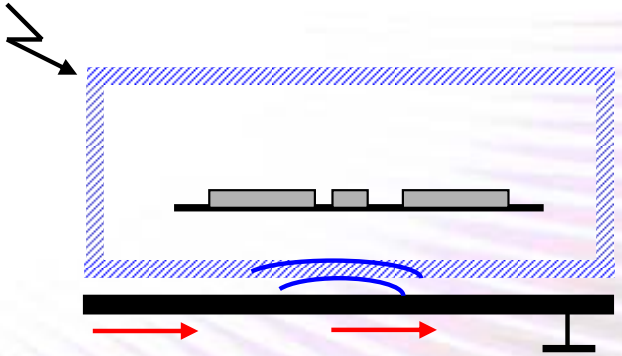
Direct discharge to cables



Influence through holes



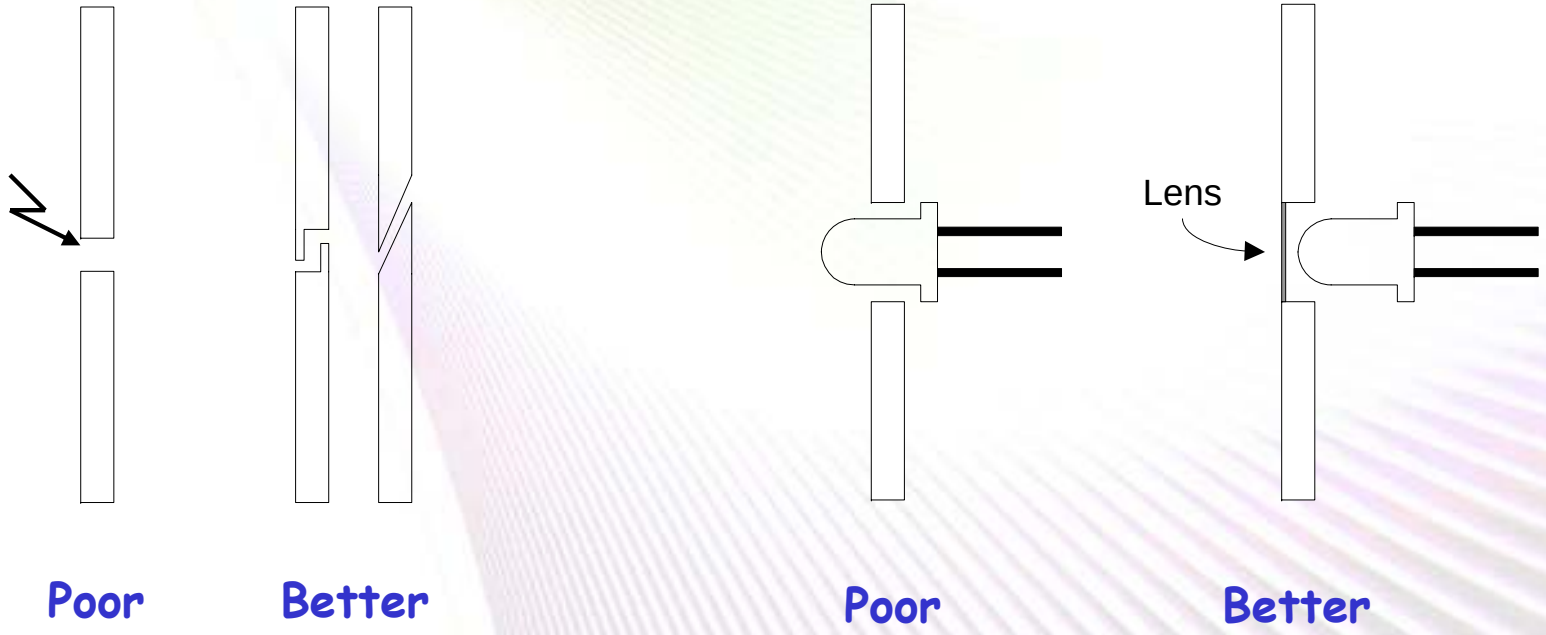
Secondary discharge from isolated metal



Plastic enclosure

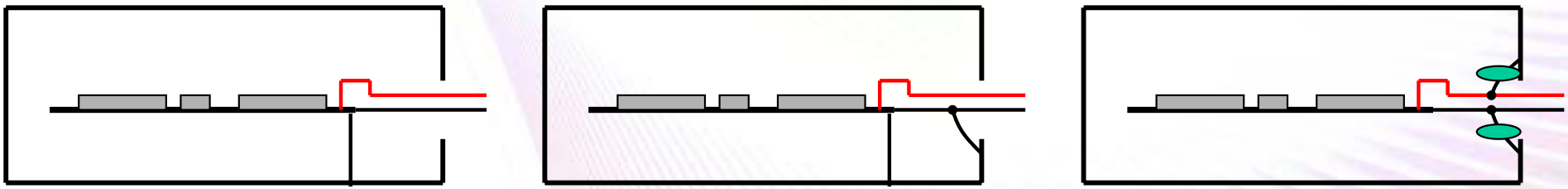
Enclosure Openings

- No direct openings or keep PCB away from openings
- Use gasket around LCD opening
- LEDs are particularly vulnerable - direct path to PC board



Enclosure Cables

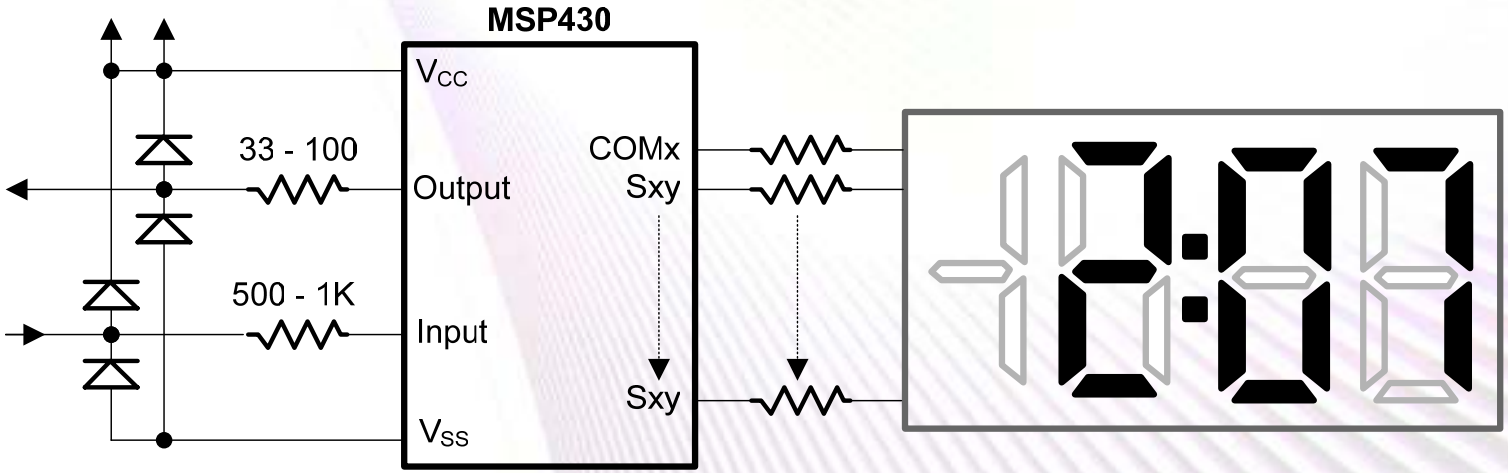
- Properly ground cables entering the enclosure
- Added protection often required



Poor Better Best

ESD Device Protection

- Series R most basic
- Also helps reduce inductive Vcc ringing at power
- Can combine series R with diodes for added protection
- Suppression devices such as varistors, thyristors, TVS diodes, etc. should be used in extreme cases



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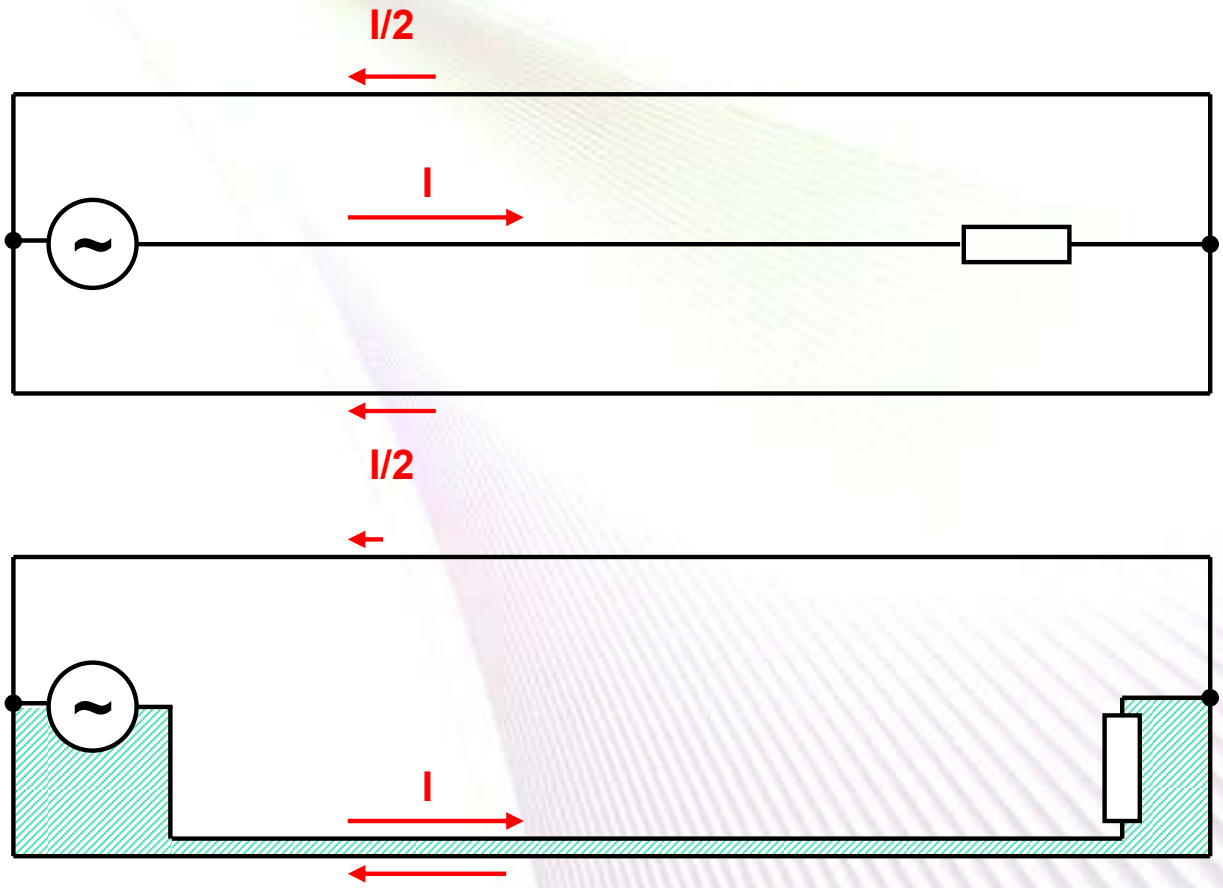
PCB Layout Fundamentals

- Use ground plane where possible to lower current-path inductance
- Properly terminate unused MSP430 pins
- No floating copper islands on PCB - they can induce noise and arc in presence of ESD
- Avoid crossing breaks in GND plane with traces as this increases loop inductance and EMI radiation
- Keep loop areas of switching signals as small as possible
- Keep loop area of the oscillator signals as small as possible
- *Always keep forward and return currents together!*

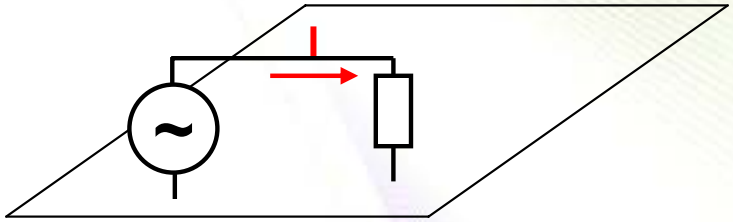
What Are Current Loops?

- The distribution of the current going through two possible paths is dependant on the inductance of those paths

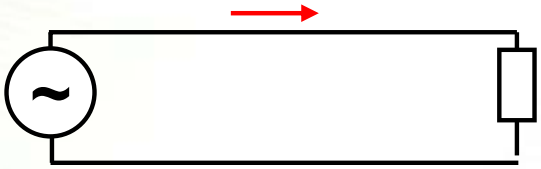


Where Are Current Loops?

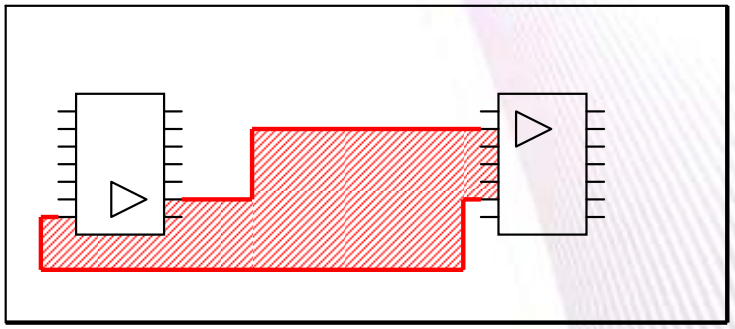
- **Examples for closed current loops as a radiation source: Multi-layer PCB, Signal loop on a single layer PCB, Cable, Gnd loop closed by cables.**



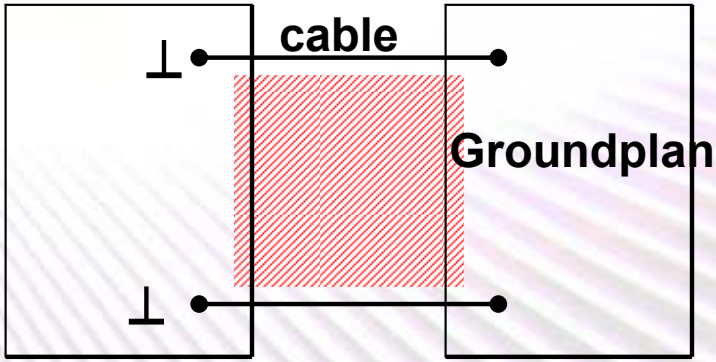
a)



c)



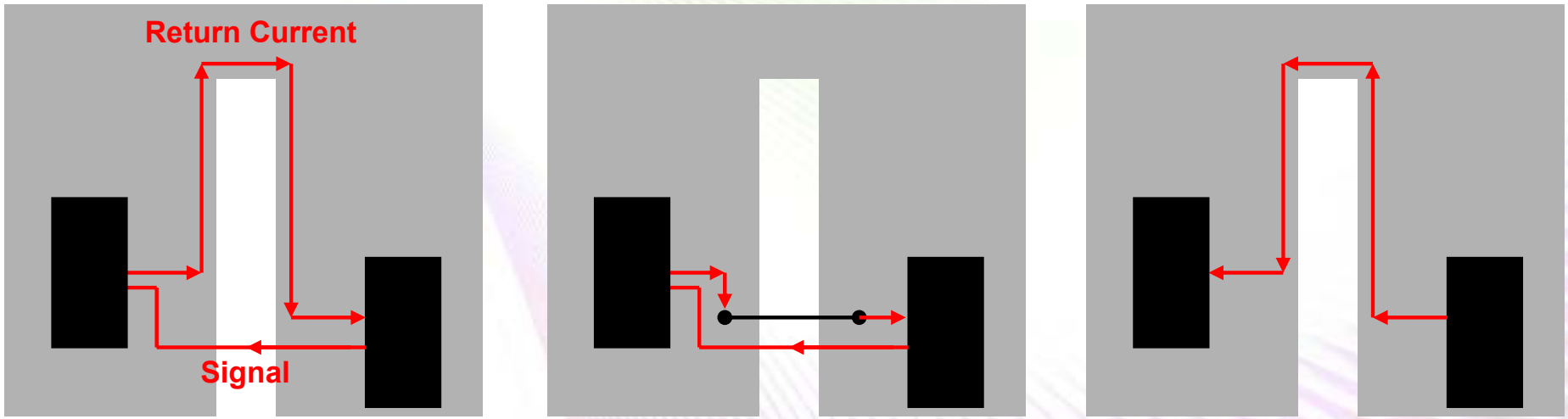
b)



d)

Minimize Current Loops In Layout

- Minimizing current loops minimizes inductive coupling
- Helps both EMI and ESD performance



Poor Better Best

How To Terminate Unused Pins?

- I/O: Open, switched to port function, output direction
- XIN: DV_{CC}, XT2IN: DV_{SS}
- XOUT, XT2OUT: Open
- ADC V_{REF+}: Open
- ADC Ve_{REF+}, V_{REF-}/Ve_{REF-}: DV_{SS}
- R03: DV_{SS}
- LCD signals COMx, Sxx: Open
- JTAG signals TDO, TDI, TMS, TCK, Test: Open
- RST/NMI: 47kΩ pullup + 10nF pulldown
- *See MSP430xxx Family User's Guides*

System Design Best Practices

- Proper layout is important!
- No direct enclosure openings or keep PCB away from openings
- Ground the connector shrouds
- Ground the enclosure
- Provide ESD a path to ground
- Keep MSP430 out of path of ESD
- Use gasket around LCD opening
- LEDs are particularly vulnerable - direct path to PC board (use light conductors or lenses)

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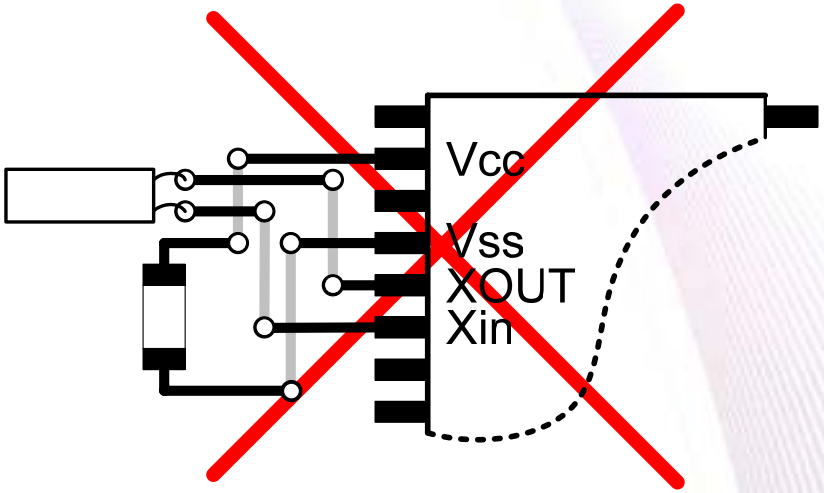
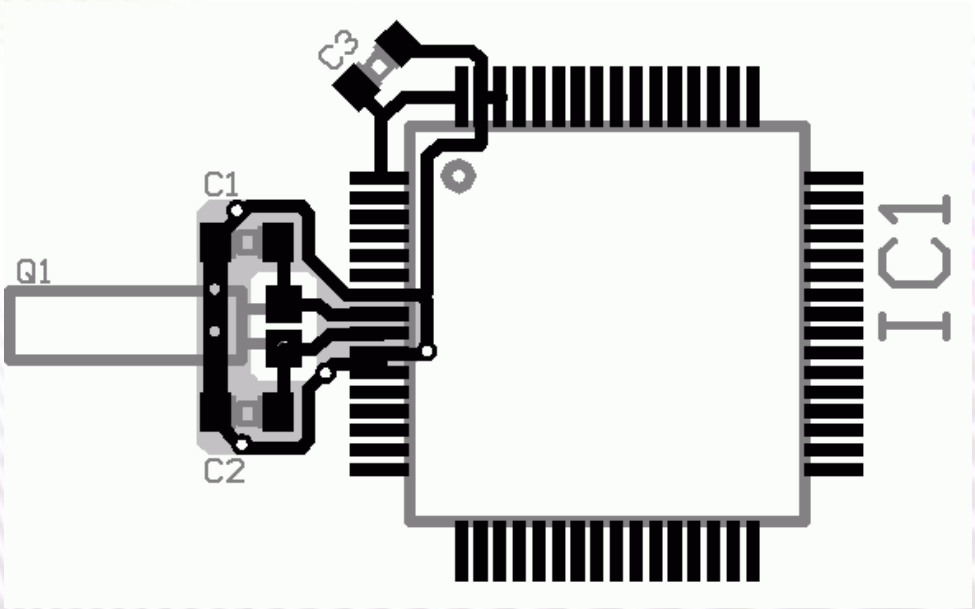
Crystal Layout

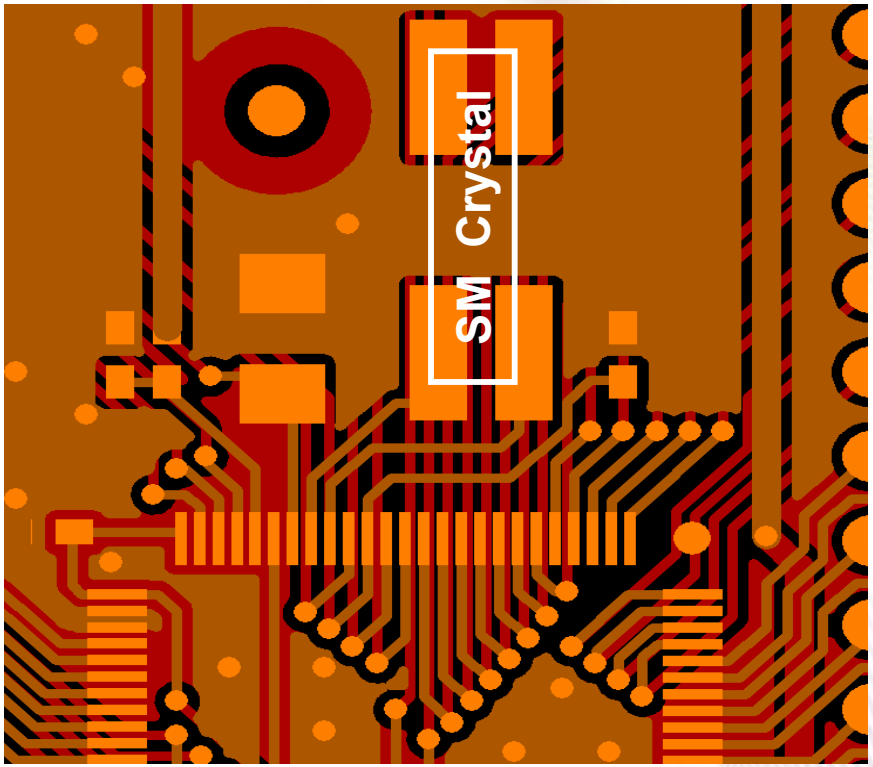
- Crystal as close the to MSP430 as possible
- Short and direct traces, no traces underneath
- Keep away switching signals
- Ground crystal can, use guard ring around leads
- Ground plane underneath crystal

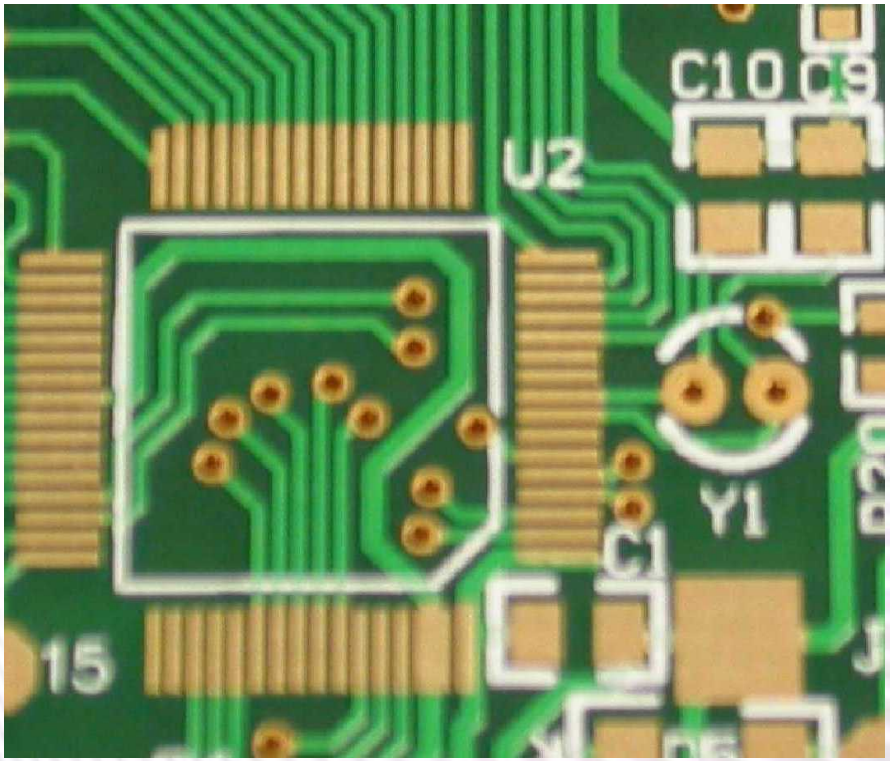




Crystal Layout Examples

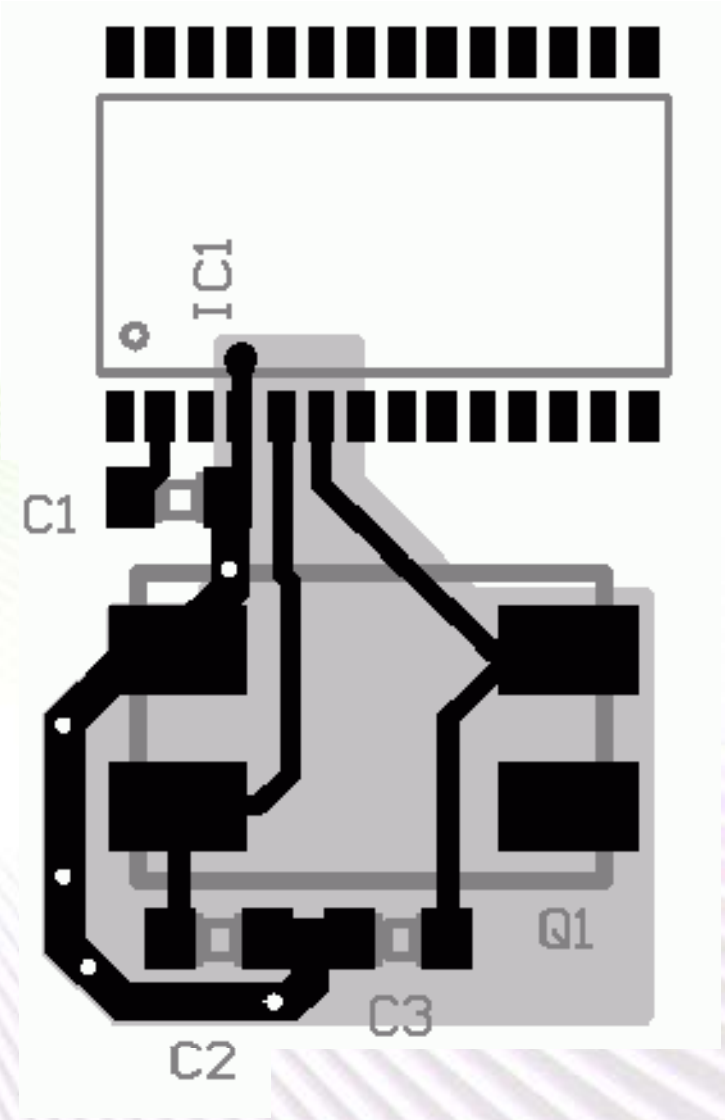
- XTAL signal / GND routing
- Component placement





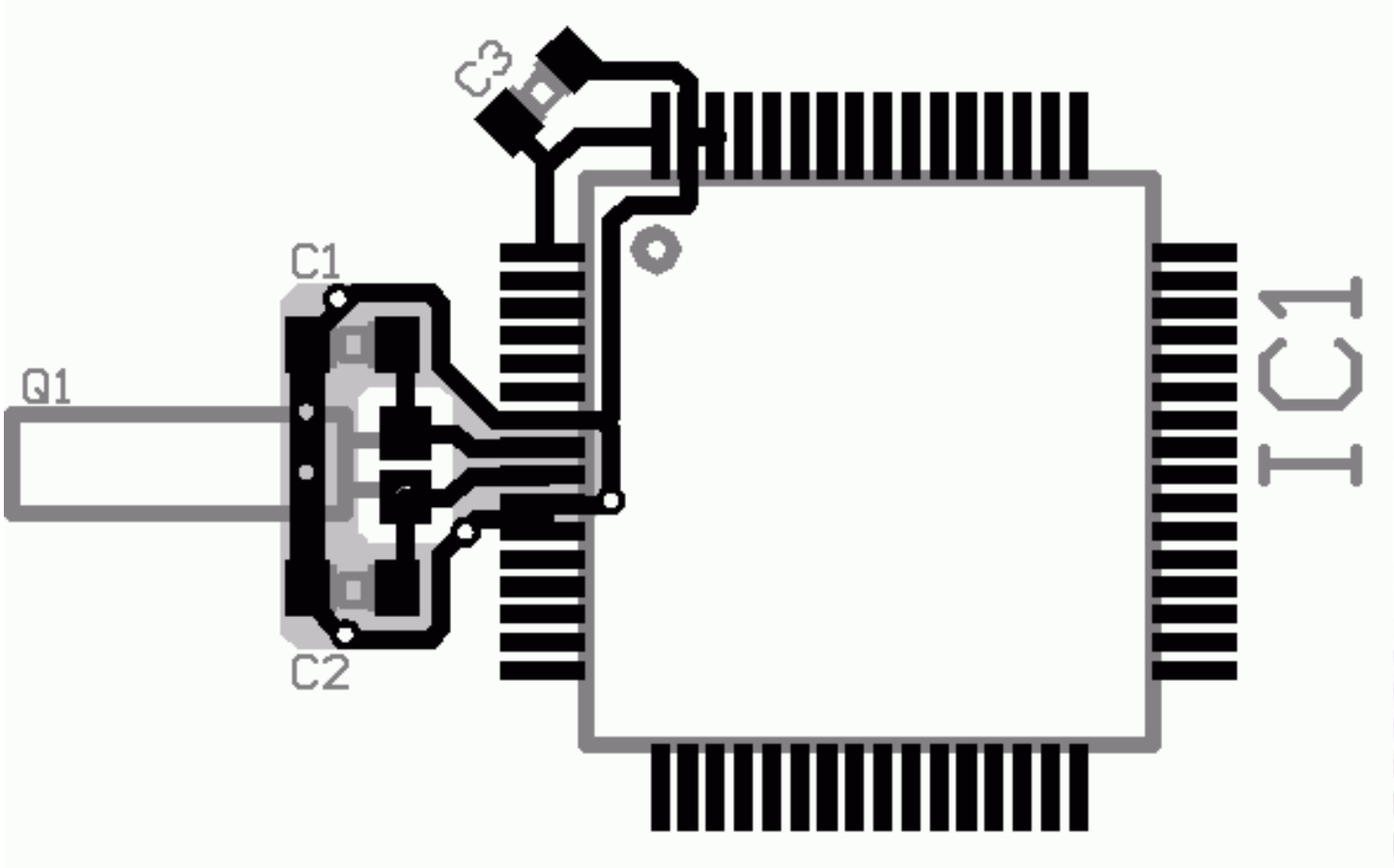
Crystal Layout Example - 28 Pin

- Crystal as close as possible at XIN/XOUT terminals
- GND below the crystal and load capacitors connected to the Vss terminal
- Load capacitors grounded closely to each other

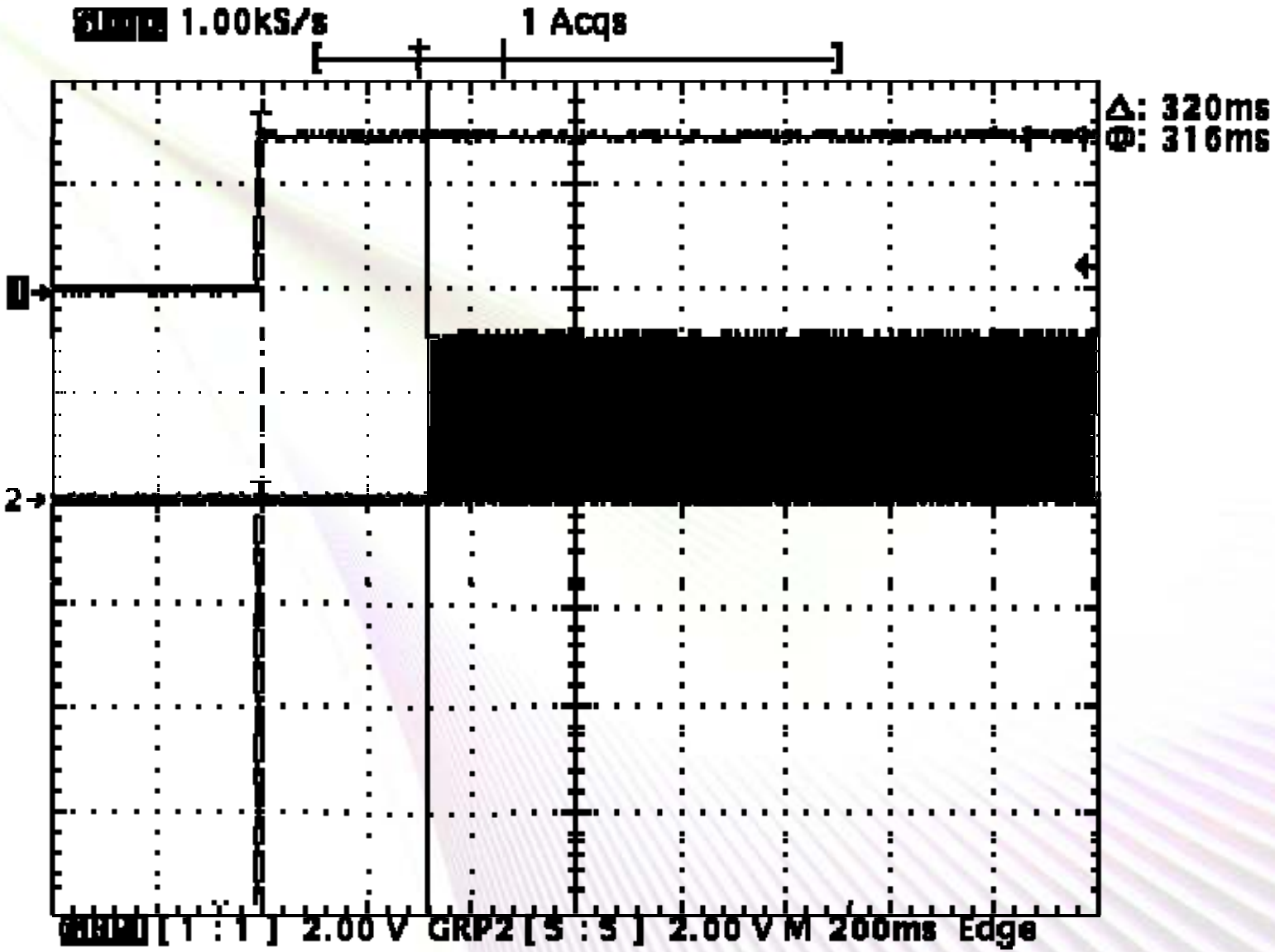


Crystal Layout Examples - F41x

- Same principles
- Use the NC pins beside XIN/XOUT for GND ring

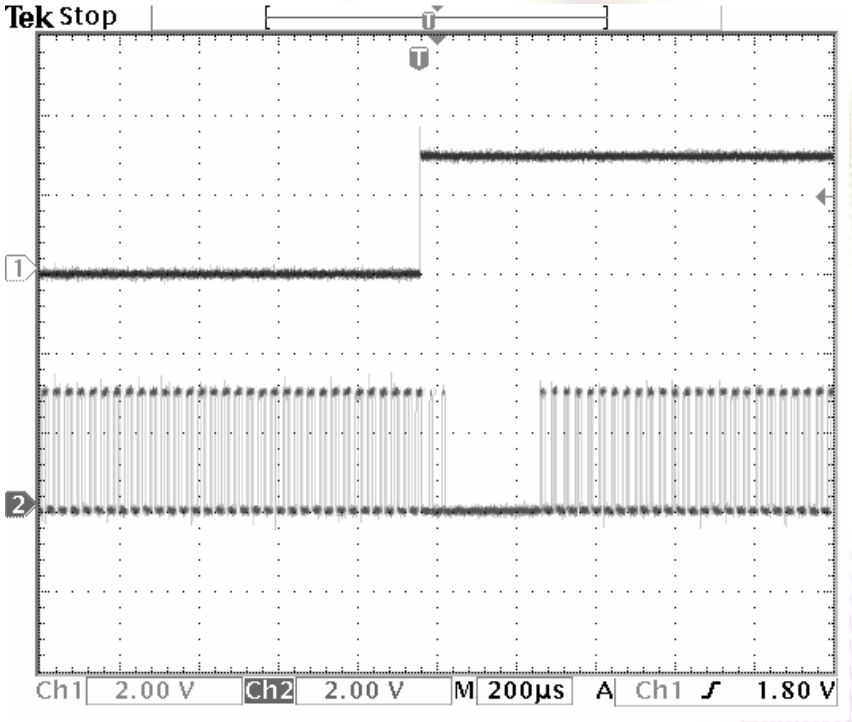


32kHz Crystal Oscillator Start-Up

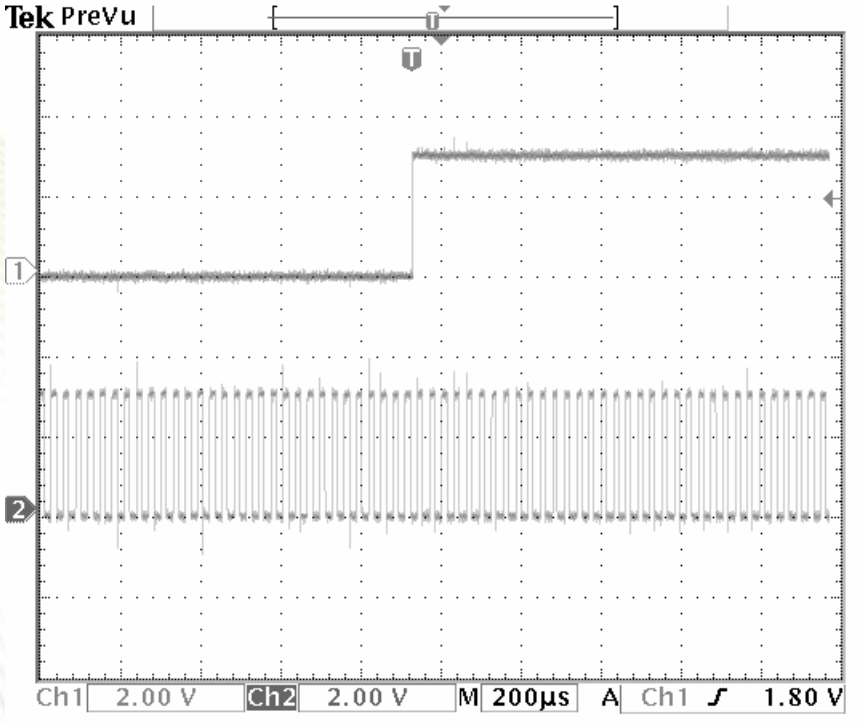


Crystal Dropout

- Switching signals near the crystal can cause dropout



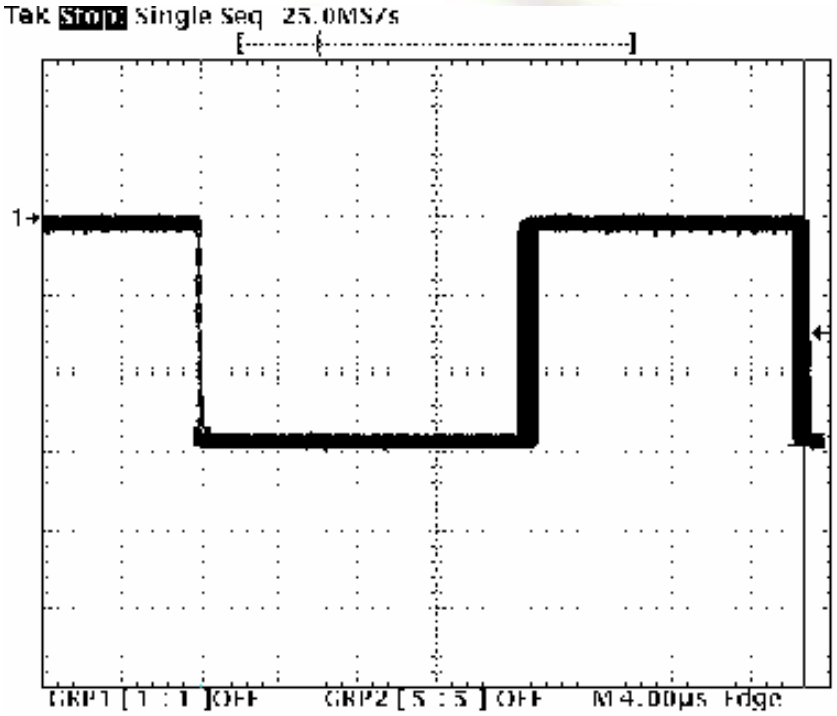
Poor Layout



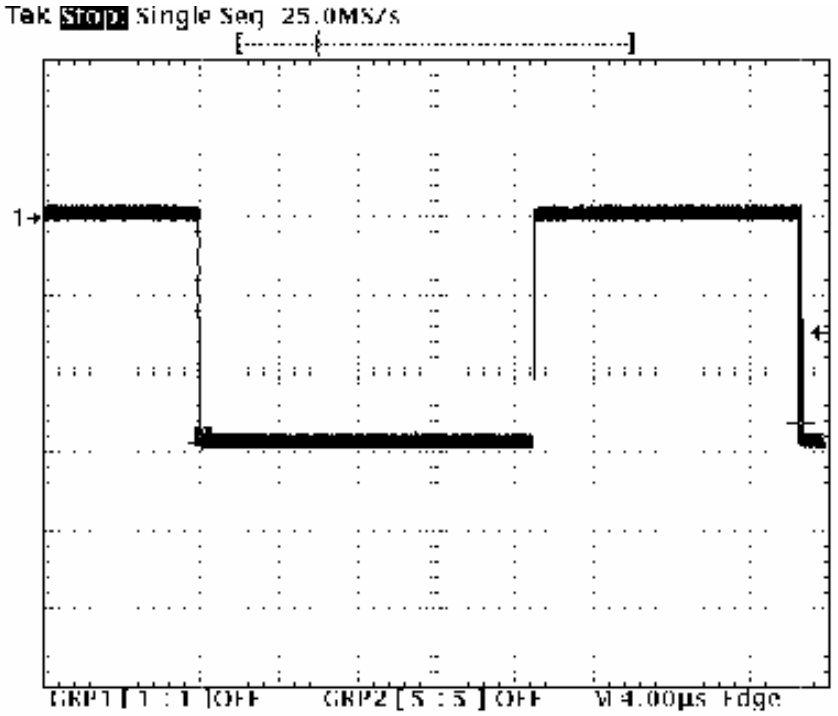
Good Layout

Crystal Oscillator Jitter

- **Poor design can cause jitter**



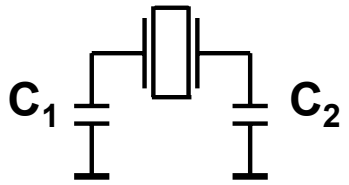
Poor Layout

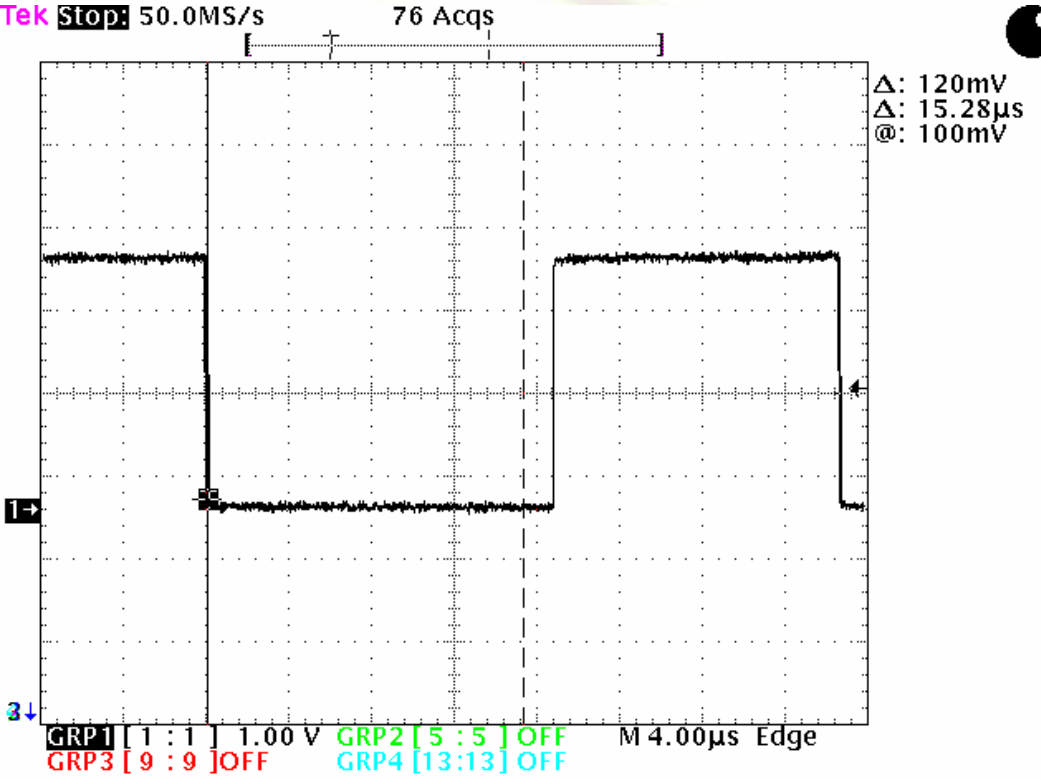


Good Layout

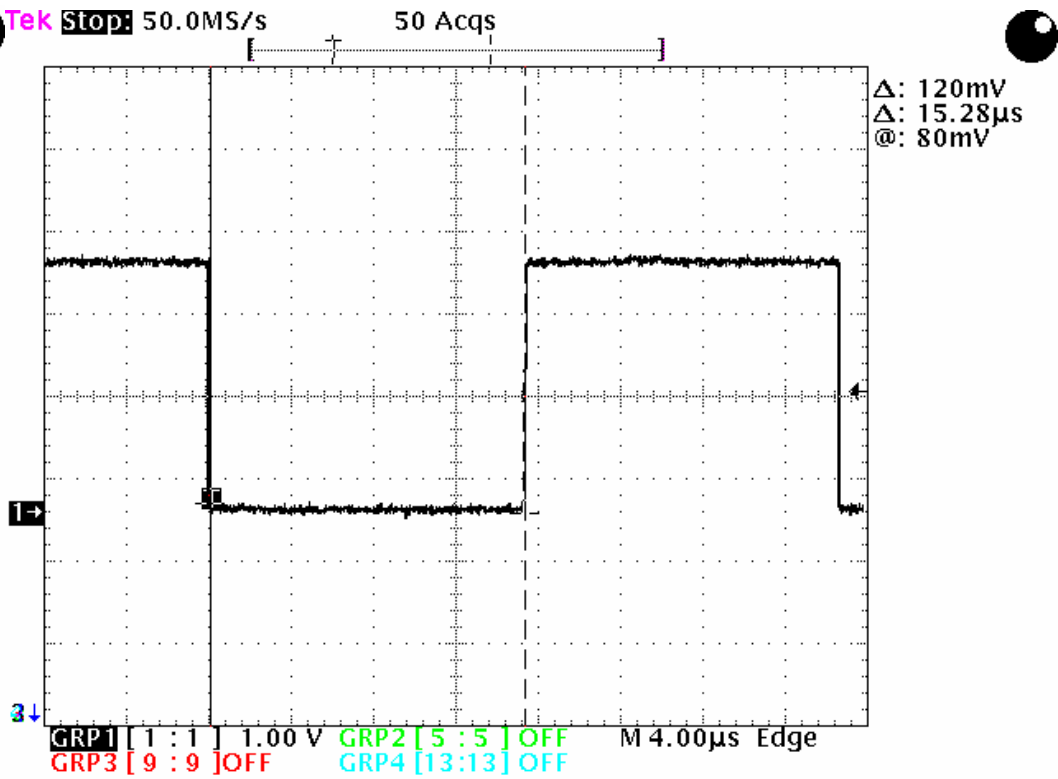
Crystal Oscillator Duty Cycle

- **Unbalanced load caps can change duty cycle**





Unbalanced



Balanced

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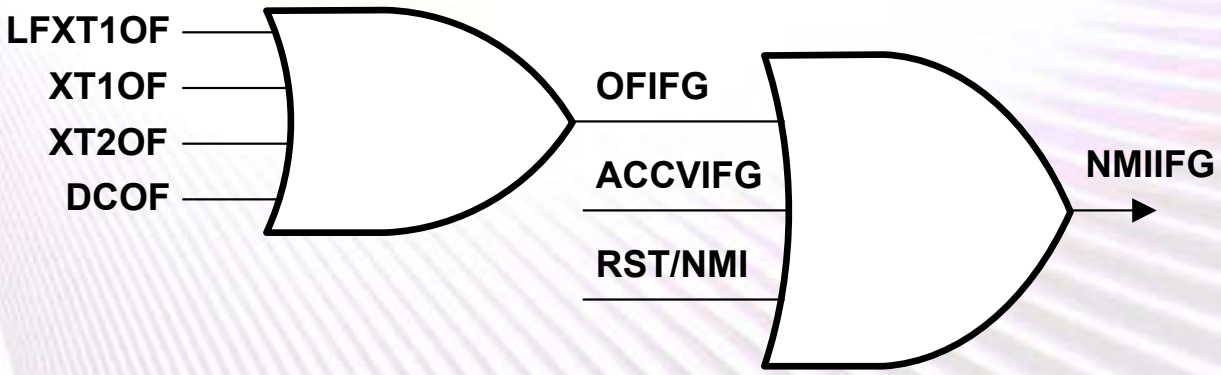
XTAL Fault Detection Overview

	‘F1xx	‘F2xx	‘F4xx
XT1 HF Mode	**YES**	**YES**	**YES**
XT1 LF Mode	**NO**	**YES**	**YES**
XT2 Mode	**YES**	**YES**	**YES**
FLL	**N/A**	**N/A**	**YES**

What if…

- **FLL? Flash ISP?**
- **RTC? WDT?**
- **LPMx wakeup?**

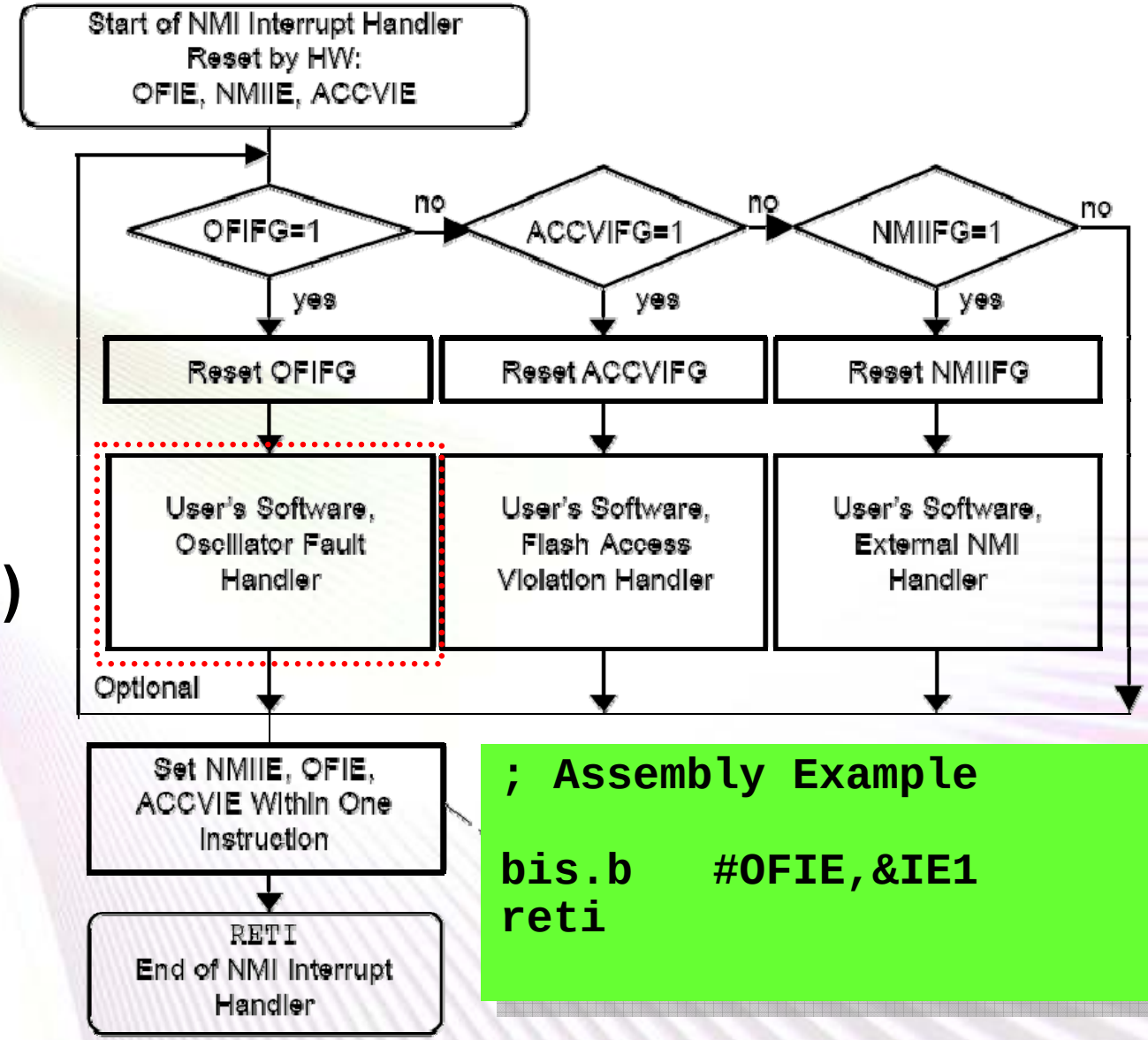


XTAL Failsafe Operation

- **XTAL Oscillator Faults are…**
  - Set if respective OSC is turned on and failing
  - Set on POR
  - Reset if oscillator functions normally again
- **DCOF set when DCO is on min/max boundary (‘F4xx)**
- **Individual Oscillator Faults will set OFIFG**
- **OFIFG can generate NMI**
- ***OFIFG switches MCLK to DCO***
- **OFIFG is latched on POR**

NMI Handler Flow

- De-mux as shown
- Re-enable with very last ISR instruction
- Use C-compiler intrinsic: _BIS_NMI_IE1(…)
- *IFG must be truly clear before re-enabling*



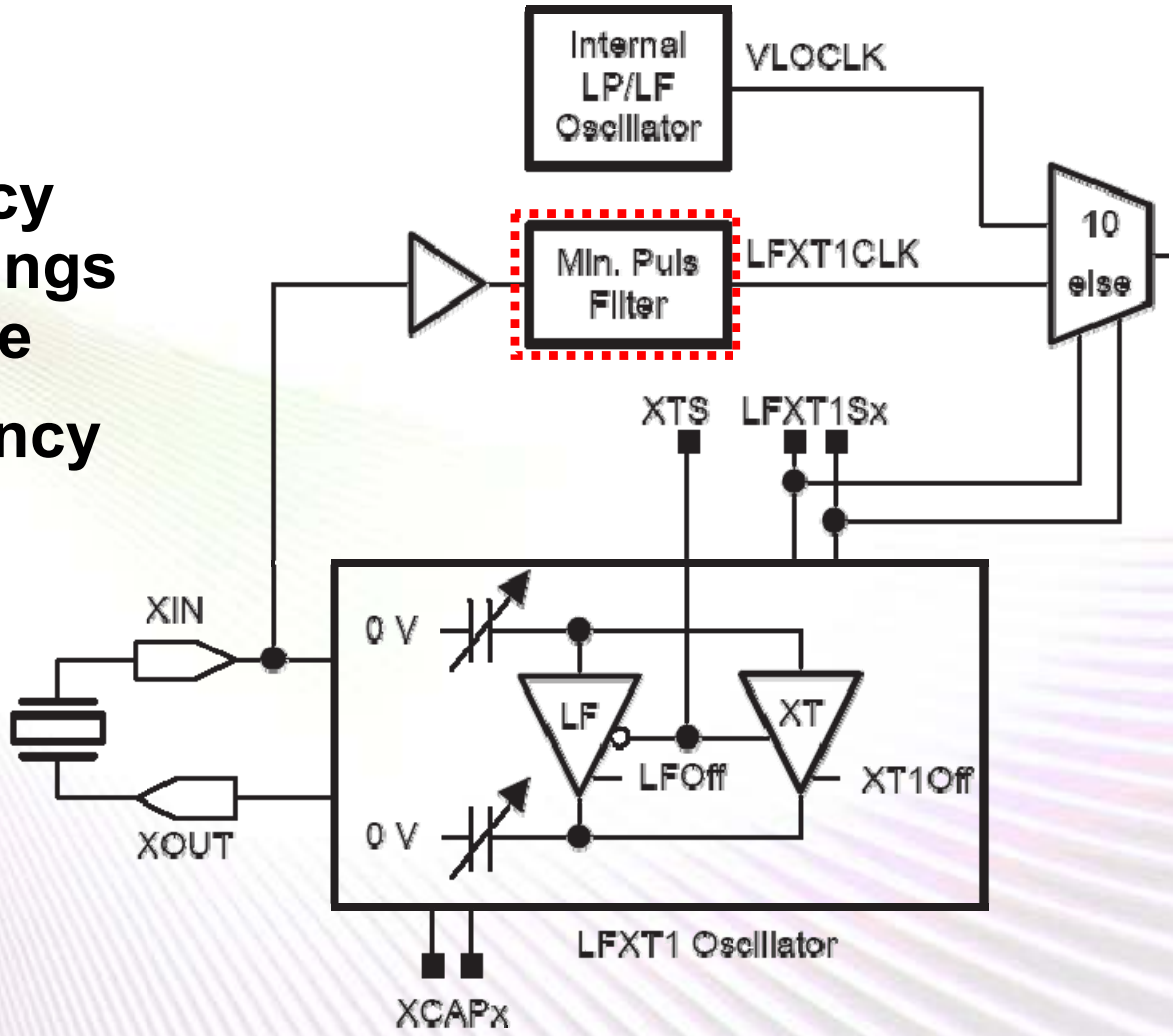

```
; Assembly Example

bis.b   #OFIE,&IE1
reti
```

XTAL Fault - Limp Mode Ideas

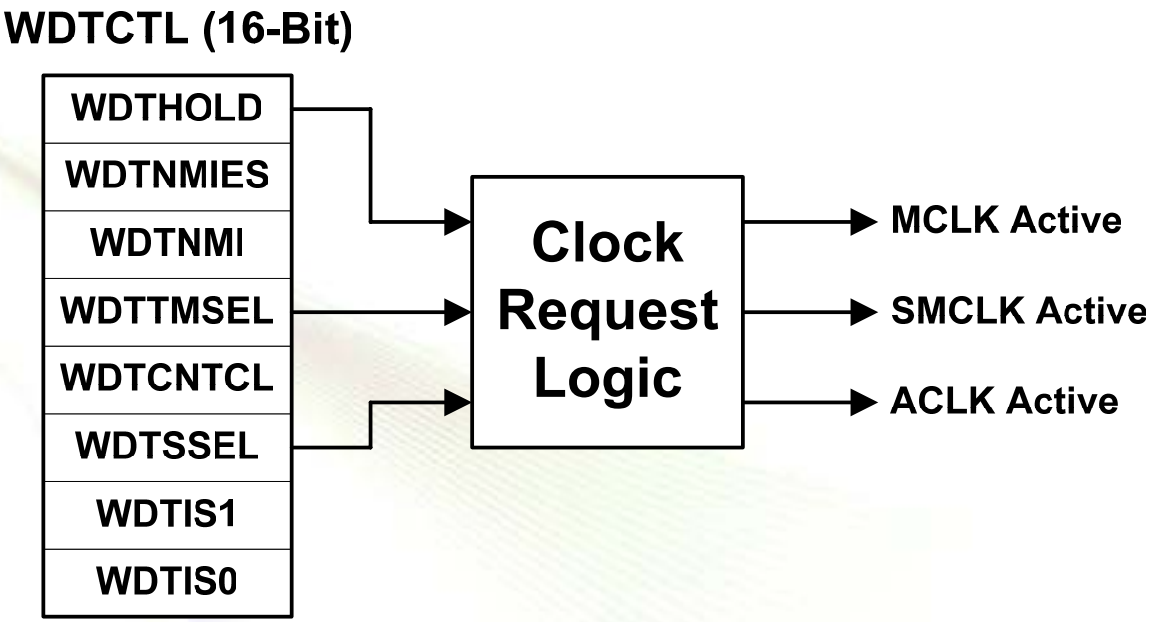
- ***How to maintain basic functionality?***
- **Constraints:**
  - Available clock sources
  - System requirements
- **'F1xx / 'F2xx / 'F4xx: Use DCO instead of HF-XTAL**
- **'F2xx: Use VLOCLK instead of LF-XTAL**
- **'F4xx: If LF-XTAL fails, disable FLL (SCG0 = 1) & control DCO manually. If LCD is used, A/C waveforms can be generated by manipulating BTCNT1 directly.**
- **Periodically clear, wait, & re-check OFIFG**
- **Use original clock-setup once OFIFG stays clear**

Minimum Pulse Clock Filter

- All ’F2xx devices
- On all clock input(s)
- Prevents high-frequency components > max ratings from entering clock tree
- Glitches & high-frequency pulses can cause erroneous instruction fetching
- Always-on
- *Increases system robustness*



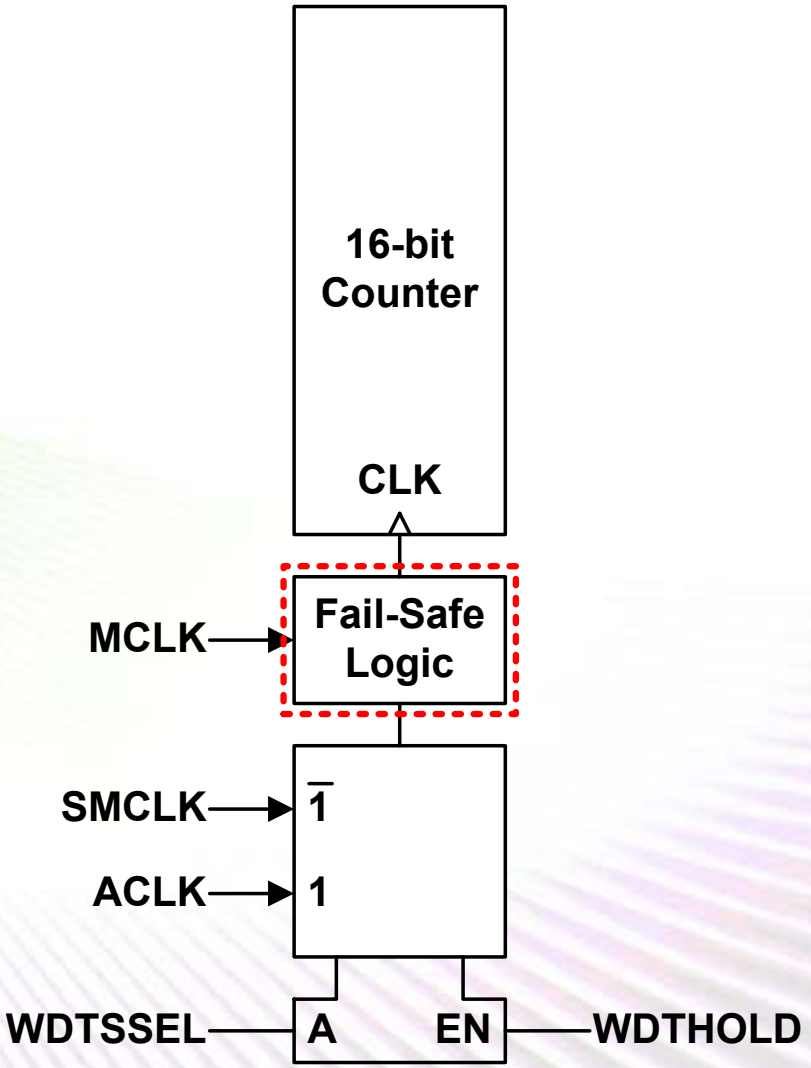
Watchdog Timer+ Clock Source



- All ‘F2xx devices and ‘F(E)42x(x)
- Active clock source can’t be disabled (WDT mode)
- May affect LPMx behavior & current consumption
- WDT(+) ***always*** powers up active on ***ALL*** MSP430’s

WDT+ Failsafe Operation

- If ACLK / SMCLK fail, clock source = MCLK (WDT+ fail safe feature)
- If MCLK is sourced from a crystal, and the crystal has failed, MCLK = DCO (XTAL fail safe feature)



PC Range Monitoring

- Additional protection against software errors
- On all MSP430F2xx devices, MSP430F(E)42x(x)
- An instruction fetch from the peripheral address range *0x0000 – 0x01FF* resets the device

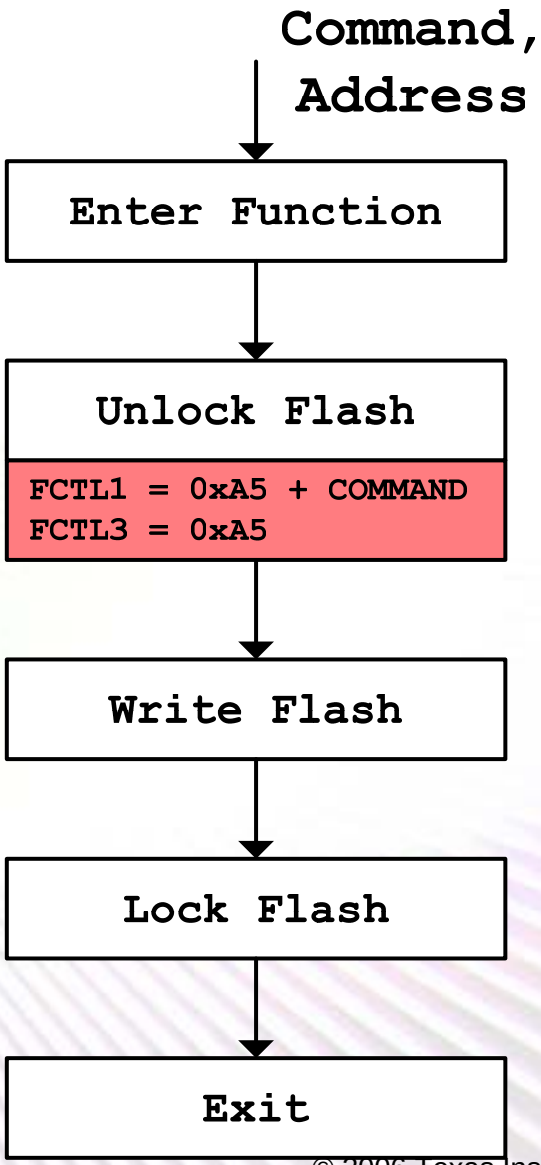
```
#include  <msp430x42x0.h>

void main(void)
{
  P1DIR |= 0x01;                  // Set P1.0 to output direction
  for (;;) {
    volatile unsigned int i = 50000;
    P1OUT ^= 0x01;                // Toggle P1.0 using XOR
    do i--; while (i != 0);       // Delay
    ((void (*)())0x170)();        // Invalid fetch causes POR
  }                               // ("call #0170h")
}
```

Agenda

- Startup and Power Supply
- ESD
- Board Design
- Crystal Considerations
- Built-in Protection
- Software Considerations

Software Considerations – Flash

- **Simple Flash Write Routine**
- **Improvements**
  - Variable generated keys
  - Address range checking
  - SVS usage during flash write
  - Destruction of variable keys before exit
  - Writing checksum of data



Software considerations - Startup

- Checksum of all program code is stored in flash
- On startup, code calculates a checksum against all program code, compares this to saved value
- Only ‘known good’ code gets executed.
- Can be accomplished as a Vcc rise / Crystal delay.

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