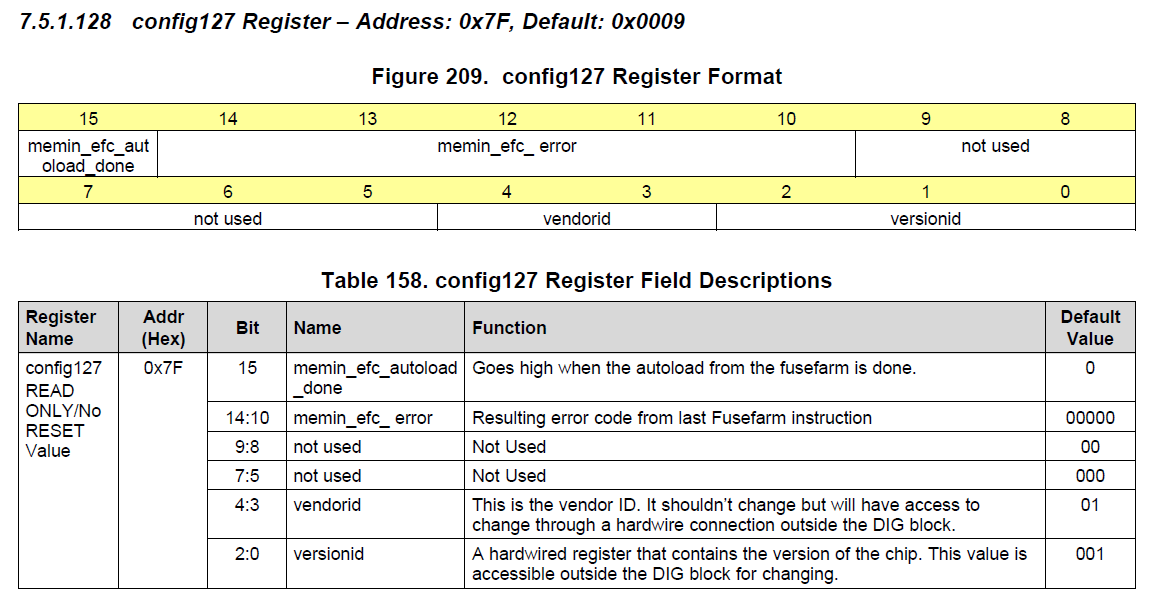
DAC39J84

Typical Start-up Procedure for DC Coupled SYSREF Network

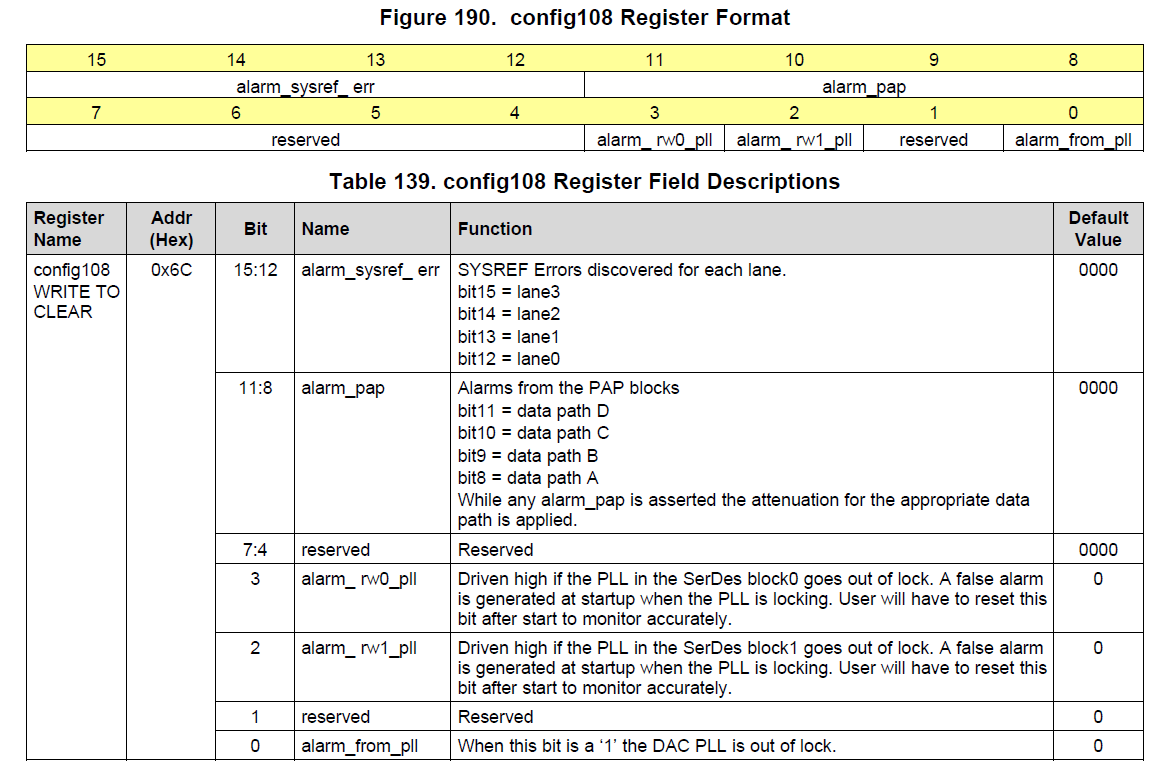
1. Power up the FPGA/ASIC and program the LMK to get the clocks running.
2. Power up the FPGA/ASIC and start the JESD204B transmitter system.
3. Power DAC3xJ84 and Provide DACCLK.
4. Reset DAC3xJ8x by toggling the RESETB pin from logic HIGH to logic LOW and then back to Logic HIGH. This will load the fusefarm.
5. Read config127 and verify bit 15 is “1” to verify fuses loaded properly.

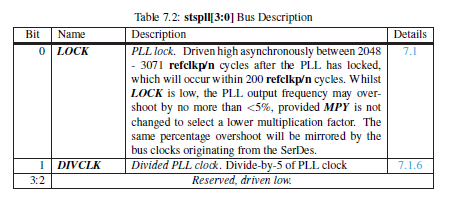


1. Program DAC3xJ8x per applications need.
   1. Clocking Configurations Registers: On-chip PLL: config49 (0x31) to config51 (0x33)
   2. SERDES Parameter: config59 (0x3B) to config63 (0x3F)
   3. JESD204B parameters: config70 (0x46) to config98 (0x62)
   4. Various DSP blocks: config0 (0x00) to config2 (0x02) and respective coefficients from config 8 (0x08) to config25 (0x19). DSP block initializers are set from config30 (0x1E) to config32 (0x20).

**Note: These can be written in any order.**

1. Write 0x0000 to config108 to clear alarms the read this register. Check alarm\_from\_pll, alarm\_rw0\_pll, and alarm\_rw1\_pll (if applicable) in config108, 0x6C to see if the on-chip PLL and SERDES PLLs are locked. If not, please double check the check the DAC programming and DACCLK and make sure it is running and at the correct frequency.





The time for the serdes PLL to lock is based on the info in the table above. It is dependent on the serdes refclk, which is programmed by the GUI. With your settings,

refclk = (1228.8MHz/2) = 614.4MHz.

The PLL lock time ~ 1.62ns \* 200 = 0.32us,

PLL lock indicator ~ 1.62ns \* 3071 = 5us + 0.32us = 5.32us.

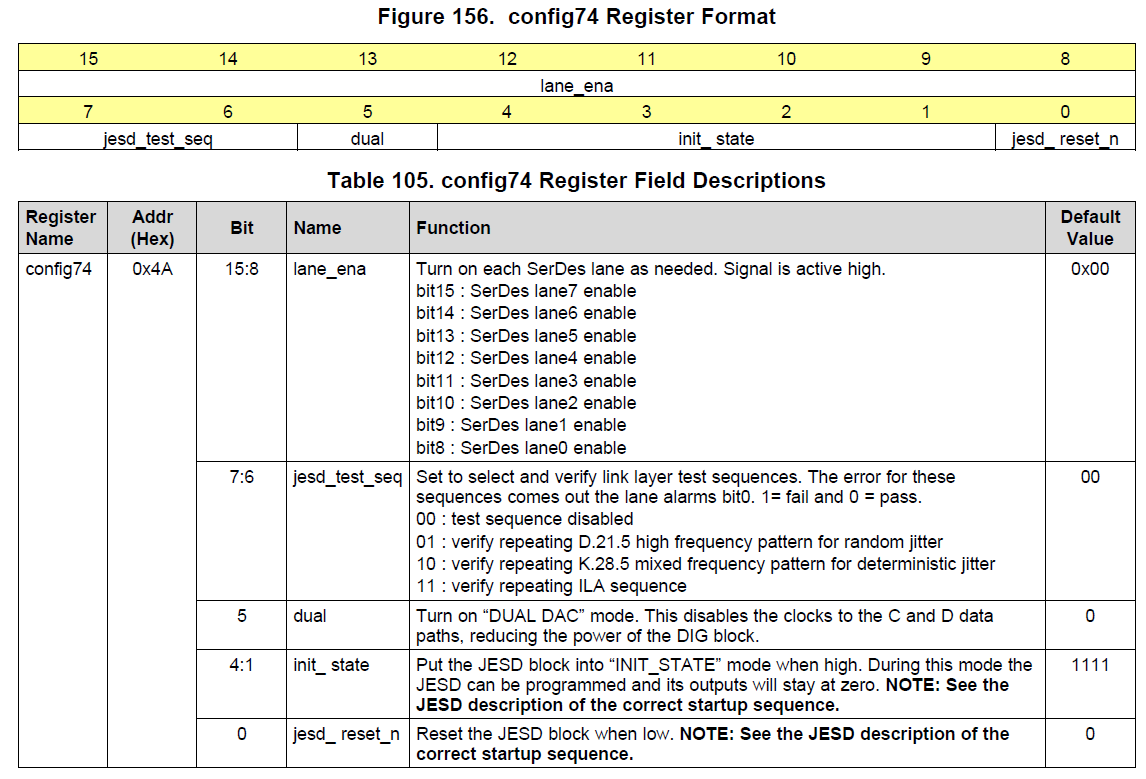
This should be plenty of time to allow the SPI read to get a valid reading.

1. Program config74 (0x4A) to initialize JESD204B block of the DAC.
   1. Enable lanes used (bits 15:8)
   2. Set init\_state (bits 4:1) = “1111”
   3. Set jesd\_reset\_n (bit 0) = “0”).

The SYNCB\_P/N should be in logic HIGH at this point. This holds the JESD block into reset, forcing the SYNCB LVDS output to a high state.

SYNC\_N\_AB will follow the SYNCBP/N state if link0 is used by default.

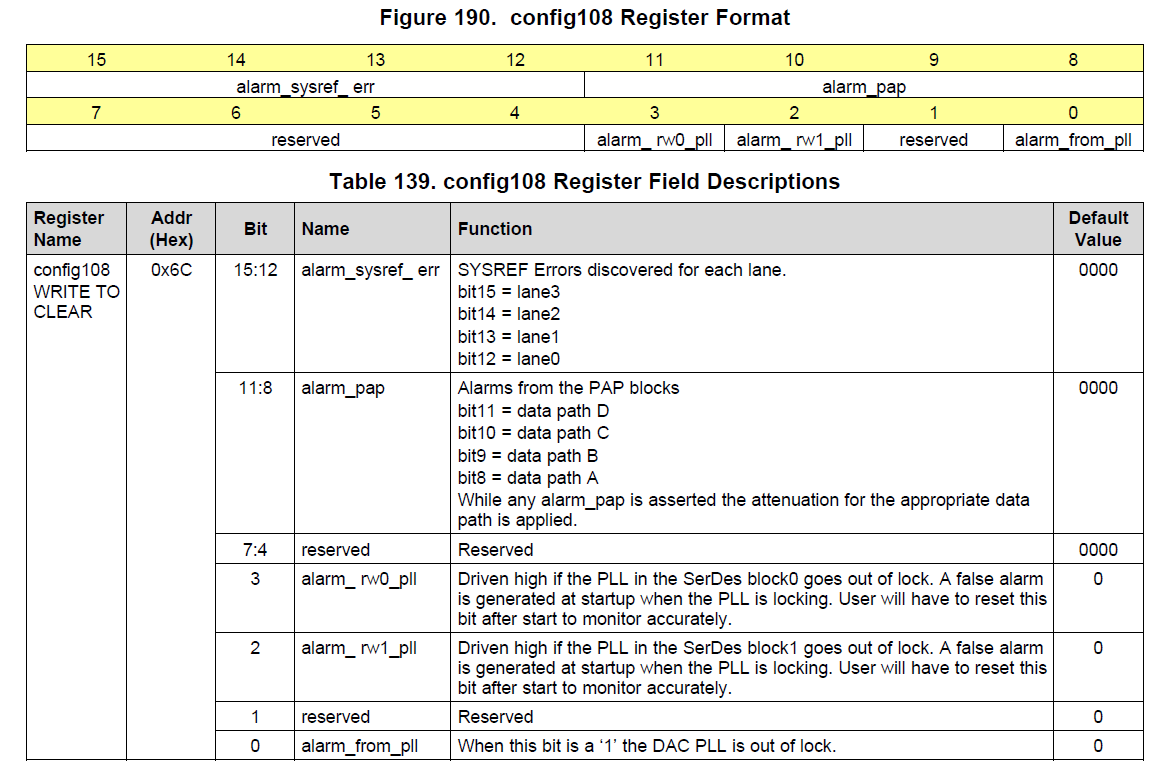
SYNC\_N\_CD will follow the SYNCBP/N state if link1 is used by default.



1. Program Config36, 0x24 = 0x30 => clock divider use sysref skip one pulse and then use next.
2. Program Config92, 0x5c = 0x0005 => use skip two pulses and then use next. Ignore link1, link2, and link3 since they are not used.
3. Program Config74 (0x4A) to initialize JESD204B block of the DAC.
   1. Enable lanes used (bits 15:8)
   2. Set init\_state (bits 4:1) = “1111”
   3. Set jesd\_reset\_n (bit 0) = “1”).
4. Program Config74 (0x4A) to initialize JESD204B block of the DAC.
   1. Enable lanes used (bits 15:8)
   2. Set init\_state (bits 4:1) = “0000”
   3. Set jesd\_reset\_n (bit 0) = “1”).

The JESD block is now waiting on SYSREF pulse to send SYNCBP/N low to start the link initialization.

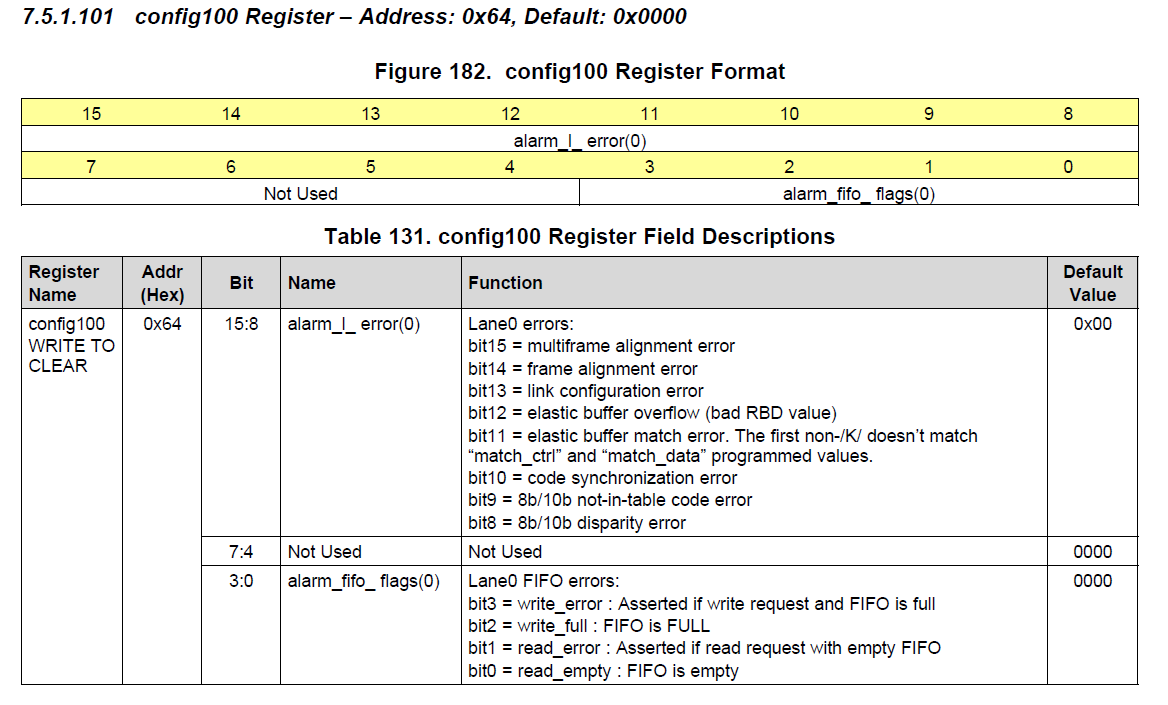
1. If periodic SYSREF is present or if gapped periodic SYSREF is triggered, the LVDS SYNCBP/N should be in logic Low. User can now disable SYSREF with known logic level present at SYSREF port.
2. Write “0000” to clear alarm\_sysref\_err in config108, bit13 for link1 (if needed), and bit12 for link0 at this point. Read bit 12 for Link0 and bit 13 for Link1 (if used) to check for errors. Table below has a typo. Bits 15:12 correspond to Links 0-3 (link 2-3 are not used) not lane0-3. Repeat step 8 to 13 again if error persists.



1. Write “0000” to clear alarms in registers config100 (0x64) to config109 (0x6D). Read the alarms and also ALARM CMOS pin L8 of the device. If error is observed, please repeat steps 7 to step 14 again to ensure correct SYSREF is provided for LMFC alignment.

Check for standard JESD204B errors, FIFO errors, and LOS errors. If these errors are observed, TI recommends to repeat steps 6 to 15 to ensure optimal initialization.

* 1. For the JESD204B errors, JESD204B standard requires at least resync upon code synchronization error, 8b/10b not in table error, and 8b/10b disparity error.
  2. The end user will need to decide how to response to other JESD204B errors.



1. If DAC3xJ8x is error free, enable TXENABLE and start DAC output transmission.