ADC调试问题

当前问题

1 根据当前对ADC的配置需求，ADC的配置流程中，ADC的寄存器配置顺序和配置值是否有问题？

2 S-PLL and C-PLL locked, JESD_STATUS = 0x1D (link up bit[6] = 0), ADC 的S-PLL 和C-PLL 显示都已经锁定，但是，link up bit[6] = 0，是否link up bit[6] 变为1，才表示ADC初始化成功了？

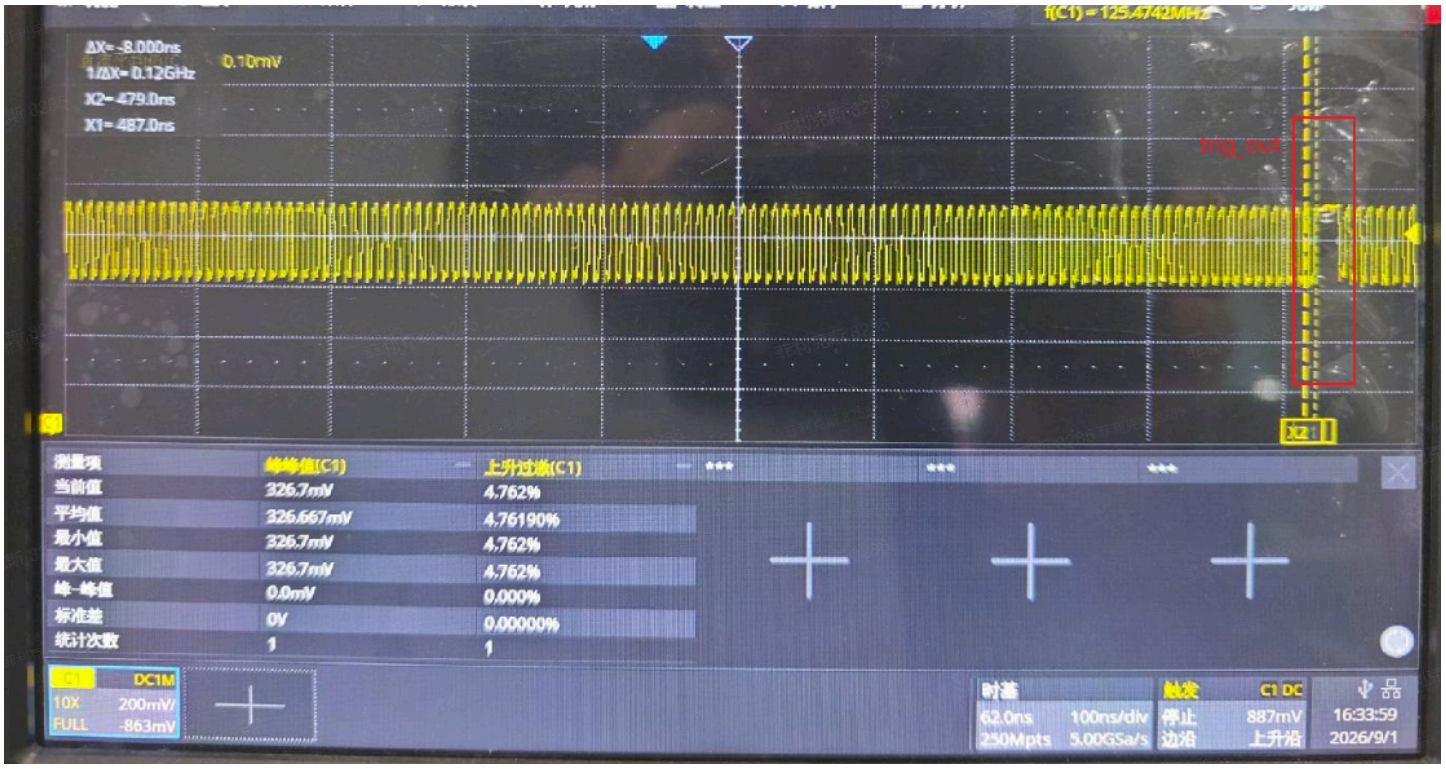
2 0x208 = 0x1D ， REALIGNED字段为1，是否是因为同步信号 sysref 没有同步成功？如果没有同步成功，可能是什么原因导致的？能够就

3 如果adc侧配置成功了，是否不需要接收侧就能够单独输出正常的数据流？

4 当前接收侧数据流：ADC->JESD204 PHY IP ->JESD204C IP, JESD204 PHY IP 的每个lane输出数据不稳定，有时候有，有时候没有，JESD204C IP的多块有时候能够锁定有时候不能。是否是因为ADC一直在进行同步，导致输出数据流不稳定？

5 ADC 输出的4对lane信号，每一对都和FPGA的GTH 接反了，即 adc_d0+接到 fpga_lane0_n,adc_d0-接到 fpga_lane0_p, 但是在接收端通过寄存器对jesd204 phy 的极性取反了，这会不会有什么问题？

6 trig_out信号输出的时钟信号不是连续的，中间有一段高电平，这可能是什么原因导致的？



7 0x330 、0x332、0x33C、0x33E，这几个寄存器是否需要配置，如果需要，有什么配置方法吗?

8 对于硬件上面有什么需要注意的？是否可以给出一些排查建议

- **下面内容为ADC配置的相关信息**

1 ADC特性

- 型号：ADC09DJ1300
- 通道：双通道
- 分辨率：9 位
- 最大采样率：1.3GSPS
- JMODE模式：14
- 线速率：8.04375 Gbps

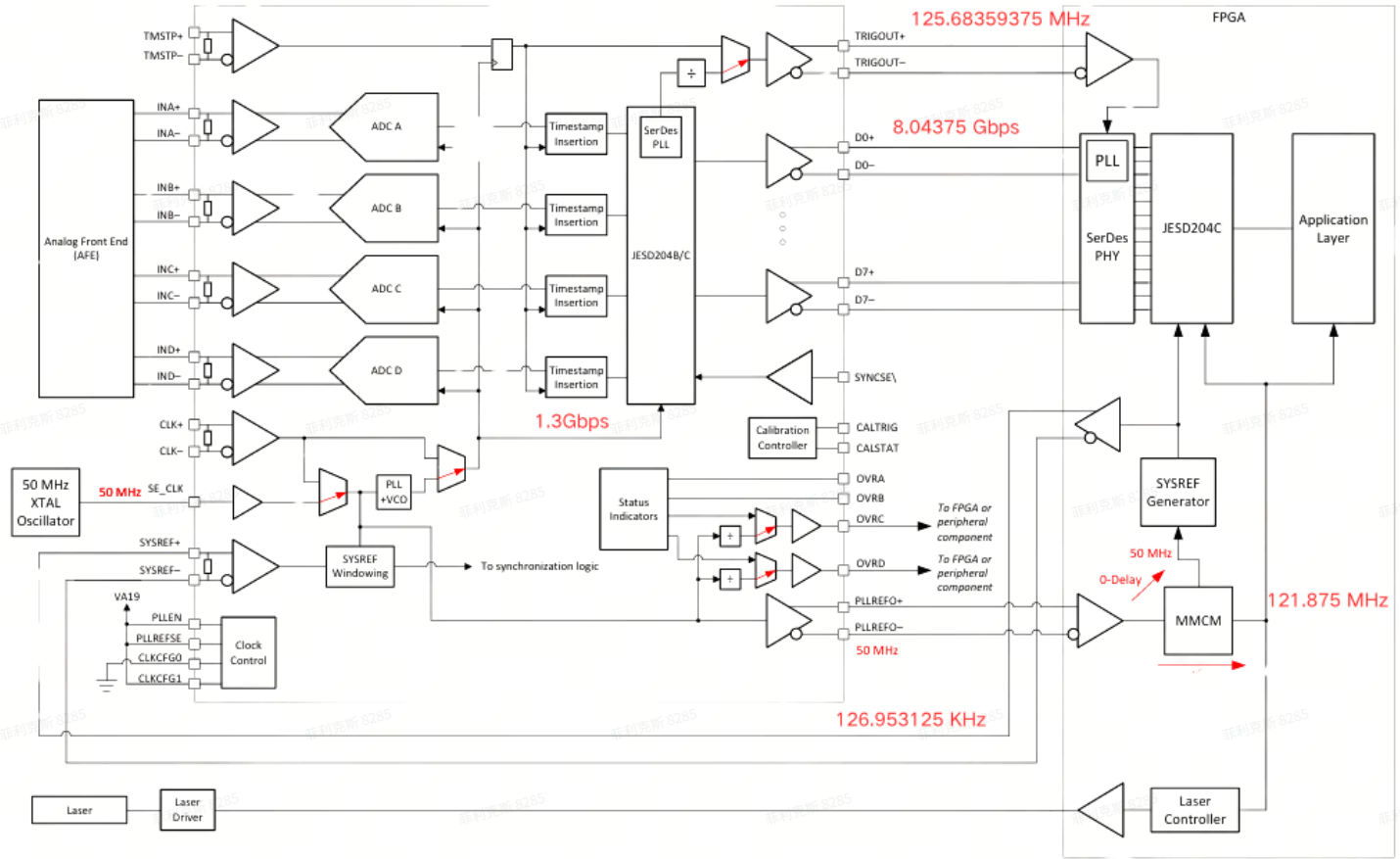
表 8-17. Operating Modes for Dual Channel Device

OPERATING MODE	USER-SPECIFIED PARAMETER		DERIVED PARAMETERS												INPUT CLOCK RANGE (MHz)
	JMODE	K [Min:Step:Max]	Encoding	N	CS	N'	CF	L	M	F	S	HD	E	R (Fbit / Fclk)	
9-Bit, 8B/10B, 4 Lanes	0	4:4:256	8B/10B	9	0	12	0	4	4(1)	8	5	0	—	8	500-1300
9-Bit, 8B/10B, 3 Lanes	1	16:16:256	8B/10B	9	0	12	0	3	2	2	2	1	—	10	500-1300
8-Bit, 8B/10B, 2 Lanes	2	32:32:256	8B/10B	8	0	8	0	2	2	1	1	0	—	10	500-1300
9-Bit, 8B/10B, 2 Lanes	3	32:32:256	8B/10B	9	0	10	0	2	2	5	4	0	—	12.5	500-1300
9-Bit, 64B/66B, 2 Lanes	4	128(2)	64B/66B	9	0	12	0	2	2	2	1	1	3	16.5	500-1040
8-Bit, 64B/66B, 1 Lane	5	128(2)	64B/66B	8	0	8	0	1	2	2	1	0	1	16.5	500-1040
9-Bit, 64B/66B, 3 Lanes	6	128(2)	64B/66B	9	0	12	0	3	2	2	2	1	3	8.25	500-1300
8-Bit, 64B/66B, 2 Lanes	7	256(2)	64B/66B	8	0	8	0	2	2	1	1	0	1	8.25	500-1300
9-Bit, 64B/66B, 2 Lanes	8	256(2)	64B/66B	9	0	12	0	2	2	3	2	0	3	12.375	500-1300
8-Bit, 8B/10B, 4 Lanes	9	32:32:256	8B/10B	8	0	8	0	3	2	1	2	0	—	5	500-1300
9-Bit, 8B/10B, 4 Lanes	10	32:32:256	8B/10B	9	0	10	0	4	4(1)	5	4	0	—	6.25	500-1300
9-Bit, 8B/10B, 8 Lanes	11	4:4:256	8B/10B	9	0	12	0	8	8(1)	8	5	0	—	4	500-1300
8-Bit, 8B/10B, 8 Lanes	12	32:32:256	8B/10B	8	0	8	0	8	2	1	4	0	—	2.5	500-1300
9-Bit, 8B/10B, 8 Lanes	13	32:32:256	8B/10B	9	0	10	0	8	8(1)	5	4	0	—	3.125	500-1300
9-Bit, 64B/66B, 4 Lanes	14	256(2)	64B/66B	9	0	12	0	4	4(1)	3	2	0	3	6.1875	500-1300
9-Bit, 64B/66B, 8 Lanes	15	256(2)	64B/66B	9	0	12	0	8	8(1)	3	2	2	2	3.09375	500-1300

(1) M equals L in these modes to allow the samples to be sent in time-order over L lanes without unnecessary buffering. The M parameter does not represent the actual number of converters. Interleave the M sample streams from each link in the receiver to produce the correct sample data; see mode diagrams for more details.

(2) In the 64B/66B modes, the K parameter is not directly programmable. K is related to E and F according to the equation K = 8 x 32 x E/F. K is not an actual parameter of the 64B/66B link layer.

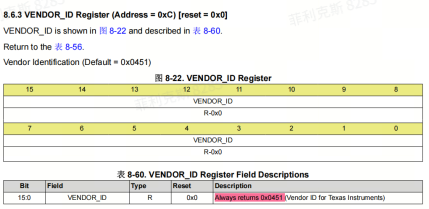
3 时钟架构



- Line rate: 8.04375 Gbps
- TRIGOUT: 8.04375/64 *1000= 125.68359375 MHz
- SYSREF: 8.04375/(66*32*3*10) * 1000*1000 = 126.953125 KHz
- CORE CLOCK: 8.04375/66 * 1000 = 121.875 MHz
- fpga使用的系统时钟为ADC给出的50M
- Fpga 型号：xczu4ev-sfvc-784-2

4 ADC配置流程

- 默认使用前台校准，只在初始化过程中校准一次
- SPI 接口
  - SCLK和SDI 是空闲为低
  - SCS 是空闲为高
  - SDO 是空闲为高阻态
  - 使用streaming mode时，默认是Ascend
  - 每个寄存器之间的间隔时间设置为10us
- 注： 以下Num 的序号即为寄存器配置的顺序

Num	Register Name	W/R	Address	Data	Reset	Description
0	**VENDOR_ID**	r	0xC		0x0	读出值为0x0451才进行初始化(测试通路使用) 
1	**CONFIG_A**	w	0x00	0xB0	0x30	• 芯片复位使能，复位时间至少750ns。

8.6.3 VENDOR_ID Register (Address = 0xC) [reset = 0x0]
VENDOR_ID is shown in 图 8-22 and described in 表 8-60.
Return to the 表 8-56.
Vendor Identification (Default = 0x0451)

图 8-22. VENDOR_ID Register

15	14	13	12	11	10	9	8
VENDOR_ID							
R-0x0							
7	6	5	4	3	2	1	0
VENDOR_ID							
R-0x0							

表 8-60. VENDOR_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	VENDOR_ID	R	0x0	Always returns 0x0451 (Vendor ID for Texas Instruments)

						6.6.1 CONFIG_A Register (Address = 0x0) [reset = 0x30] CONFIG_A is shown in Figure 6-20 and described in Table 6-58. Return to the Summary Table. Configuration A (default: 0x30) **Figure 6-20. CONFIG_A Register** 7 6 5 4 3 2 1 0 SOFT_RESET RESERVED ASCEND SDO_ACTIVE RESERVED R/W-0x0 R/W-0x0 R/W-0x1 R-0x1 R/W-0x0 **Table 6-58. CONFIG_A Register Field Descriptions** Bit / Field / Type / Reset / Description 7 / SOFT_RESET / R/W / 0x0 / Setting this bit causes a full reset of the chip and all SPI registers (including CONFIG_A). This bit is self-clearing. After writing this bit, the part may take up to 750ns to reset. During this time, do not perform any SPI transactions. 6 / RESERVED / R/W / 0x0 / Must write default value. 5 / ASCEND / R/W / 0x1 / 0 : Address is decremented during streaming reads/writes 1 : Address is incremented during streaming reads/writes (default) 4 / SDO_ACTIVE / R / 0x1 / Always returns 1. Always use SDO for SPI reads. No SDIO mode supported. 3:0 / RESERVED / R/W / 0x0 /
2	**INIT_STATUS**	r	0x270	0x01	0x00	每间隔1ms轮询一次，直到INIT_STATUS寄存器读出值为1，表示完成复位，才进行下一步。 **6.6.55 INIT_STATUS Register (Address = 0x270) [reset = 0x0]** INIT_STATUS is shown in Figure 6-74 and described in Table 6-112. Return to the Summary Table. Initialization Status (read-only) **Figure 6-74. INIT_STATUS Register** 7 6 5 4 3 2 1 0 RESERVED INIT_DONE R-0x0 R-0x0 **Table 6-112. INIT_STATUS Register Field Descriptions** Bit / Field / Type / Reset / Description 7:1 / RESERVED / R / 0x0 / 0 / INIT_DONE / R / 0x0 / Returns 1 when the initialization logic has finished initializing the device. This indicates that it is now safe to proceed with startup. No SPI transactions should be performed before INIT_DONE returns 1 (except SOFT_RESET).
3	**CPLL_OVR**	w	0x58	0x83	0x00	• 使用SPI进行寄存器配置 • ADC使用单端源时钟 50M **6.6.18 CPLL_OVR Register (Address = 0x58) [reset = 0x00]** CPLL_OVR is shown in Figure 6-37 and described in Table 6-75. Return to the Summary Table. C-PLL Pin Override (default: 0x00) **Figure 6-37. CPLL_OVR Register** 7 6 5 4 3 2 1 0 CPLL_OVR_EN RESERVED DIVREF_D_MODE DIVREF_C_MODE CPLLREF_SE_OVR_VALUE CPLL_EN_OVR_VALUE R/W-0x0 R/W-0x0 R/W-0x0 R/W-0x0 R/W-0x0 R/W-0x0 **Table 6-75. CPLL_OVR Register Field Descriptions** Bit / Field / Type / Reset / Description 7 / CPLL_OVR_EN / R/W / 0x0 / Set this bit to ignore the C-PLL configuration pins and use SPI registers instead. 0 : Pin Mode : The C-PLL is controlled by chip pins (PLL_EN, PLLREF_SE, CLKCFG0, CLKCFG1) 1 : SPI Mode : The C-PLL is controlled by SPI registers (CPLLREF_SE_OVR_VALUE, CPLL_EN_OVR_VALUE, DIVREF_C_MODE, DIVREF_D_MODE) 6 / RESERVED / R/W / 0x0 / Must write default value. 5:4 / DIVREF_D_MODE / R/W / 0x0 / When CPLL_OVR_EN=1, this field sets the ORD output function. When CPLL_OVR_EN=0, this field has no effect (CLKCFG0 and CLKCFG1 controls ORD functionality). 0 : Divided reference output is disabled. 1 : Output C-PLL reference clock divided by 1 on ORD. 2 : Output C-PLL reference clock divided by 2 on ORD. 3 : Output C-PLL reference clock divided by 4 on ORD. **Important Note: ORD cannot produce a clock unless ORC is also producing a clock). 3:2 / DIVREF_C_MODE / R/W / 0x0 / When CPLL_OVR_EN=1, this field sets the ORC output function. When CPLL_OVR_EN=0, this field has no effect (CLKCFG0 and CLKCFG1 controls ORC functionality). 0 : Divided reference output is disabled. 1 : Output C-PLL reference clock divided by 1 on ORC. 2 : Output C-PLL reference clock divided by 2 on ORC. 3 : Output C-PLL reference clock divided by 4 on ORC. 1 / CPLLREF_SE_OVR_VALUE / R/W / 0x0 / When CPLL_OVR_EN=1, this bit enables the single-ended C-PLL reference clock input (SE_CLK) when set to 1 instead of the PLLREF_SE pin. 0 / CPLL_EN_OVR_VALUE / R/W / 0x0 / When CPLL_OVR_EN=1, this bit enables the C-PLL when set to 1 instead of the PLL_EN pin.
4	**CPLL_RESET**	w	0x5C	0x01	0x00	(固定值)C-PLL / VCO 校准复位 **6.6.20 CPLL_RESET Register (Address = 0x5C) [reset = 0x00]** CPLL_RESET is shown in Figure 6-39 and described in Table 6-77. Return to the Summary Table. C-PLL / VCO Calibration Reset (default: 0x00) **Figure 6-39. CPLL_RESET Register** 7 6 5 4 3 2 1 0 RESERVED CPLL_RESET R/W-0x0 R/W-0x0 **Table 6-77. CPLL_RESET Register Field Descriptions** Bit / Field / Type / Reset / Description 7:1 / RESERVED / R/W / 0x0 / Must write default value. 0 / CPLL_RESET / R/W / 0x0 / C-PLL / VCO calibration reset. Program CPLL_RESET=1 before programming the C-PLL (PLL_P_DIV, PLL_V_DIV, PLL_N_DIV, VCO_BIAS or VCO_CAL_CTRL). Program CPLL_RESET=0 after programming is completed.
5	**CPLL_VCOCTRL1**	w	0x3F	0x4A	0x4F	(固定值)Sets the bias levels for the C-PLL VCO **6.6.15 CPLL_VCOCTRL1 Register (Address = 0x3F) [reset = 0x4F, recommended 0x4A]** CPLL_VCOCTRL1 is shown in Figure 6-34 and described in Table 6-72. C-PLL Feedback Divider N (default: 0x4F) **Figure 6-34. CPLL_VCOCTRL1 Register** 7 6 5 4 3 2 1 0 RESERVED VCO_BIAS R/W-0x0 R/W-0x4F **Table 6-72. CPLL_VCOCTRL1 Register Field Descriptions** Bit / Field / Type / Reset / Description 7 / RESERVED / R/W / 0x0 / Must write default value. 6:0 / VCO_BIAS / R/W / 0x4F / Sets the bias levels for the C-PLL VCO. Write 0x4A to this field when using the C-PLL. Do not use the default value of 0x4F.
6	**CPLL_FBDIV1**	w	0x3D	0x06	0x00	配置ADC PLL 分频值 • PLL_P_DIV为2，PLL_V_DIV为3

						6.6.13 CPLL_FBDIV1 Register (Address = 0x3D) [reset = 0x00] CPLL_FBDIV1 is shown in Figure 6-32 and described in Table 6-70. Return to the Summary Table. C-PLL Feedback Divider V and P (default: 0x00) **Figure 6-32. CPLL_FBDIV1 Register** 7 6 5 4 3 2 1 0 RESERVED PLL_P_DIV PLL_V_DIV R/W-0x0 R/W-0x0 R/W-0x0 **Table 6-70. CPLL_FBDIV1 Register Field Descriptions** Bit | Field | Type | Reset | Description 7:4 | RESERVED | R/W | 0x0 | Must write default value. 3:2 | PLL_P_DIV | R/W | 0x0 | Controls the second feedback divider of C-PLL. The output of this divider is the sampling clock. Set CPLL_RESET=1 before changing PLL_P_DIV. 0 : divide-by-1 (default) 1 : divide-by-2 2 : divide-by-4 3 : RESERVED 1:0 | PLL_V_DIV | R/W | 0x0 | Controls the first feedback divider of C-PLL. The output of this divider feeds the P divider. Set CPLL_RESET=1 before changing PLL_V_DIV. 0 : divide-by-5 (default) 1 : divide-by-4 2 : divide-by-3 3 : RESERVED
7	**CPLL_FBDIV2**	w	0x3E	0x1A	0x20	配置ADC采样速率 • PLL_N_DIV为26(采样速率：50M*26 = 1.3G) **6.6.14 CPLL_FBDIV2 Register (Address = 0x3E) [reset = 0x20]** CPLL_FBDIV2 is shown in Figure 6-33 and described in Table 6-71. Return to the Summary Table. C-PLL Feedback Divider N (default: 0x20) **Figure 6-33. CPLL_FBDIV2 Register** 7 6 5 4 3 2 1 0 RESERVED PLL_N_DIV R/W-0x0 R/W-0x20 **Table 6-71. CPLL_FBDIV2 Register Field Descriptions** Bit | Field | Type | Reset | Description 7:6 | RESERVED | R/W | 0x0 | Must write default value. 5:0 | PLL_N_DIV | R/W | 0x20 | Controls the third feedback divider of C-PLL (default is divide-by-32). This divider divides the sampling clock to generate the PFD feedback clock. The value of PLL_N_DIV is the divider value. Values from 1 to 63 are supported. Set CPLL_RESET=1 before changing PLL_N_DIV.
8	**VCO_CAL_CTRL**	w	0x5D	0x41	0x40	1、使能VCO校准 2、调节VCO引擎给到C-PLL的时间 **6.6.21 VCO_CAL_CTRL Register (Address = 0x5D) [reset = 0x40]** VCO_CAL_CTRL is shown in Figure 6-40 and described in Table 6-78. Return to the Summary Table. VCO Calibration Control (default: 0x40) **Figure 6-40. VCO_CAL_CTRL Register** 7 6 5 4 3 2 1 0 RESERVED VCO_CAL_STL RESERVED VCO_CAL_EN R/W-0x0 R/W-0x4 R/W-0x0 R/W-0x0 **Table 6-78. VCO_CAL_CTRL Register Field Descriptions** Bit | Field | Type | Reset | Description 7 | RESERVED | R/W | 0x0 | Must write default value. 6:4 | VCO_CAL_STL | R/W | 0x4 | Program this field to adjust the settling time that the VCO calibration engine gives to the C-PLL each time it changes the VCO frequency trim (VCO_FREQ_TRIM). Larger numbers result in longer settling times. 3:1 | RESERVED | R/W | 0x0 | Must write default value. 0 | VCO_CAL_EN | R/W | 0x0 | Set this bit to enable the VCO calibration engine. The calibration commences once CPLL_RESET is programmed to 0. The calibration will automatically tune VCO_FREQ_TRIM to center the VCO frequency based on the reference frequency and PLL configuration. Note: The VCO_CAL_CTRL register should only be changed when CPLL_RESET=1.
9	**CPLL_RESET**	w	0x5C	0x00	0x00	取消C-PLL / VCO 校准复位 **6.6.20 CPLL_RESET Register (Address = 0x5C) [reset = 0x00]** CPLL_RESET is shown in Figure 6-39 and described in Table 6-77. Return to the Summary Table. C-PLL / VCO Calibration Reset (default: 0x00) **Figure 6-39. CPLL_RESET Register** 7 6 5 4 3 2 1 0 RESERVED CPLL_RESET R/W-0x0 R/W-0x0 **Table 6-77. CPLL_RESET Register Field Descriptions** Bit | Field | Type | Reset | Description 7:1 | RESERVED | R/W | 0x0 | Must write default value. 0 | CPLL_RESET | R/W | 0x0 | C-PLL / VCO calibration reset. Program CPLL_RESET=1 before programming the C-PLL (PLL_P_DIV, PLL_V_DIV, PLL_N_DIV, VCO_BIAS or VCO_CAL_CTRL). Program CPLL_RESET=0 after programming is completed.
10	**VCO_CAL_STATUS**	r	0x5E	0x01	0x00	• 返回1，表示VCO校准完成。 • 等待10ms之后，每间隔1ms轮询一次，并打印，直到读出数据bit[0]为1表示VCO完成校准，才进行下一步。 **6.6.22 VCO_CAL_STATUS Register (Address = 0x5E) [reset = 0x0]** VCO_CAL_STATUS is shown in Figure 6-41 and described in Table 6-79. Return to the Summary Table. VCO Calibration Status (read-only) (default: undefined) **Figure 6-41. VCO_CAL_STATUS Register** 7 6 5 4 3 2 1 0 RESERVED VCO_CAL_DONE R-0x0 R-0x0 **Table 6-79. VCO_CAL_STATUS Register Field Descriptions** Bit | Field | Type | Reset | Description 7:1 | RESERVED | R | 0x0 | 0 | VCO_CAL_DONE | R | 0x0 | This bit returns '1' once the VCO calibration engine has completed calibration (or calibration was skipped because VCO_CAL_EN=0). Once the calibration is completed, you can safely read or write the VCO_FREQ_TRIM register (never write VCO_FREQ_TRIM during calibration).

11	**JESD_EN**	w	0x200	0x00	0x01	0 : 关闭JESD204C 接口 6.6.41 JESD_EN Register (Address = 0x200) [reset = 0x01] JESD_EN is shown in Figure 6-60 and described in Table 6-98. JESD204C Subsystem Enable (default: 0x01) Figure 6-60. JESD_EN Register 7 6 5 4 3 2 1 0 RESERVED JESD_EN R/W-0x0 R/W-0x1 Table 6-98. JESD_EN Register Field Descriptions Bit Field Type Reset Description 7:1 RESERVED R/W 0x0 Must write default value. 0 JESD_EN R/W 0x1 0 : Disable JESD204C interface 1 : Enable JESD204C interface Note: Before altering other JESD204C registers, you must clear JESD_EN. When JESD_EN is 0, the block is held in reset and the serializers are powered down. The clocks are gated off to save power. The LMFC/LEMC counter is also held in reset, so SYSREF will not align the LMFC/LEMC. Note: Always set CAL_EN before setting JESD_EN. Note: Always clear JESD_EN before clearing CAL_EN.
12	**CAL_EN**	w	0x61	0x00	0x01	关闭校准使能 • 在JESD_EN 之前先设置 CAL_EN。请务必在清零 CAL_EN 之前先清零 JESD_EN 8.6.23 CAL_EN Register (Address = 0x61) [reset = 0x01] CAL_EN is shown in 图 8-42 and described in 表 8-80. Return to the 表 8-56. Calibration Enable (Default: 0x01) 图 8-42. CAL_EN Register 7 6 5 4 3 2 1 0 RESERVED CAL_EN R/W-0x0 R/W-0x1 表 8-80. CAL_EN Register Field Descriptions Bit Field Type Reset Description 7:1 RESERVED R/W 0x0 Must write default value. 0 CAL_EN R/W 0x1 Calibration Enable. Set high to run calibration. Set low to hold calibration in reset to program new calibration settings. Clearing CAL_EN also resets the clock dividers that clock the digital block and JESD204C interface. Some calibration registers require clearing CAL_EN before making any changes. All registers with this requirement contain a note in their descriptions. After changing the registers, set CAL_EN to re-run calibration with the new settings. Always set CAL_EN before setting JESD_EN. Always clear JESD_EN before clearing CAL_EN.
13	**LOW_POWER 1**	w	0x37	0x46	0x4B	**本方案采用默认值** 0x06 : Low Power Mode (only valid when sampling rate is less than or equal to 1 GSPS) 0x0F : High Performance Mode (default) 6.6.10 LOW_POWER1 Register (Address = 0x37) [reset = 0x4B] LOW_POWER1 is shown in Figure 6-29 and described in Table 6-67. Return to the Summary Table. Low Power Mode 1 (default: 0x4B) Figure 6-29. LOW_POWER1 Register 7 6 5 4 3 2 1 0 LOW_POW_MODE1 R/W-0x4B Table 6-67. LOW_POWER1 Register Field Descriptions Bit Field Type Reset Description 7:0 LOW_POW_MODE1 R/W 0x4B Set this register along with LOW_POWER2, LOW_POWER3 and LOW_POWER4 to enable Low Power Mode. All registers must be set together. Calibration must be performed after changing the operating mode: 0x46 : Low Power Mode (only valid when sampling rate is less than or equal to 1 GSPS) 0x4B : High Performance Mode (default) All other values are RESERVED Note: Must set CAL_EN to 0 and JESD_EN to 0 before changing this register.
14	**LOW_POWER 2**	w	0x29A	0x06	0x0F	**本方案采用默认值** 0x06 : Low Power Mode (only valid when sampling rate is less than or equal to 1 GSPS) 0x0F : High Performance Mode (default)
15	**LOW_POWER 3**	w	0x29B	0x00	0x04	**本方案采用默认值** 0x00 : Low Power Mode (only valid when sampling rate is less than or equal to 1 GSPS)

<table>
<tr><td></td><td></td><td></td><td></td><td></td><td></td><td>0x04 : High Performance Mode (default)</td></tr>
<tr><td>16</td><td>LOW_POWER 4</td><td>w</td><td>0x29C</td><td>0X14</td><td>0X1B</td><td>本方案采用默认值
0x14 : Low Power Mode (only valid when sampling rate is less than or equal to 1 GSPS)
0x1B : High Performance Mode (default)</td></tr>
<tr><td>17</td><td>JMODE</td><td>w</td><td>0x201</td><td>0x0E</td><td>0x00</td><td>• 指定 JESD204C 输出的 JMODE 模式
• 工程使用JMODE 14
6.6.42 JMODE Register (Address = 0x201) [reset = 0x00]
JMODE is shown in Figure 6-61 and described in Table 6-99.
Return to the Summary Table.
JESD204C Mode (default: 0x00)
Figure 6-61. JMODE Register
7 6 5 4 3 2 1 0
RESERVED | JMODE
R/W-0x0 | R/W-0x0
Table 6-99. JMODE Register Field Descriptions
Bit | Field | Type | Reset | Description
7:6 | RESERVED | R/W | 0x0 | Must write default value.
5:0 | JMODE | R/W | 0x0 | Specifies the JESD204C output mode. See JESD204C Mode table. Note: This register should only be changed when JESD_EN=0 and CAL_EN=0.</td></tr>
<tr><td>18</td><td>KM1</td><td>w</td><td>0x202</td><td>0xFF</td><td>0x1F</td><td>注意：对于使用 64B/66B 链路层的模式，KM1 寄存器将被忽略
6.6.43 KM1 Register (Address = 0x202) [reset = 0x1F]
KM1 is shown in Figure 6-62 and described in Table 6-100.
Return to the Summary Table.
JESD204C K Parameter (minus 1) (default: 0x1F)
Figure 6-62. KM1 Register
7 6 5 4 3 2 1 0
KM1
R/W-0x1F
Table 6-100. KM1 Register Field Descriptions
Bit | Field | Type | Reset | Description
7:0 | KM1 | R/W | 0x1F | K is the number of frames per multiframe and this register must be programmed as K-1. Depending on the JMODE setting, there are constraints on the legal values of K (see K parameter in JESD204C Mode table). The default value is KM1=31, which corresponds to K=32.
Note: For modes using the 64B/66B link layer, the KM1 register is ignored and the value of K is determined from E and F (which are derived from JMODE). The effective value of K is 256*E/F.
Note: This register should only be changed when JESD_EN is 0.</td></tr>
<tr><td>19</td><td>JCTRL (lane)</td><td>w</td><td>0x204</td><td>0x00</td><td>0x03</td><td>• lane mapping使用默认方式
• ADC输出数据格式： Offset binary
6.6.45 JCTRL Register (Address = 0x204) [reset = 0x03]
JCTRL is shown in Figure 6-64 and described in Table 6-102.
Return to the Summary Table.
JESD204C Control (default: 0x03)
Figure 6-64. JCTRL Register
7 6 5 4 3 2 1 0
RESERVED | ALT_LANES | SYNC_SEL | SFORMAT | SCR
R/W-0x0 | R/W-0x0 | R/W-0x0 | R/W-0x1 | R/W-0x1
Table 6-102. JCTRL Register Field Descriptions
Bit | Field | Type | Reset | Description
7:5 | RESERVED | R/W | 0x0 | Must write default value.
Table 6-102. JCTRL Register Field Descriptions (continued)
Bit | Field | Type | Reset | Description
4 | ALT_LANES | R/W | 0x0 | 0 : Normal lane mapping (default) as shown in the JESD204C output mode section.
Lanes 0 thru L−1 are used.
1 : Alternate lane mapping (use upper lanes).
Lanes 4 to 4+L-1 are used. Lanes 0 to 3 are unused. This option is only supported when JMODE selects a mode that uses 4 or less lanes per link (L<=4). The behavior is undefined for modes that use more than 4 lanes.
3:2 | SYNC_SEL | R/W | 0x0 | 0 : Use the SYNCSE input for SYNC~ function (default)
1 : Use the TMSTPx input for SYNC~ function. TMSTP_RECV_EN must also be set.
2 : Do not use any SYNC~ input pin (use JSYNC_N as a software SYNC~)
1 | SFORMAT | R/W | 0x1 | Output sample format for JESD204C samples
0 : Offset binary
1 : Signed 2's complement (default)</td></tr>
<tr><td>20</td><td>JTEST</td><td>w</td><td>0x205</td><td>0x04</td><td>0x00</td><td>设置ADC测试方式
• 写入0x00: 关闭测试模式
• 写入0x04: 输出三角波</td></tr>
</table>

						6.6.46 JTEST Register (Address = 0x205) [reset = 0x00] JTEST is shown in Figure 6-65 and described in Table 6-103. Return to the Summary Table. JESD204C Test Control (default: 0x00) **Figure 6-65. JTEST Register** 7 6 5 4 3 2 1 0 RESERVED JTEST R/W-0x0 R/W-0x0 **Table 6-103. JTEST Register Field Descriptions** Bit Field Type Reset Description 7:5 RESERVED R/W 0x0 Must write default value. **Table 6-103. JTEST Register Field Descriptions (continued)** Bit Field Type Reset Description 4:0 JTEST R/W 0x0 0 : Test mode disabled. Normal operation (default) 1 : PRBS7 test mode 2 : PRBS15 test mode 3 : PRBS23 test mode 4 : Ramp test mode 5 : Transport Layer test mode 6 : D21.5 test mode 7 : K28.5 test mode* 8 : Repeated ILA test mode* 9 : Modified RPAT test mode* 10: Serial outputs held low 11: Serial outputs held high 12: RESERVED 13: PRBS9 test mode 14: PRBS31 test mode 15: Clock test pattern (0x00FF) 16: K28.7 test mode* 17-31: RESERVED * These test modes are only supported when JMODE is selecting a mode that utilizes 8B/10B encoding. Note: This register should only be changed when JESD_EN is 0.
21	**DID**	w	0x206	0x00	0x00	指定 the DID (Device ID) **6.6.47 DID Register (Address = 0x206) [reset = 0x00]** DID is shown in Figure 6-66 and described in Table 6-104. Return to the Summary Table. JESD204C DID Parameter (default: 0x00) **Figure 6-66. DID Register** 7 6 5 4 3 2 1 0 DID R/W-0x0 **Table 6-104. DID Register Field Descriptions** Bit Field Type Reset Description 7:0 DID R/W 0x0 Specifies the DID (Device ID) value that is transmitted during the second multiframe of the JESD204B ILA. Note: This register should only be changed when JESD_EN is 0.
22	**TRIGOUT_CTRL**	w	0x57	0x02	0x00	trigout 输出频率设置 • 设置64分频（8.04375/64 =125.68359375MHz） **6.6.17 TRIGOUT_CTRL Register (Address = 0x57) [reset = 0x00]** TRIGOUT_CTRL is shown in Figure 6-36 and described in Table 6-74. Return to the Summary Table. TRIGOUT Output Control (default: 0x00) **Figure 6-36. TRIGOUT_CTRL Register** 7 6 5 4 3 2 1 0 TRIGOUT_EN RESERVED TRIGOUT R/W-0x0 R/W-0x0 R/W-0x0 **Table 6-74. TRIGOUT_CTRL Register Field Descriptions** Bit Field Type Reset Description 7 TRIGOUT_EN R/W 0x0 0 : TRIGOUTx output buffer/divider is disabled. 1 : TRIGOUTx output buffer/divider is enabled. The RXCLK output can be used to provide a reference clock for the JESD204C receiver. Use the TRIGOUT_MODE field to adjust the output mode. 6:3 RESERVED R/W 0x0 Must write default value. **Table 6-74. TRIGOUT_CTRL Register Field Descriptions (continued)** Bit Field Type Reset Description 2:0 TRIGOUT R/W 0x0 Set the mode for the TRIGOUTx output. 0 : 16 UI clock (RX_DIV = 16) 1 : 32 UI clock (RX_DIV = 32) 2 : 64 UI clock (RX_DIV = 64) 3 : Resampled timestamp from TMSTPx 4-7 : RESERVED Note 1: Only change TRIGOUT_MODE when TRIGOUT_EN=0. Note 2: When TRIGOUT_MODE is 2 or less, TRIGOUTx is derived from the SerDes block. As a result, the TRIGOUTx output is briefly disrupted any time the serializer is re-initialized.
23	**TRIGOUT_CTRL**	w	0x57	0x82		使能TRIGOUT输出 **6.6.17 TRIGOUT_CTRL Register (Address = 0x57) [reset = 0x00]** TRIGOUT_CTRL is shown in Figure 6-36 and described in Table 6-74. Return to the Summary Table. TRIGOUT Output Control (default: 0x00) **Figure 6-36. TRIGOUT_CTRL Register** 7 6 5 4 3 2 1 0 TRIGOUT_EN RESERVED TRIGOUT R/W-0x0 R/W-0x0 R/W-0x0 **Table 6-74. TRIGOUT_CTRL Register Field Descriptions** Bit Field Type Reset Description 7 TRIGOUT_EN R/W 0x0 0 : TRIGOUTx output buffer/divider is disabled. 1 : TRIGOUTx output buffer/divider is enabled. The RXCLK output can be used to provide a reference clock for the JESD204C receiver. Use the TRIGOUT_MODE field to adjust the output mode. 6:3 RESERVED R/W 0x0 Must write default value. **Table 6-74. TRIGOUT_CTRL Register Field Descriptions (continued)** Bit Field Type Reset Description 2:0 TRIGOUT R/W 0x0 Set the mode for the TRIGOUTx output. 0 : 16 UI clock (RX_DIV = 16) 1 : 32 UI clock (RX_DIV = 32) 2 : 64 UI clock (RX_DIV = 64) 3 : Resampled timestamp from TMSTPx 4-7 : RESERVED Note 1: Only change TRIGOUT_MODE when TRIGOUT_EN=0. Note 2: When TRIGOUT_MODE is 2 or less, TRIGOUTx is derived from the SerDes block. As a result, the TRIGOUTx output is briefly disrupted any time the serializer is re-initialized.
24	**VCO_CAL_STATUS**	r	0x5E		0x00	VCO校准完成指示 • bit[0]为1，表示校准完成，才进行下一步 **6.6.22 VCO_CAL_STATUS Register (Address = 0x5E) [reset = 0x0]** VCO_CAL_STATUS is shown in Figure 6-41 and described in Table 6-79. Return to the Summary Table. VCO Calibration Status (read-only) (default: undefined) **Figure 6-41. VCO_CAL_STATUS Register** 7 6 5 4 3 2 1 0 RESERVED VCO_CAL_DONE R-0x0 R-0x0 **Table 6-79. VCO_CAL_STATUS Register Field Descriptions** Bit Field Type Reset Description 7:1 RESERVED R 0x0 0 VCO_CAL_DONE R 0x0 This bit returns '1' once the VCO calibration engine has completed calibration (or calibration was skipped because VCO_CAL_EN=0). Once the calibration is completed, you can safely read or write the VCO_FREQ_TRIM register (never write VCO_FREQ_TRIM during calibration).
25		r	0x208	0x01	0x00	

	JESD_STATUS					• 每间隔1ms轮询一次，直到读出的bit[0]为1(指示 PLL (C-PLL) 已经锁定),才进行下一步 表 8-106. JESD_STATUS Register Field Descriptions Bit | Field | Type | Reset | Description 7 | RESERVED | R/W | 0x0 | 6 | LINK_UP | R/W | 0x0 | When set, indicates that the JESD204C link is up. 5 | SYNC_STATUS | R/W | 0x0 | Returns the state of the JESD204C SYNC~ signal. 0 : SYNC~ asserted 1 : SYNC~ de-asserted 4 | REALIGNED | R/W | 0x0 | When high, indicates that the digital block clock, frame clock, or multiframe clock phase was realigned by SYSREF. Writing a 1 to this bit will clear it. 3 | ALIGNED | R/W | 0x0 | When high, indicates that the multiframe (LMFC) clock phase has been established by SYSREF. The first SYSREF event after enabling the JESD204B encoder will set this bit. Writing a 1 to this bit will clear it. 2 | SPLL_LOCKED | R/W | 0x0 | When high, indicates that the SerDes PLL (S-PLL) is locked. 1 | RESERVED | R/W | 0x0 | 0 | CPLL_LOCKED | R/W | 0x0 | When high, indicates that the converter PLL (C-PLL) is locked.
26	**CAL_EN**	w	0x61	0x01	0x01	开启校准使能 8.6.23 CAL_EN Register (Address = 0x61) [reset = 0x01] CAL_EN is shown in 图 8-42 and described in 表 8-80. Return to the 表 8-56. Calibration Enable (Default: 0x01) 图 8-42. CAL_EN Register 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 RESERVED | CAL_EN R/W-0x0 | R/W-0x1 表 8-80. CAL_EN Register Field Descriptions Bit | Field | Type | Reset | Description 7:1 | RESERVED | R/W | 0x0 | Must write default value. 0 | CAL_EN | R/W | 0x1 | Calibration Enable. Set high to run calibration. Set low to hold calibration in reset to program new calibration settings. Clearing CAL_EN also resets the clock dividers that clock the digital block and JESD204C interface. Some calibration registers require clearing CAL_EN before making any changes. All registers with this requirement contain a note in their descriptions. After changing the registers, set CAL_EN to re-run calibration with the new settings. Always set CAL_EN before setting JESD_EN. Always clear JESD_EN before clearing CAL_EN.
27	**OVR_CFG**	w	0x213	0x00	0x07	过范围检测(暂时未开启) 8.6.54 OVR_CFG Register (Address = 0x213) [reset = 0x07] OVR_CFG is shown in 图 8-73 and described in 表 8-111. Return to the 表 8-56. Over-range Enable / Hold Off (default: 0x07) 图 8-73. OVR_CFG Register 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 RESERVED | OVR_EN | OVR_N R/W-0x0 | R/W-0x0 | R/W-0x7 表 8-111. OVR_CFG Register Field Descriptions Bit | Field | Type | Reset | Description 7:4 | RESERVED | R/W | 0x0 | Must write default value. 3 | OVR_EN | R/W | 0x0 | Enables over-range status output pins when set high. The ORA, ORB, ORC and ORD outputs are held low when OVR_EN is set low. 2:0 | OVR_N | R/W | 0x7 | Program this register to adjust the pulse extension for the ORA, ORB, ORC and ORD outputs. The minimum pulse duration of the over-range outputs is $4 * 2^{OVR\_N}$ sampling cycles. Incrementing this field doubles the monitoring period.
28	**JESD_EN**	w	0x200	0x01	0x01	写 0x00 : 关闭 JESD204C interface 写 0x01 : 使能 JESD204C interface JESD204C Subsystem Enable (default: 0x01) Figure 6-60. JESD_EN Register 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 RESERVED | JESD_EN R/W-0x0 | R/W-0x1 Table 6-98. JESD_EN Register Field Descriptions Bit | Field | Type | Reset | Description 7:1 | RESERVED | R/W | 0x0 | Must write default value. 0 | JESD_EN | R/W | 0x1 | 0 : Disable JESD204C interface 1 : Enable JESD204C interface Note: Before altering other JESD204C registers, you must clear JESD_EN. When JESD_EN is 0, the block is held in reset and the serializers are powered down. The clocks are gated off to save power. The LMFC/LEMC counter is also held in reset, so SYSREF will not align the LMFC/LEMC. Note: Always set CAL_EN before setting JESD_EN. Note: Always clear JESD_EN before clearing CAL_EN.
29	**CAL_SOFT_TRIG**	w	0x6C	0x00	0x01	先写0x00,为下一步准备 6.6.29 CAL_SOFT_TRIG Register (Address = 0x6C) [reset = 0x01] CAL_SOFT_TRIG is shown in Figure 6-48 and described in Table 6-86. Return to the Summary Table. Calibration Software Trigger (default: 0x01) Figure 6-48. CAL_SOFT_TRIG Register 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 RESERVED | CAL_SOFT_TRIG R/W-0x0 | R/W-0x1 Table 6-86. CAL_SOFT_TRIG Register Field Descriptions Bit | Field | Type | Reset | Description 7:1 | RESERVED | R/W | 0x0 | Must write default value. Table 6-86. CAL_SOFT_TRIG Register Field Descriptions (continued) Bit | Field | Type | Reset | Description 0 | CAL_SOFT_TRIG | R/W | 0x1 | CAL_SOFT_TRIG is a software bit to provide the functionality of the CALTRIG input pin when there are no hardware resources to drive CALTRIG. Program CAL_TRIG_EN=0 to use CAL_SOFT_TRIG for the calibration trigger. Note: If no calibration trigger is needed, leave CAL_TRIG_EN=0 and CAL_SOFT_TRIG=1 (trigger set high).
30	**CAL_SOFT_TRIG**	w	0x6C	0x01		使能软件触发校准的功能

						6.6.29 CAL_SOFT_TRIG Register (Address = 0x6C) [reset = 0x01] CAL_SOFT_TRIG is shown in Figure 6-48 and described in Table 6-86. Return to the Summary Table. Calibration Software Trigger (default: 0x01) **Figure 6-48. CAL_SOFT_TRIG Register** 7 6 5 4 3 2 1 0 RESERVED CAL_SOFT_TRIG R/W-0x0 R/W-0x1 **Table 6-86. CAL_SOFT_TRIG Register Field Descriptions** Bit | Field | Type | Reset | Description 7:1 | RESERVED | R/W | 0x0 | Must write default value. **Table 6-86. CAL_SOFT_TRIG Register Field Descriptions (continued)** Bit | Field | Type | Reset | Description 0 | CAL_SOFT_TRIG | R/W | 0x1 | CAL_SOFT_TRIG is a software bit to provide the functionality of the CALTRIG input pin when there are no hardware resources to drive CALTRIG. Program CAL_TRIG_EN=0 to use CAL_SOFT_TRIG for the calibration trigger. Note: If no calibration trigger is needed, leave CAL_TRIG_EN=0 and CAL_SOFT_TRIG=1 (trigger set high).
31	**CAL_STATUS**	r(read-only))	0x6A		0x0	• bit[0]指示前台校准是否完成 • 等待100ms之后，每间隔10ms轮询一次，并打印，直到读出的bit[0]为1(表示前台校准已经完成),才进行下一步 表 8-84. CAL_STATUS Register Field Descriptions Bit | Field | Type | Reset | Description 7:5 | RESERVED | R | 0x0 4:2 | CAL_STAT | R | 0x0 | Calibration status code 1 | CAL_STOPPED | R | 0x0 | This bit returns a 1 when background calibration is successfully stopped at the requested phase. This bit returns a 0 when calibration starts operating again. If background calibration is disabled, this bit is set when foreground calibration is completed or skipped. 0 | FG_DONE | R | 0x0 | This bit is high to indicate that foreground calibration has completed (or was skipped).
32	**CLK_CTRL0**	w	0x29	0xA0		开启SYSREF处理 **6.6.5 CLK_CTRL0 Register (Address = 0x29) [reset = 0x80]** CLK_CTRL0 is shown in Figure 6-24 and described in Table 6-62. Return to the Summary Table. Clock Control 0 (default: 0x80) **Figure 6-24. CLK_CTRL0 Register** 7 6 5 4 3 2 1 0 RESERVED SYSREF_PROC_EN SYSREF_RECV_EN SYSREF_ZOOM SYSREF_SEL R/W-0x1 R/W-0x0 R/W-0x0 R/W-0x0 R/W-0x0 **Table 6-62. CLK_CTRL0 Register Field Descriptions** Bit | Field | Type | Reset | Description 7 | RESERVED | R/W | 0x1 | Must write default value. 6 | SYSREF_PROC_EN | R/W | 0x0 | This bit enables the SYSREF processor, which allows the device to process SYSREF events (default: disabled). SYSREF_RECV_EN must be set before setting SYSREF_PROC_EN. 5 | SYSREF_RECV_EN | R/W | 0x0 | Set this bit to enable the SYSREF receiver circuit (default: disabled) 4 | SYSREF_ZOOM | R/W | 0x0 | Set this bit to zoom in the SYSREF windowing status and delays (impacts SYSERF_POS and SYSREF_SEL). When set, the delays used in the SYSREF windowing feature (reported in the SYSREF_POS register) become smaller. Use SYSREF_ZOOM for high clock rates, specifically when multiple SYSREF valid windows are encountered in the SYSREF_POS register; see the SYSREF Position Detector and Sampling Position Selection (SYSREF Windowing) section. 3:0 | SYSREF_SEL | R/W | 0x0 | Set this field to select which SYSREF delay to use. Set this field based on the results returned by SYSREF_POS; see the SYSREF Position Detector and Sampling Position Selection (SYSREF Windowing) section.
33	**CLK_CTRL0**	w	0x29	0xE0		开启SYSREF处理 **6.6.5 CLK_CTRL0 Register (Address = 0x29) [reset = 0x80]** CLK_CTRL0 is shown in Figure 6-24 and described in Table 6-62. Return to the Summary Table. Clock Control 0 (default: 0x80) **Figure 6-24. CLK_CTRL0 Register** 7 6 5 4 3 2 1 0 RESERVED SYSREF_PROC_EN SYSREF_RECV_EN SYSREF_ZOOM SYSREF_SEL R/W-0x1 R/W-0x0 R/W-0x0 R/W-0x0 R/W-0x0 **Table 6-62. CLK_CTRL0 Register Field Descriptions** Bit | Field | Type | Reset | Description 7 | RESERVED | R/W | 0x1 | Must write default value. 6 | SYSREF_PROC_EN | R/W | 0x0 | This bit enables the SYSREF processor, which allows the device to process SYSREF events (default: disabled). SYSREF_RECV_EN must be set before setting SYSREF_PROC_EN. 5 | SYSREF_RECV_EN | R/W | 0x0 | Set this bit to enable the SYSREF receiver circuit (default: disabled) 4 | SYSREF_ZOOM | R/W | 0x0 | Set this bit to zoom in the SYSREF windowing status and delays (impacts SYSERF_POS and SYSREF_SEL). When set, the delays used in the SYSREF windowing feature (reported in the SYSREF_POS register) become smaller. Use SYSREF_ZOOM for high clock rates, specifically when multiple SYSREF valid windows are encountered in the SYSREF_POS register; see the SYSREF Position Detector and Sampling Position Selection (SYSREF Windowing) section. 3:0 | SYSREF_SEL | R/W | 0x0 | Set this field to select which SYSREF delay to use. Set this field based on the results returned by SYSREF_POS; see the SYSREF Position Detector and Sampling Position Selection (SYSREF Windowing) section.
34	**SYSREF_POS**	r	0x2C			读出24bit状态值，其中 bit[23] 和 bit[0] 一定为1，指示SYSREF边沿相对时钟的位置，下一步使用这个读出的值。 **6.6.8 SYSREF_POS Register (Address = 0x2C) [reset = 0x0]** SYSREF_POS is shown in Figure 6-27 and described in Table 6-65. Return to the Summary Table. SYSREF Capture Position (read-only status) **Figure 6-27. SYSREF_POS Register** 23 22 21 20 19 18 17 16 SYSREF_POS R-0x0 15 14 13 12 11 10 9 8 SYSREF_POS R-0x0 7 6 5 4 3 2 1 0 SYSREF_POS **Table 6-65. SYSREF_POS Register Field Descriptions** Bit | Field | Type | Reset | Description 23:0 | SYSREF_POS | R | 0x0 | Returns a 24-bit status value that indicates the position of the SYSREF edge with respect to CLKx. Use this to program SYSREF_SEL.
35	**CLK_CTRL0**	w	0X29	0xE6(需要调整)		

						6.6.5 CLK_CTRL0 Register (Address = 0x29) [reset = 0x80] CLK_CTRL0 is shown in Figure 6-24 and described in Table 6-62. Return to the Summary Table. Clock Control 0 (default: 0x80) **Figure 6-24. CLK_CTRL0 Register** 7 6 5 4 3 2 1 0 RESERVED / SYSREF_PROC_EN / SYSREF_RECV_EN / SYSREF_ZOOM / SYSREF_SEL R/W-0x1 / R/W-0x0 / R/W-0x0 / R/W-0x0 / R/W-0x0 **Table 6-62. CLK_CTRL0 Register Field Descriptions** Bit / Field / Type / Reset / Description 7 / RESERVED / R/W / 0x1 / Must write default value. 6 / SYSREF_PROC_EN / R/W / 0x0 / This bit enables the SYSREF processor, which allows the device to process SYSREF events (default: disabled). SYSREF_RECV_EN must be set before setting SYSREF_PROC_EN. 5 / SYSREF_RECV_EN / R/W / 0x0 / Set this bit to enable the SYSREF receiver circuit (default: disabled) 4 / SYSREF_ZOOM / R/W / 0x0 / Set this bit to zoom in the SYSREF windowing status and delays (impacts SYSERF_POS and SYSREF_SEL). When set, the delays used in the SYSREF windowing feature (reported in the SYSREF_POS register) become smaller. Use SYSREF_ZOOM for high clock rates, specifically when multiple SYSREF valid windows are encountered in the SYSREF_POS register; see the SYSREF Position Detector and Sampling Position Selection (SYSREF Windowing) section. 3:0 / SYSREF_SEL / R/W / 0x0 / Set this field to select which SYSREF delay to use. Set this field based on the results returned by SYSREF_POS; see the SYSREF Position Detector and Sampling Position Selection (SYSREF Windowing) section. 1、高4bit固定为0xE 2、低4bit值按照下面方法确定 根据SYSREF_POS的值,并参考下表，来设置SYSREF_SEL的值 表 8-7. Examples of SYSREF_POS Readings and SYSREF_SEL Selections SYSREF_POS[23:0] / OPTIMAL SYSREF_SEL SETTING 0x02E[7:0] (Largest Delay) / 0x02D[7:0][1] / 0x02C[7:0][1] (Smallest Delay) b10000000 / b01100000 / b00011001 / 8 or 9 b10011000 / b00000000 / b00110001 / 12 b10000000 / b01100000 / b00000001 / 6 or 7 b10000000 / b00000011 / b00000001 / 4 or 15 b10001100 / b01100011 / b00011001 / 6 (1) Red coloration indicates the bits that are selected, as given in the last column of this table. 例如：SYSREF_POS读出的值为： 0x01 0x00 0x80 0X02E: 0x80; 0X02D: 0x00; 0x02C: 0x01 0x80 0x00 0x01 二进制值： 10000000_00000000_00000001 SYSREF_SEL值：虽然SYSREF_POS有24位，但是仅使用前16位bit[15:0],按照表8-7，应该选择长连0串中的中间0的位置，应该选择8，这里选择6也是可以的，因为靠近8。 注：选择6可能考虑了，由于温度升高sysref延时增大的原因。
36	**TMSTP_CTRL**	w	0x3B	0x01	0x00	TMSTP 接口设置为差分 **6.6.11 TMSTP_CTRL Register (Address = 0x3B) [reset = 0x00]** TMSTP_CTRL is shown in Figure 6-30 and described in Table 6-68. Return to the Summary Table. TIMESTAMP (TMSTP) Control (default: 0x00) **Figure 6-30. TMSTP_CTRL Register** 7 6 5 4 3 2 1 0 RESERVED / TMSTP_LVPECL_EN / TMSTP_RECV_EN R/W-0x0 / R/W-0x0 / R/W-0x0 **Table 6-68. TMSTP_CTRL Register Field Descriptions** Bit / Field / Type / Reset / Description 7:2 / RESERVED / R/W / 0x0 / Must write default value. 1 / TMSTP_LVPECL_EN / R/W / 0x0 / When set, activates the low voltage PECL mode for the differential TMSTP± input. The internal termination for each input pin (TMSTP+ and TMSTP−) becomes a 50-Ω resistor to ground. There is no input common-mode self-biasing for TMSTP± when TMSTP_LVPECL_EN is set to 1. 0 / TMSTP_RECV_EN / R/W / 0x0 / Enables the differential differential TMSTP± input.
37	**JESD_STATUS**	r	0x208	0x1D	0x00	• 等待10ms之后，每间隔1ms轮询一次，并打印，直到读出的： • bit[6]为1(表示 JESD204C 链路建立)；

- bit[2]为1(表示 SerDes PLL (S-PLL) 锁定);
- bit[0]为1(表示 converter PLL (C-PLL) 锁定),才进行下一步

6.6.49 JESD_STATUS Register (Address = 0x208) [reset = 0x0]

JESD_STATUS is shown in Figure 6-68 and described in Table 6-106.

Return to the Summary Table.

JESD204C / System Status Register

Figure 6-68. JESD_STATUS Register

7	6	5	4	3	2	1	0
RESERVED	LINK_UP	SYNC_STATUS	REALIGNED	ALIGNED	SPLL_LOCKED	RESERVED	CPLL_LOCKED
R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0

Table 6-106. JESD_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0x0	
6	LINK_UP	R/W	0x0	When set, indicates that the JESD204C link is up.
5	SYNC_STATUS	R/W	0x0	Returns the state of the JESD204C SYNC~ signal. 0 : SYNC~ asserted 1 : SYNC~ de-asserted
4	REALIGNED	R/W	0x0	When high, indicates that the digital block clock, frame clock, or multiframe clock phase was realigned by SYSREF. Writing a 1 to this bit will clear it.
3	ALIGNED	R/W	0x0	When high, indicates that the multiframe (LMFC) clock phase has been established by SYSREF. The first SYSREF event after enabling the JESD204B encoder will set this bit. Writing a 1 to this bit will clear it.
2	SPLL_LOCKED	R/W	0x0	When high, indicates that the SerDes PLL (S-PLL) is locked.
1	RESERVED	R/W	0x0	
0	CPLL_LOCKED	R/W	0x0	When high, indicates that the converter PLL (C-PLL) is locked.

5 ADC配置后输出的信息

=== ADC09DJ1300 + JESD204C RX bring-up ===

adc_spi_init ok, SCLK<=1000 Hz (t_half=500 us)

[adc_init] ADC_PWR_EN(MIO23) = 1, wait 1ms

VENDOR_ID : 51

[adc_init] CONFIG_A (0x000) = 0x30 (expect 0x30)

[poll] INIT_STATUS (0x270) = 0x01

[poll] VCO_CAL_STATUS (0x05E) = 0x03

[adc_init] low power registers SKIPPED (out of documented range at 1.3 GSPS)

[adc_init] JMODE (0x201) = 0x0E, JTEST (0x205) = 0x04 (Ramp pattern)

[adc_init] VCO_CAL_STATUS (0x05E) = 0x03

[poll] JESD_STATUS(C-PLL) (0x208) = 0x01

[poll] CAL_STATUS (0x06A) = 0x0C

[poll] CAL_STATUS (0x06A) = 0x0C

[poll] CAL_STATUS (0x06A) = 0x0C

[poll] CAL_STATUS (0x06A) = 0x0F

[adc_init] SYSREF_POS = 0x01 0x00 0x80 -> 0x800001

[poll] JESD_STATUS(PLL) (0x208) = 0x1D

[adc_init] done: S-PLL and C-PLL locked, JESD_STATUS = 0x1D (link up bit[6] = 0)

读 REG_FIFO_LANE_ALM : FF

写0x01 之后，再读 REG_FIFO_LANE_ALM : FE

读 REG_ALM_STATUS : E

写0x3F 之后，再读REG_ALM_STATUS : 3F

adc_init ok