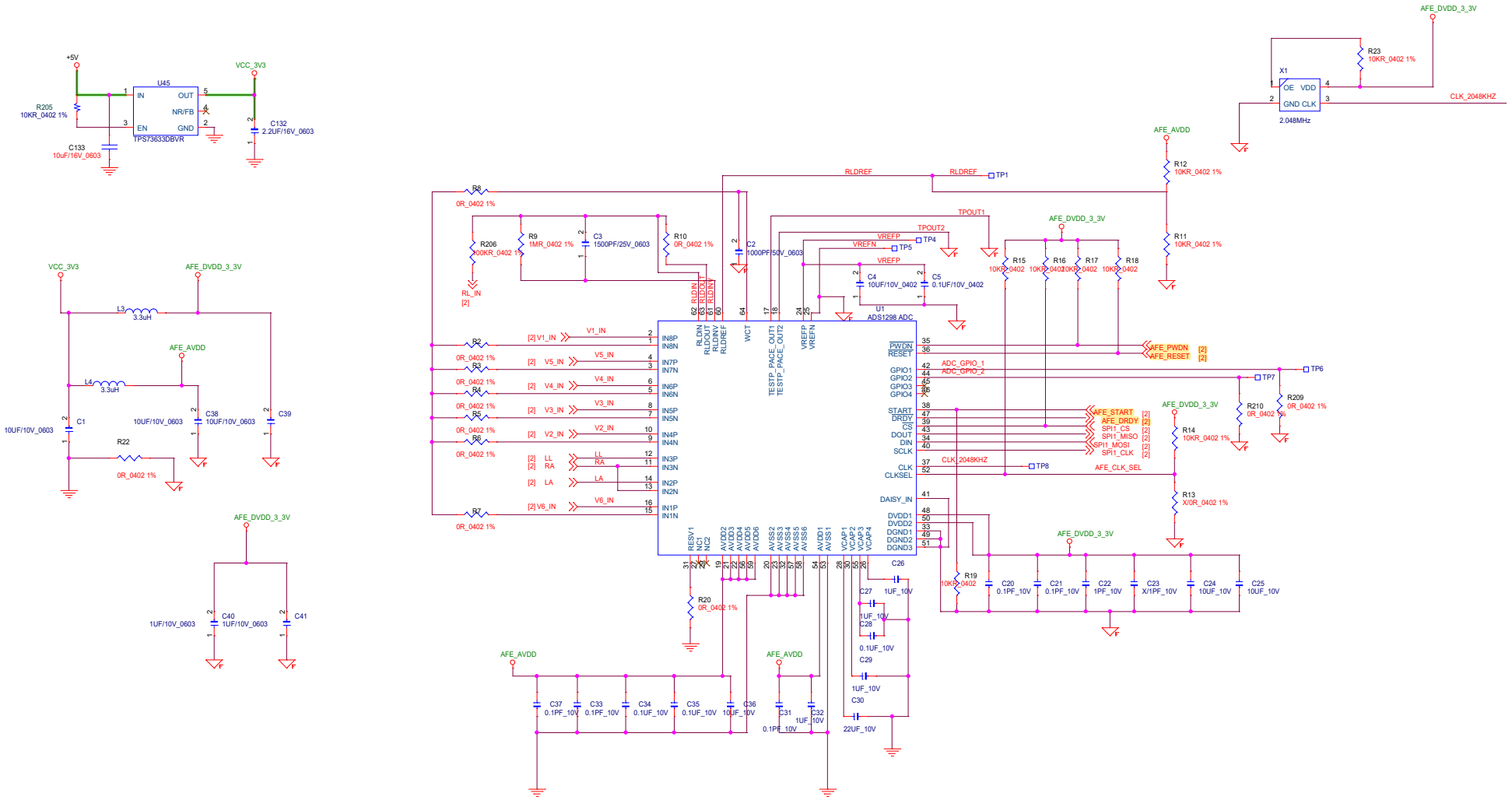

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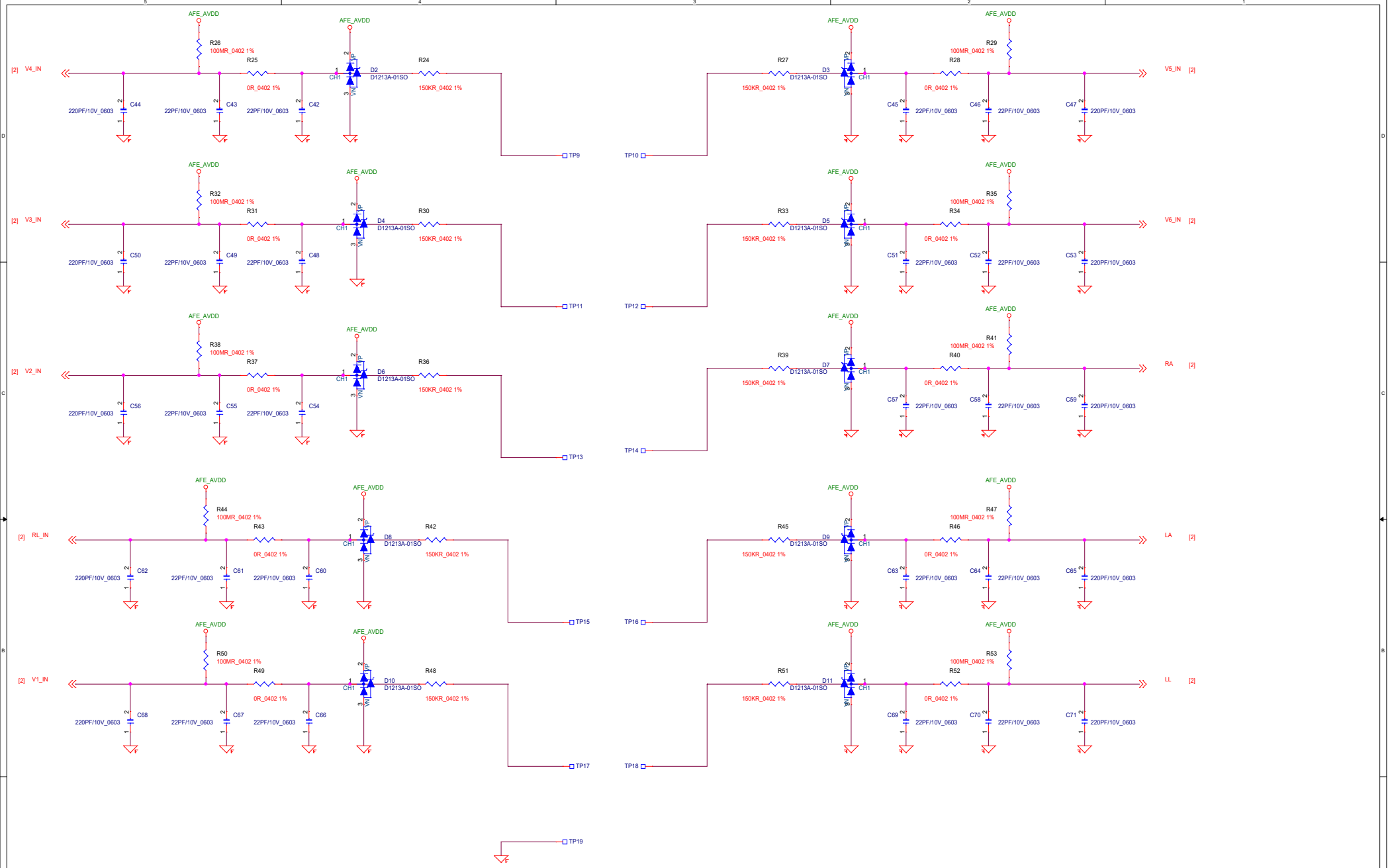

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BOOT0: HIGH

PA13=JTMS-SWDIO
PA14=JTCK-SWCLK
燒code用的保留

external reset (NRST pin)

FT, TC and NRST I/O input low level voltage==>VIL: 0.3VDD
FT, TC and NRST I/O input high level voltage==>VIH: 0.7VDD

VBAT operation is activated when VDD is not present

VBAT supply for RTC: 1 μ A @25 °C

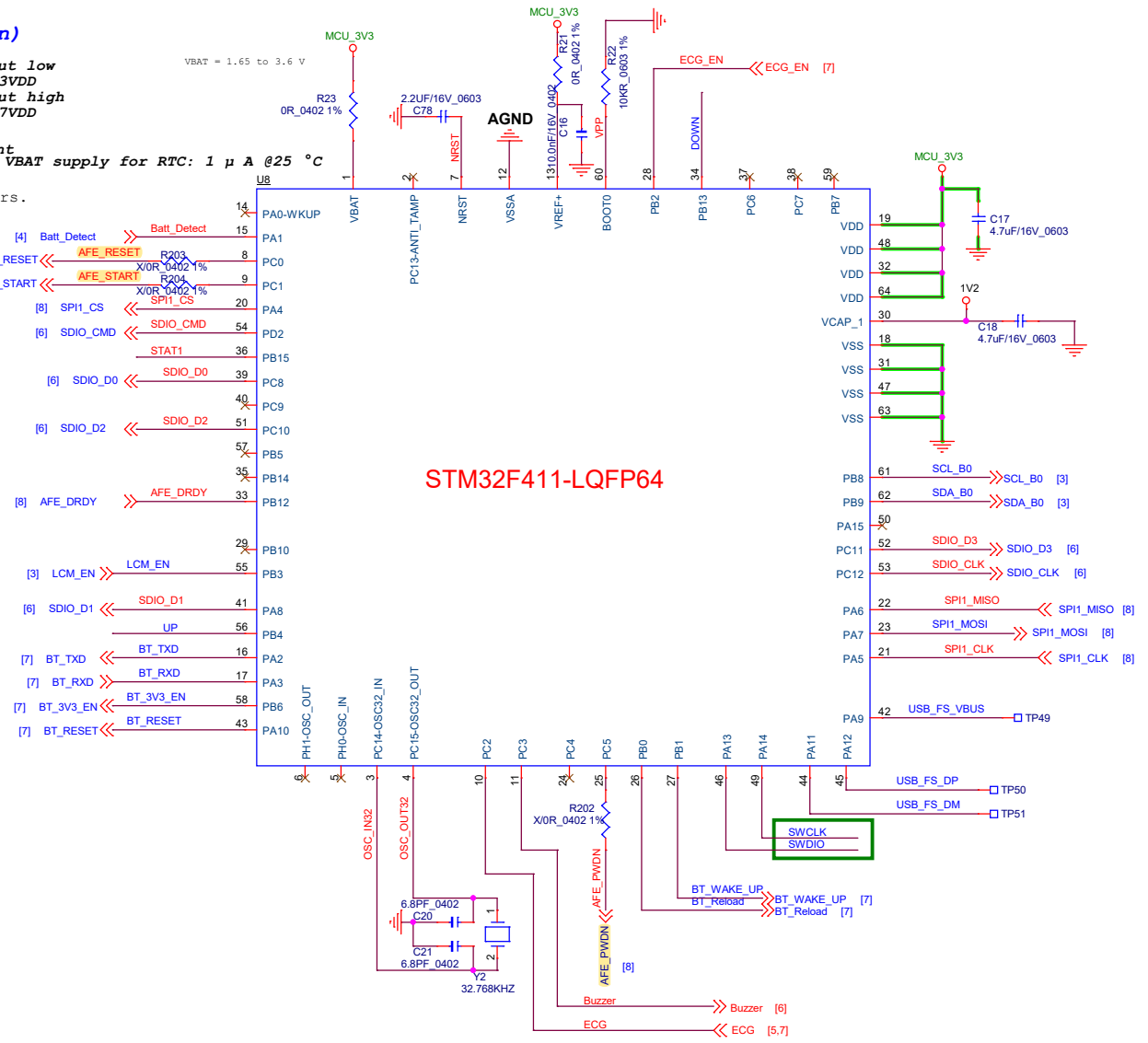
The VBAT pin supplies the RTC and the backup registers.

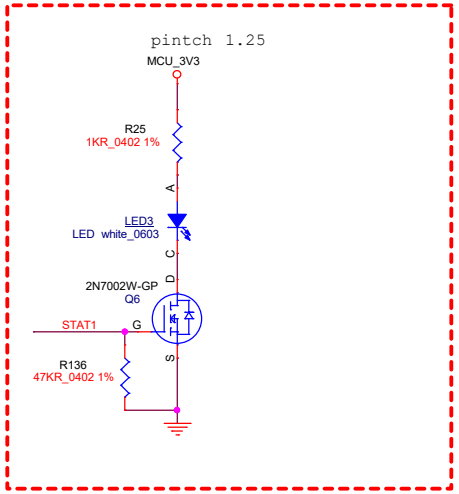
When PDR_ON pin is not connected to VDD (internal Reset OFF), the VBAT functionality is no more available and VBAT pin should be connected to VDD.

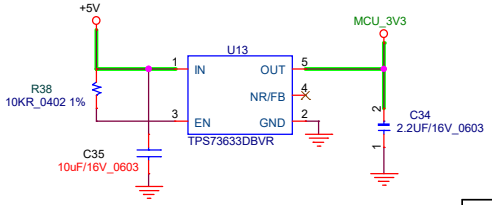
The 4.7 μ F ceramic capacitor must be connected to one of the VDD pin.

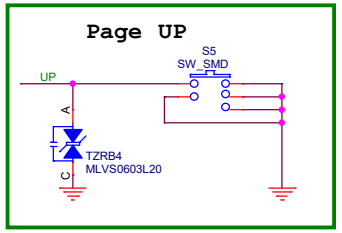
PA0 cannot be used as a GPIO pin since it allows to reset a part of the V12 logic power domain which is not reset by the NRST pin.

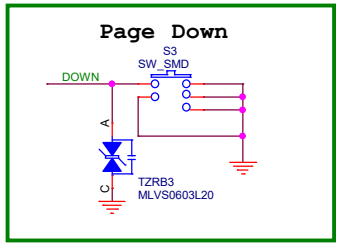
the use of GPIOs PC13 to PC15 in output mode is limited

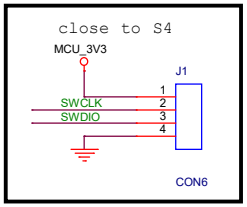












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