8.3 Initialization Setup

1. Set TXENABLE pin to logic LOW. This set the DAC38J84 output to midscale and prevents any potential output glitches during the power up process from propagating through the rest of the signal chain.
2. Set SLEEP pin to logic LOW.

Note: by default, config35 sleep\_cntl bits are set to 0xFFFF. This allows the SLEEP pin state to be routed directly to various DAC38J84 circuits to control the power down mode of the circuits directly. If SLEEP pin is set to logic HIGH upon power, certain DAC38J84 circuit blocks may not be powered up correctly and cause incorrect operation. Thus, SLEEP pin should be set to logic LOW before start-up of the DAC38J84 device.

1. Supply all 0.9-V supplies (VDDDIG, VDDT, VDDDAC, VDDCLK), all 1.8-V supplies (VDDR, VDDS, VQPS, VDDIO, VDDAPLL, VDDAREF), and all 3.3-V supplies (VDDADAC). The supplies can be powered up simultaneously or in any order. There are no specific requirements on the ramp rate for the supplies.
2. RESET the JTAG port by either toggling TRSTB low if using the JTAG port or holding TRSTB low if not using JTAG.
3. Provide the DACCLK to the device.
4. SYSREF State (before completing the device configuration)
	1. If continuous SYSREF is implemented in the system, the SYSREF can be provided to the device at this point.
	2. If pulsed SYSREF is implemented in the system, hold off the triggering of pulsed SYSREF until the DAC38J84 device is near the completion of programming. Refer to step 17.
5. Toggle RESETB to logic LOW to reset the SIF registers. This step ensures all the fuse logics are reset correctly.
6. Set the DAC38J84 clock divider and JESD logic to stand-by mode and gate any initialization activities until all internal clocks, JESD, and SERDES blocks are programmed.
	1. Set the JESD block to initialization and reset state: init\_state = 1111 and jesd\_reset\_n = 0 in config74.
	2. Disarm the clock divider initialization circuit: cdrvser\_sysref\_mode = 000 in config36.
	3. Disarm the JESD link0 initialization circuit: sysref\_mode\_link0 = 000 in config92.
	4. Note: both the clock divider and JESD link0 initialization circuits are not armed so the SYSREF signal will not start the circuit initialization. They will be armed again later after all the internal clocks, JESD, and SERDES blocks are program to ensure the programming sequence would not interrupt the initialization afterwards.
7. Program the DAC PLL settings in config26, config49, config50, and config51.
	1. If the PLL is not used, set pll\_sleep and pll\_reset to “1” and pll\_ena to “0”.
	2. If the PLL is used, check config49 for pll\_lpvolt(2:0) register and config108 for alarm\_from\_pll register for PLL lock status.
8. Program the SERDES settings in config59 (the serdes\_clk\_sel and serdes\_refclk\_div), config61, and config62.
9. Program the SERDES lane settings in config63, config71, config73, config74, and config96.
10. Program clkjesd\_div, cdrvser\_sysref\_mode, and interp registers.
11. Verify the SERDES PLL lock status by checking the SERDES PLL alarms: alarm\_rw0\_pll (alarm for lanes 0 through 3) and alarm\_rw1\_pll (alarm for lanes 4 through 7).
12. Program the JESD settings in config3, config74-77, config79, config80-85, config92, and config97.
13. Program the DSP block settings (NCO, PA protection, QMC, fractional delay, etc.) and set the preferred initialization modes for the digital blocks from config30 to config32.
14. Preparing the DAC38J84 clock divider and JESD logic for initialization through continuous SYSREF
	1. Arm the clock divider initialization circuit to the desired triggering mode. For instance, set cdrvser\_sysref\_mode = 011 in config36 to set the initialization logic to skip one SYSREF pulse and then use only the next pulse.
	2. Arm the JESD link0 initialization circuit to the desired triggering mode. For instance, set sysref\_mode\_link0 = 101 in config92 to set the initialization logic to skip two SYSREF pulses and then use only the next pulse.
	3. Set the JESD block to exit out of the reset state: jesd\_reset\_n = 1 in config74.
	4. Set the JESD block to exit out of the initialization state: init\_state = 0000 in config74.
	5. Note: TI recommends programming step 15.c and 15.d separately.
15. SYSREF State (after device programming is completed)
	1. If continuous SYSREF is implemented in the system, the SYSREF can be provided to the device can be disabled at this point to prevent any coupling of SYSREF signal onto the DAC output.

Note: if the SYSREF driver cannot shut-off the SYSREF signal immediately at the last pulse due to finite active driver to tri-state time, TI recommends arm the clock divider initialization circuit and JESD link0 initialization circuit to trigger upon only on a single pulse instead of continuous pulses (i.e. use only the next pulse instead of use all SYSREF pulses).

* 1. If pulsed SYSREF is implemented in the system, start the triggering of pulsed SYSREF.