1. 具体配置



只用一个DAC通道，L-M-F-S-Hd为42111，K是20，sysref是26.66MHz，interpolation是12。DAC采样率6.4GHz，采用片上PLL，DAC PLL参考时钟400MHz（通过DACCLKP/N脚差分输入），M是4，N是1；Serdes 速率5.333GHz，Serdes PLL对DAC PLL输出3分频，得到参考时钟是533.3MHz，对533.3MHz进行5倍频（寄存器SRDS\_PLL\_CFG中的MPY是5），RATE配置成half rate





1. 存在问题
2. 初始化完成后，读寄存器0x05的值，发现低3位都是1，说明DAC PLL和Serdes PLL都没有锁定，但可以测到CLKOUT脚上有输出，而且频率也和配置的频率一样。我同时也使能了Serdes PLL在ALARM脚上的输出（根据手册，如下图），应该是Serdes PLL输出频率的80分频，但在ALARM脚上测不到任何输出。



1. DAC正常工作下，SYNC信号在上电时默认是高，初始化完成后会变低。但现在SYNC始终保持高，初始化完成后也没有变低。

**所有配置的寄存器及顺序如下：**

0x00FF0000, //0x7F

0x00019A85, // IO\_CONFIG enable 4 wire SPI

0x00860000, //0x06 read

0x00090004, //PAGE\_SET

0x00230000, // SLEEP\_CNTL

0x000C4F00, //CLK\_OUT

0x001B0020, // DTEST

0x00240803, // SYSR\_CAPTURE enable sysref monitor

0x000B0000, //SLEEP\_CONFIG

0x003B1001, //SRDS\_CLK\_CFG dacclk pll 1.6G/3=533.33M (3B9001)

0x003C9851, //SRDS\_PLL\_CFG MPY 0x28(5x)/VRANGE 0

0x003E0C29, //SRDS\_CFG2 RATE half

0x00336410, //PLL\_CONFIG2

0x00311438, //PLL\_CONFIG1 dac pll N=8/ N in reset to set M

0x00320308, //PLL\_CONFIG1 dac pll M=4

0x00310438, //PLL\_CONFIG1 dac pll N=8/ N out of reset

0x00090001, //PAGE\_SET

0x000C27F7, //MULTIDUC\_CFG2 enable NCO

0x001E0000, //FREQ\_NCOAB set NCO frequency

0x001F0000, //FREQ\_NCOAB set NCO frequency

0x00200000, //FREQ\_NCOAB set NCO frequency

0x000D8000, //JESD\_FIFO set SPI\_TXENABLE to 0

0x000A060F, //MULTIDUC\_CFG1 INTERP 12

0x00256600, // SERDES\_CLK

0x004C1303, // JESD\_K\_L 20

0x004B1300, //JESD\_RBD\_F

0x004D0100, //JESD\_M\_S

0x004E0F6F, //JESD\_N\_HD\_SCR scramble on

0x004A0F03, //JESD\_LN\_EN

0x00090002, //PAGE\_SET

0x000C27F7, //MULTIDUC\_CFG2 enable NCO

0x001E0000, //FREQ\_NCOAB set NCO frequency

0x001F0000, //FREQ\_NCOAB set NCO frequency

0x00200000, //FREQ\_NCOAB set NCO frequency

0x000D8000, //JESD\_FIFO set SPI\_TXENABLE to 0

0x000A060F, //MULTIDUC\_CFG1 INTERP 12

0x00256600, // SERDES\_CLK

0x004C1303, // JESD\_K\_L 20

0x004B1300, //JESD\_RBD\_F

0x004D0100, //JESD\_M\_S

0x004E0F6F, //JESD\_N\_HD\_SCR scramble on

0x004A0F03, //JESD\_LN\_EN

0x00090001, //PAGE\_SET

0x00240000, //SYSREF\_CLKDIV Don't use SYSREF pulse

0x005C0000, //JESD SYSREF Mode Don't use SYSREF pulse

0x00090002, //PAGE\_SET

0x00240000, //SYSREF\_CLKDIV Don't use SYSREF pulse

0x005C0000, //JESD SYSREF Mode Don't use SYSREF pulse

0x00090004, //PAGE\_SET

0x000AF000, //CLK\_CONFIG sync the clock divider

0x008AF000, //空一个周期来保证有至少两个sysref上升沿

0x000A7000, //CLK\_CONFIG finish sync the clock divider

0x00090000, //PAGE\_SET

0x00007861, //RESET\_CONFIG only one link used/Put JESD204B core in reset

0x00090001, //PAGE\_SET

0x00240020, //SYSREF\_CLKDIV Sync CDRV

0x005C0003, //JESD SYSREF Mode Sync JESD204B blocks

0x00090002, //PAGE\_SET

0x00240020, //SYSREF\_CLKDIV Sync CDRV

0x005C0003, //JESD SYSREF Mode Sync JESD204B blocks

0x00090000, //PAGE\_SET

0x00007860, //RESET\_CONFIG only one link used/Put JESD204B core out of reset

0x00040000, // Clear all DAC alarms

0x00050000,

0x00090001,

0x00640000,

0x00650000,

0x00660000,

0x00670000,

0x00680000,

0x00690000,

0x006A0000,

0x006B0000,

0x006C0000,

0x006D0000,

0x000D8001, //JESD\_FIFO set SPI\_TXENABLE to 1

0x00090002,

0x00640000,

0x00650000,

0x00660000,

0x00670000,

0x00680000,

0x00690000,

0x006A0000,

0x006B0000,

0x006C0000,

0x006D0000,

0x000D8001 //JESD\_FIFO set SPI\_TXENABLE to 1

原理图见下图









