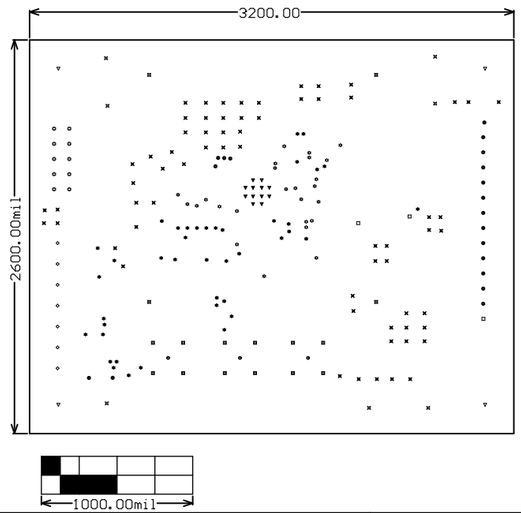
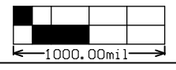
Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	L1-TOP	Copper	1.40mil		
4	Dielectric1	FR-406	10.00mil	4.6	
5	L2-GND	Copper	1.42mil		
6	Dielectric2	FR-4	32.60mil	4.8	
7	L3-POWER	Copper	1.40mil		
8	Dielectric3	FR-406	10.00mil	4.6	
9	L4-BOTTOM	Copper	1.40mil		
10	Bottom Solder	Solder Resist	0.40mil	3.5	
11	Bottom Overlay				





Symbol	Count	Hole Size	Plated
□	3	16.00mil (0.406mm)	PTH
◎	3	62.00mil (1.575mm)	PTH
▽	4	145.67mil (3.700mm)	PTH
⊠	4	150.00mil (3.810mm)	PTH
◇	7	47.24mil (1.200mm)	PTH
⊠	7	63.00mil (1.600mm)	PTH
⊕	10	40.16mil (1.020mm)	PTH
▼	12	7.87mil (0.200mm)	PTH
⊡	12	67.00mil (1.702mm)	PTH
⊕	19	12.00mil (0.305mm)	PTH
✡	25	10.00mil (0.254mm)	PTH
✡	41	14.00mil (0.356mm)	PTH
✖	64	18.00mil (0.457mm)	PTH
	211 Total		

DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL
MIN. CLEARANCE: 0.2 mm
MIN. VIA PAD SIZE: 24 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
☐ FR-408 ☒ FR-4 High Tg ☐ OTHER _____
THICKNESS: ☒ 62 MIL (1.6mm) +/-10% ☐ OTHER _____
TOLERANCE: ☒ ANSI IPC-6012 TYPE 3 CLASS 2
☐ OTHER +/- _____
BOW & TWIST: ☒ ANSI IPC-6012 TYPE 3 CLASS 2
☐ OTHER +/- _____

DRILLING:
REFERENCE: ☒ AS SHOWN ☒ NC_DRILL FILES
PTH COPPER THICKNESS: ☒ 20-30 um ☐ OTHER _____

BOARD FINISH:
SILKSCREEN: ☒ TOP ☒ BOTTOM
SILKSCREEN COLOR: ☒ WHITE ☐ OTHER _____
SOLDER RESIST COLOR: ☒ GREEN ☐ OTHER _____
☒ MATTE ☐ SEMI-GLOSS

SURFACE FINISH: ☒ IMMERSION GOLD (ENIG) ☐ ENEPIG
☐ IMM. TIN/SILVER OR EQUIV ☐ OTHER _____

ARRAY/PANEL: ☐ CUT AND TRIM PER M1 BOARD OUTLINE
☐ N.C. ROUTE ☒ V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
☒ ANSI IPC-A-600F CLASS -> ☐ 1 ☒ 2 ☐ 3
☒ RoHS ☐ OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: ☐ YES
BARE BOARD ELEC. TEST: ☐ NONE ☒ REQUIRED ☐ PER ORDER
☐ XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
☐ XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
☐ OUTER XX MIL VIAS REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
☐ LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: DAC814xx EVM
DESIGNED FOR: Public Release
FILE NAME: DC051A.PcbDoc

ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: DC051	REV: A	SVN REV: Not In VersionControl
LAYER NAME = [illegible]nsions	TID #: N/A		
PLOT NAME = Fabrication Drawing	GENERATED : 8/9/2018 6:16:51 PM		TEXAS INSTRUMENTS

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ENGINEER:	LAYOUT BY:
Uttama Kumar Sahu	VENU
SCALE: 1.00	ALTIUM DESIGNER VERSION: 17.1.5.472